S-1000 Series

ULTRA-SMALL PACKAGE HIGH-PRECISION VOLTAGE DETECTOR

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Rev.3.1_02

The S-1000 series is a series of high-precision voltage detectors developed using CMOS process. The detection voltage is fixed internally with an accuracy of ±1.0%. It operates with low current consumption of 350 nA typ. Two output forms, Nch open-drain and CMOS output, are available. CMOS voltage detector, S-1000 Series is the most suitable for the portable equipments with ultra low current consumption, high precision and corresponding to the small package.

■ Features

- Ultra-low current consumption — 350 nA typ. (V_{DD} = detection voltage + 1.5 V)
- High-precision detection voltage — ±1.0%
- Operating voltage range — 0.95 to 5.5 V
- Hysteresis characteristics — 5% typ.
- Detection voltage — 1.5 to 4.6 V (0.1 V step)
- Output form — Nch open-drain output (Active “L”)
  CMOS output (Active “L”)
- Lead-free, Sn 100%, halogen-free*1

***1.** Refer to “■ **Product Name Structure**” for details.

■ Applications

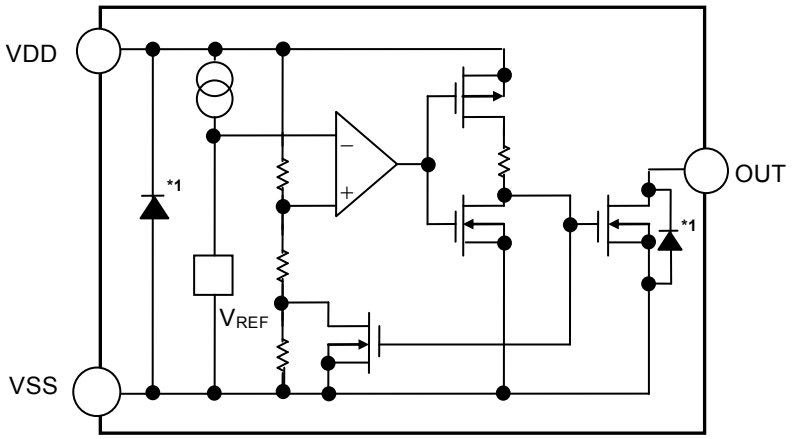
- Power monitor for microcomputers and reset for CPUs.
- Power monitor for portable equipments such as cellular phones, digital still cameras and PDAs.
- Constant voltage power monitor for cameras, video equipments and communication devices.

■ Packages

- SC-82AB
- SOT-23-5
- SNT-4A

■ Block Diagrams

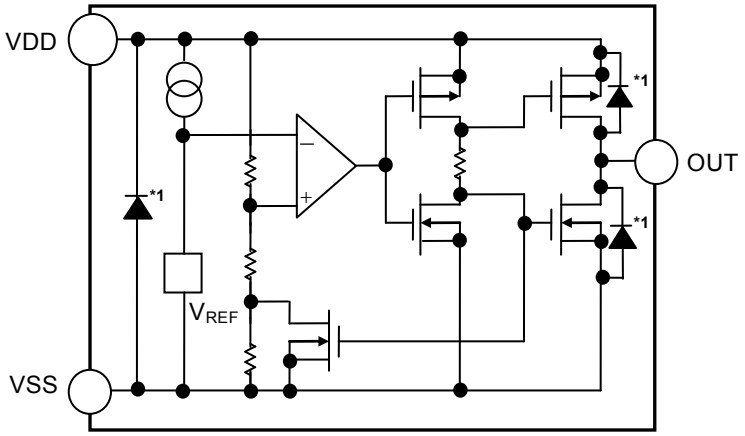
1. Nch open-drain output products



***1.** Parasitic diode

Figure 1

2. CMOS output products



***1.** Parasitic diode

Figure 2

■ Product Name Structure

The detection voltage, output form and packages for S-1000 series can be selected at the user's request. Refer to the "**1. Product name**" for the construction of the product name, "**2. Package**" regarding the package drawings and "**3. Product name list**" for the full product names.

1. Product name

1. 1 SC-82AB, SOT-23-5

S-1000 x xx - xxxx x

- Environmental code
  - U: Lead-free (Sn 100%), halogen-free
  - G: Lead-free (for details, please contact our sales office)
- Package name (abbreviation) and packing specifications*1
  - N4T1: SC-82AB, tape
  - M5T1: SOT-23-5, tape
- Detection voltage value
  - 15 ~ 46
  - (e.g. When the detection voltage is 1.5 V, it is expressed as 15.)
- Output form
  - N: Nch open-drain output (Active "L")
  - C: CMOS output (Active "L")

***1.** Refer to the taping specifications at the end of this book.

1. 2 SNT-4A

S-1000 x xx - I4T1 U

- Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- Package name (abbreviation) and packing specifications*1
  - I4T1: SNT-4A, tape
- Detection voltage value
  - 15 ~ 46
  - (e.g. When the detection voltage is 1.5 V, it is expressed as 15.)
- Output form
  - N: Nch open-drain output (Active "L")
  - C: CMOS output (Active "L")

***1.** Refer to the taping specifications at the end of this book.

2. Packages

Package name	Drawing code			
	Package	Tape	Reel	Land
SC-82AB	NP004-A-P-SD	NP004-A-C-SD NP004-A-C-S1	NP004-A-R-SD	–
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD	–
SNT-4A	PF004-A-P-SD	PF004-A-C-SD	PF004-A-R-SD	PF004-A-L-SD

3. Product name list

3. 1 Nch open-drain output products

Table 1

Detection voltage range	SC-82AB	SOT-23-5	SNT-4A
1.5 V ± 1.0%	S-1000N15-N4T1x	S-1000N15-M5T1x	S-1000N15-I4T1U
1.6 V ± 1.0%	S-1000N16-N4T1x	S-1000N16-M5T1x	S-1000N16-I4T1U
1.7 V ± 1.0%	S-1000N17-N4T1x	S-1000N17-M5T1x	S-1000N17-I4T1U
1.8 V ± 1.0%	S-1000N18-N4T1x	S-1000N18-M5T1x	S-1000N18-I4T1U
1.9 V ± 1.0%	S-1000N19-N4T1x	S-1000N19-M5T1x	S-1000N19-I4T1U
2.0 V ± 1.0%	S-1000N20-N4T1x	S-1000N20-M5T1x	S-1000N20-I4T1U
2.1 V ± 1.0%	S-1000N21-N4T1x	S-1000N21-M5T1x	S-1000N21-I4T1U
2.2 V ± 1.0%	S-1000N22-N4T1x	S-1000N22-M5T1x	S-1000N22-I4T1U
2.3 V ± 1.0%	S-1000N23-N4T1x	S-1000N23-M5T1x	S-1000N23-I4T1U
2.4 V ± 1.0%	S-1000N24-N4T1x	S-1000N24-M5T1x	S-1000N24-I4T1U
2.5 V ± 1.0%	S-1000N25-N4T1x	S-1000N25-M5T1x	S-1000N25-I4T1U
2.6 V ± 1.0%	S-1000N26-N4T1x	S-1000N26-M5T1x	S-1000N26-I4T1U
2.7 V ± 1.0%	S-1000N27-N4T1x	S-1000N27-M5T1x	S-1000N27-I4T1U
2.8 V ± 1.0%	S-1000N28-N4T1x	S-1000N28-M5T1x	S-1000N28-I4T1U
2.9 V ± 1.0%	S-1000N29-N4T1x	S-1000N29-M5T1x	S-1000N29-I4T1U
3.0 V ± 1.0%	S-1000N30-N4T1x	S-1000N30-M5T1x	S-1000N30-I4T1U
3.1 V ± 1.0%	S-1000N31-N4T1x	S-1000N31-M5T1x	S-1000N31-I4T1U
3.2 V ± 1.0%	S-1000N32-N4T1x	S-1000N32-M5T1x	S-1000N32-I4T1U
3.3 V ± 1.0%	S-1000N33-N4T1x	S-1000N33-M5T1x	S-1000N33-I4T1U
3.4 V ± 1.0%	S-1000N34-N4T1x	S-1000N34-M5T1x	S-1000N34-I4T1U
3.5 V ± 1.0%	S-1000N35-N4T1x	S-1000N35-M5T1x	S-1000N35-I4T1U
3.6 V ± 1.0%	S-1000N36-N4T1x	S-1000N36-M5T1x	S-1000N36-I4T1U
3.7 V ± 1.0%	S-1000N37-N4T1x	S-1000N37-M5T1x	S-1000N37-I4T1U
3.8 V ± 1.0%	S-1000N38-N4T1x	S-1000N38-M5T1x	S-1000N38-I4T1U
3.9 V ± 1.0%	S-1000N39-N4T1x	S-1000N39-M5T1x	S-1000N39-I4T1U
4.0 V ± 1.0%	S-1000N40-N4T1x	S-1000N40-M5T1x	S-1000N40-I4T1U
4.1 V ± 1.0%	S-1000N41-N4T1x	S-1000N41-M5T1x	S-1000N41-I4T1U
4.2 V ± 1.0%	S-1000N42-N4T1x	S-1000N42-M5T1x	S-1000N42-I4T1U
4.3 V ± 1.0%	S-1000N43-N4T1x	S-1000N43-M5T1x	S-1000N43-I4T1U
4.4 V ± 1.0%	S-1000N44-N4T1x	S-1000N44-M5T1x	S-1000N44-I4T1U
4.5 V ± 1.0%	S-1000N45-N4T1x	S-1000N45-M5T1x	S-1000N45-I4T1U
4.6 V ± 1.0%	S-1000N46-N4T1x	S-1000N46-M5T1x	S-1000N46-I4T1U

Remark 1. x: G or U
2. Please select products of environmental code = U for Sn 100%, halogen-free products.

3. 2 CMOS output products

Table 2

Detection voltage range	SC-82AB	SOT-23-5	SNT-4A
1.5 V ± 1.0%	S-1000C15-N4T1x	S-1000C15-M5T1x	S-1000C15-I4T1U
1.6 V ± 1.0%	S-1000C16-N4T1x	S-1000C16-M5T1x	S-1000C16-I4T1U
1.7 V ± 1.0%	S-1000C17-N4T1x	S-1000C17-M5T1x	S-1000C17-I4T1U
1.8 V ± 1.0%	S-1000C18-N4T1x	S-1000C18-M5T1x	S-1000C18-I4T1U
1.9 V ± 1.0%	S-1000C19-N4T1x	S-1000C19-M5T1x	S-1000C19-I4T1U
2.0 V ± 1.0%	S-1000C20-N4T1x	S-1000C20-M5T1x	S-1000C20-I4T1U
2.1 V ± 1.0%	S-1000C21-N4T1x	S-1000C21-M5T1x	S-1000C21-I4T1U
2.2 V ± 1.0%	S-1000C22-N4T1x	S-1000C22-M5T1x	S-1000C22-I4T1U
2.3 V ± 1.0%	S-1000C23-N4T1x	S-1000C23-M5T1x	S-1000C23-I4T1U
2.4 V ± 1.0%	S-1000C24-N4T1x	S-1000C24-M5T1x	S-1000C24-I4T1U
2.5 V ± 1.0%	S-1000C25-N4T1x	S-1000C25-M5T1x	S-1000C25-I4T1U
2.6 V ± 1.0%	S-1000C26-N4T1x	S-1000C26-M5T1x	S-1000C26-I4T1U
2.7 V ± 1.0%	S-1000C27-N4T1x	S-1000C27-M5T1x	S-1000C27-I4T1U
2.8 V ± 1.0%	S-1000C28-N4T1x	S-1000C28-M5T1x	S-1000C28-I4T1U
2.9 V ± 1.0%	S-1000C29-N4T1x	S-1000C29-M5T1x	S-1000C29-I4T1U
3.0 V ± 1.0%	S-1000C30-N4T1x	S-1000C30-M5T1x	S-1000C30-I4T1U
3.1 V ± 1.0%	S-1000C31-N4T1x	S-1000C31-M5T1x	S-1000C31-I4T1U
3.2 V ± 1.0%	S-1000C32-N4T1x	S-1000C32-M5T1x	S-1000C32-I4T1U
3.3 V ± 1.0%	S-1000C33-N4T1x	S-1000C33-M5T1x	S-1000C33-I4T1U
3.4 V ± 1.0%	S-1000C34-N4T1x	S-1000C34-M5T1x	S-1000C34-I4T1U
3.5 V ± 1.0%	S-1000C35-N4T1x	S-1000C35-M5T1x	S-1000C35-I4T1U
3.6 V ± 1.0%	S-1000C36-N4T1x	S-1000C36-M5T1x	S-1000C36-I4T1U
3.7 V ± 1.0%	S-1000C37-N4T1x	S-1000C37-M5T1x	S-1000C37-I4T1U
3.8 V ± 1.0%	S-1000C38-N4T1x	S-1000C38-M5T1x	S-1000C38-I4T1U
3.9 V ± 1.0%	S-1000C39-N4T1x	S-1000C39-M5T1x	S-1000C39-I4T1U
4.0 V ± 1.0%	S-1000C40-N4T1x	S-1000C40-M5T1x	S-1000C40-I4T1U
4.1 V ± 1.0%	S-1000C41-N4T1x	S-1000C41-M5T1x	S-1000C41-I4T1U
4.2 V ± 1.0%	S-1000C42-N4T1x	S-1000C42-M5T1x	S-1000C42-I4T1U
4.3 V ± 1.0%	S-1000C43-N4T1x	S-1000C43-M5T1x	S-1000C43-I4T1U
4.4 V ± 1.0%	S-1000C44-N4T1x	S-1000C44-M5T1x	S-1000C44-I4T1U
4.5 V ± 1.0%	S-1000C45-N4T1x	S-1000C45-M5T1x	S-1000C45-I4T1U
4.6 V ± 1.0%	S-1000C46-N4T1x	S-1000C46-M5T1x	S-1000C46-I4T1U

Remark 1. x: G or U
2. Please select products of environmental code = U for Sn 100%, halogen-free products.

■ Output Forms

1. Output forms in S-1000 series

Table 3

	Nch open-drain output products (Active "L")	CMOS output products (Active "L")
S-1000 series	"N" is the last letter of the product name. e.g. S-1000N	"C" is the last letter of the product name. e.g. S-1000C

2. Output form and their usage

Table 4

Usage	Nch open-drain output products (Active "L")	CMOS output products (Active "L")
Different power supplies	Yes	No
Active "L" reset for CPUs	Yes	Yes
Active "H" reset for CPUs	No	No
Detection voltage change by resistor divider	Yes	No

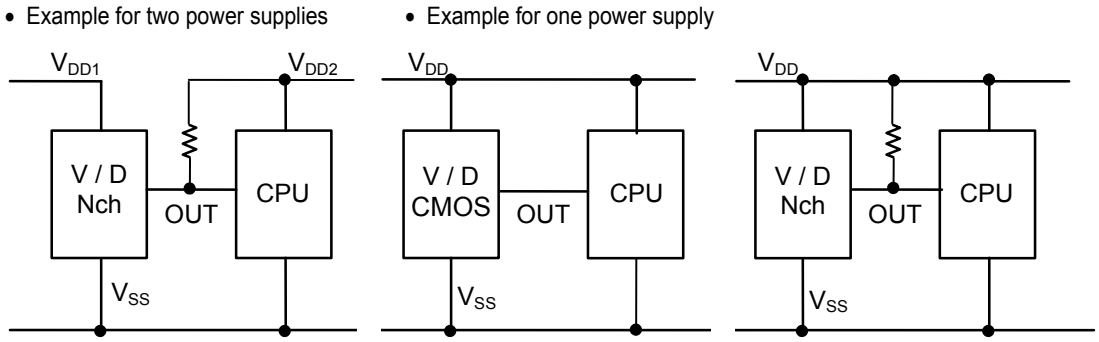


Figure 3

■ Pin Configurations

SC-82AB
Top view

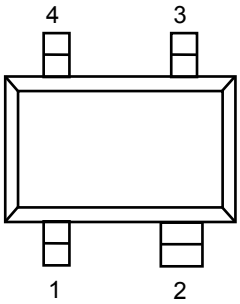


Figure 4

Table 5

Pin No.	Pin name	Pin description
1	OUT	Voltage detection output pin
2	VDD	Voltage input pin
3	NC*1	No connection
4	VSS	GND pin

***1.** The NC pin is electrically open.
The NC pin can be connected to VDD or VSS.

SOT-23-5
Top view

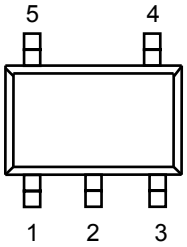


Figure 5

Table 6

Pin No.	Pin name	Pin description
1	OUT	Voltage detection output pin
2	VDD	Voltage input pin
3	VSS	GND pin
4	NC*1	No connection
5	NC*1	No connection

***1.** The NC pin is electrically open.
The NC pin can be connected to VDD or VSS.

SNT-4A
Top view

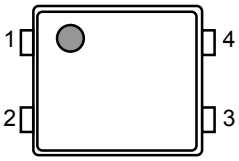


Figure 6

Table 7

Pin No.	Pin name	Pin description
1	OUT	Voltage detection output pin
2	VSS	GND pin
3	NC*1	No connection
4	VDD	Voltage input pin

***1.** The NC pin is electrically open.
The NC pin can be connected to VDD or VSS.

■ Absolute Maximum Ratings

Table 8

(Ta = 25 °C unless otherwise specified)

Item		Symbol	Absolute maximum ratings	Unit
Power supply voltage		$V_{DD} - V_{SS}$	6	V
Output voltage	Nch open-drain output products	V_{OUT}	$V_{SS} - 0.3$ to $V_{SS} + 6$	V
	CMOS output products		$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Output current		I_{OUT}	50	mA
Power dissipation	SC-82AB	P_D	200 (When not mounted on board)	mW
			350*1	mW
	SOT-23-5		300 (When not mounted on board)	mW
			600*1	mW
	SNT-4A		300*1	mW
Operating ambient temperature		T_{opr}	−40 to +85	°C
Storage temperature		T_{stg}	−40 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

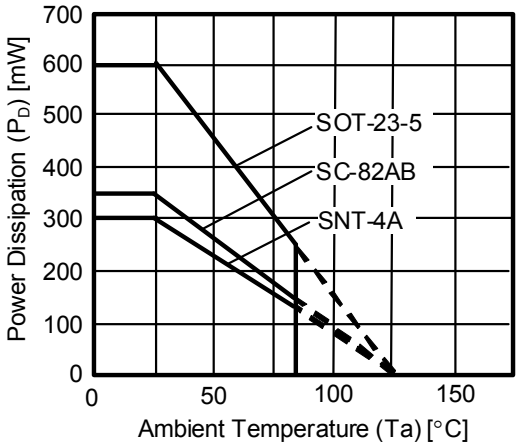


Figure 7 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

1. Nch open-drain output products

Table 9

(Ta = 25 °C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Measure-ment circuit
Detection voltage*1	$-V_{DET}$	–		$-V_{DET(S)}$ ×0.99	$-V_{DET(S)}$	$-V_{DET(S)}$ ×1.01	V	1
Hysteresis width	V_{HYS}	–		$-V_{DET}$ ×0.03	$-V_{DET}$ ×0.05	$-V_{DET}$ ×0.07	V	1
Current consumption	I_{SS}	$V_{DD} = -V_{DET(S)} + 1.5$ V	S-1000N15 to 39	–	350	900	nA	2
		$V_{DD} = 5.5$ V	S-1000N40 to 46	–	350	900	nA	2
Operating voltage	V_{DD}	–		0.95	–	5.5	V	1
Output current	I_{OUT}	Output transistor, Nch, $V_{DS} = 0.5$ V, $V_{DD} = 1.2$ V		1.36	2.55	–	mA	3
Leakage current	I_{LEAK}	Output transistor, Nch, $V_{DS} = 5.5$ V, $V_{DD} = 5.5$ V		–	–	100	nA	3
Response time	t_{PLH}	–		–	–	60	μs	1
Detection voltage temperature coefficient*2	$\frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}$	Ta = −40 to +85 °C		–	±100	±350	ppm / °C	1

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Specified detection voltage value (The center value of the detection voltage range in **Table 1**.)

***2.** The temperature change ratio in the detection voltage [mV / °C] is calculated by using the following equation.

$$\frac{\Delta - V_{DET}}{\Delta Ta}[mV/°C]^{*1} = -V_{DET(S)}(Typ.)[V]^{*2} \times \frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}}[ppm/°C]^{*3} \div 1000$$

***1.** Temperature change ratio of the detection voltage

***2.** Specified detection voltage

***3.** Detection voltage temperature coefficient

2. CMOS output products

Table 10

(Ta = 25 °C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Measure-ment circuit
Detection voltage*1	$-V_{DET}$	–		$-V_{DET(S)}$ ×0.99	$-V_{DET(S)}$	$-V_{DET(S)}$ ×1.01	V	1
Hysteresis width	V_{HYS}	–		$-V_{DET}$ ×0.03	$-V_{DET}$ ×0.05	$-V_{DET}$ ×0.07	V	1
Current consumption	I_{SS}	$V_{DD} = -V_{DET(S)} + 1.5$ V	S-1000C15 to 39	–	350	900	nA	2
		$V_{DD} = 5.5$ V	S-1000C40 to 46	–	350	900	nA	2
Operating voltage	V_{DD}	–		0.95	–	5.5	V	1
Output current	I_{OUT}	Output transistor, Nch, $V_{DS} = 0.5$ V, $V_{DD} = 1.2$ V		1.36	2.55	–	mA	3
		Output transistor, Pch, $V_{DS} = 0.5$ V, $V_{DD} = 5.5$ V		1.71	2.76	–	mA	4
Response time	t_{PLH}	–		–	–	60	μs	1
Detection voltage temperature coefficient*2	$\frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}$	Ta = −40 to +85 °C		–	±100	±350	ppm/°C	1

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Specified detection voltage value (The center value of the detection voltage range in **Table 2**.)

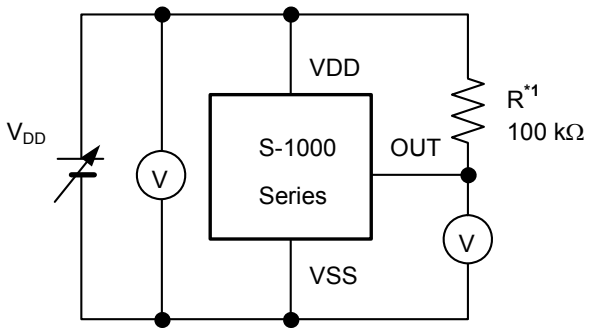
***2.** The temperature change ratio in the detection voltage [mV / °C] is calculated by using the following equation.

$$\frac{\Delta - V_{DET}}{\Delta Ta}[mV/°C]^{*1} = -V_{DET(S)}(Typ.)[V]^{*2} \times \frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}}[ppm/°C]^{*3} \div 1000$$

***1.** Temperature change ratio of the detection voltage
***2.** Specified detection voltage
***3.** Detection voltage temperature coefficient

■ Measurement Circuits

1.



1. R is unnecessary for CMOS output products.

Figure 8

2.

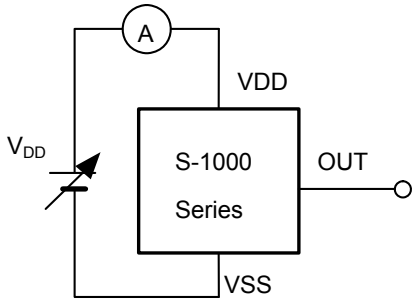


Figure 9

3.

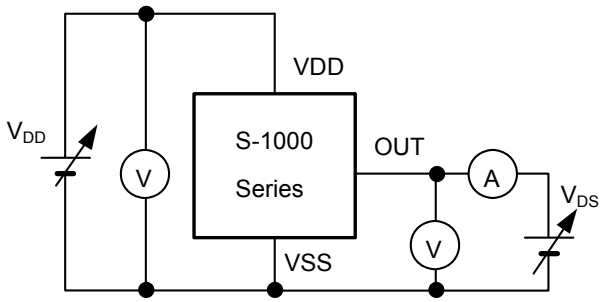


Figure 10

4.

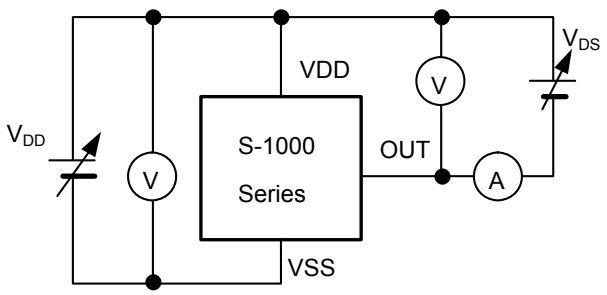


Figure 11

■ Timing Chart

1. Nch open-drain output products

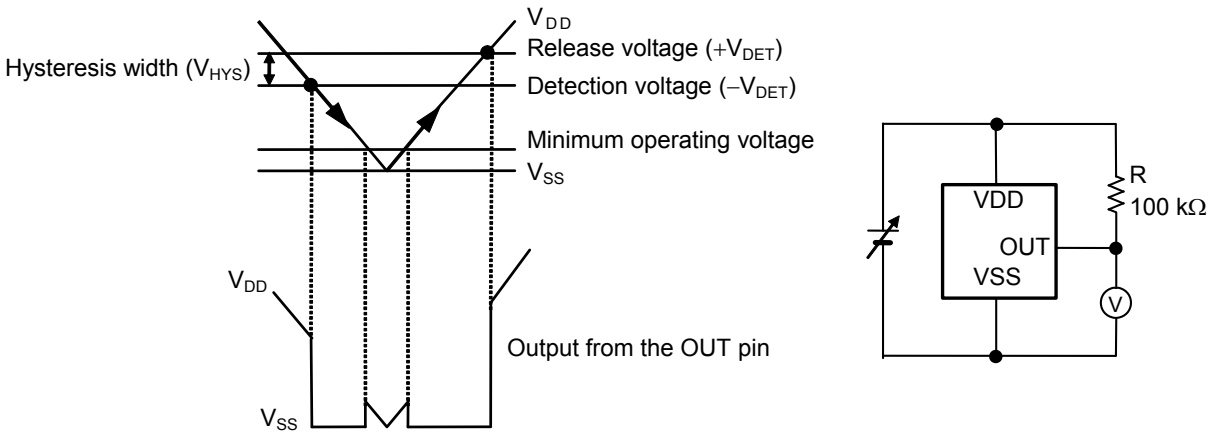
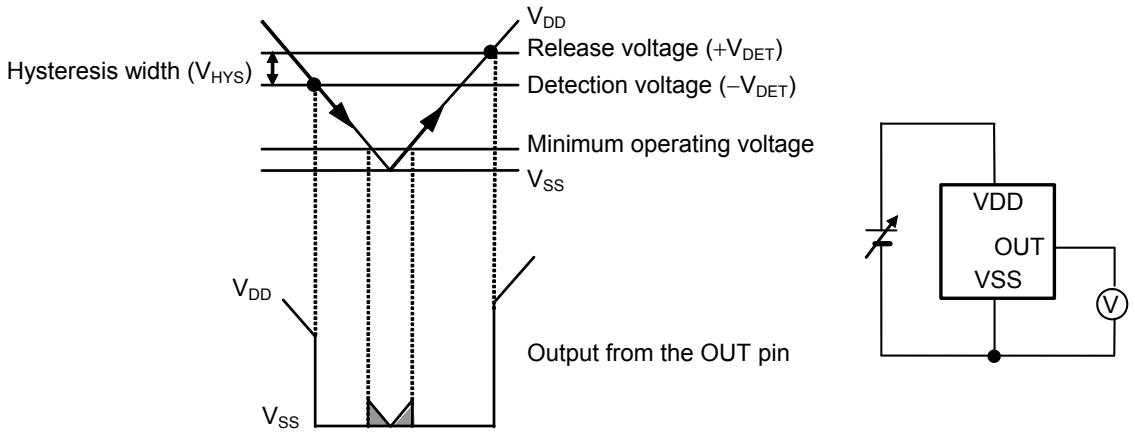


Figure 12

2. CMOS output products



Remark For values of V_{DD} less than minimum operating voltage, values of OUT terminal output is free in the shaded region.

Figure 13

■ Operation

1. Basic operation: CMOS output (Active "L")

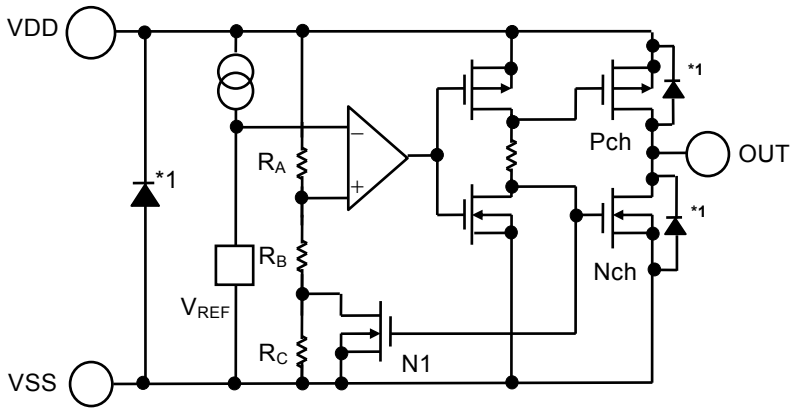
(1) When the power supply voltage (V_{DD}) is higher than the release voltage ($+V_{DET}$), the Nch transistor is OFF and the Pch transistor is ON to provide V_{DD} ("H") at the output. Since the Nch transistor N1 in **Figure 14** is OFF, the comparator input voltage is $\frac{(R_B + R_C) \bullet V_{DD}}{R_A + R_B + R_C}$.

(2) When the V_{DD} goes below $+V_{DET}$, the output provides the V_{DD} level, as long as the V_{DD} remains above the detection voltage $-V_{DET}$. When the V_{DD} falls below $-V_{DET}$ (point A in **Figure 15**), the Nch transistor becomes ON, the Pch transistor becomes OFF, and the V_{SS} level appears at the output. At this time the Nch transistor N1 in **Figure 14** becomes ON, the comparator input voltage is changed to $\frac{R_B \bullet V_{DD}}{R_A + R_B}$.

(3) When the V_{DD} falls below the minimum operating voltage, the output becomes undefined, or goes to the V_{DD} when the output is pulled up to the V_{DD}.

(4) The V_{SS} level appears when the V_{DD} rises above the minimum operating voltage. The V_{SS} level still appears even when the V_{DD} surpasses $-V_{DET}$, as long as it does not exceed the release voltage $+V_{DET}$.

(5) When the V_{DD} rises above $+V_{DET}$ (point B in **Figure 15**), the Nch transistor becomes OFF and the Pch transistor becomes ON to provide V_{DD} level at the output.



***1.** Parasiteic diode

Figure 14 Operation 1

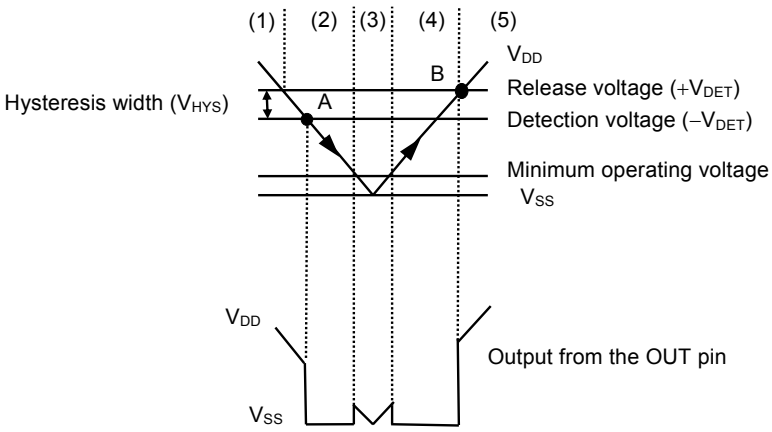
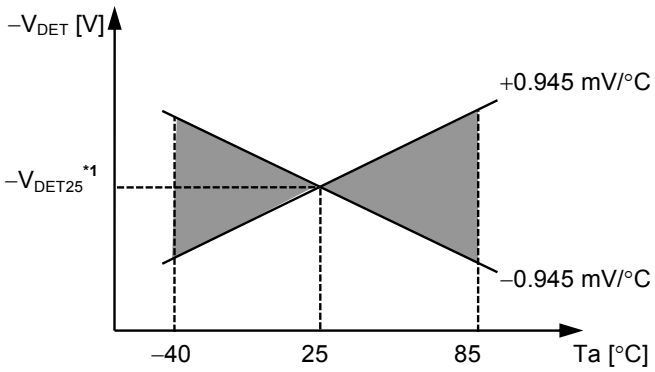


Figure 15 Operation 2

2. Other characteristics

2. 1 Temperature characteristics of detection voltage

The shaded area in **Figure 16** shows the temperature characteristics of the detection voltage.



***1.** □–V_{DET25} is an actual detection voltage value at 25°C.

Figure 16 Temperature characteristics of detection voltage (□Example for –V_{DET} = 2.7 V)

2. 2 Temperature characteristics of release voltage

The temperature change $\frac{\Delta + V_{DET}}{\Delta Ta}$ of the release voltage is calculated by the temperature change $\frac{\Delta - V_{DET}}{\Delta Ta}$ of the detection voltage as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} = \frac{+V_{DET}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

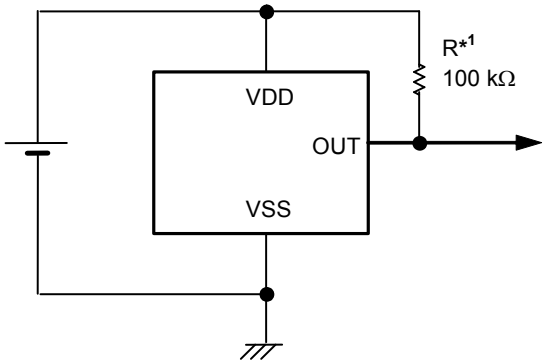
The temperature changes of the release voltage and the detection voltage have the same sign consequently.

2. 3 Temperature characteristics of hysteresis voltage

The temperature changes of the hysteresis voltage is expressed as $\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta}$ and is calculated as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta} = \frac{V_{HYS}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

■ Standard Circuit



***1.** R is unnecessary for CMOS output products.

Figure 17

Caution The above connection diagram and constants do not guarantee correct operation. Perform sufficient evaluation using the actual application to set the constants.

■ Explanation of Terms

1. Detection voltage ($-V_{DET}$), release voltage ($+V_{DET}$)

The detection voltage ($-V_{DET}$) is a voltage at which the output turns to "L". The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum ($-V_{DET}$) Min. and the maximum ($-V_{DET}$) Max. is called the detection voltage range (Refer to **Figure 18**).

Example: For the S-1000C15, the detection voltage lies in the range of $1.485 \leq (-V_{DET}) \leq 1.515$.
This means that some S-1000C15s have 1.485 V for $-V_{DET}$ and some have 1.515 V.

The release voltage is a voltage at which the output turns to "H". The release voltage varies slightly among products of the same specification. The variation of release voltages between the specified minimum ($+V_{DET}$) Min. and the maximum ($+V_{DET}$) Max. is called the release voltage range (Refer to **Figure 19**). The range is calculed from the actual detection voltage ($-V_{DET}$) of a product and is expressed by $-V_{DET} \times 1.03 \leq +V_{DET} \leq -V_{DET} \times 1.07$.

Example: For the S-1000C15, the release voltage lies in the range of $1.530 \leq (+V_{DET}) \leq 1.621$.
This means that some S-1000C15s have 1.530 V for $+V_{DET}$ and some have 1.621 V.

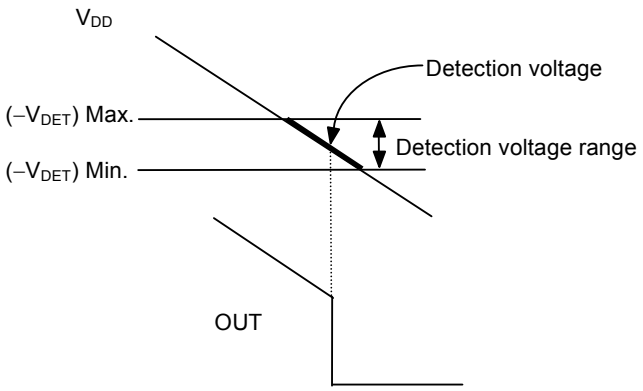


Figure 18 Detection voltage (CMOS output products)

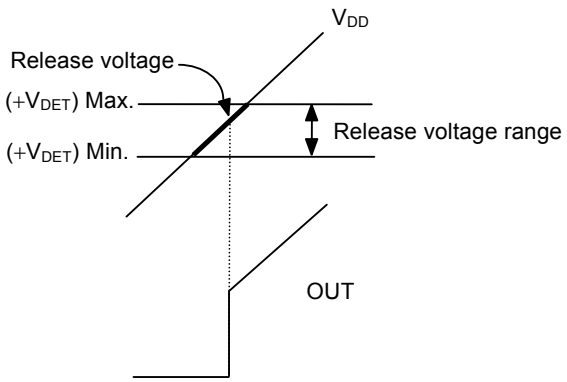


Figure 19 Release voltage (CMOS output products)

2. Hysteresis width (V_{HYS})

The hysteresis width is the voltage difference between the detection voltage and the release voltage (The voltage at point B − The voltage at point A = V_{HYS} in **Figure 15**). The existence of the hysteresis width prevents malfunction caused by noise on input signal.

3. Through-type current

The through-type current refers to the current that flows instantaneously at the time of detection and release of a voltage detector. The through-type current is large in CMOS output products, small in Nch open-drain output products.

4. Oscillation

In applications where a resistor is connected to the voltage detector input (**Figure 20**), taking a CMOS active "L" product for example, the through-type current which is generated when the output goes from "L" to "H" (release) causes a voltage drop equal to [through-type current] × [input resistance] across the resistor. When the input voltage drops below the detection voltage ($-V_{DET}$) as a result, the output voltage goes to low level. In this state, the through-type current stops and its resultant voltage drop disappears, and the output goes from "L" to "H". The through-type current is then generated again, a voltage drop appears, and repeating the process finally induces oscillation.

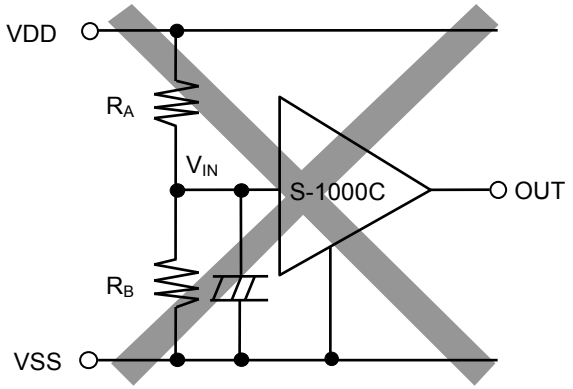


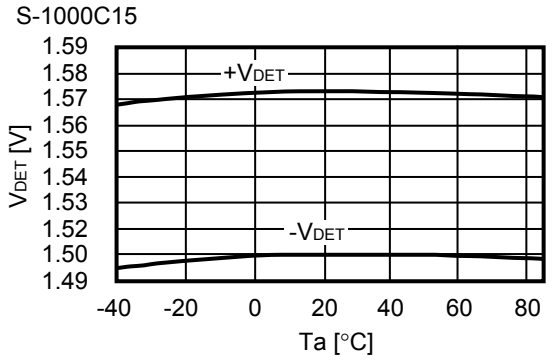
Figure 20 An example for bad implementation of input voltage divider

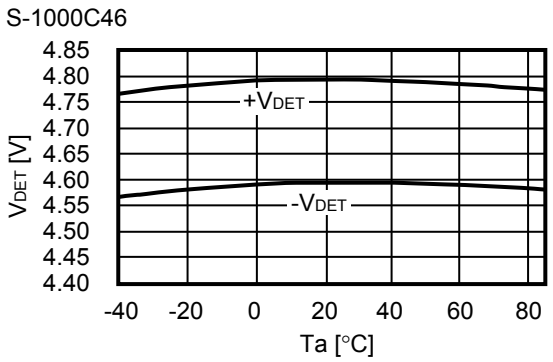
■ Precautions

- If the input impedance is high, oscillation may occur due to the through-type current etc. In COMS output products, impedance should not be connected to the input pin. In Nch open drain output products, input impedance is recommended to be 800 Ω or less. However be sure to perform sufficient evaluation under the actual usage conditions for selection, including evaluation of temperature characteristics.
- In CMOS output products oscillation may occur when a pull-down resistor is used, and falling speed of the power supply voltage (V_{DD}) is slow near the detection voltage.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics should be taken into consideration. ABLIC Inc. shall not bear any responsibility for the products on the circuits described herein.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

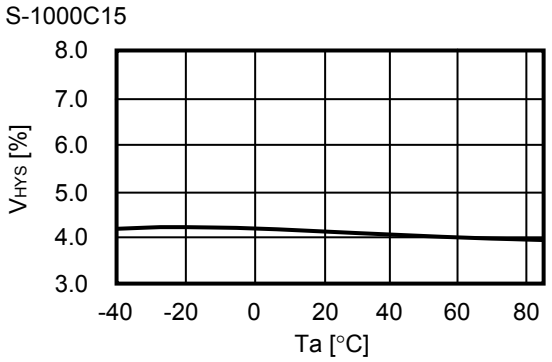
■ Typical Characteristics (Typical Data)

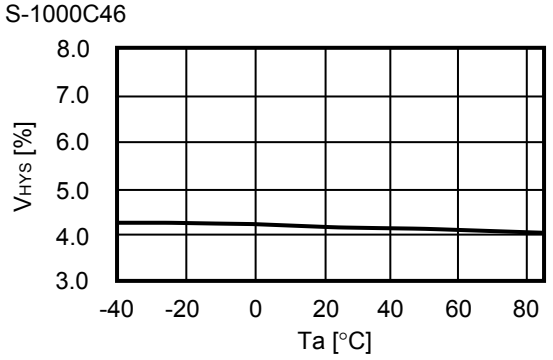
1. Detection voltage (V_{DET}) – temperature (Ta)



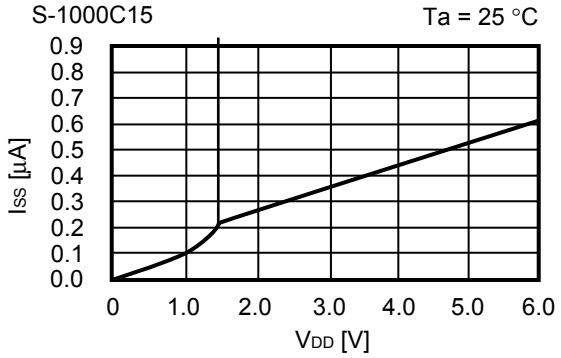


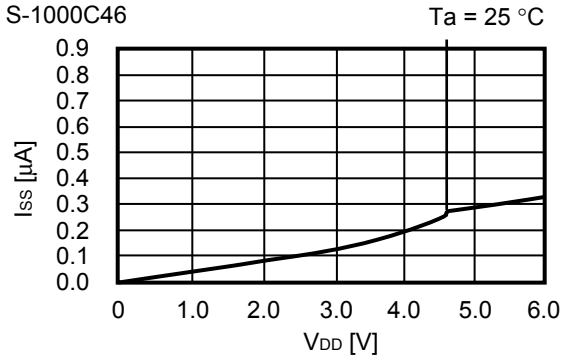
2. Hysteresis voltage width – (V_{HYS}) - temperature (Ta)



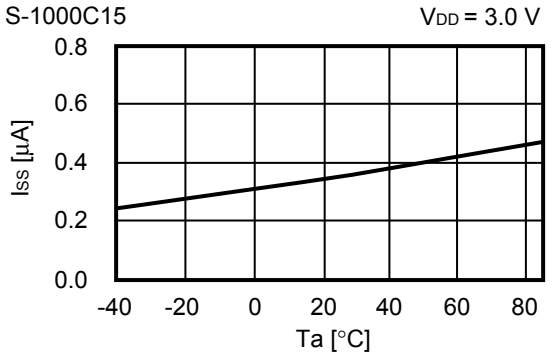


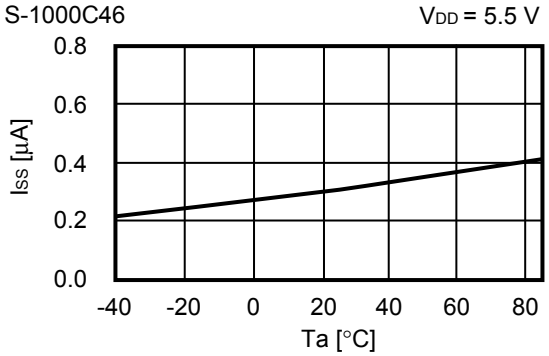
3. Current consumption (I_{SS}) – input voltage (V_{DD})



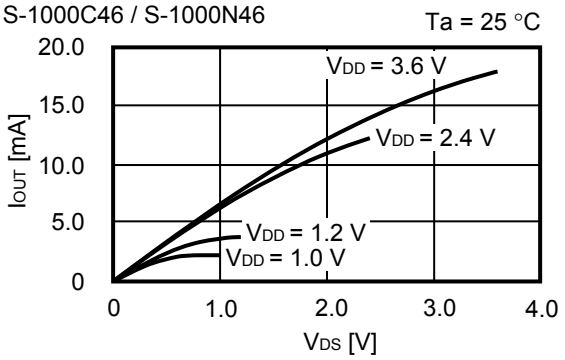


4. Current consumption (I_{SS}) – temperature (Ta)

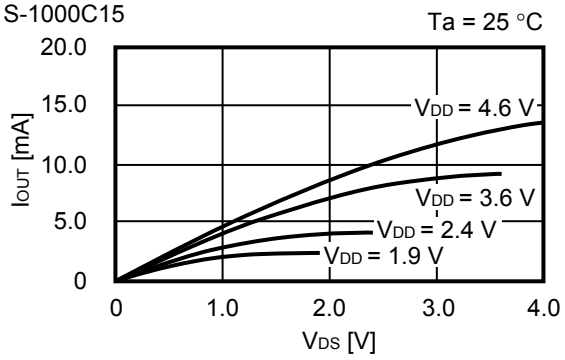




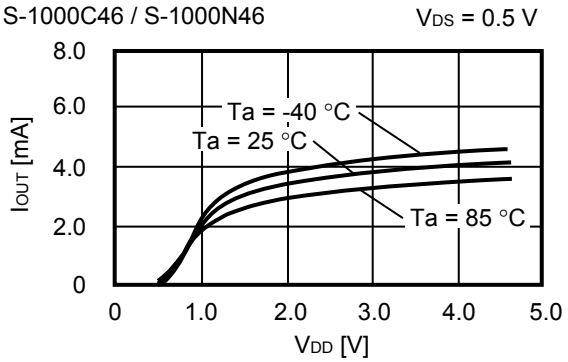
5. Nch transistor output current (I_{OUT}) – V_{DS}



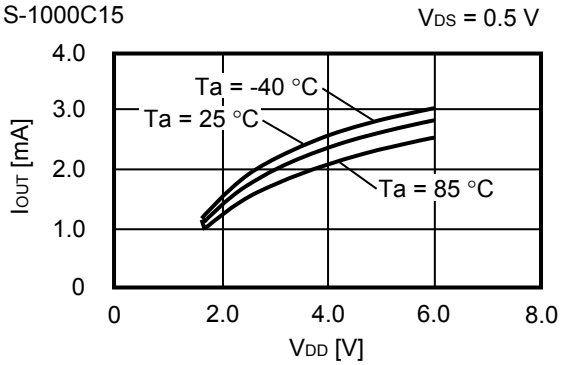
6. Pch transistor output current (I_{OUT}) – V_{DS}



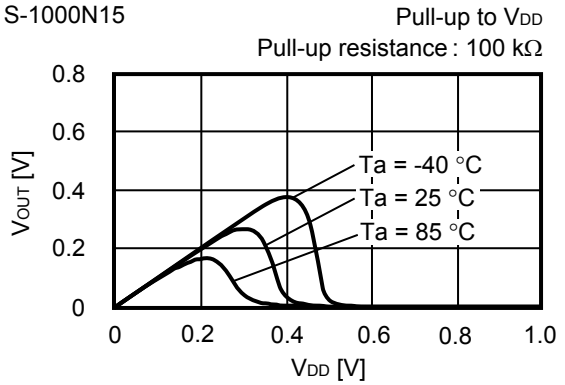
7. Nch transistor output current (I_{OUT})

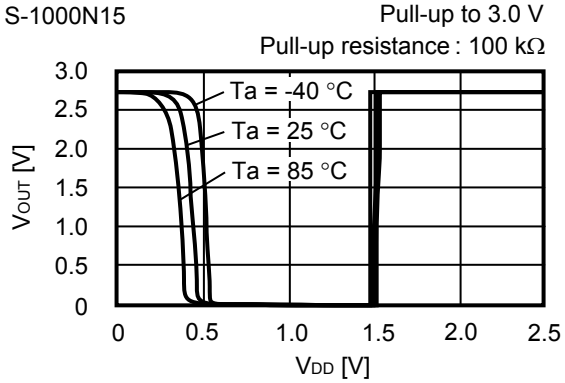


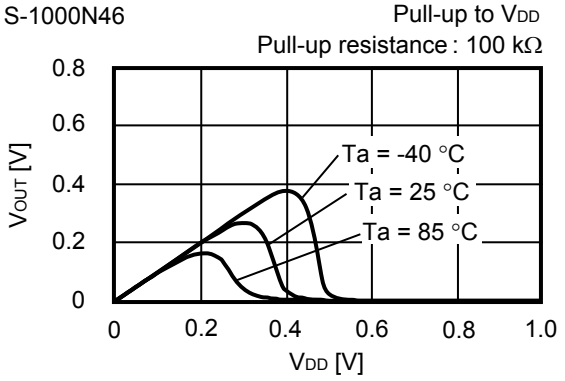
8. Pch transistor output current (I_{OUT})

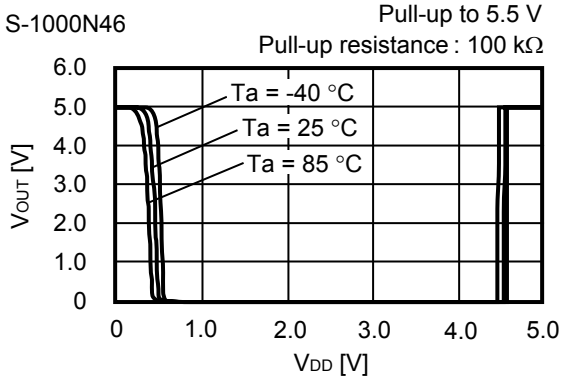


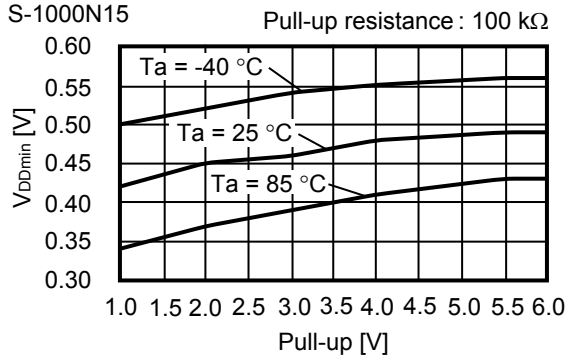
9. Minimum operating voltage - input voltage (V_{DD})

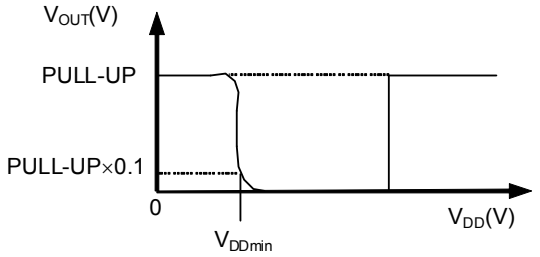






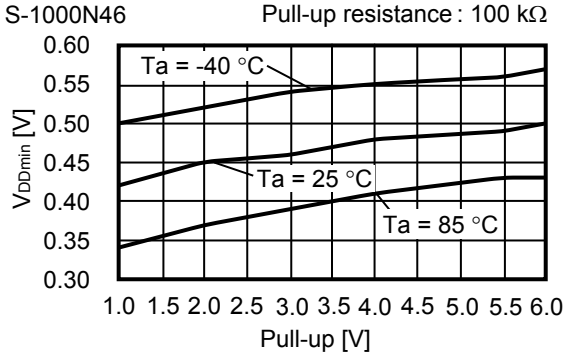




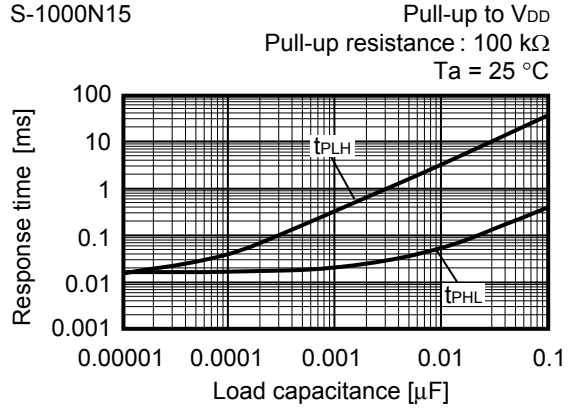


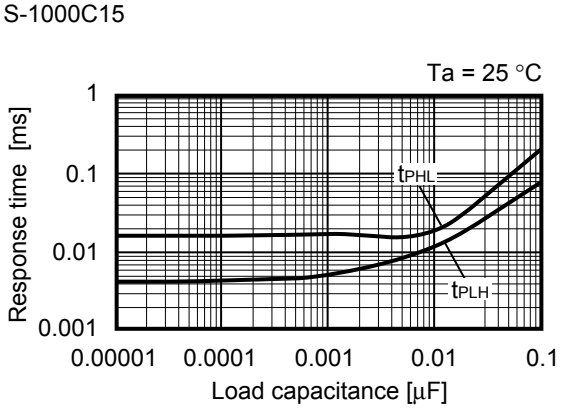
Remark $V_{DDmin.}$ is defined by the V_{DD} voltage at which V_{OUT} goes below 10% of pull-up voltage when the V_{DD} increase from 0 V.

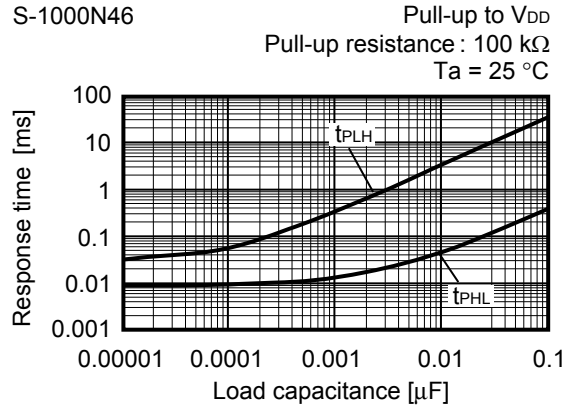
Figure 21

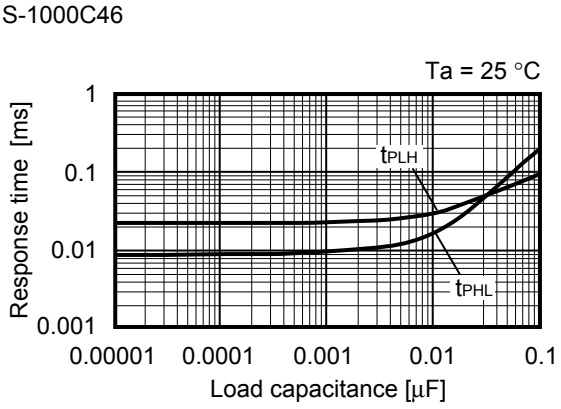


10. Dynamic response - C_{OUT}









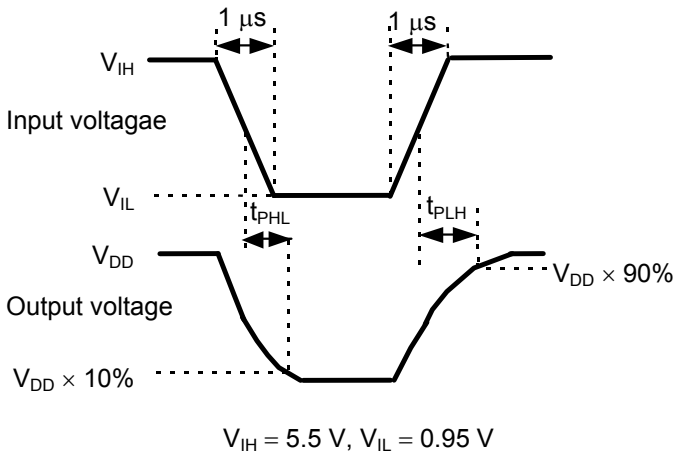
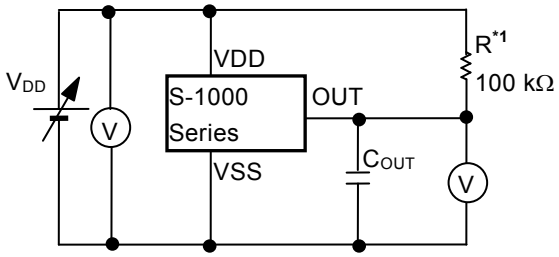


Figure 22 Measurement condition for response time



*1. R is unnecessary for CMOS output products.

Figure 23 Measurement circuit for response time

Caution The above connection diagram and constants do not guarantee correct operation. Perform sufficient evaluation using the actual application to set the constants.

■ Application Circuit Examples

1. Microcomputer reset circuits

If the power supply voltage to a microcomputer falls below the specified level, an unspecified operation may be performed or the contents of the memory register may be lost. When power supply voltage returns to normal, the microcomputer needs to be initialized before normal operations can be done.
Reset circuits protect microcomputers in the event of current being momentarily switched off or lowered.
Reset circuits shown in **Figures 24, 25** can be easily constructed with the help of the S-1000 series, that has low operating voltage, a high-precision detection voltage and hysteresis.

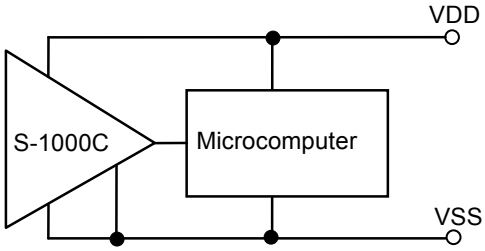
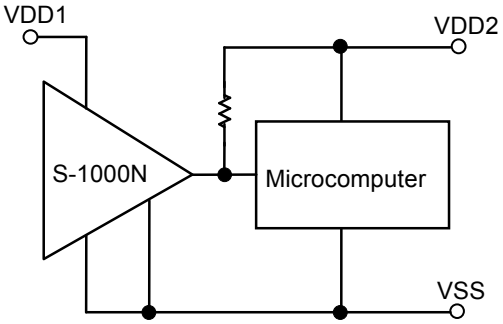


Figure 24 Reset circuit example(S-1000C)



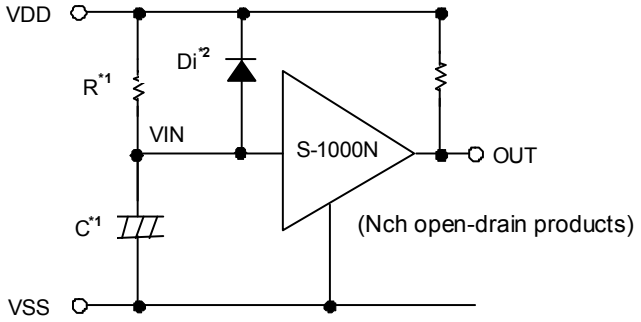
(Only for Nch open-drain products)

Figure 25 Reset circuit example (S-1000N)

Caution The above connection diagram and constants do not guarantee correct operation. Perform sufficient evaluation using the actual application to set the constants.

2. Power-on reset circuit

A power-on reset circuit can be constructed using Nch open-drain output product of S-1000 Series.



***1.** R should be 75 kΩ or less, and C should be 0.01 μF or more to prevent oscillation.
If C is not connected, R should be 800 Ω or less.

***2.** Diode Di instantaneously discharges the charge stored in the capacitor (C) at the power falling, Di can be removed when the delay of the falling time is not important.

Figure 26

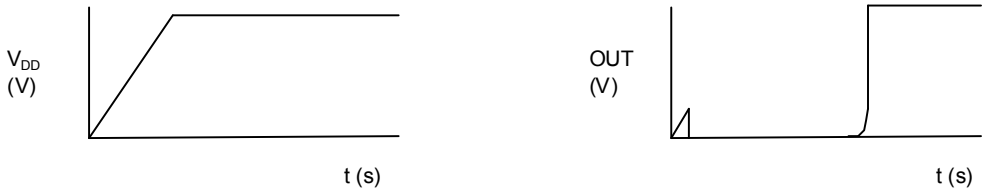


Figure 27

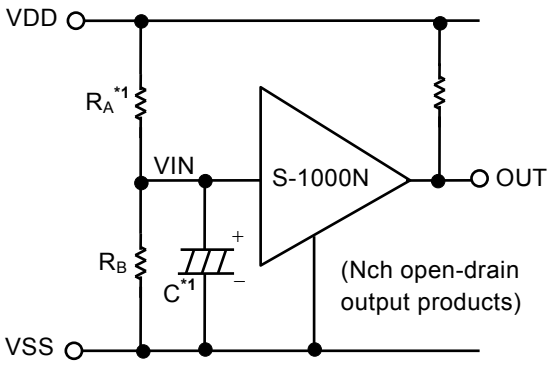
Remark When the power rises sharply as shown in the **Figure 28** left, the output may go to the high level for an instant in the undefined region where the output voltage is undefined since the power voltage is less than the minimum operation voltage.

Figure 28

Caution The above connection diagram and constants do not guarantee correct operation. Perform sufficient evaluation using the actual application to set the constants.

3. Change of detection voltage

In Nch open-drain output products of the S-1000 series, detection voltage can be changed using resistance dividers or diodes as shown in **Figures 29 to 30**. In **Figure 29**, hysteresis width also changes.



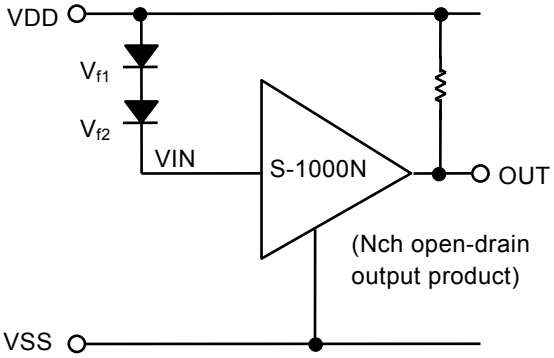
$$\text{Detection voltagae} = \frac{R_A + R_B}{R_B} \bullet -V_{DET}$$

$$\text{Hysterisis width} = \frac{R_A + R_B}{R_B} \bullet V_{HYS}$$

***1.** R_A should be 75 kΩ or less, and C should be 0.01 μF or more to prevent oscillation.
If C is not connected, R_A should be 800 Ω or less.

Caution If R_A and R_B are large, the hysteresis width may also be larger than the value given by the above equation due to the through-type current (which flows slightly in an Nch open-drain product).

Figure 29



Detection voltage = $V_{f1}+V_{f2}+(-V_{DET})$

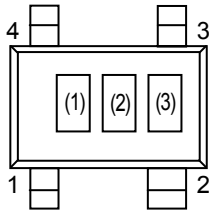
Figure 30

Caution The above connection diagram and constants do not guarantee correct operation. Perform sufficient evaluation using the actual application to set the constants.

■ Marking Specifications

(1) SC-82AB

SC-82AB
Top view



(1) to (3) : Product code (refer to **Product name vs. Product code**)

Product name vs. Product code

(a) Nch open-drain output products

Product Name	Product Code		
	(1)	(2)	(3)
S-1000N15-N4T1x	P	L	A
S-1000N16-N4T1x	P	L	B
S-1000N17-N4T1x	P	L	C
S-1000N18-N4T1x	P	L	D
S-1000N19-N4T1x	P	L	E
S-1000N20-N4T1x	P	L	F
S-1000N21-N4T1x	P	L	G
S-1000N22-N4T1x	P	L	H
S-1000N23-N4T1x	P	L	I
S-1000N24-N4T1x	P	L	J
S-1000N25-N4T1x	P	L	K
S-1000N26-N4T1x	P	L	L
S-1000N27-N4T1x	P	L	M
S-1000N28-N4T1x	P	L	N
S-1000N29-N4T1x	P	L	O
S-1000N30-N4T1x	P	L	P

Product Name	Product Code		
	(1)	(2)	(3)
S-1000N31-N4T1x	P	L	Q
S-1000N32-N4T1x	P	L	R
S-1000N33-N4T1x	P	L	S
S-1000N34-N4T1x	P	L	T
S-1000N35-N4T1x	P	L	U
S-1000N36-N4T1x	P	L	V
S-1000N37-N4T1x	P	L	W
S-1000N38-N4T1x	P	L	X
S-1000N39-N4T1x	P	L	Y
S-1000N40-N4T1x	P	L	Z
S-1000N41-N4T1x	P	L	2
S-1000N42-N4T1x	P	L	3
S-1000N43-N4T1x	P	L	4
S-1000N44-N4T1x	P	L	5
S-1000N45-N4T1x	P	L	6
S-1000N46-N4T1x	P	L	7

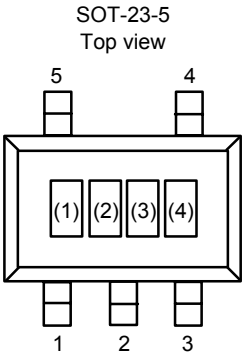
(b) CMOS output products

Product Name	Product Code		
	(1)	(2)	(3)
S-1000C15-N4T1x	P	K	A
S-1000C16-N4T1x	P	K	B
S-1000C17-N4T1x	P	K	C
S-1000C18-N4T1x	P	K	D
S-1000C19-N4T1x	P	K	E
S-1000C20-N4T1x	P	K	F
S-1000C21-N4T1x	P	K	G
S-1000C22-N4T1x	P	K	H
S-1000C23-N4T1x	P	K	I
S-1000C24-N4T1x	P	K	J
S-1000C25-N4T1x	P	K	K
S-1000C26-N4T1x	P	K	L
S-1000C27-N4T1x	P	K	M
S-1000C28-N4T1x	P	K	N
S-1000C29-N4T1x	P	K	O
S-1000C30-N4T1x	P	K	P

Product Name	Product Code		
	(1)	(2)	(3)
S-1000C31-N4T1x	P	K	Q
S-1000C32-N4T1x	P	K	R
S-1000C33-N4T1x	P	K	S
S-1000C34-N4T1x	P	K	T
S-1000C35-N4T1x	P	K	U
S-1000C36-N4T1x	P	K	V
S-1000C37-N4T1x	P	K	W
S-1000C38-N4T1x	P	K	X
S-1000C39-N4T1x	P	K	Y
S-1000C40-N4T1x	P	K	Z
S-1000C41-N4T1x	P	K	2
S-1000C42-N4T1x	P	K	3
S-1000C43-N4T1x	P	K	4
S-1000C44-N4T1x	P	K	5
S-1000C45-N4T1x	P	K	6
S-1000C46-N4T1x	P	K	7

Remark 1. x: G or U
2. Please select products of environmental code = U for Sn 100%, halogen-free products.

(2) SOT-23-5



(1) to (3) : Product code (refer to **Product name vs. Product code**)
(4) : Lot number

Product name vs. Product code

(a) Nch open-drain output products

Product Name	Product Code		
	(1)	(2)	(3)
S-1000N15-M5T1x	P	L	A
S-1000N16-M5T1x	P	L	B
S-1000N17-M5T1x	P	L	C
S-1000N18-M5T1x	P	L	D
S-1000N19-M5T1x	P	L	E
S-1000N20-M5T1x	P	L	F
S-1000N21-M5T1x	P	L	G
S-1000N22-M5T1x	P	L	H
S-1000N23-M5T1x	P	L	I
S-1000N24-M5T1x	P	L	J
S-1000N25-M5T1x	P	L	K
S-1000N26-M5T1x	P	L	L
S-1000N27-M5T1x	P	L	M
S-1000N28-M5T1x	P	L	N
S-1000N29-M5T1x	P	L	O
S-1000N30-M5T1x	P	L	P

Product Name	Product Code		
	(1)	(2)	(3)
S-1000N31-M5T1x	P	L	Q
S-1000N32-M5T1x	P	L	R
S-1000N33-M5T1x	P	L	S
S-1000N34-M5T1x	P	L	T
S-1000N35-M5T1x	P	L	U
S-1000N36-M5T1x	P	L	V
S-1000N37-M5T1x	P	L	W
S-1000N38-M5T1x	P	L	X
S-1000N39-M5T1x	P	L	Y
S-1000N40-M5T1x	P	L	Z
S-1000N41-M5T1x	P	L	2
S-1000N42-M5T1x	P	L	3
S-1000N43-M5T1x	P	L	4
S-1000N44-M5T1x	P	L	5
S-1000N45-M5T1x	P	L	6
S-1000N46-M5T1x	P	L	7

(b) CMOS output products

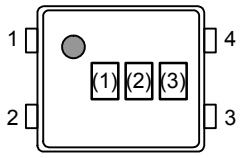
Product Name	Product Code		
	(1)	(2)	(3)
S-1000C15-M5T1x	P	K	A
S-1000C16-M5T1x	P	K	B
S-1000C17-M5T1x	P	K	C
S-1000C18-M5T1x	P	K	D
S-1000C19-M5T1x	P	K	E
S-1000C20-M5T1x	P	K	F
S-1000C21-M5T1x	P	K	G
S-1000C22-M5T1x	P	K	H
S-1000C23-M5T1x	P	K	I
S-1000C24-M5T1x	P	K	J
S-1000C25-M5T1x	P	K	K
S-1000C26-M5T1x	P	K	L
S-1000C27-M5T1x	P	K	M
S-1000C28-M5T1x	P	K	N
S-1000C29-M5T1x	P	K	O
S-1000C30-M5T1x	P	K	P

Product Name	Product Code		
	(1)	(2)	(3)
S-1000C31-M5T1x	P	K	Q
S-1000C32-M5T1x	P	K	R
S-1000C33-M5T1x	P	K	S
S-1000C34-M5T1x	P	K	T
S-1000C35-M5T1x	P	K	U
S-1000C36-M5T1x	P	K	V
S-1000C37-M5T1x	P	K	W
S-1000C38-M5T1x	P	K	X
S-1000C39-M5T1x	P	K	Y
S-1000C40-M5T1x	P	K	Z
S-1000C41-M5T1x	P	K	2
S-1000C42-M5T1x	P	K	3
S-1000C43-M5T1x	P	K	4
S-1000C44-M5T1x	P	K	5
S-1000C45-M5T1x	P	K	6
S-1000C46-M5T1x	P	K	7

Remark 1. x: G or U
2. Please select products of environmental code = U for Sn 100%, halogen-free products.

(3) SNT-4A

SNT-4A
Top view



(1) to (3) : Product code (refer to **Product name vs. Product code**)

Product name vs. Product code

(a) Nch open-drain output products

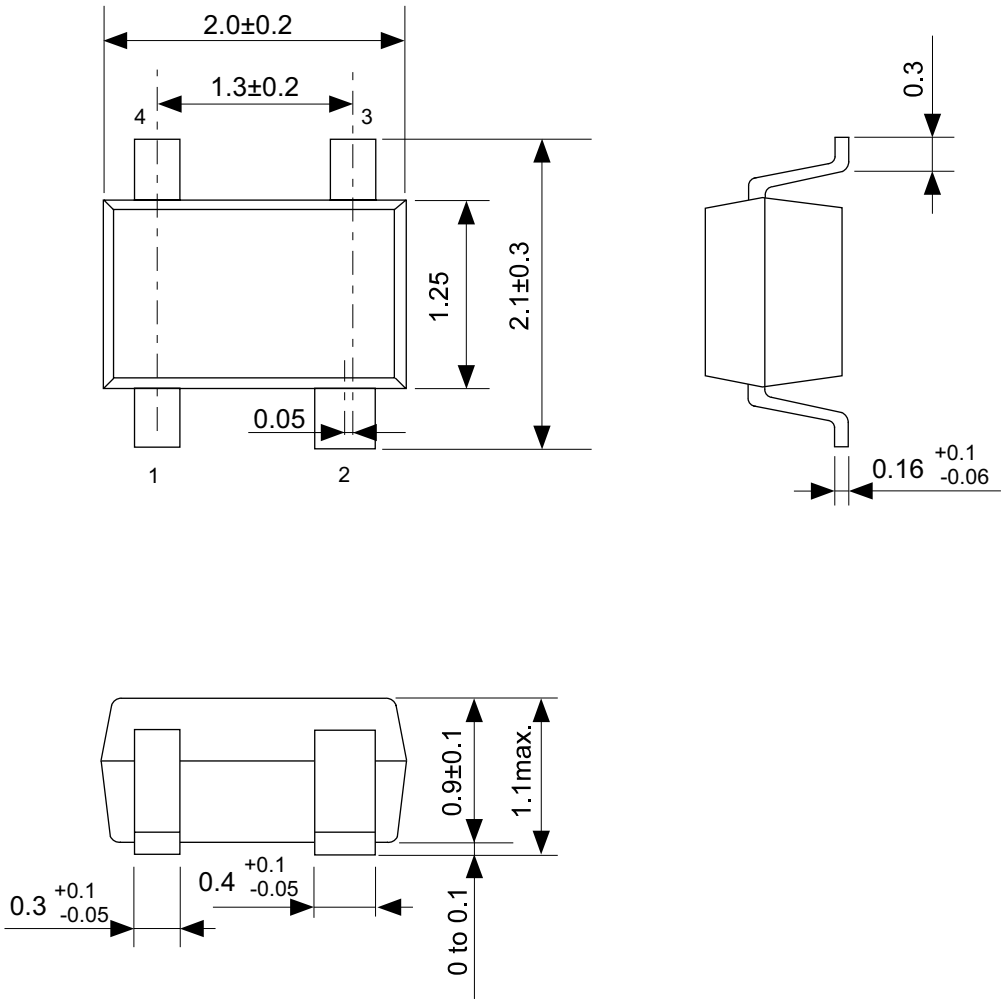
Product Name	Product Code		
	(1)	(2)	(3)
S-1000N15-I4T1U	P	L	A
S-1000N16-I4T1U	P	L	B
S-1000N17-I4T1U	P	L	C
S-1000N18-I4T1U	P	L	D
S-1000N19-I4T1U	P	L	E
S-1000N20-I4T1U	P	L	F
S-1000N21-I4T1U	P	L	G
S-1000N22-I4T1U	P	L	H
S-1000N23-I4T1U	P	L	I
S-1000N24-I4T1U	P	L	J
S-1000N25-I4T1U	P	L	K
S-1000N26-I4T1U	P	L	L
S-1000N27-I4T1U	P	L	M
S-1000N28-I4T1U	P	L	N
S-1000N29-I4T1U	P	L	O
S-1000N30-I4T1U	P	L	P

Product Name	Product Code		
	(1)	(2)	(3)
S-1000N31-I4T1U	P	L	Q
S-1000N32-I4T1U	P	L	R
S-1000N33-I4T1U	P	L	S
S-1000N34-I4T1U	P	L	T
S-1000N35-I4T1U	P	L	U
S-1000N36-I4T1U	P	L	V
S-1000N37-I4T1U	P	L	W
S-1000N38-I4T1U	P	L	X
S-1000N39-I4T1U	P	L	Y
S-1000N40-I4T1U	P	L	Z
S-1000N41-I4T1U	P	L	2
S-1000N42-I4T1U	P	L	3
S-1000N43-I4T1U	P	L	4
S-1000N44-I4T1U	P	L	5
S-1000N45-I4T1U	P	L	6
S-1000N46-I4T1U	P	L	7

(b) CMOS output products

Product Name	Product Code		
	(1)	(2)	(3)
S-1000C15-I4T1U	P	K	A
S-1000C16-I4T1U	P	K	B
S-1000C17-I4T1U	P	K	C
S-1000C18-I4T1U	P	K	D
S-1000C19-I4T1U	P	K	E
S-1000C20-I4T1U	P	K	F
S-1000C21-I4T1U	P	K	G
S-1000C22-I4T1U	P	K	H
S-1000C23-I4T1U	P	K	I
S-1000C24-I4T1U	P	K	J
S-1000C25-I4T1U	P	K	K
S-1000C26-I4T1U	P	K	L
S-1000C27-I4T1U	P	K	M
S-1000C28-I4T1U	P	K	N
S-1000C29-I4T1U	P	K	O
S-1000C30-I4T1U	P	K	P

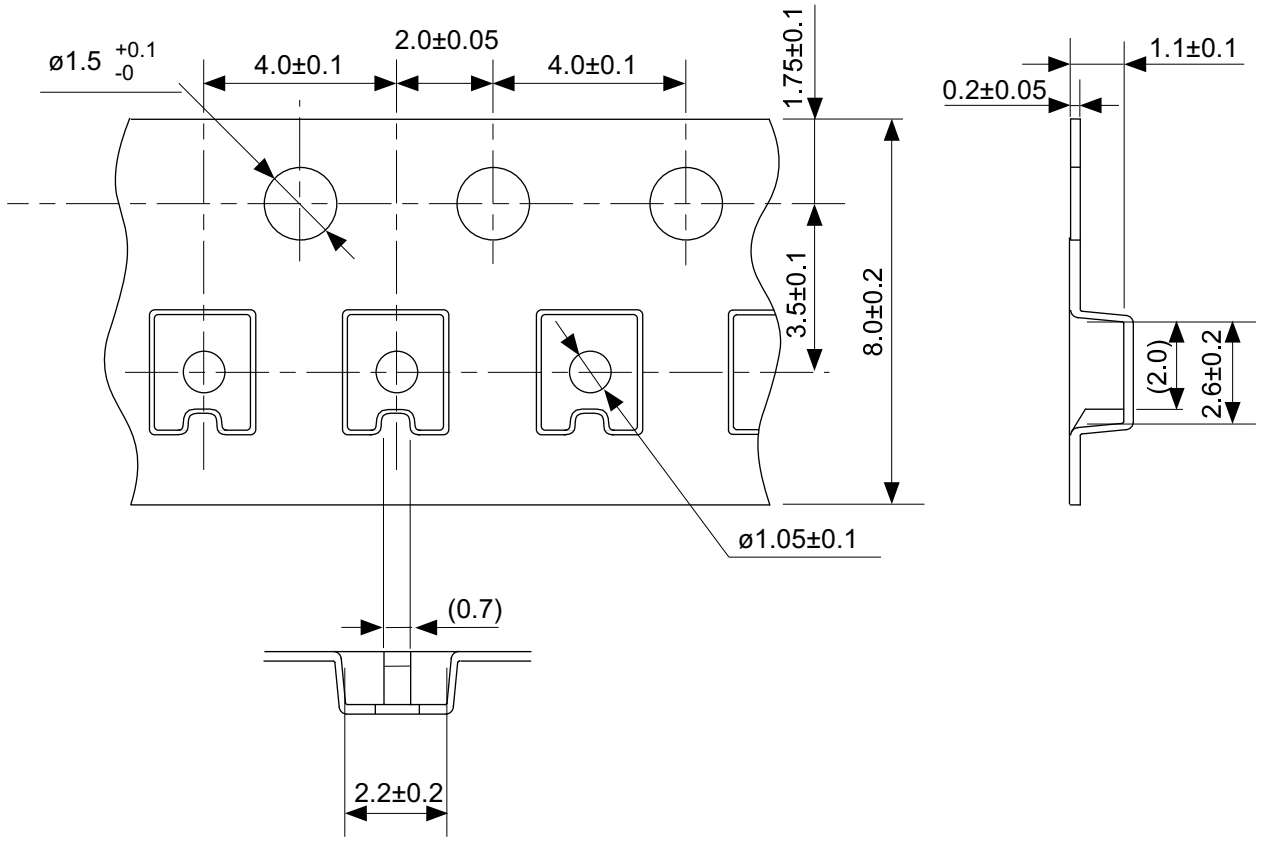
Product Name	Product Code		
	(1)	(2)	(3)
S-1000C31-I4T1U	P	K	Q
S-1000C32-I4T1U	P	K	R
S-1000C33-I4T1U	P	K	S
S-1000C34-I4T1U	P	K	T
S-1000C35-I4T1U	P	K	U
S-1000C36-I4T1U	P	K	V
S-1000C37-I4T1U	P	K	W
S-1000C38-I4T1U	P	K	X
S-1000C39-I4T1U	P	K	Y
S-1000C40-I4T1U	P	K	Z
S-1000C41-I4T1U	P	K	2
S-1000C42-I4T1U	P	K	3
S-1000C43-I4T1U	P	K	4
S-1000C44-I4T1U	P	K	5
S-1000C45-I4T1U	P	K	6
S-1000C46-I4T1U	P	K	7

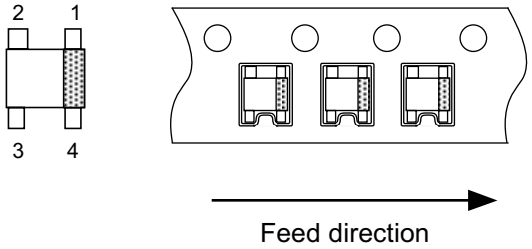


No. NP004-A-P-SD-2.0

TITLE	SC82AB-A-PKG Dimensions
No.	NP004-A-P-SD-2.0
ANGLE	
UNIT	mm

ABLIC Inc.

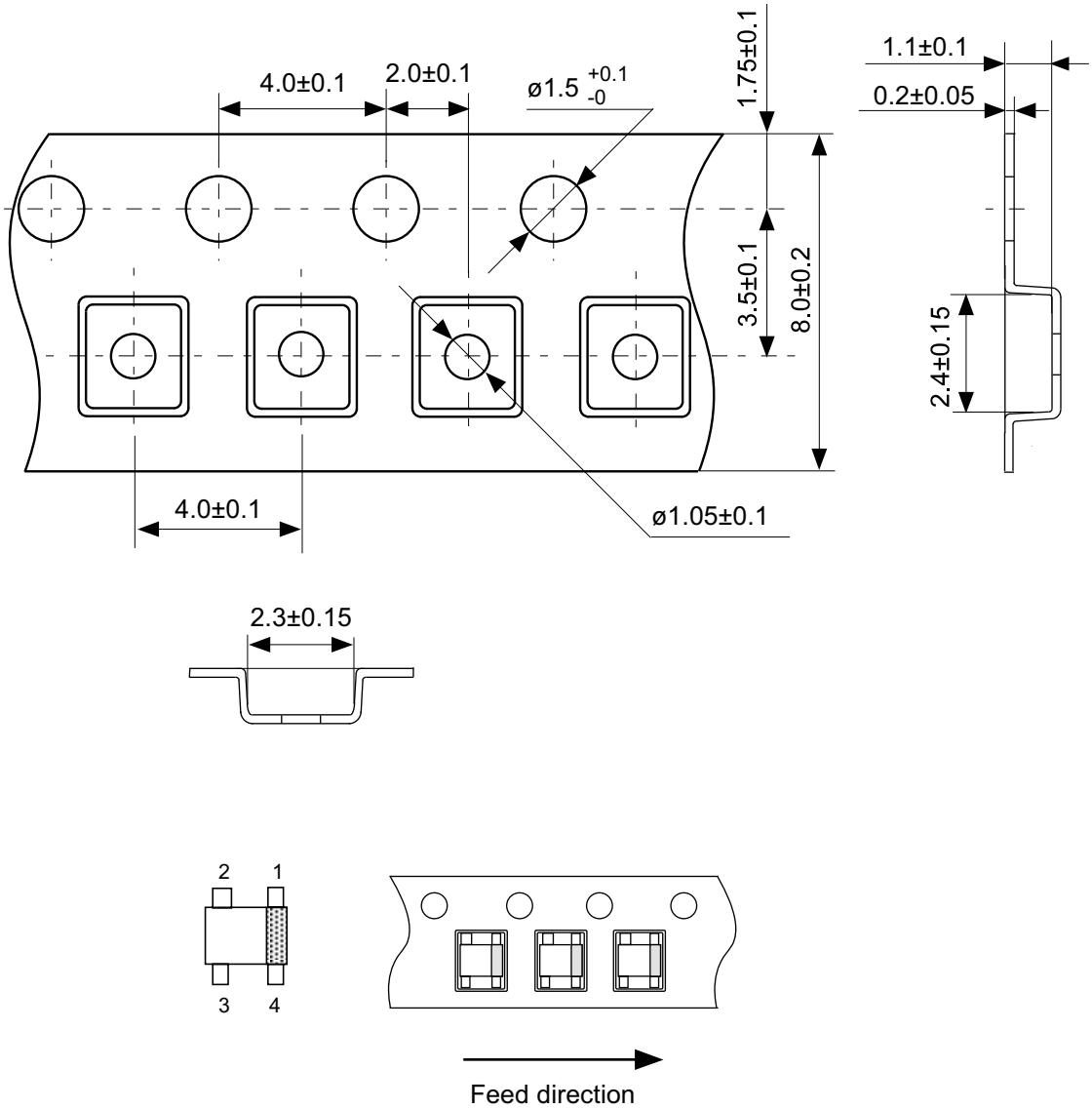




Feed direction

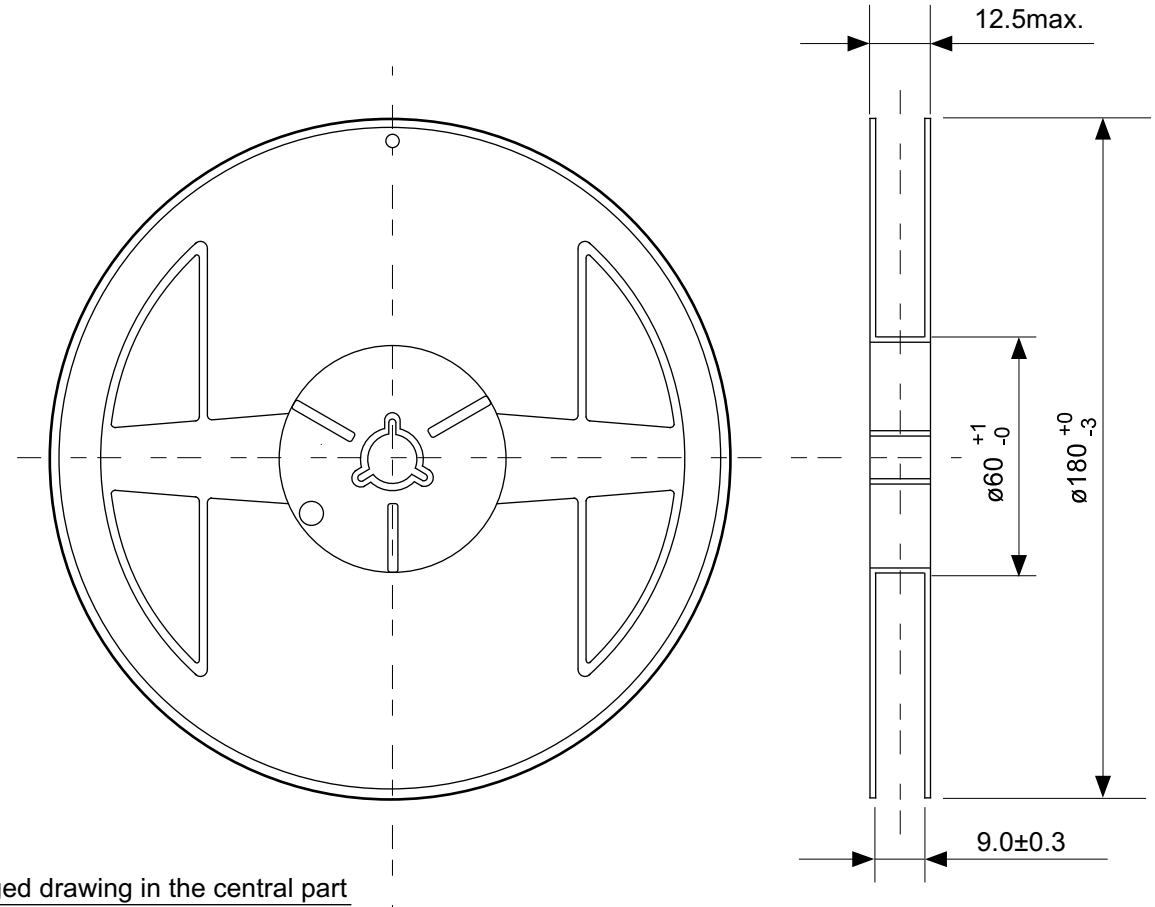
No. NP004-A-C-SD-3.0

TITLE	SC82AB-A-Carrier Tape
No.	NP004-A-C-SD-3.0
ANGLE	
UNIT	mm
ABLIC Inc.	

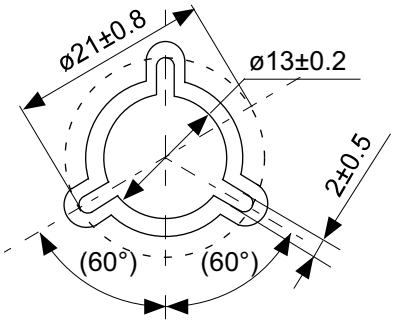


No. NP004-A-C-S1-2.0

TITLE	SC82AB-A-Carrier Tape
No.	NP004-A-C-S1-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

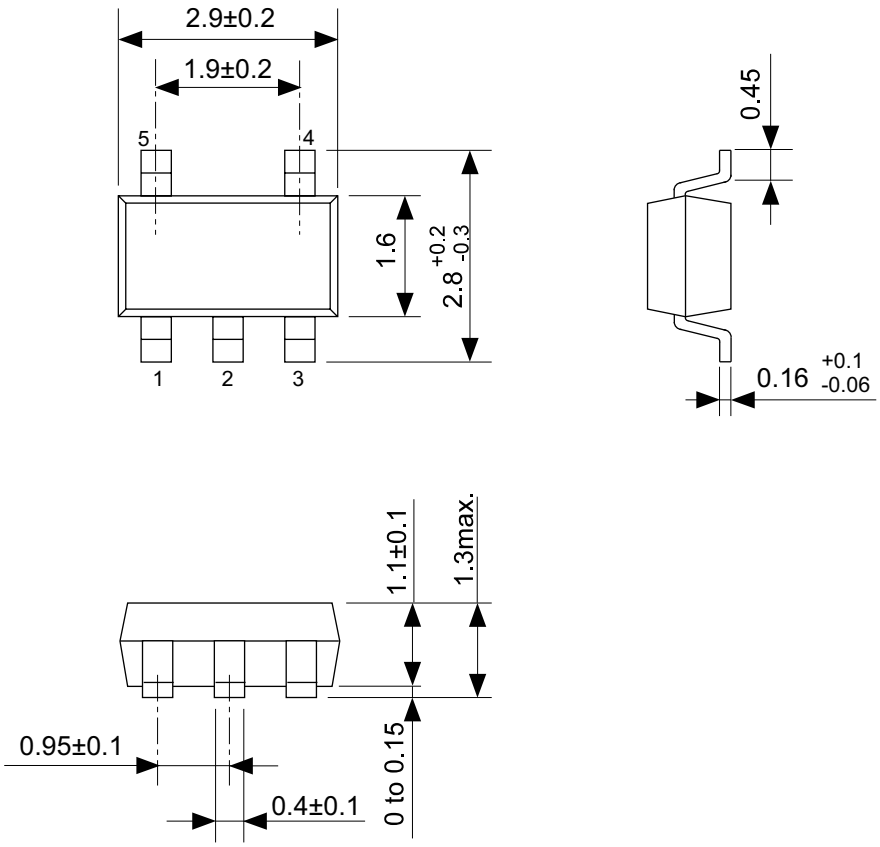


Enlarged drawing in the central part



No. NP004-A-R-SD-1.1

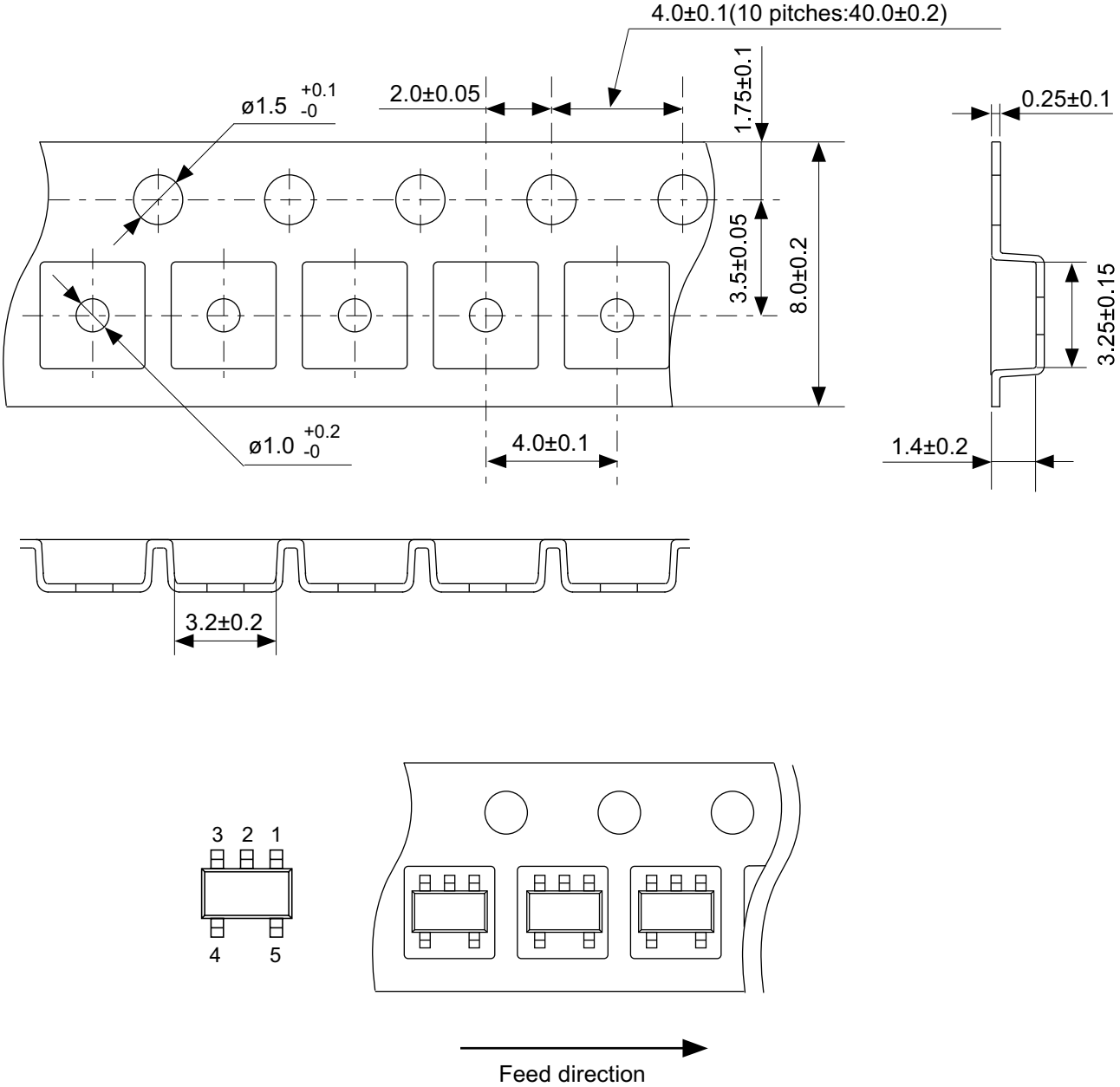
TITLE	SC82AB-A-Reel		
No.	NP004-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
	ABLIC Inc.		



No. MP005-A-P-SD-1.3

TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.3
ANGLE	
UNIT	mm

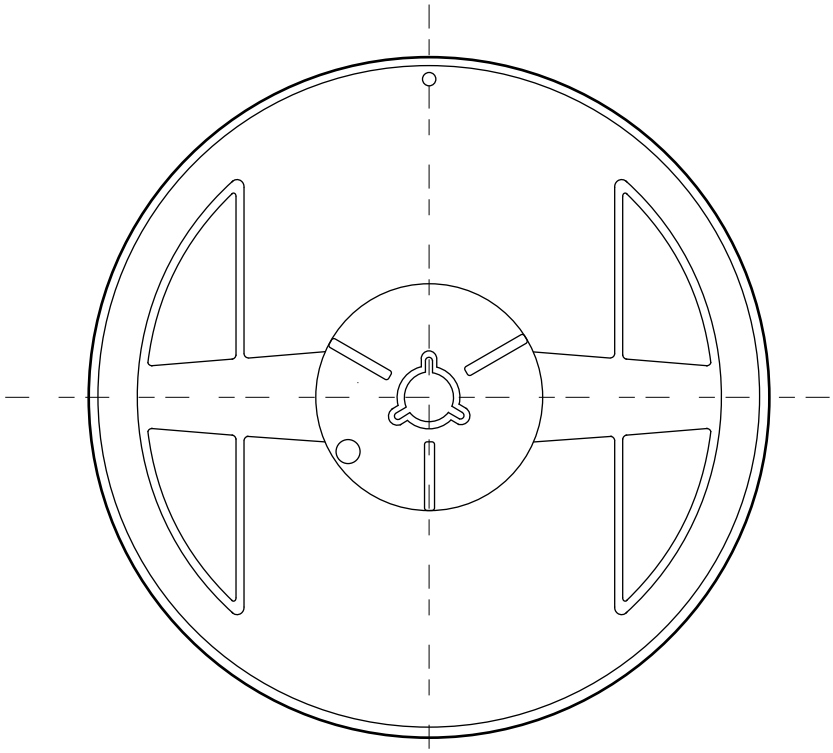
ABLIC Inc.

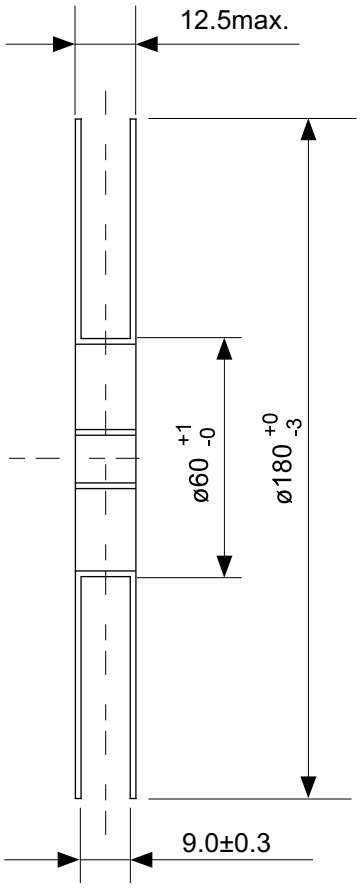


No. MP005-A-C-SD-2.1

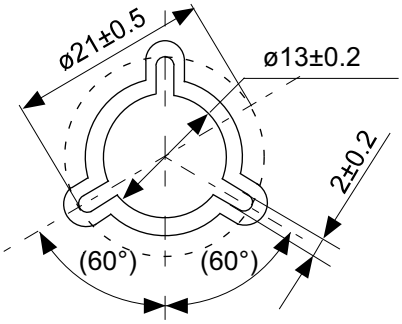
TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
ANGLE	
UNIT	mm

ABLIC Inc.



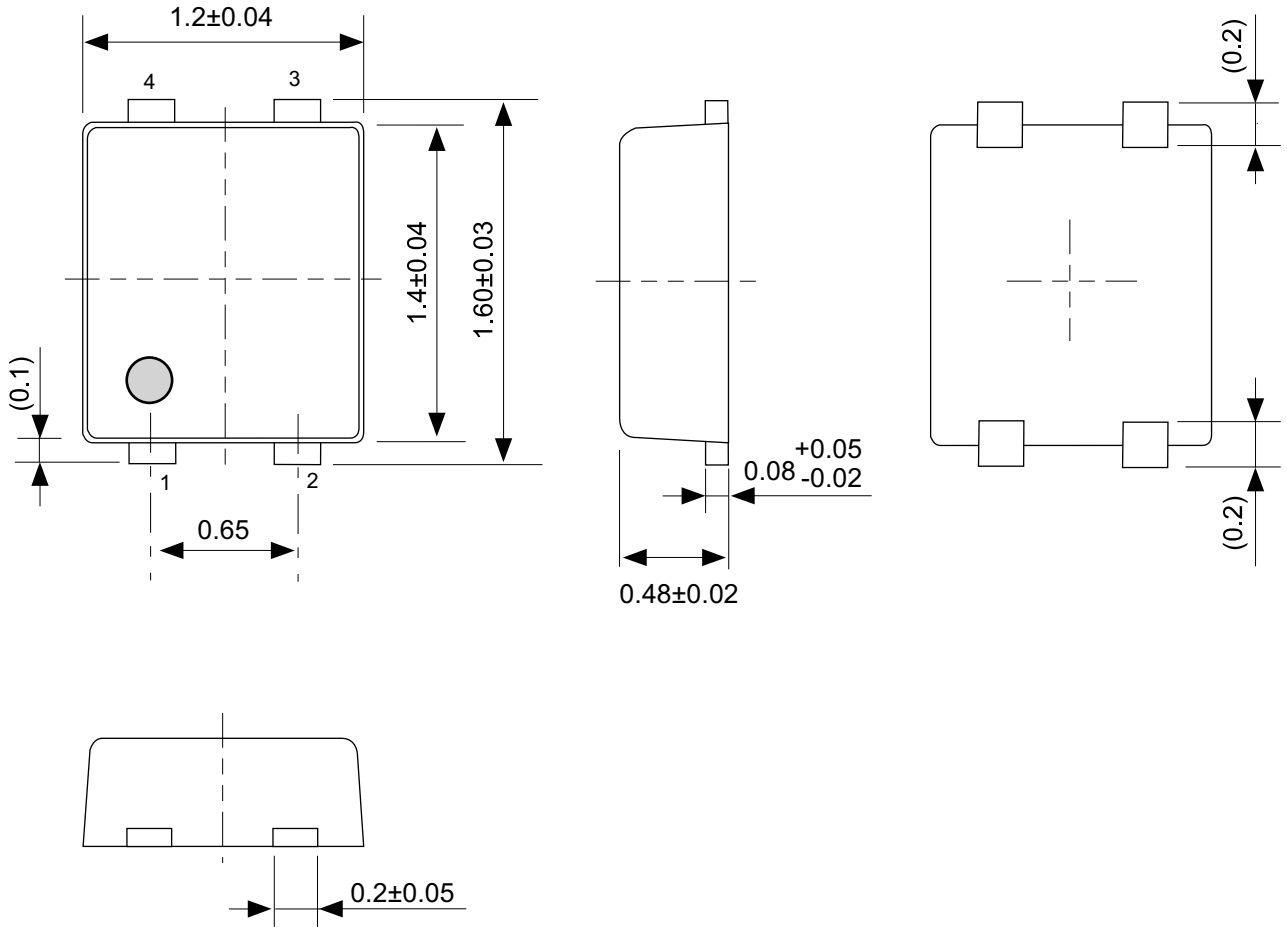


Enlarged drawing in the central part



No. MP005-A-R-SD-1.1

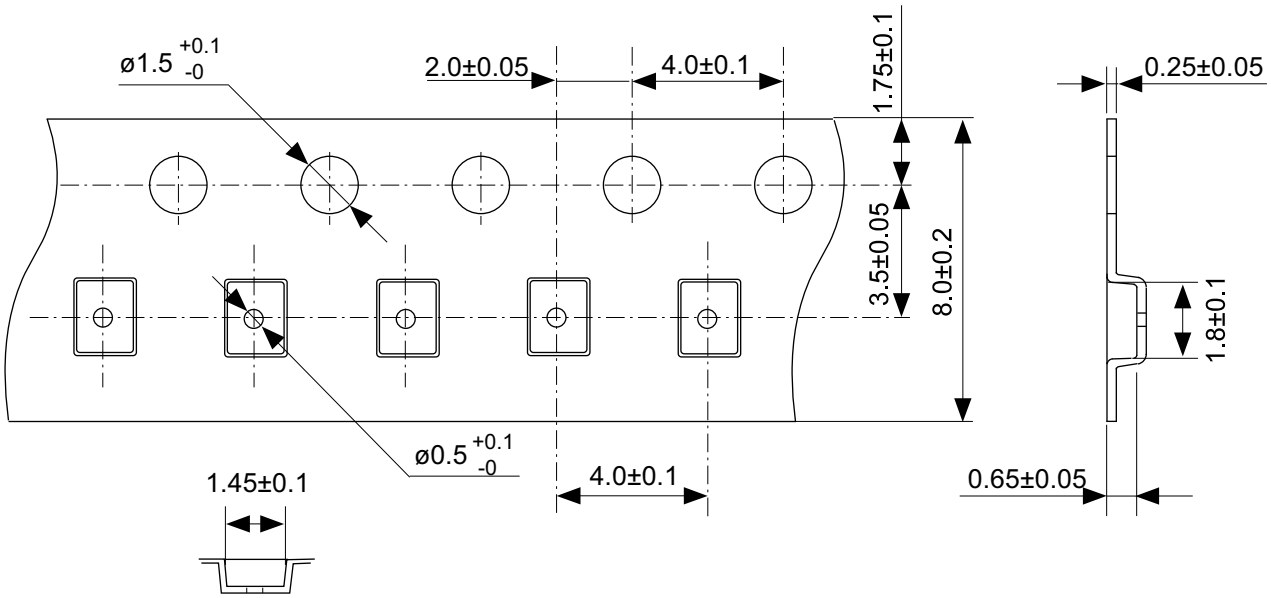
TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			

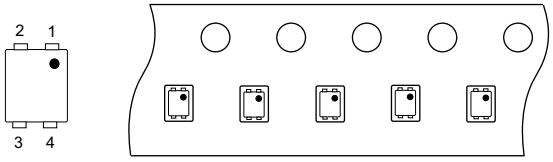


No. PF004-A-P-SD-6.0

TITLE	SNT-4A-A-PKG Dimensions
No.	PF004-A-P-SD-6.0
ANGLE	
UNIT	mm

ABLIC Inc.



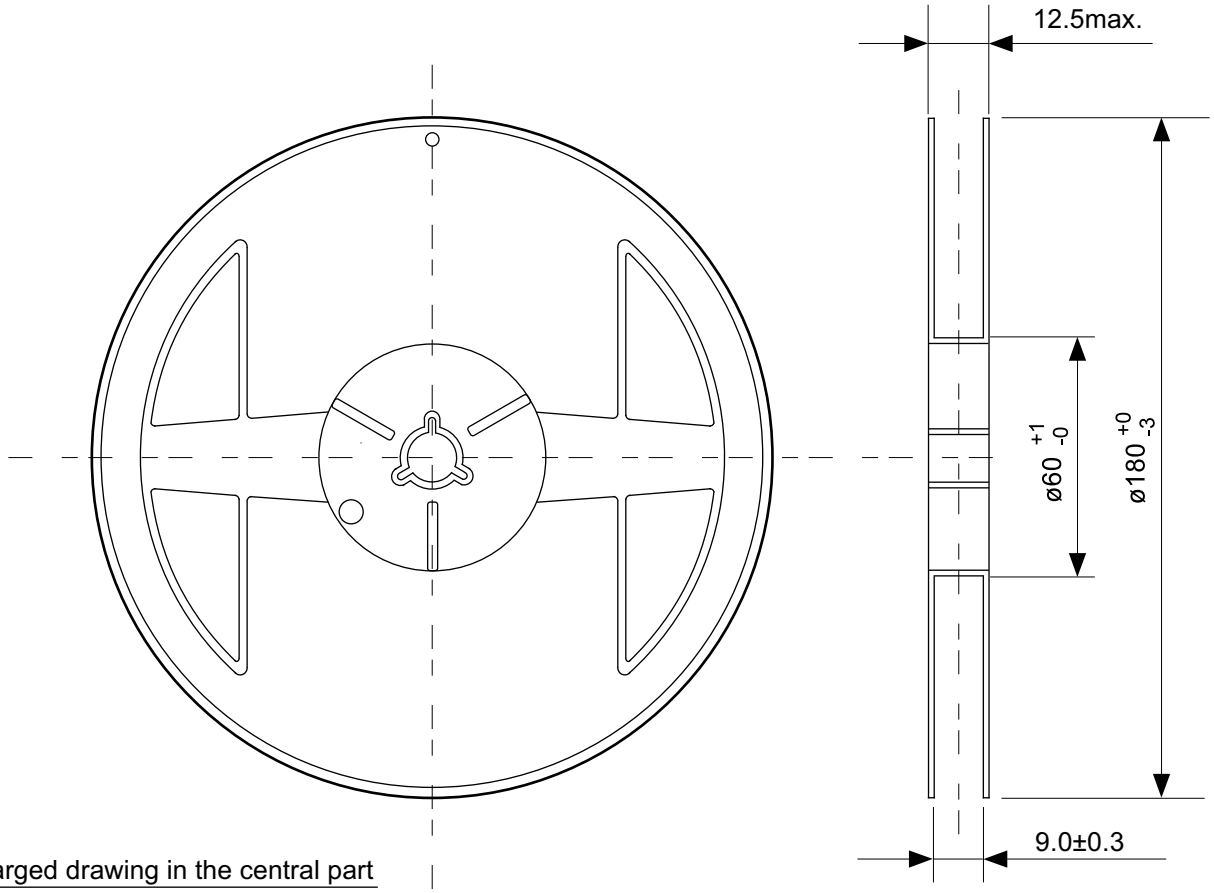


Feed direction

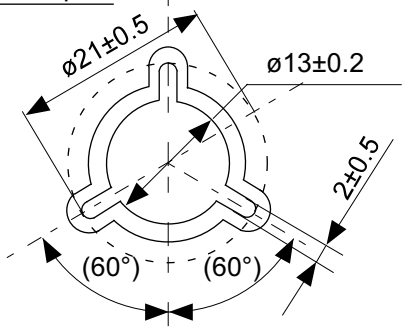
No. PF004-A-C-SD-2.0

TITLE	SNT-4A-A-Carrier Tape
No.	PF004-A-C-SD-2.0
ANGLE	
UNIT	mm

ABLIC Inc.

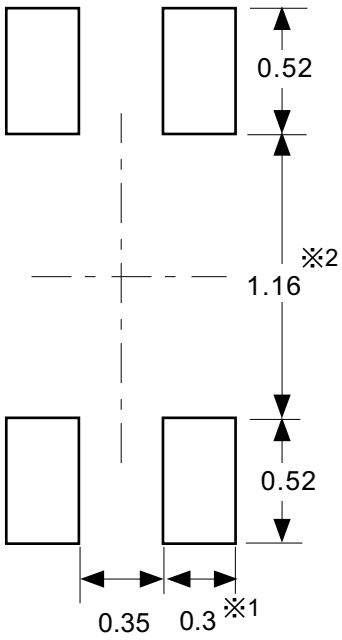


Enlarged drawing in the central part



No. PF004-A-R-SD-1.0

TITLE	SNT-4A-A-Reel		
No.	PF004-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.10 mm ~ 1.20 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から**0.03 mm** 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は "SNTパッケージ活用の手引き" を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.10 mm to 1.20 mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.10 mm ~ 1.20 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PF004-A-L-SD-4.1

TITLE	SNT-4A-A -Land Recommendation
No.	PF004-A-L-SD-4.1
ANGLE	
UNIT	mm

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