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December 2013

FDH44N50

N-Channel SMPS Power MOSFET

500 V, 44 A, 120 mΩ

Features

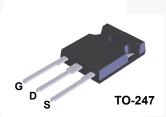
- \bullet Low Gate Charge Q_g Results in Simple Drive Requirement (Typ. 90 nC)
- Improved Gate, Avalanche and High Reapplied dv/dt Ruggedness
- Reduced $R_{DS(on)}$ (110 m Ω (Typ.) @ V_{GS} = 10 V, I_D = 22 A)
- Reduced Miller Capacitance and Low Input Capacitance (Typ. C_{rss} = 40 pF)
- Improved Switching Speed with Low EMI
- 175°C Rated Junction Temperature

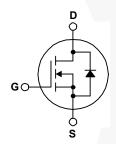
Description

UniFETTM MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

Applications

- Lighting
- · Uninterruptible Power Supply
- AC-DC Power Supply





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter	FDH44N50	Unit	
V _{DSS}	Drain to Source Voltage	500	V	
V _{GS}	Gate to Source Voltage	±30	V	
	Drain Current			
I _D	Continuous ($T_C = 25^{\circ}C$, $V_{GS} = 10 \text{ V}$)	44	Α	
	Continuous ($T_C = 100$ °C, $V_{GS} = 10 \text{ V}$)	32	Α	
	Pulsed ¹	176	Α	
В	Power Dissipation	750	W	
P _D Derate Above 25°C	5	W/ºC		
Γ _J , Τ _{STG}	Operating and Storage Temperature	-55 to 175	°C	
Soldering Temperature for 10 Seconds Mounting Torque, 8-32 or M3 Screw		300 (1.6mm from case)	°C	
		10ibf*in (1.1N*m)		

Thermal Characteristics

Symbol	Parameter	FDH44N50	Unit	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.2	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	°C/W	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDH44N50	FDH44N50	TO-247	Tube	N/A	N/A	30 units

Electrical Characteristics

Symbol	Parameter	ameter Test Conditions		Min.	Тур.	Max.	Unit
atics							
B _{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$		500	-	-	V
ΔB _{VDSS} / ΔT _{.I}	Breakdown Voltage Temp. Coefficient	Reference to 25°C,		-	0.61	-	V/°(
r _{DS(ON)}	Drain to Source On-Resistance	V _{GS} = 10 V, I _D = 22 A		-	0.11	0.12	Ω
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} =$	= 250 µA	2	3.15	4	V
	7 0 1 1/1 5 1 0 1	V _{DS} = 500 V	$T_{\rm C} = 25^{\rm o}{\rm C}$	-	-	25	
I _{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0 V$	$T_{\rm C} = 150^{\rm o}{\rm C}$	-	-	250	μΑ
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V		-	-	±100	nA
/namics							
9 _{fs}	Forward Transconductance	V _{DS} = 50 V, I _D	= 22 A	11	-	-	S
Q _{g(TOT)}	Total Gate Charge at 10V	V _{GS} = 10 V, V _{DS} = 400 V, I _D = 44 A		-	90	108	nC
Q _{gs}	Gate to Source Gate Charge			-	24	29	nC
Q _{gd}	Gate to Drain "Miller" Charge			-	31	37	nC
t _{d(ON)}	Turn-On Delay Time	$V_{DD} = 250 \text{ V},$ $I_{D} = 44 \text{ A},$ $R_{G} = 2.15 \Omega,$ $R_{D} = 5.68 \Omega$		-/	16	-	ns
t _r	Rise Time			- \	84	-	ns
t _{d(OFF)}	Turn-Off Delay Time			-	45	-	ns
t _f	Fall Time			-	79	-	ns
C _{ISS}	Input Capacitance	V _{DS} = 25V, V _{GS} = 0 V, f = 1 MHz		-	5335	-	pF
Coss	Output Capacitance			-	645	-	pF
C _{RSS}	Reverse Transfer Capacitance			-	40	-	pF
/alanch	e Characteristics			•			
E _{AS}	Single Pulse Avalanche Energy ²			1500	-	-	m
I _{AR}	Avalanche Current			-	-	44	Α
	rce Diode Characteristics						
I _S	Continuous Source Current	MOSFET symbol		- 7	_	44	A
I _{SM}	(Body Diode) Pulsed Source Current ¹ (Body Diode)	showing the integral reverse p-n junction diode.		-	-	176	A

I_{SD} = 44 A

 $I_{SD} = 44 \text{ A}, dI_{SD}/dt = 100 \text{ A/}\mu\text{s}$

 $I_{SD} = 44 \text{ A}, dI_{SD}/dt = 100 \text{ A}/\mu\text{s}$

 V_{SD}

 t_{rr}

 Q_{RR}

1: Repetitive rating; pulse-width limited by maximum junction temperature. 2: Starting T_J = 25°C, L = 1.61 mH, I_{AS} = 44 A

Reverse Recovered Charge

Source to Drain Diode Voltage

Reverse Recovery Time

0.900

920

14

1.2

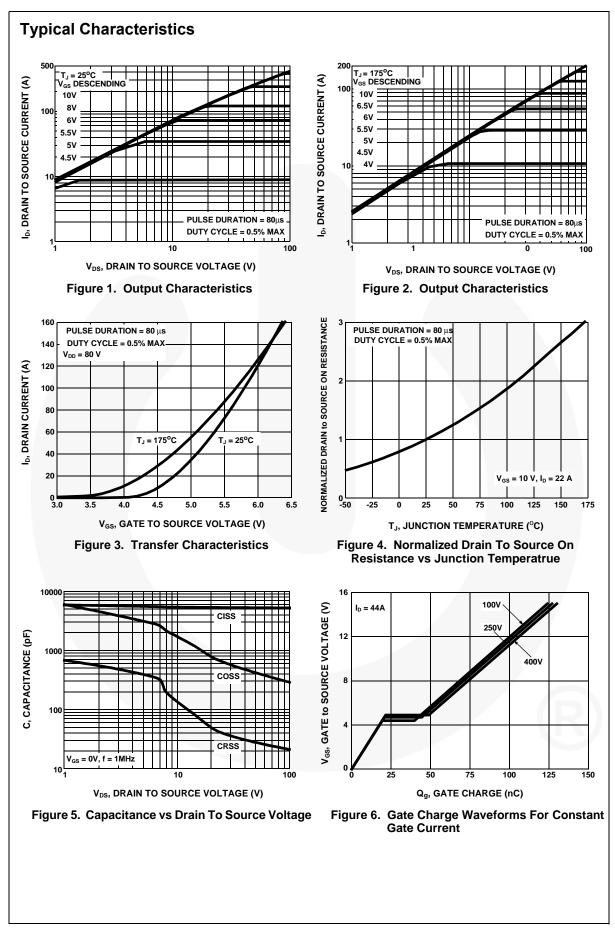
1100

18

٧

ns

μС



Typical Characteristics (Continued)

Figure 7. Body Diode Forward Voltage vs Body Diode Current

V_{SD}, SOURCE TO DRAIN VOLTAGE (V)

Figure 8. Maximum Safe Operating Area

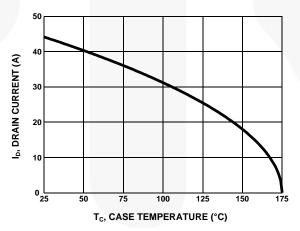


Figure 9. Maximum Drain Current vs Case Temperature

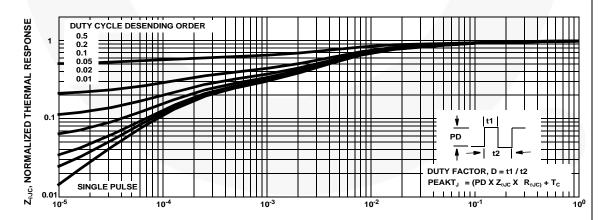


Figure 10. Normalized Transient Thermal Impedance, Junction to Case

t1, RECTANGULAR PULSE DURATION (S)

Test Circuits and Waveforms

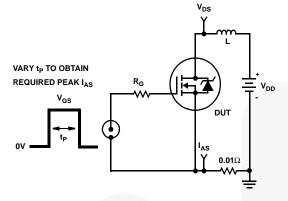


Figure 11. Unclamped Energy Test Circuit

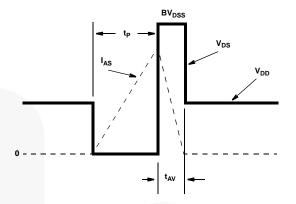


Figure 12. Unclamped Energy Waveforms

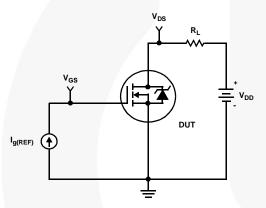


Figure 13. Gate Charge Test Circuit

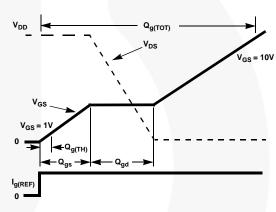


Figure 14. Gate Charge Waveforms

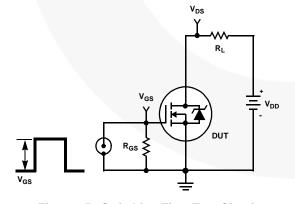


Figure 15. Switching Time Test Circuit

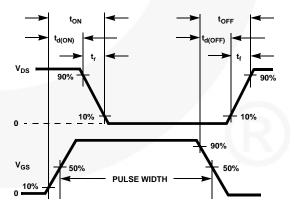
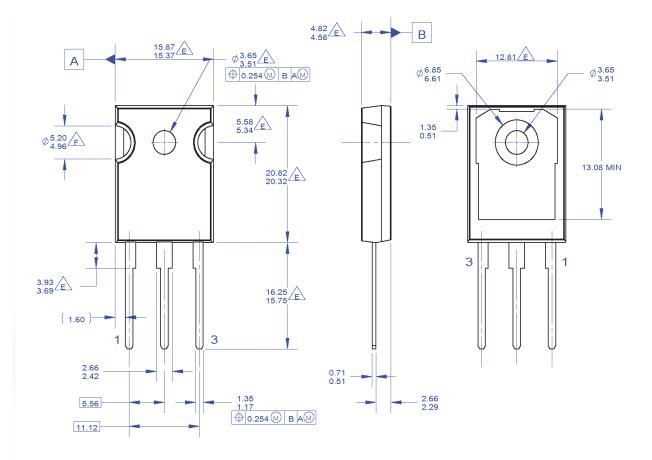


Figure 16. Switching Time Waveform

Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. PACKAGE REFERENCE: JEDEC TO-247, ISSUE E, VARIATION AB, DATED JUNE, 2004.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
 D. DRAWING CONFORMS TO ASME Y14.5 1994

E DOES NOT COMPLY JEDEC STANDARD VALUE

NOTCH MAY BE SQUARE

DRAWING FILENAME: MKT-TO247A03_REV03

Figure 17. TO-247, Molded, 3-Lead, Jedec Variation AB

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