CY7C9689A

TAXI™-compatible HOTLink® Transceiver

Features

- Second-generation HOTLink® technology
- AMD™ AM7968/7969 TAXIchip™-compatible
- 8-bit 4B/5B or 10-bit 5B/6B NRZI encoded data transport
- 10-bit or 12-bit NRZI pre-encoded (bypass) data transport
- Synchronous TTL parallel interface
- Embedded/bypassable 256-character Transmit and Receive FIFOs
- 50- to 200-MBaud serial signaling rate
- Internal phase-locked loops (PLLs) with no external PLL components
- Dual differential PECL-compatible serial inputs and outputs
- Compatible with fiber-optic modules and copper cables
- Built-in self-test (BIST) for link testing
- Link Quality Indicator
- Single +5.0 V ±10%supply
- 100-pin TQFP
- Pb-free package option available

Functional Description

The CY7C9689A HOTLink Transceiver is a point-to-point communications building block allowing the transfer of data over high-speed serial links (optical fiber, balanced, and unbalanced copper transmission lines) at speeds ranging between 50 and 200 MBaud. The transmit section accepts parallel data of selectable widths and converts it to serial data, while the receiver section accepts serial data and converts it to parallel data of selectable widths. Figure 1 illustrates typical connections between two independent host systems and corresponding CY7C9689A parts. The CY7C9689A provides enhanced technology, increased functionality, a higher level of integration, higher data rates, and lower power dissipation over the AMD AM7968/7969 TAXIchip products.

The transmit section of the CY7C9689A HOTLink can be configured to accept either 8- or 10-bit data characters on each clock cycle, and stores the parallel data into an internal synchronous Transmit FIFO. Data is read from the Transmit FIFO and is encoded using embedded 4B/5B or 5B/6B encoders to improve its serial transmission characteristics. These encoded characters are then serialized, converted to NRZI, and output from two PECL-compatible differential transmission line drivers at a bit-rate of either 10 or 20 times the input reference clock in 8-bit (or 10-bit bypass) mode, or 12 or 24 times the reference clock in 10-bit (or 12-bit bypass) mode.

The receive section of the CY7C9689A HOTLink accepts a serial bit-stream from one of two PECL compatible differential line receivers and, using a completely integrated PLL clock synchronizer, recovers the timing information necessary for data reconstruction. The recovered bit stream is converted from NRZI to NRZ, deserialized, framed into characters, 4B/5B or 5B/6B decoded, and checked for transmission errors. The recovered 8- or 10-bit decoded characters are then written to an internal Receive FIFO, and presented to the destination host system.

The integrated 4B/5B and 5B/6B encoder/decoder may be bypassed (disabled) for systems that present externally encoded or scrambled data at the parallel interface. With the encoder bypassed, the pre-encoded parallel data stream is converted to and from a serial NRZI stream. The embedded FIFOs may also be bypassed (disabled) to create a reference-locked serial transmission link. For those systems requiring even greater FIFO storage capability, external FIFOs may be directly coupled to the CY7C9689A through the parallel interface without the need for additional glue-logic.

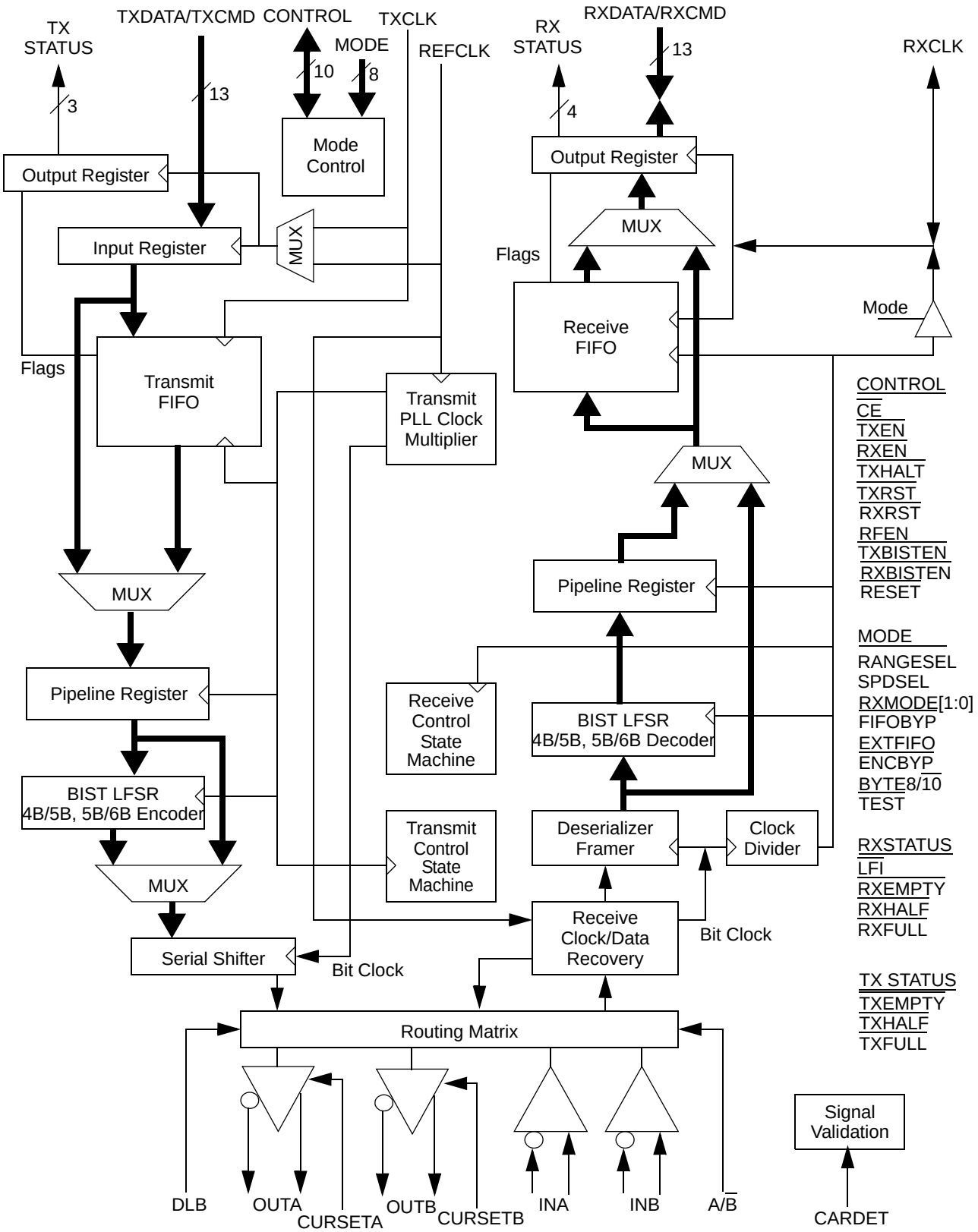
The TTL parallel I/O interface may be configured as either a FIFO (configurable for depth expansion through external FIFOs) or as a pipeline register extender. The FIFO configurations are optimized for transport of time-independent (asynchronous) 8- or 10-bit character-oriented data across a link. A Built-In Self-Test (BIST) pattern generator and checker allows for testing of the high-speed serial data paths in both the transmit and receive sections, and across the interconnecting links.

HOTLink devices are ideal for a variety of applications where parallel interfaces can be replaced with high-speed, point-to-point serial links. Some applications include interconnecting workstations, backplanes, servers, mass storage, and video transmission equipment.

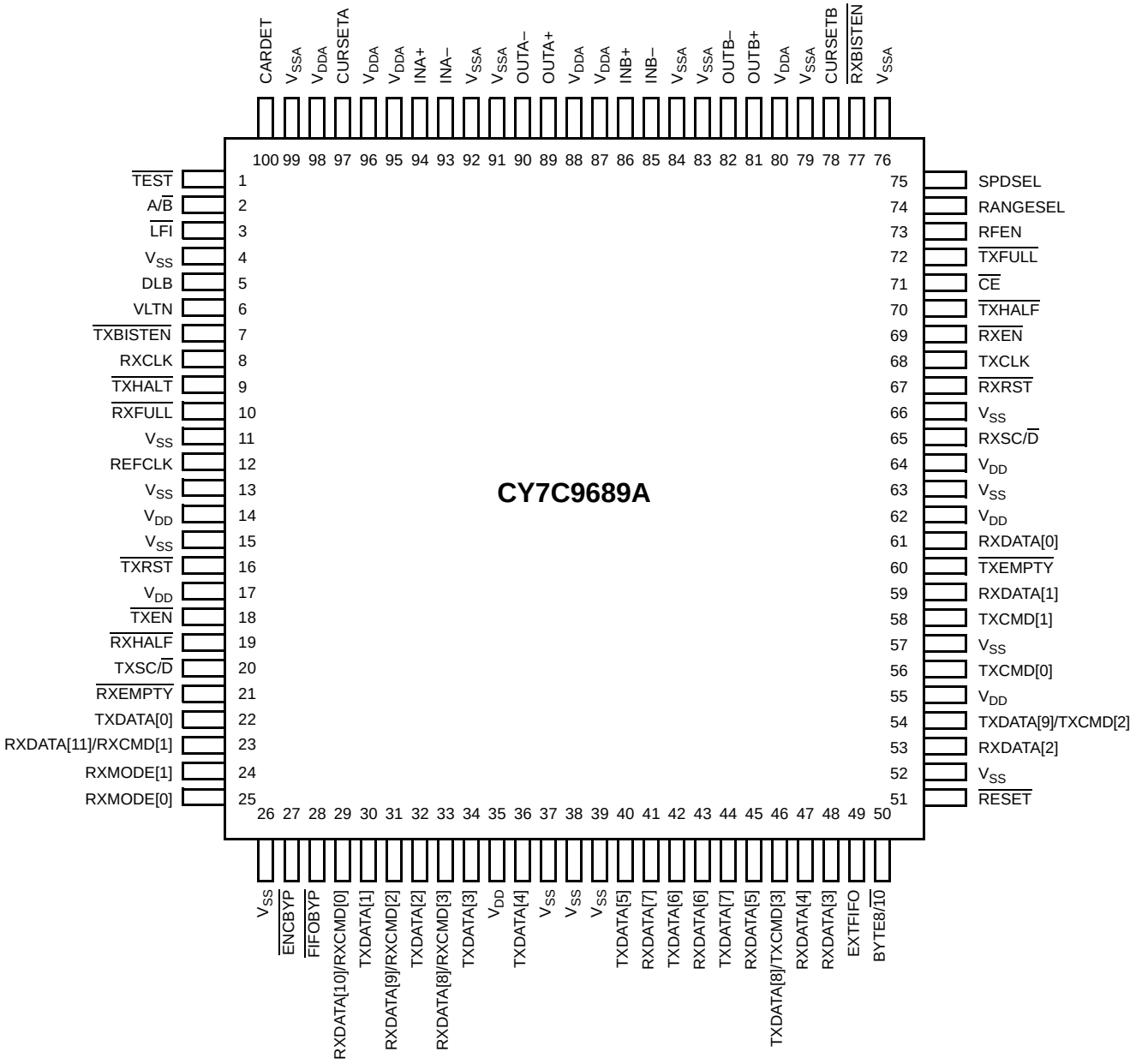
Contents

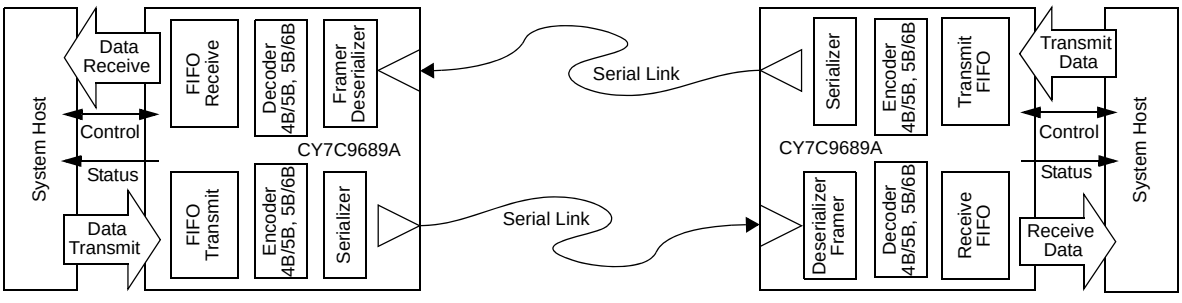
Figure 1. HOTLink System Connections

TAXI™ HOTLink Transceiver Logic Block Diagram



Pin Configuration





Pin Descriptions

Pin	Name	I/O Characteristics	Signal Description
Transmit Path Signals			
68	TXCLK	TTL clock input Internal Pull-up	Transmit FIFO Clock. Used to sample all Transmit FIFO and related interface signals.
44, 42, 40, 36, 34, 32, 30, 22	TXDATA[7:0]	TTL input, sampled on TXCLK↑ or REFCLK↑ Internal Pull-up	Parallel Transmit DATA Input. When selected (CE = LOW and TXEN = asserted), information on these inputs is processed as DATA when TXSC/D is LOW and ignored otherwise. When the encoder is bypassed (ENCBYP is LOW), TXDATA[7:0] functions as the least significant eight bits of the 10- or 12-bit pre-encoded transmit character. When the Transmit FIFO is enabled (FIFOBYP is HIGH), these inputs are sampled on the rising edge of TXCLK. When the Transmit FIFO is bypassed (FIFOBYP is LOW) these inputs are captured on the rising edge of REFCLK.
54, 46	TXDATA[9:8]/ TXCMD[2:3]	TTL input, sampled on TXCLK↑ or REFCLK↑ Internal Pull-up	Parallel Transmit DATA or COMMAND Input. When selected, BYTE8/10 is HIGH, and the encoder is enabled ($\overline{\text{ENCBYP}}$ is HIGH), information on these inputs are processed as TXCMD[2:3] if TXSC/D is HIGH and ignored otherwise. When selected, BYTE8/10 is LOW, and the encoder is enabled ($\overline{\text{ENCBYP}}$ is HIGH), information on these inputs are processed as TXDATA[9:8] if TXSC/D is LOW and ignored otherwise. When the encoder is bypassed ($\overline{\text{ENCBYP}}$ is LOW), TXDATA[9:8] functions as the 9th and 10th bits of the 10- or 12-bit pre-encoded transmit character. When the Transmit FIFO is enabled (FIFOBYP is HIGH), these inputs are sampled on the rising edge of TXCLK. When the Transmit FIFO is bypassed (FIFOBYP is LOW), these inputs are captured on the rising edge of REFCLK.
58, 56	TXCMD[1:0]	TTL input, sampled on TXCLK↑ or REFCLK↑ Internal Pull-up	Parallel Transmit COMMAND Input. When selected and the encoder is enabled ($\overline{\text{ENCBYP}}$ is HIGH), information on these inputs is processed as a COMMAND when TXSC/D is HIGH and ignored otherwise. When BYTE8/10 is HIGH and the encoder is bypassed ($\overline{\text{ENCBYP}}$ is LOW), the TXCMD[1:0] inputs are ignored. When BYTE8/10 is LOW and when the encoder is bypassed ($\overline{\text{ENCBYP}}$ is LOW), the TXCMD[1:0] inputs function as the 11th and 12th (MSB) bits of the 12-bit pre-encoded transmit character. When the Transmit FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH), these inputs are sampled on the rising edge of TXCLK. When the Transmit FIFO is bypassed ($\overline{\text{FIFOBYP}}$ is LOW), these inputs are sampled on the rising edge of REFCLK.
20	TXSC/$\overline{\text{D}}$	TTL input, sampled on TXCLK↑ or REFCLK↑ Internal Pull-up	COMMAND or DATA input selector. When selected, BYTE8/10 is HIGH, and the encoder is enabled ($\overline{\text{ENCBYP}}$ is HIGH), this input selects if the DATA or COMMAND inputs are processed. If TXSC/D is HIGH, the value on TXCMD[3:0] is captured as one of sixteen possible COMMANDs, and the data on the TXDATA[7:0] bits are ignored. If TXSC/D is LOW, the information on TXDATA[7:0] is captured as one of 256 possible 8-bit DATA values, and the information on the TXCMD[3:0] bus is ignored. When BYTE8/10 is LOW and the encoder is enabled (ENCBYP is HIGH) this input selects if the DATA or COMMAND inputs are processed. If TXSC/D is HIGH, the information on TXCMD[1:0] is captured as one of four possible COMMANDs, and the information on the TXDATA[9:0] bits are ignored. If TXSC/D is LOW, the information on TXDATA[9:0] is captured as one of 1024 possible 10-bit DATA values, and the information on the TXCMD[1:0] bus is ignored. When the encoder is bypassed (ENCBYP is LOW) TXSC/$\overline{\text{D}}$ is ignored

Pin Descriptions (continued)

Pin	Name	I/O Characteristics	Signal Description
18	$\overline{\text{TXEN}}$	TTL input, sampled on TXCLK↑ or REFCLK↑ Internal Pull-up	Transmit Enable. $\overline{\text{TXEN}}$ is sampled on the rising edge of the TXCLK or REFCLK input and enables parallel data bus write operations (when selected). The device is selected when $\overline{\text{TXEN}}$ is asserted during a clock cycle immediately following one in which $\overline{\text{CE}}$ is sampled LOW. Depending on the level on EXTFIFO, the asserted state for $\overline{\text{TXEN}}$ can be active HIGH or active LOW. If EXTFIFO is LOW, then $\overline{\text{TXEN}}$ is active LOW and data is captured on the same clock cycle where $\overline{\text{TXEN}}$ is sampled LOW. If EXTFIFO is HIGH, then $\overline{\text{TXEN}}$ is active HIGH and data is captured on the clock cycle following any clock edge when $\overline{\text{TXEN}}$ is sampled HIGH.
7	$\overline{\text{TXBISTEN}}$	TTL input, asynchronous Internal Pull-up	Transmitter BIST Enable. When $\overline{\text{TXBISTEN}}$ is LOW, the transmitter generates a 511-character repeating sequence that can be used to validate link integrity. This 4B/5B BIST sequence is generated regardless of the state of other configuration inputs. The transmitter returns to normal operation when $\overline{\text{TXBISTEN}}$ is HIGH. All Transmit FIFO read operations are suspended when BIST is active.
16	$\overline{\text{TXRST}}$	TTL input, sampled on TXCLK↑ Internal Pull-up	Reset Transmit FIFO. When the Transmit FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH), $\overline{\text{TXEN}}$ is deasserted, $\overline{\text{CE}}$ is asserted (LOW), and $\overline{\text{TXRST}}$ is sampled LOW by TXCLK for seven cycles, the Transmit FIFO begins its internal reset process. The Transmit FIFO TXFULL flag is asserted and the host interface counter and address pointer are zeroed. This reset propagates to the serial transmit side, any remaining counters and pointers. The TXFULL flag is asserted until both sides of the Transmit FIFO have reset. While $\overline{\text{TXRST}}$ remains asserted, the Transmit FIFO remains in reset and the TXFULL output remains asserted. When the Transmit FIFO is bypassed ($\overline{\text{FIFOBYP}}$ is LOW), $\overline{\text{TXRST}}$ is ignored.
9	$\overline{\text{TXHALT}}$	TTL input, sampled on TXCLK↑ Internal Pull-up	Transmitter Halt Control Input. When $\overline{\text{TXHALT}}$ is asserted LOW, transmission of data is suspended and the HOTLink TAXI transmits SYNC characters. When $\overline{\text{TXHALT}}$ is deasserted HIGH, normal data processing proceeds. If the Transmit FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH), the interface is allowed to continue loading data into the Transmit FIFO while $\overline{\text{TXHALT}}$ is asserted.
72	$\overline{\text{TXFULL}}$	Three-state TTL output, changes following TXCLK↑ or REFCLK↑	Transmit FIFO Full Status Flag. When the Transmit FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH) and its flags are driven ($\overline{\text{CE}}$ is LOW), $\overline{\text{TXFULL}}$ is asserted when four or fewer characters can be written to the HOTLink Transmit FIFO. If a Transmit FIFO reset has been initiated ($\overline{\text{TXRST}}$ was sampled asserted for a minimum of seven TXCLK cycles), $\overline{\text{TXFULL}}$ is asserted to enforce the full/unavailable status of the Transmit FIFO during reset. When the Transmit FIFO is bypassed (FIFOBYP is LOW), the $\overline{\text{TXFULL}}$ output changes after the rising edge of REFCLK. $\overline{\text{TXFULL}}$ is asserted when the transmitter is BUSY (not accepting a new data or command characters) and deasserted when new characters can be accepted. When the Transmit FIFO is bypassed and RANGESEL is HIGH or SPDSEL is LOW, $\overline{\text{TXFULL}}$ toggles at the character rate to provide a character rate reference control-indication since REFCLK is operating at twice of the data rate. The asserted state of this output (HIGH or LOW) is determined by the state of the EXTFIFO input. When EXTFIFO is LOW, $\overline{\text{TXFULL}}$ is active LOW. When EXTFIFO is HIGH, TXFULL is active HIGH.

Pin Descriptions (continued)

Pin	Name	I/O Characteristics	Signal Description
70	$\overline{\text{TXHALF}}$	Three-state TTL output, changes following TXCLK↑	Transmit FIFO Half-full Status Flag. $\overline{\text{FIFOBYP}}$ is HIGH and $\overline{\text{CE}}$ is LOW) $\overline{\text{TXHALF}}$ is asserted when the HOTLink Transmit FIFO is half full (128 characters is half full). If a Transmit FIFO reset has been initiated ($\overline{\text{TXRST}}$ was sampled asserted for a minimum of seven TXCLK cycles), $\overline{\text{TXHALF}}$ is asserted to enforce the full/unavailable status of the Transmit FIFO during reset. When the Transmit FIFO is bypassed ($\overline{\text{FIFOBYP}}$ is LOW), $\overline{\text{TXHALF}}$ remains deasserted, having no logical function. $\overline{\text{TXHALF}}$ is forced to the High-Z state only during a “full-chip” reset (i.e., while $\overline{\text{RESET}}$ is LOW).
60	$\overline{\text{TXEMPTY}}$	Three-state TTL output, changes following TXCLK↑ or REFCLK↑	Transmit FIFO Empty Status Flag. When the Transmit FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH and $\overline{\text{CE}}$ is LOW), $\overline{\text{TXEMPTY}}$ is asserted when the HOTLink Transmit FIFO has no data to forward to the encoder. If a Transmit FIFO reset has been initiated ($\overline{\text{TXRST}}$ was sampled asserted for a minimum of seven TXCLK cycles), $\overline{\text{TXEMPTY}}$ is deasserted and remains deasserted until the Transmit FIFO reset operation is complete. When the Transmit FIFO is bypassed ($\overline{\text{FIFOBYP}}$ is LOW), $\overline{\text{TXEMPTY}}$ is asserted to indicate that the transmitter can accept data. $\overline{\text{TXEMPTY}}$ is also used as a BIST progress indicator when $\overline{\text{TXBISTEN}}$ is asserted. When $\overline{\text{TXBISTEN}}$ is asserted LOW, $\overline{\text{TXEMPTY}}$ becomes the transmit BIST-loop counter indicator (regardless of the logic state of $\overline{\text{FIFOBYP}}$). In this mode $\overline{\text{TXEMPTY}}$ is asserted for one TXCLK or REFCLK period at the end of each transmitted BIST sequence. **Note**: During BIST operations, when the Transmit FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH), it is necessary to keep TXCLK operating, even though no data is loaded into the Transmit FIFO and TXEN is never asserted, to allow the $\overline{\text{TXEMPTY}}$ flag to respond to the BIST state changes. The asserted state of this output (HIGH or LOW) is determined by the state of the EXTFIFO input. When EXTFIFO is LOW, $\overline{\text{TXEMPTY}}$ is active LOW. When EXTFIFO is HIGH, TXEMPTY is active HIGH. If $\overline{\text{CE}}$ is sampled asserted (LOW), $\overline{\text{TXEMPTY}}$ is driven to an active state. If $\overline{\text{CE}}$ is sampled deasserted (HIGH), $\overline{\text{TXEMPTY}}$ is placed into a High-Z state.
Receive Path Signals			
8	RXCLK	Bidirectional TTL clock Internal Pull-up	Receive Clock. When the Receive FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH), this clock is the Receive interface *input* clock and is used to control Receive FIFO read and reset, operations. When the Receive FIFO is bypassed ($\overline{\text{FIFOBYP}}$ is LOW), this clock becomes the recovered Receive PLL character clock *output* which runs continuously at the character rate.
41, 43, 45, 47, 48, 53, 59,61	RXDATA[7:0]	Three-state TTL output, changes following RXCLK↑	Parallel Receive DATA Outputs. When the decoder is enabled ($\overline{\text{ENCBYP}}$ is HIGH), the low-order eight bits of the decoded DATA character are presented on the RXDATA[7:0] outputs. COMMAND characters, when they are received, do not disturb these outputs. When the decoder is bypassed, the low order eight bits of the non-decoded character are presented on the RXDATA[7:0] outputs. When the Receive FIFO is disabled ($\overline{\text{FIFOBYP}}$ is LOW), these outputs change on the rising edge of the RXCLK output. When the Receive FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH), these outputs change on the rising edge of RXCLK input. RXEN is the three-state control for RXDATA[7:0].

Pin Descriptions (continued)

Pin	Name	I/O Characteristics	Signal Description
31, 33	RXDATA[9:8]/ RXCMD[2:3]	Three-state TTL output, changes following RXCLK↑	Parallel Receive DATA or COMMAND Output. When BYTE8/10 is HIGH and the decoder is enabled ($\overline{\text{ENCBYP}}$ is HIGH) these outputs reflects the value for the most recently received RXCMD[2:3]. When BYTE8/10 is LOW and the decoder is enabled ($\overline{\text{ENCBYP}}$ is HIGH) these outputs reflects the value for the most recently received RXDATA[9:8]. When the decoder is bypassed ($\overline{\text{ENCBYP}}$ is LOW), RXDATA[9:8] functions as the 9th and 10th bits of the 10- or 12-bit non-decoded receive character. When the Receive FIFO is disabled ($\overline{\text{FIFOBYP}}$ is LOW), these outputs change on the rising edge of the RXCLK output. When the Receive FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH), these outputs change on the rising edge of the RXCLK input. RXEN is a three-state control for RXDATA[9:8]/RXCMD[2:3].
23, 29	RXDATA[11:10] /RXCMD[1:0]	Three-state TTL output, changes following RXCLK↑	Parallel Receive COMMAND Outputs. When the decoder is enabled (ENCBYP is HIGH) these outputs reflect the value for the most recently received RXCMD[1:0]. When BYTE8/10 is HIGH and the decoder is bypassed ($\overline{\text{ENCBYP}}$ is LOW), these outputs have no meaning and are driven LOW. When BYTE8/10 is LOW and the decoder is bypassed ($\overline{\text{ENCBYP}}$ is LOW), RXCMD[1:0] functions as the 11th and 12th (MSB) bits of the 12-bit non-decoded receive character. When the Receive FIFO is disabled ($\overline{\text{FIFOBYP}}$ is LOW), this output changes on the rising edge of the RXCLK output. When the Receive FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH), these outputs change on the rising edge of the RXCLK input. RXEN is a three-state control for RXCMD[1:0].
69	$\overline{\text{RXEN}}$	TTL input, sampled on RXCLK↑ Internal Pull-up	Receive Enable Input. $\overline{\text{RXEN}}$ is a three-state control for the parallel data bus read operations. $\overline{\text{RXEN}}$ is sampled on the rising edge of the RXCLK input (or output) and enables parallel data bus read operations (when selected). The device is selected when $\overline{\text{RXEN}}$ is asserted during an RXCLK cycle immediately following one in which $\overline{\text{CE}}$ is sampled LOW. The parallel data pins are driven to active levels after the rising edge of RXCLK. When $\overline{\text{RXEN}}$ is de-asserted (ending the selection) the parallel data pins are High-Z after the rising edge of RXCLK. Depending on the level on EXTFIFO, this signal can be active HIGH or active LOW. If EXTFIFO is LOW, then $\overline{\text{RXEN}}$ is active LOW. If EXTFIFO is HIGH, then $\overline{\text{RXEN}}$ is active HIGH. Data is delivered on the clock cycle following any clock edge when $\overline{\text{RXEN}}$ is active.
65	RXSC/$\overline{\text{D}}$	Three-state TTL output, changes following RXCLK↑	COMMAND or DATA Output Indicator. When BYTE8/10 is HIGH and the decoder is enabled ($\overline{\text{ENCBYP}}$ is HIGH), this output indicates which group of outputs have been updated. If RXSC/$\overline{\text{D}}$ is HIGH, RXCMD[3:0] contains a new COMMAND. The DATA on the RXDATA[7:0] pins remain unchanged. If RXSC/$\overline{\text{D}}$ is LOW, RXDATA[7:0] contains a new DATA character. The COMMAND output on RXCMD[3:0] remain unchanged. When BYTE8/10 is LOW and the decoder is enabled ($\overline{\text{ENCBYP}}$ is HIGH), this output indicates which group of outputs have been updated. If RXSC/$\overline{\text{D}}$ is HIGH, RXCMD[1:0] contains a new COMMAND and the DATA on the RXDATA[9:0] remain unchanged. If RXSC/$\overline{\text{D}}$ is LOW, RXDATA[9:0] contains a new DATA character and the COMMAND output on RXCMD[1:0] remain unchanged. When the decoder is bypassed ($\overline{\text{ENCBYP}}$ is LOW) RXSC/$\overline{\text{D}}$ is not used and may be left unconnected. RXEN is a three-state control for RXSC/$\overline{\text{D}}$.
6	VLTN	Three-state TTL output, changes following RXCLK↑ Internal Pull-down	Code Rule Violation Detected. VLTN is asserted in response to detection of a 4B/5B or 5B/6B character that does not meet the coding rules of these characters. When VLTN is asserted, the values on the output DATA and COMMAND buses remain unchanged. VLTN remains asserted for one RXCLK period. VLTN is used to report character mismatches when $\overline{\text{RXBISTEN}}$ is driven LOW. VLTN is driven LOW when the decoder is bypassed ($\overline{\text{ENCBYP}}$ is LOW). RXEN is a three-state control for VLTN.

Pin Descriptions (continued)

Pin	Name	I/O Characteristics	Signal Description
67	RXRST	TTL input, sampled on RXCLK↑ Internal Pull-up	Receive FIFO Reset. Active LOW. When the Receive FIFO is enabled (FIFOBYP is HIGH), RXEN is deasserted, CE is asserted (LOW), and RXRST is sampled while asserted (LOW) by RXCLK for seven cycles, the Receive FIFO begins its internal reset process. Once the reset operation is started, the RXEMPTY flag is asserted and the interface counters and address pointer are zeroed. The reset operation proceeds to clear out the internal write pointers and counters. The RXEMPTY output remains asserted through the reset operation and remains asserted until new data is written to the Receive FIFO. While RXRST remains asserted, the Receive FIFO remains in reset and cannot accept received characters. When the Receive FIFO is bypassed (FIFOBYP is LOW), RXRST is ignored.
24, 25	RXMODE[1:0]	Static control input TTL levels Normally wired HIGH or LOW	Receiver Discard Policy Mode Select. 00b—allows all characters to be written into the Receive FIFO or output to the Receive data bus 01b—discards all JK or LM sync characters except the “last” one of a string of sync characters. Single sync characters in a data stream are included in the data written into the Receive FIFO. 1Xb—discards all JK or LM sync characters. The data stream written into the Receive FIFO does not include sync characters.
77	RXBISTEN	TTL input, asynchronous Internal Pull-up	Receiver BIST Enable. Active LOW. When LOW, the receiver is configured to perform a character-for-character match of the incoming data stream with a 511-character BIST sequence. The result of character mismatches are indicated on the VLTN pin. Completion of each 511-character BIST loop is accompanied by an assertion pulse on the RXFULL flag. The state of ENCBYP, FIFOBYP, and BYTE8/10 have no effect on BIST operation.
73	RFEN	TTL input, asynchronous Internal Pull-up	Reframe Enable. Used to control when the framer is allowed to adjust the character boundaries based on detection of one or more framing characters in the data stream. When framing is enabled (RFEN is HIGH) the receive framer realigns the serial stream to the incoming 10-bit JK sync character (if BYTE8/10 is HIGH) or the 12-bit LM sync character (if BYTE8/10 is LOW). Framing is disabled when RFEN is LOW. The deassertion of RFEN freezes the character boundary relationship between the serial stream and character clock. RFEN is an asynchronous input, sampled by the internal Receive PLL character clock.
10	RXFULL	Three-state TTL output, changes following RXCLK↑	Receive FIFO Full Flag. When the Receive FIFO is enabled (FIFOBYP is HIGH) and its flags are driven (CE is LOW), RXFULL is asserted when space is available for four or fewer characters to be written to the HOTLink Receive FIFO. If the RXCLK input is not continuous or the FIFO is accessed at a rate slower than data is being received, RXFULL may also indicate that some data has been lost because of FIFO overflow. When the Receive FIFO is bypassed (FIFOBYP is LOW), RXFULL is deasserted to indicate that valid data may be present. RXFULL is also used as a BIST progress indicator, and pulses once every pass through the 511 character BIST loop. When RXBISTEN is asserted (LOW), RXFULL becomes the receive BIST loop progress indicator (regardless of the logic state of FIFOBYP). While RXBISTEN is asserted, RXFULL is asserted until the receiver detects the start of the BIST pattern. Then RXFULL is deasserted for the duration of the BIST pattern, pulsing asserted for one RXCLK period on the last symbol of each BIST loop. If 14 of 28 consecutive symbols are received in error, RXFULL returns to the asserted state until the start of a BIST pattern is again detected. The asserted state of this output (HIGH or LOW) is determined by the state of the EXTFIFO input. When EXTFIFO is LOW, RXFULL is active LOW. When EXTFIFO is HIGH, RXFULL is active HIGH.

Pin Descriptions (continued)

Pin	Name	I/O Characteristics	Signal Description
19	RXHALF	Three-state TTL output, changes following RXCLK↑	Receive FIFO Half-full Flag. When the Receive FIFO is enabled (FIFOBYP is HIGH and CE is LOW) RXHALF is asserted when the HOTLink Receive FIFO is half full (128 characters is half full). If a Receive FIFO reset has been initiated (RXRST was sampled asserted for a minimum of seven RXCLK cycles), RXHALF is deasserted to enforce the empty/unavailable status of the Receive FIFO during reset. If FIFOBYP is LOW, RXHALF remains deasserted having no logical function. RXHALF is forced to the High-Z state only during a “full-chip” reset (i.e., while RESET is LOW).
21	RXEMPTY	Three-state TTL output, changes following RXCLK↑	Receive FIFO Empty Flag. When the Receive FIFO is enabled (FIFOBYP is HIGH) and its flags are driven (CE is LOW), RXEMPTY is asserted when the HOTLink Receive FIFO has no data to forward to the parallel interface. If a Receive FIFO reset has been initiated (RXRST was sampled asserted for a minimum of seven RXCLK cycles), RXEMPTY is asserted to enforce the empty/unavailable status of the Receive FIFO during reset. Any read operation occurring when RXEMPTY is asserted results in no change in the FIFO status, and the data from the last valid read remains on the RXDATA bus. When the Receive FIFO is bypassed but the decoder is enabled, RXEMPTY is used as a valid data indicator. When deasserted it indicates that valid data is present at the RXDATA or RXCMD outputs as indicated by RXSC/D. When asserted it indicates that a SYNC character (JK or LM) is present on the RXCMD output pins. When the Receive FIFO is bypassed (FIFOBYP is LOW), RXEMPTY is deasserted whenever data is ready. The asserted state of this output (HIGH or LOW) is determined by the state of the EXTFIFO input. When EXTFIFO is LOW, RXEMPTY is active LOW. When EXTFIFO is HIGH, RXEMPTY is active HIGH.
Control Signals			
71	CE	TTL input sampled on TXCLK↑, RXCLK↑, or REFCLK↑	Chip Enable Input. Active LOW. When CE is asserted and sampled LOW by RXCLK, the Receive FIFO status flags are driven to their active states. When this input is deasserted and sampled by RXCLK, the Receive FIFO status flags are placed in a High-Z state. When CE has been sampled LOW and RXEN changes from deasserted to asserted and is sampled by RXCLK, the RXSC/D, RXDATA[7:0], RXDATA[9:8]/RXCMD[2:3] and VLTN output drivers are enabled and go to their driven levels. These pins remain driven until RXEN is sampled deasserted. When the Transmit FIFO is enabled (FIFOBYP is HIGH), and CE is asserted and sampled by TXCLK, the Transmit FIFO status flags are driven to their active states. When this input is deasserted and sampled by TXCLK, the Transmit FIFO status flags are placed in a High-Z state. When the Transmit FIFO is bypassed (FIFOBYP is LOW), and CE is asserted and sampled by REFCLK, the Transmit FIFO status flags are driven to their active states. When this input is deasserted and sampled by REFCLK, the Transmit FIFO status flags are placed in a High-Z state. When the Transmit FIFO is enabled (FIFOBYP is HIGH), CE has been sampled LOW, and TXEN changes from deasserted to asserted and is sampled by TXCLK, the TXSC/D, TXDATA[7:0], TXDATA[9:8]/RXCMD[2:3], and TXCMD[1:0] inputs are sampled and passed to the Transmit FIFO. These inputs are sampled on all consecutive TXCLK cycles until TXEN is sampled deasserted. When the Transmit FIFO is bypassed (FIFOBYP is LOW), CE has been sampled LOW, and TXEN changes from deasserted to asserted and is sampled by REFCLK, the TXSC/D, TXDATA[7:0], TXDATA[9:8]/RXCMD[2:3], and TXCMD[1:0] inputs are sampled and passed to the encoder or serializer as directed by other control inputs. These inputs are sampled on all consecutive REFCLK cycles until TXEN is sampled deasserted.

Pin Descriptions (continued)

Pin	Name	I/O Characteristics	Signal Description
12	REFCLK	TTL clock input	PLL Frequency Reference Clock. This clock input is used as the timing reference for the transmit and receive PLLs. When the Transmit FIFO is bypassed (FIFOBYP is LOW), REFCLK is also used as the clock for the parallel transmit interface.
75	SPDSEL	Static control input TTL levels Normally wired HIGH or LOW	Speed Select. Used to select from one of two operating serial rates for the CY7C9689A. When SPDSEL is HIGH, the signaling rate is between 100 and 200 MBaud. When LOW, the signaling rate is between 50 and 100 MBaud. Used in combination with RANGESEL and BYTE8/10 to configure the VCO multipliers and dividers.
74	RANGESEL	Static control input TTL levels Normally wired HIGH or LOW	Range Select. Selects the proper prescaler for the REFCLK input. If RANGESEL is LOW, the REFCLK input is passed directly to the Transmit PLL clock multiplier. If RANGESEL is HIGH, REFLCK is divided by two before being sent to the Transmit PLL multiplier. When the Transmit FIFO is bypassed ($\overline{\text{FIFOBYP}}$ is LOW), with RANGESEL HIGH or SPDSEL LOW, TXFULL toggles at half the REFCLK rate to provide a character rate indication, and to show when data can be accepted.
51	$\overline{\text{RESET}}$	Asynchronous TTL input	Master Reset for Internal Logic. Pulsed LOW for one or more REFCLK cycles.
28	$\overline{\text{FIFOBYP}}$	Static control input TTL levels Normally wired HIGH or LOW	FIFO Bypass Enable. When asserted, the Transmit and Receive FIFOs are bypassed. In this mode TXCLK is not used. Instead all transmit data must be synchronous to REFCLK. Transmit FIFO status flags are synchronized to REFCLK. All received data is synchronous to RXCLK output. Receive FIFO status flags are synchronized to RXCLK (the recovered Receive PLL character clock). When not asserted, the Transmit and Receive FIFOs are enabled. In this mode all Transmit FIFO writes are synchronized to TXCLK, and all Receive FIFO reads are synchronous to the RXCLK input.
50	BYTE8/$\overline{10}$	Static control input TTL levels Normally wired HIGH or LOW	8/10-bit Parallel Data Size Select. When set for 8-bit data (BYTE8/10 is HIGH) and the encoder is enabled ($\overline{\text{ENCBYP}}$ is HIGH), 8-bit DATA characters and 4-bit COMMAND characters are captured at the TXDATA[7:0] or TXCMD[3:0] inputs (selected by the TXSC/$\overline{\text{D}}$ input) and passed to the Transmit FIFO (if enabled) and encoder. Received characters are decoded, passed through the Receive FIFO (if enabled) and presented at either the RXDATA[7:0] or RXCMD[3:0] outputs and indicated by the RXSC/$\overline{\text{D}}$ output. When set for 8-bit data (BYTE8/10 is HIGH) and the encoder is bypassed (ENCBYP is LOW), the internal data paths are set for 10-bit characters. Each received character is presented to the Receive FIFO (if enabled) and is passed to the RXDATA[9:0] outputs. When set for 10-bit data (BYTE8/$\overline{10}$ is LOW) and the encoder is enabled ($\overline{\text{ENCBYP}}$ is HIGH), 10-bit DATA characters and 2-bit COMMAND characters are captured at the TXDATA[9:0] or TXCMD[1:0] inputs (selected by the TXSC/$\overline{\text{D}}$ input) and passed to the Transmit FIFO (if enabled) and encoder. Received characters are decoded, passed through the Receive FIFO (if enabled) and presented at either the RXDATA[9:0] or RXCMD[1:0] outputs and indicated by the RXSC/$\overline{\text{D}}$ output. When set for 10-bit data (BYTE8/10 is LOW) and the encoder is bypassed (ENCBYP is LOW), the internal clock data paths are set for 12-bit characters. Each received character is presented to the Receive FIFO (if enabled) and is passed to the RXDATA[9:0] and the RXCMD[1:0] outputs.

Pin Descriptions (continued)

Pin	Name	I/O Characteristics	Signal Description
49	EXTFIFO	Static control input TTL levels Normally wired HIGH or LOW	External FIFO Mode. EXTFIFO modifies the active state of the $\overline{\text{RXEN}}$ and $\overline{\text{TXEN}}$ inputs and the timing of the Transmitter and Receiver data buses. When configured for external FIFOs (EXTFIFO is HIGH), TXEN is assumed to be driven by the empty flag of an attached CY7C42X5 FIFO, and RXEN is assumed to be driven by the almost full flag of an attached CY7C42X5 FIFO. In this mode the active data transition is in the clock following the clock edge that “enables” the data bus. When not configured for external FIFOs (EXTFIFO is LOW), TXEN is assumed to be driven as a pipeline register and RXEN is assumed to be driven by a controller for a pipeline register. In this mode the active data transition is within the same clock as the clock edge that “enables” the data bus. EXTFIFO also modifies the output state of the Receive and Transmit FIFO flags. When configured for external FIFOs (EXTFIFO is HIGH), the Full and Empty FIFO flags are active HIGH (the Half full flag is always active LOW). When not configured for external FIFOs (EXTFIFO is LOW), all of the FIFO flags are active LOW.
27	$\overline{\text{ENCBYP}}$	Static control input TTL levels Normally wired HIGH or LOW	Enable Encoder Bypass Mode. When asserted, both the encoder and decoder are bypassed. Data is transmitted without 4B/5B or 5B/6B encoding (but with NRZI encoding), LSB first. Received data are presented as parallel characters to the parallel interface without decoding. When deasserted, data is passed through both the encoder in the Transmit path and the decoder in the Receive path.
Analog I/O and Control			
89, 90, 81, 82	OUTA± OUTB±	PECL compatible differential output	Differential Serial Data Outputs. These PECL-compatible differential outputs are capable of driving terminated transmission lines or commercial fiber-optic transmitter modules. To minimize the power dissipation of unused outputs, the outputs should be left unconnected and the associated CURSETA or CURSETB should be connected to V_{DD}.
94, 93, 86, 85	INA± INB±	PECL compatible differential input	Differential Serial Data Inputs. These inputs accept the serial data stream for deserialization and decoding. Only one serial stream at a time may be fed to the receive PLL to extract the data content. This stream is selected using the A/B input.
97	CURSETA	Analog	Current-set Resistor Input for OUTA±. A precision resistor is connected between this input and a clean ground to set the output differential amplitude and currents for the OUTA± differential driver.
78	CURSETB	Analog	Current-set Resistor Input for OUTB±. A precision resistor is connected between this input and a clean ground to set the output differential amplitude and currents for the OUTB± differential driver.
100	CARDET	PECL input, asynchronous	Carrier Detect Input. Used to allow an external device to signify a valid signal is being presented to the high-speed PECL input buffers, as is typical on an Optical Module. When CARDET is deasserted LOW, the $\overline{\text{LFI}}$ indicator asserts LOW signifying a Link Fault. This input can be tied HIGH for copper media applications.
2	A/$\overline{\text{B}}$	Asynchronous TTL input	Input A or Input B Selector. When HIGH, input INA± is selected, when LOW, INB± is selected.
3	$\overline{\text{LFI}}$	TTL output, changes following RXCLK↑	Link Fault Indication Output. Active LOW. LFI changes synchronous with RXCLK. This output is driven LOW when the serial link currently selected by A/B is not suitable for data recovery. This could be because: Serial Data Amplitude is below acceptable levels Input transition density is not sufficient for PLL clock recovery Input Data stream is outside an acceptable frequency range of operation CARDET is LOW

Pin Descriptions (continued)

Pin	Name	I/O Characteristics	Signal Description
5	DLB	Asynchronous TTL input	Diagnostic Loop Back Selector. When DLB is LOW, LOOP Mode is OFF. Output of the transmitter shifter is routed to both OUTA± and OUTB± and the serial input selected by A/B is routed to the receive PLL for data recovery. When DLB is HIGH, Diagnostic Loopback is Enabled. Output of the transmitter serial data is routed to the receive PLL for data recovery. Primarily used for System Diagnostic test. The serial inputs are ignored and OUTA± and OUTB± are both active.
1	$\overline{\text{TEST}}$	Asynchronous TTL input normally wired HIGH	Test Mode Select. Used to force the part into a diagnostic test mode used for factory ATE test. This input must be tied HIGH during normal operation.
Power			
80, 87, 88, 95, 96, 98	V_{DDA}		Power for PECL-compatible I/O signals and internal circuits.
76, 79, 83, 84, 91, 92, 99	V_{SSA}		Ground for PECL-compatible I/O signals and internal circuits.
14, 17, 35, 55, 62, 64	V_{DD}		Power for TTL I/O signals and internal circuits.
4,11, 13, 15, 26, 37, 38, 39, 52, 57, 63, 66	V_{SS}		Ground for TTL I/O signals and internal circuits.

CY7C9689A HOTLink Operation

Overview

The CY7C9689A is designed to move parallel data across both short and long distances with minimal overhead or host system intervention. This is accomplished by converting the parallel characters into a serial bit-stream, transmitting these serial bits at high speed, and converting the received serial bits back into the original parallel data format.

The CY7C9689A offers a large feature set, allowing it to be used in a wide range of host systems. Some of the configuration options are

- AMD TAXIchip 4B/5B- and 5B/6B-compatible encoder/decoder
- AMD TAXIchip-compatible serial link
- AMD TAXIchip parallel COMMAND and DATA I/O bus architecture
- 8-bit or 10-bit character size
- User-definable data packet or frame structure
- Two-octave data rate range
- Asynchronous (FIFOed) or synchronous data interface
- Embedded or bypassable FIFO data storage
- Encoded or non-encoded
- Multi-PHY capability

This flexibility allows the CY7C9689A to meet the data transport needs of almost any system.

Transmit Data Path

Transmit Data Interface/Transmit Data FIFO

The transmit data interface to the host system is configurable as either an asynchronous buffered (FIFOed) parallel interface or as a synchronous pipeline register. The bus itself can be configured for operation with either 8-bit or 10-bit character widths.

When configured for asynchronous operation (where the host-bus interface clock operates asynchronous to the serial character and bit stream clocks), the host interface becomes that of a synchronous FIFO clocked by TXCLK. In this configuration an internal 256-character Transmit FIFO is enabled that allows the host interface to be written at any rate from DC to 50 MHz.

When configured for synchronous operation, the transmit interface is clocked by REFCLK and operates synchronous to the internal character and bit-stream clocks. The input register can be written at either 1/10 or 1/12 the serial bit rate. This interface can be clocked at up to 40 MHz when configured for 8-bit data width, and up to 33 MHz when configured for 10-bit data bus width. Actual clock rate depends on data rate as well as RANGESEL and SPDSEL logic levels.

Both asynchronous and synchronous interface operations support user control over the logical sense of the FIFO status flags. Full and empty flags on both the transmitter and receiver can be active HIGH or active LOW. This facilitates interfacing with existing control logic or external FIFOs with minimal or no external glue logic.

Encoder

Data from the host interface or Transmit FIFO is next passed to an Encoder block. The CY7C9689A contains both 4B/5B and 5B/6B encoders that are used to improve the serial transport characteristics of the data. For those systems that contain their own encoder or scrambler, this Encoder may be bypassed.

Serializer/Line Driver

The data from the Encoder is passed to a Serializer. This Serializer operates at 10 or 12 times the character rate. With the internal FIFOs enabled, REFCLK can run at 1x, 2x, or 4x the character rate. With the FIFOs bypassed, REFCLK can operate at 1x or 2x the character rate. The serialized data is output in NRZI format from two PECL-compatible differential line drivers configured to drive transmission lines or optical modules.

Receive Data Interface

Line Receiver/Deserializer/Framer

Serial data is received at one of two PECL-compatible differential line receivers. The data is passed to both a Clock and Data Recovery PLL and to a Deserializer that converts NRZI serial data into NRZ parallel characters. The Framer adjusts the boundaries of these characters to match those of the original transmitted characters.

Decoder

The parallel characters are passed through a pair of 5B/4B or 6B/5B decoders and returned to their original form. For systems that make use of external decoding or descrambling, the decoder may be bypassed.

Receive Data Interface/Receive Data FIFO

Data from the decoder is passed either to a synchronous Receive FIFO or is passed directly to the output register. The output register can be configured for either 8-bit character or 10-bit character operation.

When configured for an asynchronous buffered (FIFOed) interface, the data is passed through a 256-character Receive FIFO that allows data to be read at any rate from DC to 50 MHz. When configured for synchronous operation (Receive FIFO is bypassed) data is clocked out of the Receive Output register at up to 20 MHz when configured for 8-bit characters, or 16.67 MHz when configured for 10-bit characters. The receive interface is also configurable for FIFO flags with either HIGH or LOW status indication

Oscillator Speed Selection

The CY7C9689A is designed to operate over a two-octave range of serial signaling rates, covering the 50- to 200-MBaud range. To cover this wide range, the PLLs are configured into various sub-regions using the SPDSEL and RANGESEL inputs, and to a limited extent the BYTE8/10 input. These inputs are used to configure the various prescalers and clock dividers used with the transmit and receive PLLs.

CY7C9689A TAXI HOTLink Transceiver Block Diagram Description

Transmit Input/Output Register

The CY7C9689A provides a synchronous interface for data and command inputs, instead of the TAXI's asynchronous strobed interface. The Transmit Input Register, shown in Figure 2, captures the data and command to be processed by the HOTLink Transmitter, and allows the input timing to be made compatible with asynchronous or synchronous host system buses. These buses can take the form of external FIFOs, state machines, or other control structures. Data and command present on the TXDATA[9:0] and TXSC/D inputs are captured at the rising edge of the selected sample clock. The transmit data bus bit-assignments vary depending on the data encoding and bus-width selected. These bus bit-assignments are shown in Table 1, and list the functional names of these different signals. Note that the function of several of these signals changes in different operating modes. The logical sense of the enable and FIFO flag signals depends on the intended interface convention and is set by the EXTFIFO pin.

The transmit interface supports both synchronous and asynchronous clocking modes, each supporting both UTOPIA and Cascade timing models. The selection of the specific clocking mode is determined by the RANGESEL and SPDSEL inputs and the FIFO Bypass (FIFOBYP) signal.

Figure 2. Transmit Input Register

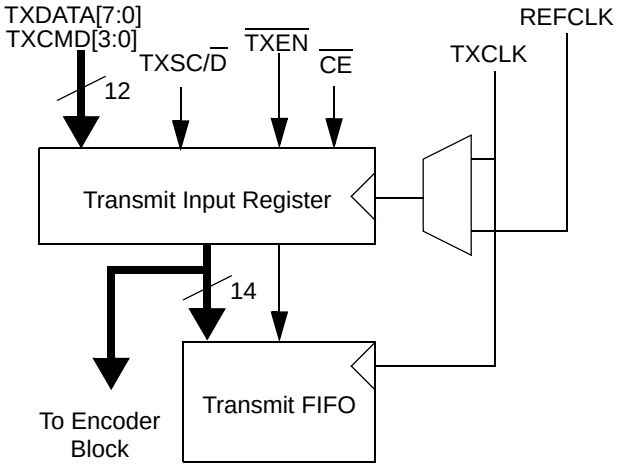


Table 1. Transmit Input Bus Signal Map

TXDATA Bus Input Bit	Transmit Encoder Mode[1]			
	Encoded 8-bit Character Stream[2]	Pre-encoded 10-bit Character Stream	Encoded 10-bit Character Stream[3]	Pre-encoded 12-bit Character Stream
TXSC/D	TXSC/D		TXSC/D	
TXDATA[0]	TXDATA[0]	TXD[0][4]	TXDATA[0]	TXD[0][5]
TXDATA[1]	TXDATA[1]	TXD[1]	TXDATA[1]	TXD[1]
TXDATA[2]	TXDATA[2]	TXD[2]	TXDATA[2]	TXD[2]
TXDATA[3]	TXDATA[3]	TXD[3]	TXDATA[3]	TXD[3]
TXDATA[4]	TXDATA[4]	TXD[4]	TXDATA[4]	TXD[4]
TXDATA[5]	TXDATA[5]	TXD[5]	TXDATA[5]	TXD[5]
TXDATA[6]	TXDATA[6]	TXD[6]	TXDATA[6]	TXD[6]
TXDATA[7]	TXDATA[7]	TXD[7]	TXDATA[7]	TXD[7]
TXDATA[8]/TXCMD[3]	TXCMD[3]	TXD[8]	TXDATA[8]	TXD[8]
TXDATA[9]/TXCMD[2]	TXCMD[2]	TXD[9]	TXDATA[9][3]	TXD[9]
TXCMD[1]	TXCMD[1]		TXCMD[1]	TXD[10][5]
TXCMD[0]	TXCMD[0]		TXCMD[0]	TXD[11]

Notes
1. All open cells are ignored.
2. When ENCBYP is HIGH and BYTE8/10 is HIGH, transmitted bit order is the encoded form (MSB to LSB) of TXDATA[7,6,5,4] and TXDATA[3,2,1,0] or TXCMD[3,2,1,0] as selected by TXSC/D.
3. When ENCBYP is HIGH and BYTE8/10 is LOW, transmitted bit order is the encoded form (MSB to LSB) of TXDATA[8,7,6,5,4] and TXDATA[9,3,2,1,0] or TXCMD[1,0] as selected by TXSC/D.
4. When ENCBYP is LOW and BYTE8/10 is HIGH, the transmitted bit order is (LSB to MSB) TXD[0,1,2,3,4,5,6,7,8,9].
5. When ENCBYP is LOW and BYTE8/10 is LOW, the transmitted bit order is (LSB to MSB) TXD[0,1,2,3,4,5,6,7,8,9,11,10].

Synchronous Interface

Synchronous interface clocking operates the entire transmit data path synchronous to REFCLK. It is enabled by connecting FIFOBYP LOW to disable the internal FIFOs.

Asynchronous Interface

Asynchronous interface clocking controls the writing of host bus data into the Transmit FIFO. It is enabled by setting FIFOBYP HIGH to enable the internal FIFOs. In these configurations, all writes to the Transmit Input Register, and associated transfers to the Transmit FIFO, are controlled by TXCLK. The remainder of the transmit data path is clocked by REFCLK or synthesized derivatives of REFCLK.

Shared Bus Timing Model

The Shared Bus Timing Model allows multiple CY7C9689A transmitters to be accessed from a common host bus. It is enabled by setting EXTFIFO LOW. In shared bus timing, the TXEMPTY and TXFULL outputs and TXEN input are all active LOW signals. If the CY7C9689A is addressed by asserting CE LOW, it becomes “selected” when TXEN is asserted LOW. Following selection, data or command is written into the Transmit FIFO on every clock cycle where TXEN remains LOW.

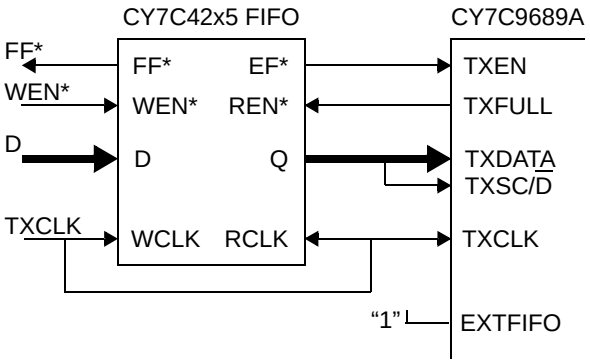
Cascade Timing Model

The Cascade timing model is a variation of the shared bus timing model. Here the TXEMPTY and TXFULL outputs, and TXEN input, are all active HIGH signals. Cascade timing makes use of the same selection sequences as shared bus timing, but write data accesses use a delayed write. This delayed write is necessary to allow direct coupling to external FIFOs, or to state machines that initiate a write operation one clock cycle before the data is available on the bus.

Cascade timing is enabled by setting EXTFIFO HIGH.

When used for FIFO depth expansion, Cascade timing allows the size of the internal Transmit FIFO to be expanded to an almost unlimited depth. It allows a CY7C42x5 series synchronous FIFO to be attached to the transmit interface without any extra logic, as shown in Figure 3.

Figure 3. External FIFO Depth Expansion of the CY7C9689A Transmit Data Path



Transmit FIFO

The Transmit FIFO is used to buffer data and command captured in the input register for later processing and transmission. This FIFO is sized to hold 256 14-bit characters. When the Transmit FIFO is enabled, and a Transmit FIFO write is enabled (the device is selected and TXEN is sampled asserted), data is captured in the transmit input register and stored into the Transmit FIFO. All Transmit FIFO write operations are clocked by TXCLK.

The Transmit FIFO presents Full, Half-Full, and Empty FIFO flags. These flags are provided synchronous to TXCLK. When the Transmit FIFO is enabled, it allows operation with a Moore-type external controlling state machine. When configured for Cascade timing, the timing and active levels of these signals are also designed to support direct expansion to Cypress CY7C42x5 synchronous FIFOs.

Regardless of bus width (8- or 10-bit characters) the Transmit FIFO can be clocked at any rate from DC to 50 MHz. This gives the Transmit FIFO a maximum bandwidth of 50 million characters per second. Since the serial outputs can only move 20 million characters per second at their fastest operating rate, there is ample time to service multiple CY7C9689A HOTLinks with a single controller.

The read port of the Transmit FIFO is connected to a logic block that performs data formatting and validation. All data read operations from the Transmit FIFO are controlled by a Transmit Control State Machine that operates synchronous to REFCLK.

Encoder Block

The Encoder logic block performs two primary functions: encoding the data for serial transmission and generating BIST patterns to allow at-speed link and device testing.

BIST LFSR

The Encoder logic block operates on data stored in a register. This register accepts information directly from the Transmit FIFO, the Transmit Input Register or from the Transmit Control State Machine when it inserts special characters into the data stream.

This same register is converted into a Linear Feedback Shift Register (LFSR) when the BIST pattern generator is enabled (TXBISTEN is LOW). When enabled, this LFSR generates a 511-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable but pseudo-random sequence that can be matched to an identical LFSR in the Receiver.

Encoder

The data passed through the Transmit FIFO and pipeline register, or as received directly from the Transmit Input Register, is seldom in a form suitable for transmission across a serial link. The characters must usually be processed or transformed to guarantee:

- a minimum transition density (to allow the serial receiver PLL to extract a clock from the data stream)
- some way to allow the remote receiver to determine the correct character boundaries (framing).

The CY7C9689A contains an integrated 4B/5B encoder that accepts 8-bit data characters and converts these into 10-bit transmission characters that have been optimized for transport on serial communications links. This 4B/5B encoding scheme is compliant with the ANSI X3T9.5 (FDDI) committee's 4B/5B code. The CY7C9689A also contains a 5B/6B encoder that accepts 10-bit data characters and converts these into 12-bit transmission characters.

The 4B/5B, 5B/6B encoder can be bypassed for those systems that operate with external 4B/5B or 5B/6B encoders or use alternate forms of encoding or scrambling to ensure good transmission characteristics. The complete encoding tables are listed in Table 7 and Table 8.

When the Encoder is enabled, the transmit data characters (as passed through the Transmit FIFO and pipeline register) are converted to either a 10-bit or 12-bit Data symbol or a 10-bit or 12-bit Command Character, depending upon the state of the TXSC/$\overline{D}$ input. If TXSC/$\overline{D}$ is HIGH, the data on the command inputs are encoded into Command Character as shown in *Table 8*. If TXSC/$\overline{D}$ is LOW, the data inputs are encoded using the Data Character encoding in Table 7.

The 4B/5B, 5B/6B coding function of the Encoder can be bypassed for systems that include an external coder or scrambler function as part of the controller or host system. This is performed by setting $\overline{ENCBYP}$ LOW. With the encoder bypassed, each 10-bit or 12-bit character (as captured in the Transmit Input Register) is passed directly to the Transmit Shifter (or Transmit FIFO) without modification.

Transmit Shifter

The Transmit Shifter accepts 10-bit (BYTE8/$\overline{10}$ = HIGH) or 12-bit (BYTE8/10 = LOW) parallel data from the Encoder block once each character time, and shifts it out the serial interface output buffers using a PLL-multiplied bit-clock with NRZI encoding. This bit-clock runs at 2.5, 5, or 10 times the REFCLK rate (3, 6, or 12 times when BYTE8/10 is LOW) as selected by RANGESEL and SPDSEL (see Table 3). Timing for the parallel transfer is controlled by the counter and dividers in the Clock Multiplier PLL and is not affected by signal levels or timing at the input pins. Bits in each character are shifted out LSB first.

Routing Matrix

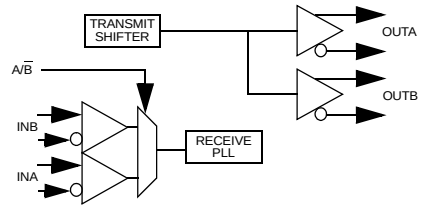
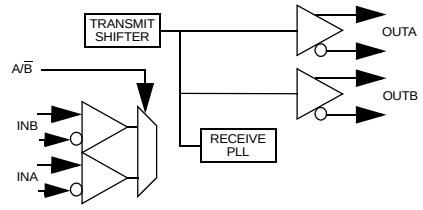
The Routing Matrix is a precision multiplexor that allows local diagnostic loopback. The signal routing for the transmit serial outputs is controlled by the DLB input as listed Table 2.in

Serial Line Drivers

The serial interface PECL Output Drivers (ECL referenced to +5 v) are the transmission line drivers for the serial media. OUTA± receives its data directly from the transmit shifter, while OUTB± receives its data from the Routing Matrix. These two outputs (OUTA± and OUTB±) are capable of direct connection to +5 v optical modules, and can also directly drive DC- or AC-coupled transmission lines.

The PECL-compatible Output Drivers can be viewed as programmable current sources. The output voltage is determined by the output current and the load impedance Z_{LOAD}. The desired output voltage swing is therefore controlled by the current-set resistor R_{CURSET} associated with that driver. Different R_{CURSET} values are required for different line

Table 2. Transmit Data Routing Matrix

DLB[0]	Data Connections
0	
1	

impedance/amplitude combinations. The output swing is designed to center around V_{DD}–1.33 v. Each output must be externally biased to V_{DD}–1.33 v.

This differential output-swing can be specified two ways: either as a peak-to-peak voltage into a single-end load, or as an absolute differential voltage into a differential load.

When specified into a single-ended load (one of the outputs switching into a load), the single output will both source and sink current as it changes between its HIGH and LOW levels. The voltage difference between this HIGH level and LOW level determine the peak-to-peak signal-swing of the output. This amplitude relationship is controlled by the load impedance on the driver, and by the resistance of the R_{CURSET} resistor for that driver, as listed in *Eq. 1*

$$R_{CURSET} = \frac{180 \times Z_{LOAD}}{V_{OPP}} \quad \text{Eq. 1}$$

In *Eq. 1*, V_{OPP} is the difference in voltage levels at one output of the differential driver when that output is driving HIGH and LOW, Z_{LOAD} is that load seen by the one output when it is sourcing and sinking current. With a known load impedance and a desired signal swing, it is possible to calculate the value of the associated CURSETA or CURSETB resistor that sets this current.

Unused differential output drivers should be left open, and can reduce their power dissipation by connecting their respective CURSETx input to V_{DD}.

Transmit PLL Clock Multiplier

The Transmit PLL Clock Multiplier accepts an external clock at the REFCLK input, and multiples that clock by 2.5, 5, or 10 (3, 6, or 12 when BYTE8/10 is LOW and the encoder is disabled) to generate a bit-rate clock for use by the transmit shifter. It also provides a character-rate clock used by the Transmit Controller state machine.

The clock multiplier PLL can accept a REFCLK input between 8 MHz and 40 MHz, however, this clock range is limited by the operation mode of the CY7C9689A as selected by the SPDSEL and RANGESEL inputs, and to a limited extent, by the BYTE8/10

and FIFOBYP signals. The operating serial signalling rate and allowable range of REFCLK frequencies is listed in Table 3.

Transmit Control State Machine

The Transmit Control State Machine responds to multiple inputs to control the data stream passed to the encoder. It operates in response to:

Table 3. Speed Select and Range Select Settings

SPDSEL	RANGESEL	Serial Data Rate (MBaud)	REFCLK[7] Frequency (MHz)
LOW	LOW	50–100	10–20
LOW	HIGH[6]	50–100	20–40
HIGH	LOW	100–200	10–20
HIGH	HIGH	100–200	20–40

- the state of the FIFOBYP input
- the presence of data in the Transmit FIFO
- the contents of the Transmit FIFO
- the state of the transmitter BIST enable (TXBISTEN)
- the state of external halt signal (TXHALT).

These signals are used by the Transmit Control State Machine to control the data formatter, read access to the Transmit FIFO and BIST. They determine the content of the characters passed to the Encoder and Transmit Shifter.

When the Transmit FIFO is bypassed, the Transmit Control State Machine operates synchronous to REFCLK. In this mode, data from the TXDATA bus is passed directly from the Input Register to the Pipeline Register. If no data is enabled into the Input register (TXEN is deasserted or TXFULL is asserted) then the Transmit Control State Machine presents a JK or LM (when BYTE8/10 = LOW) Command Character code to the Encoder to maintain link synchronization.

If both the Encoder and Transmit FIFO are bypassed and no data is enabled into the Input Register, the Transmit Control State Machine injects JK or LM (when BYTE8/10 = LOW) into the Serial Shifter Register at this time slot. This also occurs if the Encoder is bypassed, the Transmit FIFO is enabled, and the Transmit FIFO is empty.

External Control of Data Flow

The Transmit Control State Machine supports halting of data transmission by the TXHALT input. This control signal input is only interpreted when the Transmit FIFO is enabled. TXHALT is brought directly to the state machine without going through the Transmit FIFO.

The assertion of TXHALT causes character processing to stop at the next FIFO character location. No additional data is read from the Transmit FIFO until TXHALT is deasserted.

TXHALT may be used to prevent a remote FIFO overflow, which would result in lost data. This back-pressure mechanism can significantly improve data integrity in systems that cannot guarantee the full bandwidth of the host system at all times.

Serial Line Receivers

Two differential line receivers, INA± and INB±, are available for accepting serial data streams, with the active input selected using the A/B input. The DLB input allow the transmit Serializer output to be selected as a third input serial stream, but this path is generally used only for local diagnostic loopback purposes. The serial line receiver inputs are all differential, and will accommodate wire interconnect with filtering losses or transmission line attenuation greater than 9 dB ($V_{DIF} \geq 200$ mV, or 400 mV peak-to-peak differential) or can be directly connected to +5 v fiber-optic interface modules (any ECL logic family, not limited to ECL 100K). The common-mode tolerance of these line receivers accommodates a wide range of signal termination voltages.

As can be seen in *Table 2*, these inputs are configured to allow single-pin control for most applications. For those systems requiring selection of only INA± or INB±, the DLB signals can be tied LOW, and the A/B selection can be performed using only A/B. For those systems requiring only a single input and a local loopback, the A/B can be tied HIGH or LOW, and DLB can be used for loopback control.

Signal Detect

The selected Line Receiver (that routed to the clock and data recovery PLL) is simultaneously monitored for:

- analog amplitude (> 400 mV pk-pk)
- transition density
- received data stream outside normal frequency range (±400 ppm)
- carrier detected

All of these conditions must be valid for the Signal Detect block to indicate a valid signal is present. This status is presented on the LFI (Link Fault Indicator) output, which changes synchronous to RXCLK. While link status is monitored internally at all times, it is necessary to have transitions on RXCLK to allow this signal to change externally.

Clock/Data Recovery

The extraction of a bit-rate clock and recovery of data bits from the received serial stream is performed within the Clock/Data Recovery (CDR) block. The clock extraction function is performed by a high-performance embedded PLL that tracks the frequency of the incoming bit stream and aligns the phase of its internal bit-rate clock to the transitions in the serial data stream.

The CDR makes use of the clock present at the REFCLK input. It is used to ensure that the VCO (within the CDR) is operating at the correct frequency (rather than some harmonic of the bit rate), to improve PLL acquisition time, and to limit unlocked frequency excursions of the CDR VCO when no data is present at the serial inputs.

Notes
6. When SPDSEL is LOW and the FIFOs are bypassed (FIFOBYP is LOW), the RANGESEL input is ignored and is internally mapped to the LOW setting.
7. When configured for 12-bit preencoded data (BYTE8/10 and ENCBYP are both LOW) the allowable REFCLK ranges are 8.33 to 16.67 MHz and 16.67 to 33.33 MHz.

Regardless of the type of signal present, the CDR will attempt to recover a data stream from it. If the frequency of the recovered data stream is outside the limits for the range controls, the CDR PLL will track REFCLK instead of the data stream. When the frequency of the selected data stream returns to a valid frequency, the CDR PLL is allowed to track the received data stream. The frequency of REFCLK is required to be within ±400 ppm of the frequency of the clock that drives the REFCLK signal at the remote transmitter to ensure a lock to the incoming data stream.

For systems using multiple or redundant connections, the $\overline{\text{LFI}}$ output can be used to select an alternate data stream. When an LFI indication is detected, external logic can toggle selection of the INA± and INB± inputs through the A/B input. When a port switch takes place, it is necessary for the PLL to reacquire the new serial stream and frame to the incoming characters.

Clock Divider

This block contains the clock division logic, used to transfer the data from the Deserializer/Framer to the Decoder once every character (once every ten or twelve bits) clock. This counter is free running and generates outputs at the bit-rate divided by 10 (12 when the BYTE8/$\overline{10}$ is LOW). When the Receive FIFO is bypassed, one of these generated clocks is driven out the RXCLK pin.

Deserializer/Framer

The CDR circuit extracts bits from the serial data stream and clocks these bits into the Shifter/Framer at the bit-clock rate. When enabled, the Framer examines the data stream looking for JK or LM (when BYTE8/$\overline{10}$ is LOW) characters at all possible bit positions. The location of this character in the data stream is used to determine the character boundaries of all following characters.

The framer operates in two different modes, as selected by the RFEN input. When RFEN is asserted (HIGH), the framer is allowed to reset the internal character boundaries on any detected JK or LM (when BYTE8/$\overline{10}$ is LOW) character.

If RFEN is LOW, the framer is disabled and no changes are made to character boundaries.

The framer in the CY7C9689A operates by shifting the internal character position to align with the character clock. This ensures that the recovered clock does not contain any significant phase changes/hops during normal operation or framing, and allows the recovered clock to be replicated and distributed to other circuits using PLL-based logic elements.

Decoder Block

The decoder logic block performs two primary functions: decoding the received transmission characters back into Data and Command Character codes, and comparing generated BIST patterns with received characters to permit at-speed link and device testing.

5B/4B, 6B/5B Decoder

The framed parallel output of the Deserializer is passed to the 5B/4B, 6B/5B Decoder. If the Decoder is enabled, it is transformed from a 10-bit or 12-bit transmission character back to the original Data and Command Character codes. This block uses the standard decoder patterns in Table 7 and Table 8 of this data sheet. Data Patterns on the data bus are indicated by a LOW on RXSC/D, and Command Character codes on the command bus are indicated by a HIGH. Invalid patterns or disparity errors are signaled as errors by a HIGH on VLTN.

If the Decoder is bypassed and BYTE8/$\overline{10}$ is HIGH, the ten (10) data bits of each transmission character are passed unchanged from the framer to the Pipeline Register.

When the Decoder is bypassed and BYTE8/$\overline{10}$ is LOW, the twelve (12) data bits of each transmission character are passed unchanged from the framer to the Pipeline Register.

BIST LFSR

The output register of the Decoder block is normally used to accumulate received characters for delivery to the Receive Formatter block. When configured for BIST mode ($\overline{\text{RXBISTEN}}$ is LOW), this register becomes a signature pattern generator and checker by logically converting to a Linear Feedback Shift Register (LFSR). When enabled, this LFSR generates a 511-character sequence that includes all Data and Command Character codes, including the explicit violation symbols. This provides a predictable but pseudo-random sequence that can be matched to an identical LFSR in the Transmitter. When synchronized with the received data stream, it checks each character in the Decoder with each character generated by the LFSR and indicates compare errors at the VLTN output of the Receive Output Register.

The LFSR is initialized by the BIST hardware to the BIST loop start code of HEX data 00 (00 is sent only once per BIST loop). Once the start of the BIST loop has been detected by the receiver, RXRVS is asserted for pattern mismatches between the received characters and the internally generated character sequence. Code rule violations or running disparity errors that occur as part of the BIST loop do not cause an error indication. RXFULL pulses asserted for one RXCLK cycle per BIST loop and can be used to check test pattern progress.

The specific patterns checked by the receiver are described in Table 4.

If a large number of errors are detected, the receive BIST state machine aborts the compare operations and resets the LFSR to the D0.0 state to look for the start of the BIST sequence again.

Receive Control State Machine

The Receive Control State Machine responds to multiple input conditions to control the routing and handling of received characters. It controls the staging of characters across various registers and the Receive FIFO. It controls the various discard policies and error control within the receiver, and operates in response to:

- the received character stream
- the room for additional data in the Receive FIFO
- the state of the receiver BIST enable ($\overline{\text{RXBISTEN}}$)
- the state of $\overline{\text{FIFOBYP}}$.

These signals and conditions are used by the Receive Control State Machine to control the Receive Formatter, write access to the Receive FIFO, the Receive Output register, and BIST. They determine the content of the characters passed to each of these destinations.

Table 4. CY7C9689A TAXI HOTLink BIST Sequence

D.00	C.JK	C.IH	C.SR	C.SS	C.QQ	D.FB	D.77	D.3D	D.1E	C.HH	D.8F	D.4B	D.23	D.11	D.04
C.JK	C.IH	C.QI	D.EE	C.RR	D.B3	D.55	D.2C	C.JK	C.RS	D.C5	D.68	C.II	C.RS	D.C0	C.TS
C.TR	C.SR	C.SS	C.QQ	D.F8	C.TS	C.QH	D.D2	C.RR	D.BC	C.TT	C.QH	D.D7	D.6D	D.3A	C.HH
D.89	D.42	C.HI	D.94	C.TT	C.TR	C.QI	D.EB	D.73	D.35	D.1C	C.JK	C.RS	D.CF	D.6B	D.33
D.15	D.0C	C.JK	C.RS	D.CD	D.6A	C.HI	D.91	D.44	C.II	C.IH	C.QI	D.E6	C.RR	D.B2	C.HQ
D.A8	C.TT	C.QH	D.D4	C.TS	C.TR	C.QI	D.E3	D.71	D.34	C.JK	C.IH	C.QI	D.ED	D.7A	C.HI
D.99	D.46	C.HI	D.96	C.HQ	D.AE	C.HQ	D.A3	D.51	D.24	C.JK	C.IH	C.QI	D.EC	C.TS	C.QH
D.D1	D.64	C.II	C.IH	C.QI	D.E4	C.RR	C.TR	C.QI	D.E0	C.TS	C.TR	C.SR	C.SS	C.SS	C.SS
C.SS	C.QQ	D.F0	C.TS	C.TR	C.SR	C.QQ	D.F4	C.TS	C.TR	C.QI	D.E1	D.70	C.II	C.IH	C.SR
C.QQ	D.FC	C.TS	C.QH	D.D3	D.65	D.38	C.JK	C.RS	D.C6	C.RR	D.B6	C.HQ	D.AA	C.HQ	D.A1
D.50	C.II	C.IH	C.SR	C.QQ	D.FD	D.7E	C.HI	D.9B	D.47	D.29	D.12	C.HH	D.8C	C.TT	C.QH
D.DD	D.6E	C.HI	D.93	D.45	D.28	C.JK	C.RS	D.C4	C.TS	C.TR	C.QI	D.E2	C.RR	D.B0	C.TT
C.TR	C.SR	C.QQ	D.F6	C.RR	D.BA	C.HQ	D.A9	D.52	C.HI	D.9C	C.TT	C.QH	D.DF	D.6F	D.3B
D.17	D.0D	D.0A	C.HH	D.85	D.48	C.II	C.RS	D.C8	C.TS	C.QH	D.D8	C.TS	C.QH	D.DA	C.RR
D.BD	D.5E	C.HI	D.9F	D.4F	D.2B	D.13	D.05	D.08	C.JK	C.RS	D.CC	C.TS	C.QH	D.D9	D.66
C.HI	D.92	C.HQ	D.AC	C.TT	C.QH	D.D5	D.6C	C.II	C.RS	D.C1	D.60	C.II	C.IH	C.SR	C.SS
C.SS	C.SS	C.QQ	D.F1	D.74	C.II	C.IH	C.QI	D.E5	D.78	C.II	C.RS	D.C2	C.RR	D.B4	C.TT
C.TR	C.QI	D.E9	D.72	C.HI	D.98	C.TT	C.QH	D.DE	C.RR	D.BF	D.5F	D.2F	D.1B	D.07	D.09
D.02	C.HH	D.84	C.TT	C.TR	C.QI	D.EA	C.RR	D.B1	D.54	C.II	C.IH	C.QI	D.E7	D.79	D.36
C.HH	D.8A	C.HQ	D.A5	D.58	C.II	C.RS	D.CA	C.RR	D.B5	D.5C	C.II	C.RS	D.CB	D.63	D.31
D.14	C.JK	C.IH	C.QI	D.EF	D.7B	D.37	D.1D	D.0E	C.HH	D.87	D.49	D.22	C.HH	D.80	C.TT
C.TR	C.SR	C.SS	C.QQ	D.F9	D.76	C.HI	D.9A	C.HQ	D.AD	D.5A	C.HI	D.9D	D.4E	C.HI	D.97
D.4D	D.2A	C.HH	D.81	D.40	C.II	C.IH	C.SR	C.SS	C.QQ	D.FA	C.RR	D.B9	D.56	C.HI	D.9E
C.HQ	D.AF	D.5B	D.27	D.19	D.06	C.HH	D.86	C.HQ	D.A6	C.HQ	D.A2	C.HQ	D.AO	C.TT	C.TR
C.SR	C.SS	C.SS	C.QQ	D.F2	C.RR	D.B8	C.TT	C.QH	D.D6	C.RR	D.BE	C.HQ	D.AB	D.53	D.25
D.18	C.JK	C.RS	D.CE	C.RR	D.B7	D.5D	D.2E	C.HH	D.83	D.41	D.20	C.JK	C.IH	C.SR	C.SS
C.SS	C.QQ	D.F3	D.75	D.3C	C.JK	C.RS	D.C7	D.69	D.32	C.HH	D.88	C.TT	C.QH	D.DC	C.TS
C.QH	D.DB	D.67	D.39	D.16	C.HH	D.8E	C.HQ	D.A7	D.59	D.26	C.HH	D.82	C.HQ	D.A4	C.TT
C.TR	C.QI	D.E8	C.TS	C.QH	D.D0	C.TS	C.TR	C.SR	C.QQ	D.F5	D.7C	C.II	C.RS	D.C3	D.61
D.30	C.JK	C.IH	C.SR	C.QQ	D.FE	C.RR	D.BB	D.57	D.2D	D.1A	C.HH	D.8D	D.4A	C.HI	D.95

The Receive Control State Machine always operates synchronous to the recovered character clock (bit-clock/10 or bit-clock/12). When the Receive FIFO is bypassed, RXCLK becomes an output that changes synchronous to the internal character clock. RXCLK operates at the same frequency as the internal character clock.

Discard Policies

When the Receive FIFO is enabled, the Receive Control State Machine has the ability to selectively discard specific characters from the data stream that are determined by the present configuration as being unnecessary. When discarding is enabled, it reduces the host system overhead necessary to keep the Receive FIFO from overflowing and losing data.

The discard policy is configured as part of the operating mode and is set using the RXMODE[1:0] inputs. The four discard policies are listed in Table 5.

Table 5. Receiver Discard Policies

Policy #	Policy Description
0 (00)	Keep all received characters
1 (01)	Process Commands, discard all but the last JK or LM SYNC character
2 (1X)	Process Commands, discard all C5.0 characters

Policy 0 is the simplest and also applies for all conditions where the Receive FIFO is bypassed. In this mode, every character that is received is placed into the Receive FIFO (when enabled) or into the Receive Output Register.

In discard policy 1, the JK or LM SYNC character, which is automatically transmitted when no data is present in the Transmit FIFO, is treated differently here. In this mode, whenever two or more adjacent JK or LM characters are received, all of them are discarded except the last one received before any other character type. This allows these fill characters to be removed from the data stream, but the last SYNC character which can be used as a delimiter.

Policy 2 is identical to policy 1 except that all C5.0 characters are removed from the data stream.

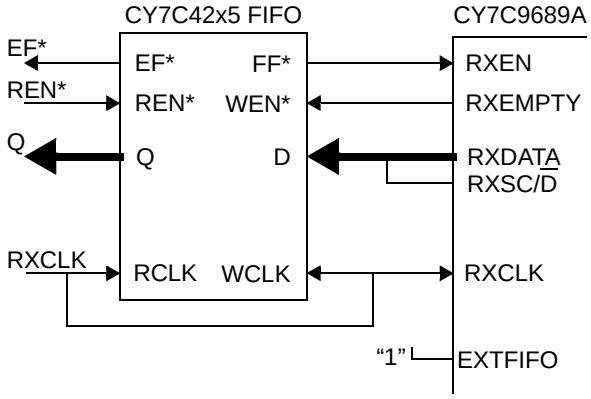
When the FIFOs are bypassed ($\overline{\text{FIFOBYP}}$ LOW), no characters are actually discarded, but the receiver discard policy can be used to control external filtering of the data. The $\overline{\text{RXEMPTY}}$ FIFO flag is used to indicate if the character on the output bus is valid or not. In discard policy 0, the $\overline{\text{RXEMPTY}}$ flag is always deasserted to indicate that valid data is always present. In discard policy 1, the $\overline{\text{RXEMPTY}}$ flag indicates an empty condition for all but the last JK or LM character before any other character is presented. In discard policy 2, the $\overline{\text{RXEMPTY}}$ flag indicates an empty condition for all JK or LM SYNC characters. When any other character is present, this flag indicates that valid or "interesting" Data or Special Characters are present.

Receive FIFO

The Receive FIFO is used to buffer data captured from the selected serial stream for later processing by the host system. This FIFO is sized to hold 256 14-bit characters. When the FIFO is enabled, it is written to by the Receive Control State Machine. When data is present in the Receive FIFO (as indicated by the RXFULL, RXHALF, and $\overline{\text{RXEMPTY}}$ Receive FIFO status flags), it can be read from the Output Register by asserting $\overline{\text{CE}}$ and $\overline{\text{RXEN}}$.

The read port on the Receive FIFO may be configured for the same two timing models as the transmit interface: UTOPIA and Cascade. Both are forms of a FIFO interface. The UTOPIA timing model has active LOW $\overline{\text{RXEMPTY}}$ and $\overline{\text{RXFULL}}$ status flags, and an active LOW $\overline{\text{RXEN}}$ enable. When configured for Cascade operation, these same signals are all active HIGH. Either timing model supports connection to various host bus interfaces, state machines, or external FIFOs for depth expansion (see *Figure 4)*

Figure 4. External FIFO Depth Expansion of the CY7C9689A Receive Data Path)



The Receive FIFO presents Full, Half-Full, and Empty FIFO status flags. These flags are provided synchronous to RXCLK to allow operation with a Moore-type external controlling state machine. When configured with the Receive FIFO enabled, RXCLK is an input. When the Receive FIFO is bypassed (FIFOBYP is LOW), RXCLK is an output operating at the received character rate.

Receive Input Register

The input register is clocked by the rising edge of RXCLK. It samples numerous signals that control the reading of the Receive FIFO and operation of the Receive Control State Machine.

Receive Output Register

The Receive Output Register changes in response to the rising edge of RXCLK. The Receive FIFO status flag outputs of this register are placed in a High-Z state when the CY7C9689A is not addressed ($\overline{\text{CE}}$ is sampled HIGH). The RXDATA bus output drivers are enabled when the device is selected by $\overline{\text{RXEN}}$ being asserted in the RXCLK cycle immediately following that in which the device was addressed ($\overline{\text{CE}}$ is sampled LOW), and $\overline{\text{RXEN}}$ being sampled by RXCLK. This initiates a Receive FIFO read cycle.

Just as with the TXDATA bus on the Transmit Input Register, the receive outputs are also mapped by the specific decoding and bus-width selected by the ENCBYP, BYTE8/10 and FIFOBYP inputs. These assignments are shown in *Table 6*.

If the Receive FIFO and Decoder are bypassed, all received characters are passed directly to the Receive Output Register. If framing is enabled, and JK or LM sync characters have been detected meeting the present framing requirements, the output characters will appear on proper character boundaries. If framing is disabled (RFEN is LOW) or sync characters have not been detected in the data stream, the received characters may not be output on their proper 10-bit boundaries. In this mode, some form of external framing and decoding/descrambling must be used to recover the original source data.

Table 6. Receiver Output Bus Signal Map

RXDATA Bus Output Bit	Receiver Decoder Mode[1]			
	Encoded 8-bit Character Stream[8]	Pre-encoded 10-bit Character Stream	Encoded 10-bit Character Stream[9]	Pre-encoded 12-bit Character Stream
RXSC/$\overline{D}$	RXSC/$\overline{D}$		RXSC/$\overline{D}$	
RXDATA[0]	RXDATA[0]	RXD[0][10, 11]	RXDATA[0]	RXD[0][10, 12]
RXDATA[1]	RXDATA[1]	RXD[1]	RXDATA[1]	RXD[1]
RXDATA[2]	RXDATA[2]	RXD[2]	RXDATA[2]	RXD[2]
RXDATA[3]	RXDATA[3]	RXD[3]	RXDATA[3]	RXD[3]
RXDATA[4]	RXDATA[4]	RXD[4]	RXDATA[4]	RXD[4]
RXDATA[5]	RXDATA[5]	RXD[5]	RXDATA[5]	RXD[5]
RXDATA[6]	RXDATA[6]	RXD[6]	RXDATA[6]	RXD[6]
RXDATA[7]	RXDATA[7]	RXD[7]	RXDATA[7]	RXD[7]
RXDATA[8]/RXCMD[3]	RXCMD[3]	RXD[8]	RXDATA[8]	RXD[8]
RXDATA[9]/RXCMD[2]	RXCMD[2]	RXD[9]	RXDATA[9][9]	RXD[9]
RXCMD[1]	RXCMD[1]		RXCMD[1]	RXD[10][12]
RXCMD[0]	RXCMD[0]		RXCMD[0]	RXD[11]
VLTN	VLTN		VLTN	

Notes
8. When BYTE8/10 is HIGH, received bit order is decoded form the serial stream and presented (MSB to LSB) at RXDATA[7,6,5,4] and RXDATA[3,2,1,0] or RXCMD[3,2,1,0] as indicated by RXSC/D.
9. When BYTE8/10 is LOW, received bit order is decoded form the serial stream and presented (MSB to LSB) at RXDATA[8,7,6,5,4] and RXDATA[9,3,2,1,0] or RXCMD[1,0] as indicated by RXSC/D.
10. First bit shifted into the receiver.
11. When ENCBYP is LOW and BYTE8/10 is HIGH, the received bit order is (LSB to MSB) RXD[0,1,2,3,4,5,6,7,8,9].
12. When ENCBYP is LOW and BYTE8/10 is LOW, the received bit order is (LSB to MSB) RXD[0,1,2,3,4,5,6,7,8,9,11,10].

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with (power applied)–55 °C to +125 °C

Supply voltage to ground potential .....–0.5 v to +6.5 v

DC voltage applied to outputs..... –0.5 v to V_{DD} + 0.5 v

Output current into TTL outputs (LOW) ..... 30 mA

DC input voltage ..... –0.5 v to V_{DD} + 0.5 v

Static discharge voltage..... > 2001 V (per MIL-STD-883, Method 3015)

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}
Commercial	0 °C to +70 °C	5.0 V ± 10%
Industrial	–40 °C to +85 °C	5.0 V ± 10%

CY7C9689A DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
TTL Outputs					
V_{OHT}	Output HIGH voltage	I_{OH} = –2 mA, V_{DD} = Min.	2.4	–	V
V_{OLT}	Output LOW voltage	I_{OL} = 8 mA, V_{DD} = Min.	–	0.4	V
I_{OST}	Output short circuit current	V_{OUT} = 0 V[13]	–30	–80	mA
I_{OZL}	High-Z output leakage current		–20	20	mA
TTL Inputs					
V_{IHT}	Input HIGH voltage		2.0	V_{CC}	V
V_{ILT}	Input LOW voltage		–0.5	0.8	V
I_{IHT}	Input HIGH current	V_{IN} = V_{DD}	–	±40	µA
I_{ILT}	Input LOW current	V_{IN} = 0.0 V	–	–40	µA
I_{ILPDT}	Input HIGH current with internal pull-down	V_{IN} = V_{CC}	–	+300	µA
I_{ILPUT}	Input LOW current with internal pull-up	V_{IN} = 0.0 V	–300	–	µA
Transmitter PECL-Compatible Output Pins: OUTA+, OUTA–, OUTB+, OUTB–					
V_{OHE}	Output HIGH voltage (V_{DD} referenced)	Load = 50 Ω to V_{DD} – 1.33 v; R_{CURSET} = 10 k	V_{DD} – 1.03	V_{DD} – 0.83	V
V_{OLE}	Output LOW voltage (V_{DD} referenced)	Load = 50 Ω to V_{DD} – 1.33 v; R_{CURSET} = 10 k	V_{DD} – 2.0	V_{DD} – 1.62	V
V_{ODIF}	Output differential voltage |(OUT+) – (OUT–)|	Load = 50 Ω to V_{DD} – 1.33 v; R_{CURSET} = 10 k	600	1100	mV
Receiver Single-ended PECL-Compatible Input Pin: CARDET					
V_{IHE}	Input HIGH voltage (V_{DD} referenced)		V_{DD} – 1.165	V_{DD}	V
V_{ILE}	Input LOW voltage (V_{DD} referenced)		2.5	V_{DD} – 1.475	V
I_{IHE}	Input HIGH current	V_{IN} = V_{IHE}(min.)	–	+40	µA
I_{ILE}	Input LOW current	V_{IN} = V_{ILE}(max.)	–40		µA
Receiver Differential Line Receiver Input Pins: INA+, INA–, INB+, INB–					
V_{DIFF}	Input differential voltage |(IN+) – (IN–)|		200	2500	mV
V_{IHH}	Highest input HIGH voltage		–	V_{DD}	V
V_{ILL}	Lowest input LOW voltage		2.5	–	V
I_{IHH}	Input HIGH current	V_{IN} = V_{IHH} Max.	–	750	µA
I_{ILL}[14]	Input LOW current	V_{IN} = V_{ILL} Min.	–200	–	µA

Notes

13. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
14. To guarantee positive currents for all PECL voltages, an external pull-down resistor must be present.

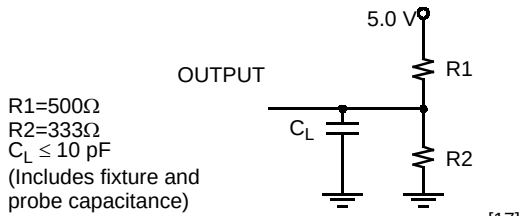
CY7C9689A DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
Miscellaneous				**Typ.**	**Max.**	
I_{DD}[15]	Power supply current	Freq. = Max.	Commercial	170	250	mA

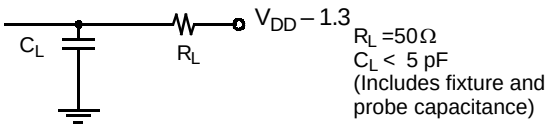
Capacitance[16]

Parameter	Description	Test Conditions	Max.	Unit
C_{INTTL}	TTL input capacitance	T_A = 25 °C, f_0 = 1 MHz, V_{DD} = 5.0 V	7	pF
C_{INPECL}	PECL input capacitance	T_A = 25 °C, f_0 = 1 MHz, V_{DD} = 5.0 V	4	pF

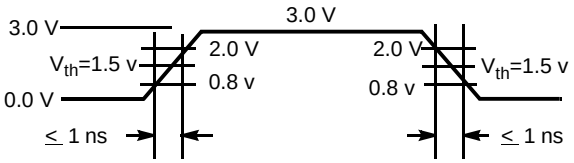
AC Test Loads and Waveforms



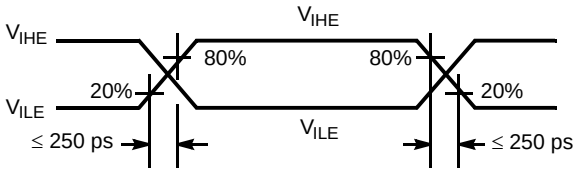
(a) TTL AC Test Load[17]



(b) PECL AC Test Load [17]



(c) TTL Input Test Waveform



(d) PECL Input Test Waveform

Notes
15. Maximum I_{CC} is measured with V_{DD} = MAX, RFEN = LOW, and outputs unloaded. Typical I_{DD} is measured with V_{DD} = 5.0 V, T_A = 25 °C, RFEN = LOW, and outputs unloaded.
16. Tested initially and after any design or process changes that may affect these parameters, but not 100% tested.
17. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only.

CY7C9689A Transmitter TTL Switching Characteristics, FIFO Enabled Over the Operating Range

Parameter	Description	Min.	Max.	Unit
f_{TS}	TXCLK clock cycle frequency with transmit FIFO enabled		50	MHz
t_{TXCLK}	TXCLK period	20	–	ns
t_{TXCPWH}	TXCLK HIGH time	6.5	–	ns
t_{TXCPWL}	TXCLK LOW time	6.5	–	ns
t_{TXCLKR}[16]	TXCLK Rise time[18]	0.7	5	ns
t_{TXCLKF}[16]	TXCLK fall time[18]	0.7	5	ns
t_{TXA}	Flag access time from TXCLK↑ to Output	2	15	ns
t_{TXDS}	Transmit data set-up time to TXCLK↑	4	–	ns
t_{TXDH}	Transmit data hold time from TXCLK↑	1	–	ns
t_{TXENS}	Transmit enable set-up time to TXCLK↑	4	–	ns
t_{TXENH}	Transmit enable hold time from TXCLK↑	1	–	ns
t_{TXRSS}	Transmit FIFO Reset ($\overline{TXRST}$) set-up time to TXCLK↑	4	–	ns
t_{TXRSH}	Transmit FIFO Reset ($\overline{TXRST}$ hold time from TXCLK↑	1	–	ns
t_{TXCES}	Transmit chip enable ($\overline{CE}$) set-up time to TXCLK↑	4	–	ns
t_{TXCEH}	Transmit chip enable ($\overline{CE}$) hold time from TXCLK↑	1	–	ns
t_{TXZA}	Sample of $\overline{CE}$ LOW by TXCLK↑, output high-Z to Active HIGH or LOW	0	–	ns
t_{TXOE}	Sample of $\overline{CE}$ LOW by TXCLK↑ to output valid	1.5	20	ns
t_{TXAZ}	Sample of $\overline{CE}$ HIGH by TXCLK↑ to output in high-Z	1.5	20	ns

CY7C9689A Receiver TTL Switching Characteristics, FIFO Enabled Over the Operating Range

Parameter	Description	Min.	Max.	Unit
f_{RIS}	RXCLK clock cycle frequency with receive FIFO enabled		50	MHz
$t_{RXCLKIP}$	RXCLK input period	20		ns
t_{RXCPWH}	RXCLK input HIGH time	6.5		ns
t_{RXCPWL}	RXCLK input LOW time	6.5		ns
$t_{RXCLKIR}$[16]	RXCLK input Rise time[18]	0.7	5	ns
$t_{RXCLKIF}$[16]	RXCLK input Fall time[18]	0.7	5	ns
t_{RXENS}	Receive enable set-up time to RXCLK↑	4		ns
t_{RXENH}	Receive enable hold time from RXCLK↑	1		ns
t_{RXRSS}	Receive FIFO reset ($\overline{RXRXT}$) set-up time to RXCLK↑	4		ns
t_{RXRSH}	Receive FIFO reset ($\overline{RXRXT}$) hold time from RXCLK↑	1		ns
t_{RXCES}	Receive chip enable ($\overline{CE}$) set-up time to RXCLK↑	4		ns
t_{RXCEH}	Receive chip enable ($\overline{CE}$) Hold Time from RXCLK↑	1		ns
t_{RXA}	Flag and data access time from RXCLK↑ to output	1.5	15	ns
t_{RXZA}	Sample of $\overline{CE}$ LOW by RXCLK↑, Output High-Z to Active HIGH or LOW,[19] or Sample of RXEN Asserted by RXCLK↑, Output High-Z to Active HIGH or LOW	0		ns
t_{RXOE}	Sample of $\overline{CE}$ LOW by RXCLK↑ to Output Valid,[19] or Sample of RXEN Asserted by RXCLK↑ to RXDATA Outputs Valid	1.5	20	ns
t_{RXZA}	Sample of $\overline{CE}$ HIGH by RXCLK↑ to Output in High-Z,[19] or Sample of RXEN Asserted by RXCLK↑ to RXDATA Outputs in High-Z	1.5	20	ns

Notes
18. Input/output rise and fall time is measured between 0.8 v and 2.0 V
19. Parallel data output specifications are only valid if all outputs are loaded with similar DC and AC loads.

CY7C9689A Transmitter TTL Switching Characteristics, FIFO Bypassed Over the Operating Range

Parameter	Description	Min.	Max.	Unit
t_{TRA}	Flag access time from REFCLK↑ to output	2	15	ns
t_{REFDS}	Write data set-up time to REFCLK↑	4		ns
t_{REFDH}	Write data hold time from REFCLK↑	2		ns
t_{REFENS}	Transmit enable set-up time to REFCLK↑	4		ns
t_{REFENH}	Transmit enable hold time from REFCLK↑	2		ns
t_{REFCES}	Transmit chip enable ($\overline{CE}$) set-up time to REFCLK↑	4		ns
t_{REFCEH}	Transmit chip enable ($\overline{CE}$) hold time from REFCLK↑	2		ns
t_{REFZA}	Sample of $\overline{CE}$ LOW by REFCLK↑, output High-Z to Active HIGH or LOW	0		ns
t_{REFOE}	Sample of $\overline{CE}$ LOW by REFCLK↑ to flag output Valid	1.5	20	ns
t_{REFAZ}	Sample of $\overline{CE}$ HIGH by REFCLK↑ to flag output High-Z	1.5	20	ns

CY7C9689A Receiver TTL Switching Characteristics, FIFO Bypassed Over the Operating Range

Parameter	Description	Min.	Max.	Unit
f_{ROS}[20]	RXCLK clock output frequency—100 to 200 MBaud 8-bit Operation (SPDSEL is HIGH and BYTE8/10 is HIGH)	10	20	MHz
	RXCLK clock output frequency—50 to 100 MBaud 8-bit Operation (SPDSEL is LOW and BYTE8/10 is HIGH)	5	10	MHz
	RXCLK clock output frequency—100 to 200 MBaud 10-bit Operation (SPDSEL is HIGH and BYTE8/10 is LOW)	8.33	16.67	MHz
	RXCLK clock output frequency—50 to 100 MBaud 10-bit Operation (SPDSEL is LOW and BYTE8/10 is LOW)	4.16	8.33	MHz
$t_{RXCLKOP}$	RXCLK output period	25	240	ns
$t_{RXCLKOD}$	RXCLK output duty cycle	40	60	%
$t_{RXCLKOR}$[16]	RXCLK output rise time[18]	0.25	2	ns
$t_{RXCLKOF}$[16]	RXCLK output fall time[18]	0.25	2	ns
t_{RXENS}	Receive enable set-up time to RXCLK↑	4		ns
t_{RXENH}	Receive enable hold time from RXCLK↑	1		ns
t_{RXZA}	Sample of $\overline{CE}$ LOW by RXCLK↑, Outputs High-Z to Active Sample of RXEN Asserted by RXCLK↑ to RXDATA Outputs High-Z to Active	0		ns
t_{RXOE}	Sample of $\overline{CE}$ LOW by RXCLK↑ to Flag Output Valid Sample of RXEN Asserted by RXCLK↑ to RXDATA Output Low-Z	1.5	20	ns
t_{RXAZ}	Sample of $\overline{CE}$ HIGH by RXCLK↑ to Flag Output High-Z Sample of RXEN Deasserted by RXCLK↑ to RXDATA Output High-Z	1.5	20	ns

Note
20. The period of t_{ROS} will match the period of the transmitter PLL reference (REFCLK) when receiving serial data. When data is interrupted, RXCLK may drift to REFCLK ±0.2%.

CY7C9689A REFCLK Input Switching Characteristics Over the Operating Range

Parameter	Description	Conditions			Min.	Max.	Unit
		SPDSEL	RANGESEL	BYTE8/10			
f_{REF}	REFCLK clock frequency—50 to 100 MBaud, 10-bit Mode, REFCLK = 2x Character Rate	0	0	0	8.33	16.67	MHz
	REFCLK clock frequency—50 to 100 MBaud, 8-bit Mode, REFCLK = 2x Character Rate	0	0	1	10	20	MHz
	REFCLK clock frequency—50 to 100 MBaud, 10-bit Mode, REFCLK = 4x Character Rate	0	1[18]	0	16.67	33.3	MHz
	REFCLK clock frequency—50 to 100 MBaud, 8-bit Mode, REFCLK = 4x Character Rate	0	1[18]	1	20	40	MHz
	REFCLK clock frequency—100 to 200 MBaud, 10-bit Mode, REFCLK = Character Rate	1	0	0	8.33	16.67	MHz
	REFCLK clock frequency—100 to 200 MBaud, 8-bit Mode, REFCLK = Character Rate	1	0	1	10	20	MHz
	REFCLK clock frequency—100 to 200 MBaud, 10-bit Mode, REFCLK = 2x Character Rate	1	1	0	16.67	33.3	MHz
	REFCLK clock frequency—100 to 200 MBaud, 8-bit Mode, REFCLK = 2x Character Rate	1	1	1	20	40	MHz
t_{REFCLK}	REFCLK period				25	120	ns
t_{REFH}	REFCLK HIGH time				6.5		ns
t_{REFL}	REFCLK LOW time				6.5		ns
t_{REFRX}	REFCLK frequency referenced to received clock period[22]				–0.04	+0.04	%

CY7C9689A Receiver Switching Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
t_B[23]	Bit time	20.0	5.0	ns
t_{SA}	Static alignment[16, 24]		600	ps
t_{EFW}	Error free window[16, 25, 26]	0.65		UI
t_{IN_J}	IN± peak-to-peak input jitter tolerance[16, 25, 27, 28]		0.5	UI

Notes

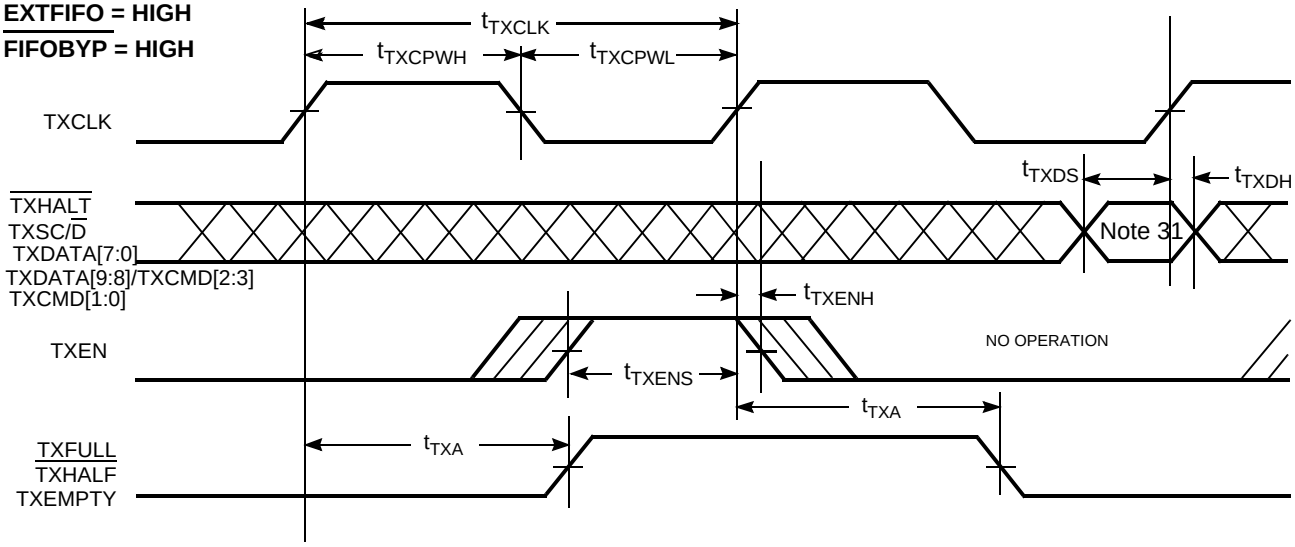
21. When configured for synchronous operation with the FIFOs bypassed ($\overline{\text{FIFOBYP}}$ is LOW), if RANGESEL is HIGH the SPDSEL input is ignored and operation is forced to the 100–200 MBaud range.
22. REFCLK has no phase or frequency relationship with RXCLK and only acts as a centering reference to reduce clock synchronization time. REFCLK must be within ±0.04% of the transmitter PLL reference (REFCLK) frequency, necessitating a ±200-PPM crystal.
23. The PECL switching threshold is the midpoint between the PECL– V_{OH}, and V_{OL} specification (approximately V_{DD} – 1.33 v).
24. Static alignment is a measure of the alignment of the Receiver sampling point to the center of a bit. Static alignment is measured by the absolute difference of the left and right edge shifts ($|t_{SH\_L} – t_{SH\_R}|$) of one bit until a character error occurs.
25. Receiver UI (Unit Interval) is calculated as $1/(f_{REF}*N)$ when operated in 8-bit mode (N = 10) and 10-bit mode (N = 12) if no data is being received, or $1/(f_{REF}*N)$ of the remote transmitter if data is being received. In an operating link this is equivalent to N * t_B when REFCLK = 1X the character rate. An alternate multiply ratios (2X or 4X, as selected by SPDSEL and RANGESEL), the numerator is multiplied by 2 or 4 respectively.
26. Error Free Window is a measure of the time window between bit centers where a transition may occur without causing a bit sampling error. EFW is measured over the operating range, input jitter < 50% Dj.
27. The specification is sum of 25% Duty Cycle Distortion (DCD), 10% Data Dependant Jitter (DDJ), 15% Random Jitter (RJ).
28. Parallel data output specifications are only valid if all outputs are loaded with similar DC and AC loads.

CY7C9689A Transmitter Switching Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
t_B[23]	Bit time	20.0	5.0	ns
t_{RISE}	PECL output rise time 20–80% (PECL Test Load)[16]	200	1700	ps
t_{FALL}	PECL output fall time 80–20% (PECL Test Load)[16]	200	1700	ps
t_{DJ}	Deterministic jitter (peak-peak)[16, 29]		0.02	UI
t_{RJ}	Random jitter (σ)[16, 30]		0.008	UI
t_{JT}	Transmitter total output jitter (peak-peak)[16]		0.08	UI

CY7C9689A HOTLink Transmitter Switching Waveforms

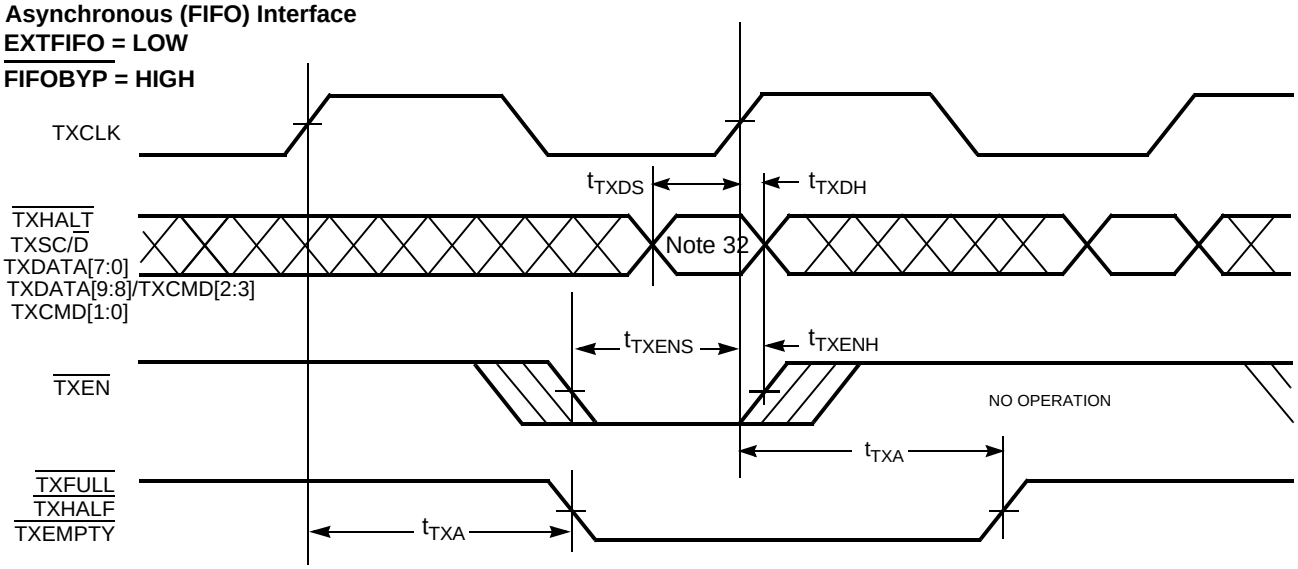
Write Cycle
Asynchronous (FIFO) Interface
EXTFIFO = HIGH
FIFOBYP = HIGH



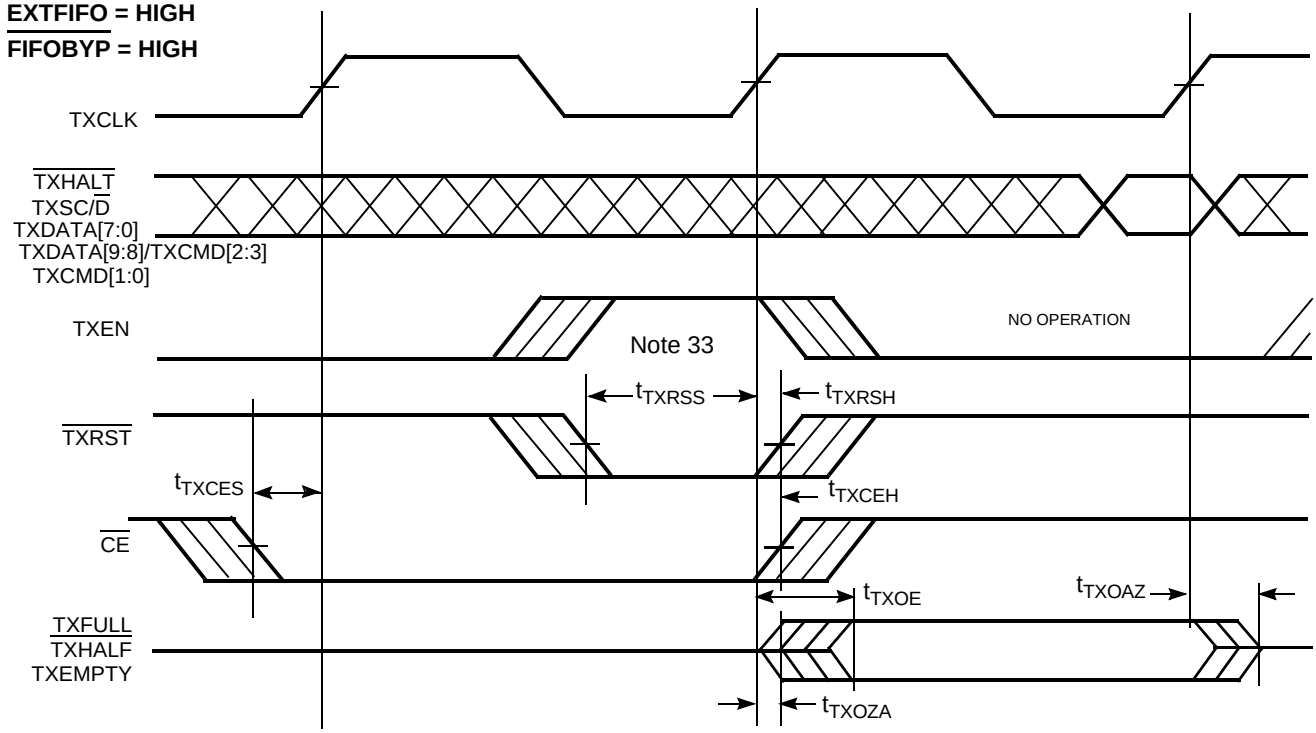
Notes
29. While sending continuous JK, outputs loaded to 50Ω to V_{DD} – 1.3 v, over the operating range.
30. While sending continuous HH, after 100,000 samples measured at the cross point of differential outputs, time referenced to REFCLK input, over the operating range.
31. When EXTFIFO is HIGH, the write data is captured on the clock cycle following TXEN = HIGH.

CY7C9689A HOTLink Transmitter Switching Waveforms (continued)

Write Cycle
Asynchronous (FIFO) Interface
EXTFIFO = LOW
$\overline{\text{FIFOBYP}}$ = HIGH



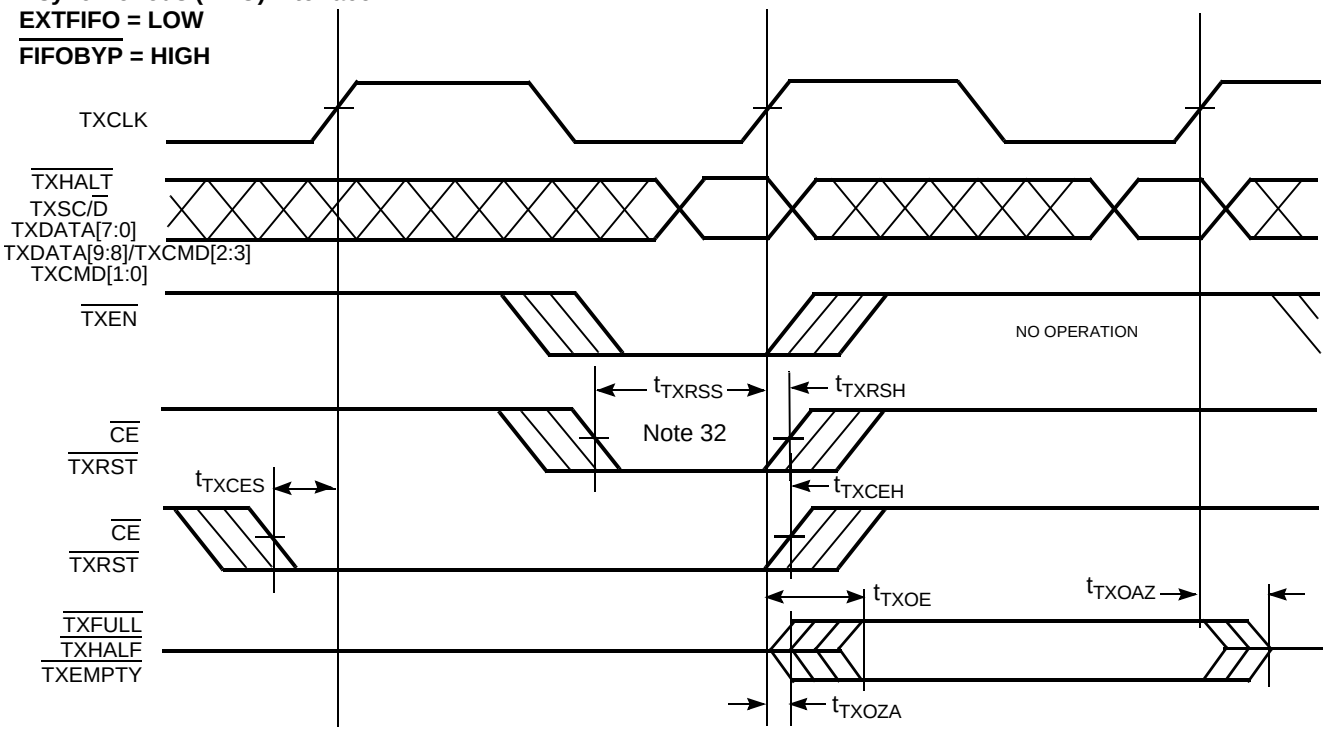
OUTPUT ENABLE Timing
Asynchronous (FIFO) Interface
EXTFIFO = HIGH
$\overline{\text{FIFOBYP}}$ = HIGH



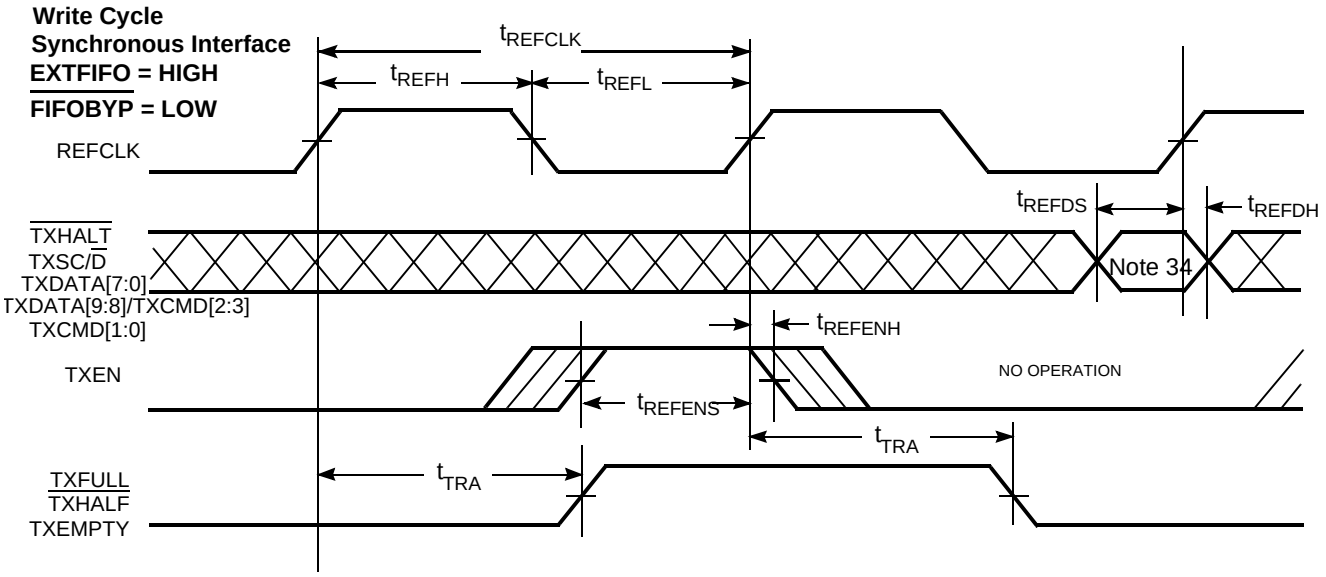
Notes
32. Illustrates timing only. TXEN and $\overline{\text{TXRST}}$ not usually active in same time period.
33. When transferring data to the Transmitter input from a depth expanded external FIFO, the data is captured from the external FIFO one clock cycle following the actual enable (TXEN = HIGH).

CY7C9689A HOTLink Transmitter Switching Waveforms (continued)

OUTPUT ENABLE Timing
Asynchronous (FIFO) Interface
EXTFIFO = LOW
$\overline{\text{FIFOBYP}}$ = HIGH



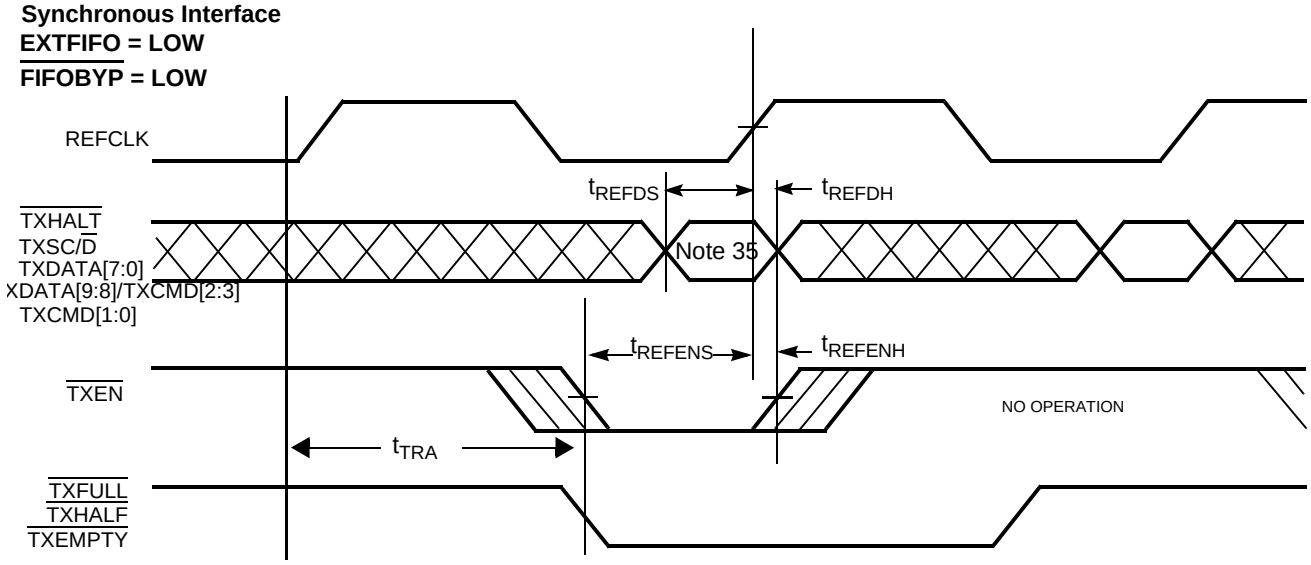
Write Cycle
Synchronous Interface
EXTFIFO = HIGH
$\overline{\text{FIFOBYP}}$ = LOW



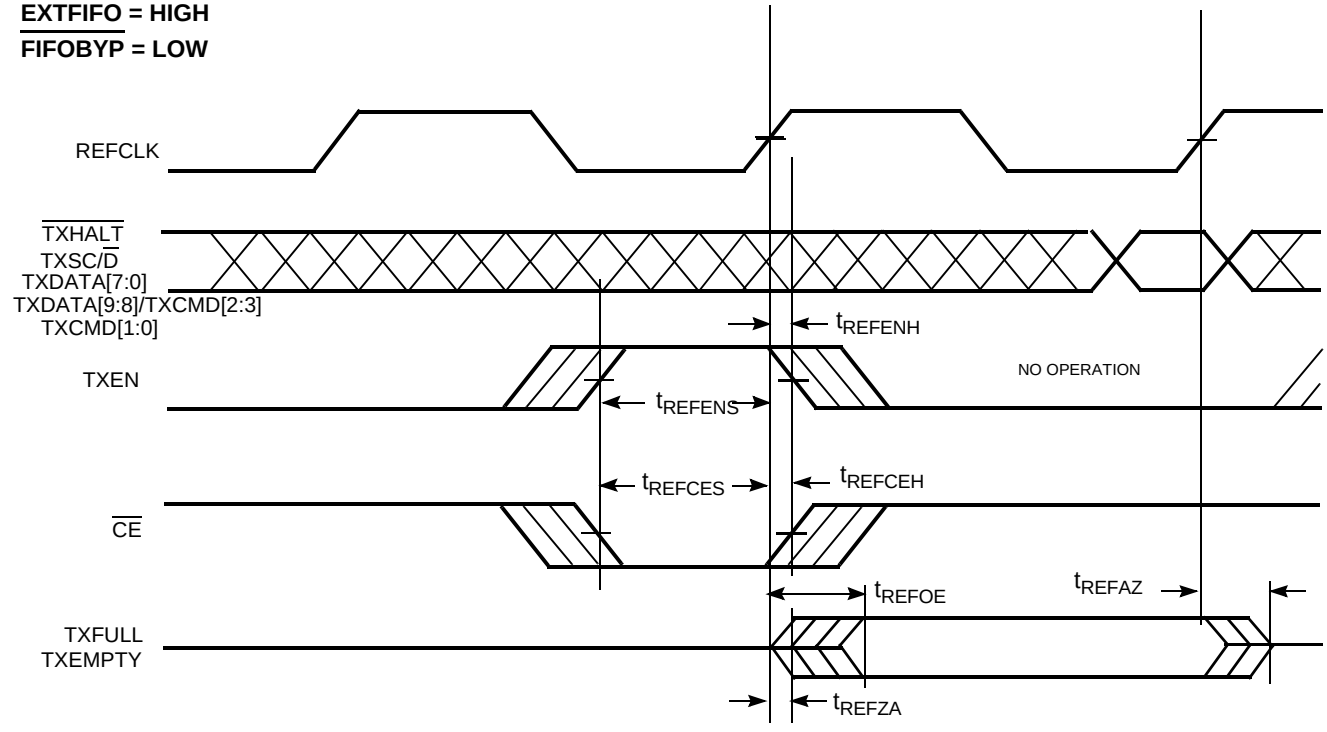
Note
34. \When transferring data to the Transmitter input from a synchronous external controller, the data is captured in the same clock cycle as the actual enable ($\overline{\text{TXEN}}$ = LOW).

CY7C9689A HOTLink Transmitter Switching Waveforms (continued)

Write Cycle
Synchronous Interface
EXTFIFO = LOW
FIFOBYP = LOW



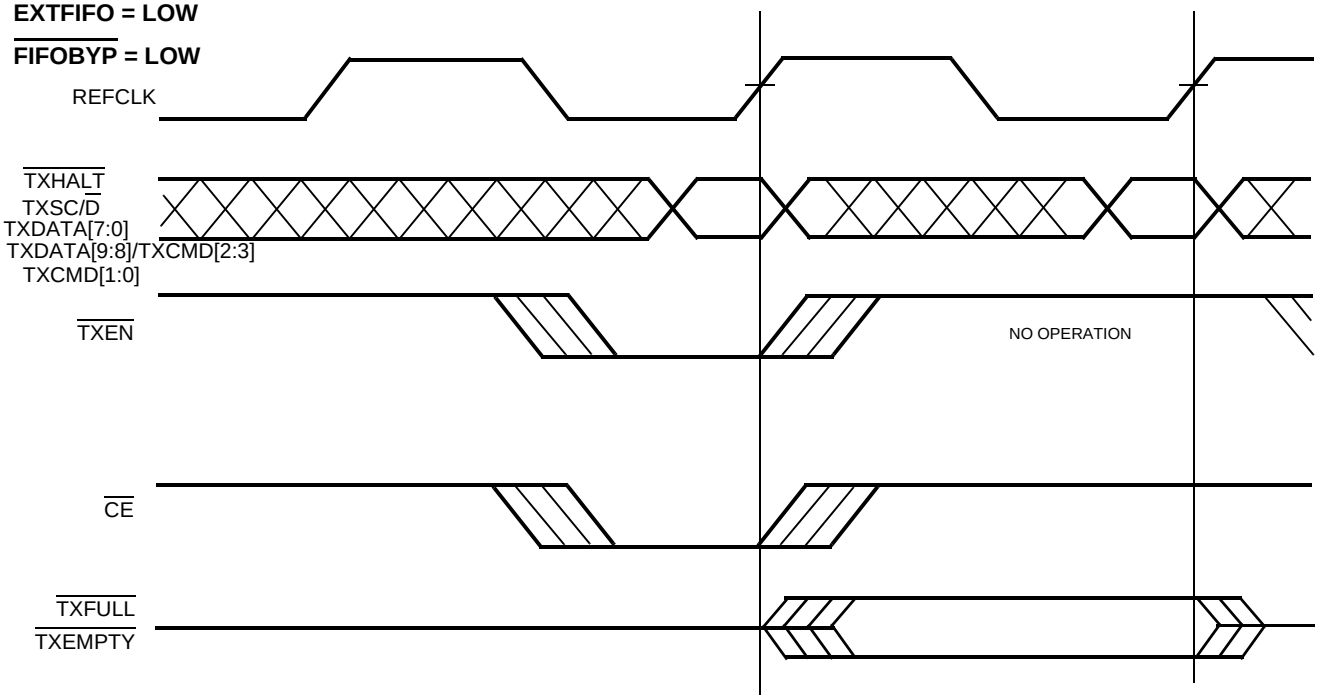
OUTPUT ENABLE Timing
Synchronous Interface
EXTFIFO = HIGH
FIFOBYP = LOW



Note
35. On inhibited reads, or if the Receive FIFO goes empty, the data outputs do not change.

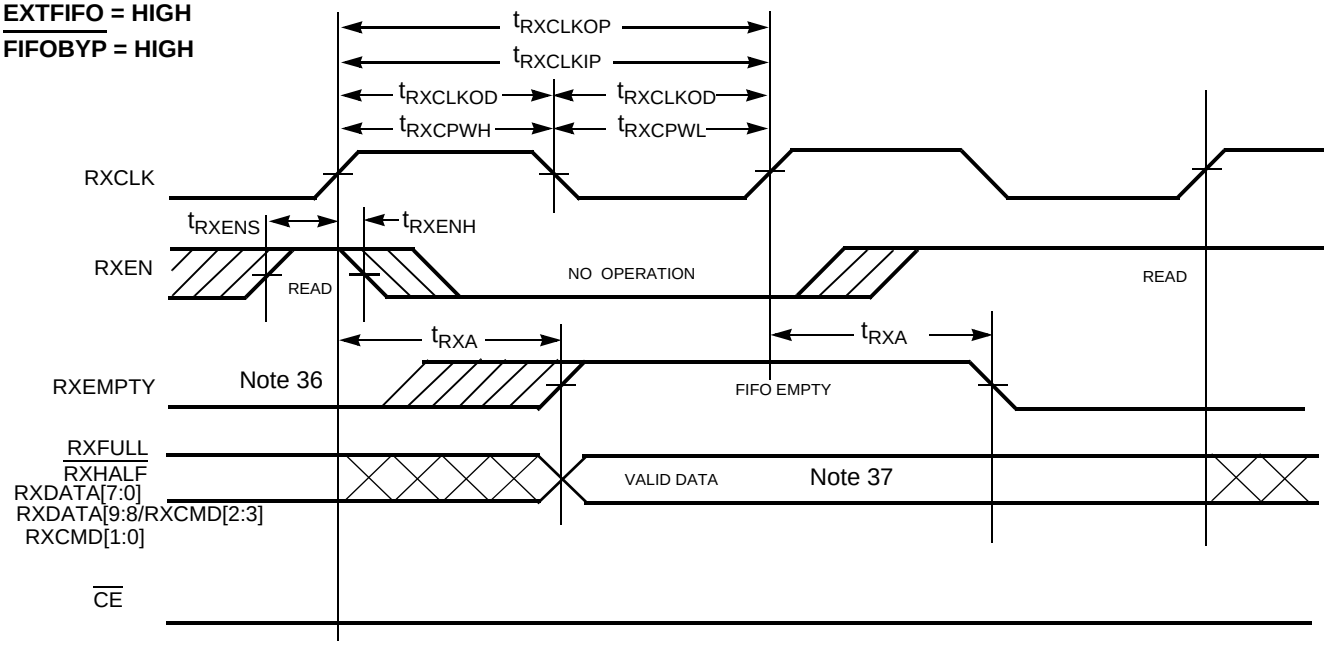
CY7C9689A HOTLink Transmitter Switching Waveforms (continued)

OUTPUT ENABLE Timing
Synchronous Interface
EXTFIFO = LOW
$\overline{\text{FIFOBYP}}$ = LOW

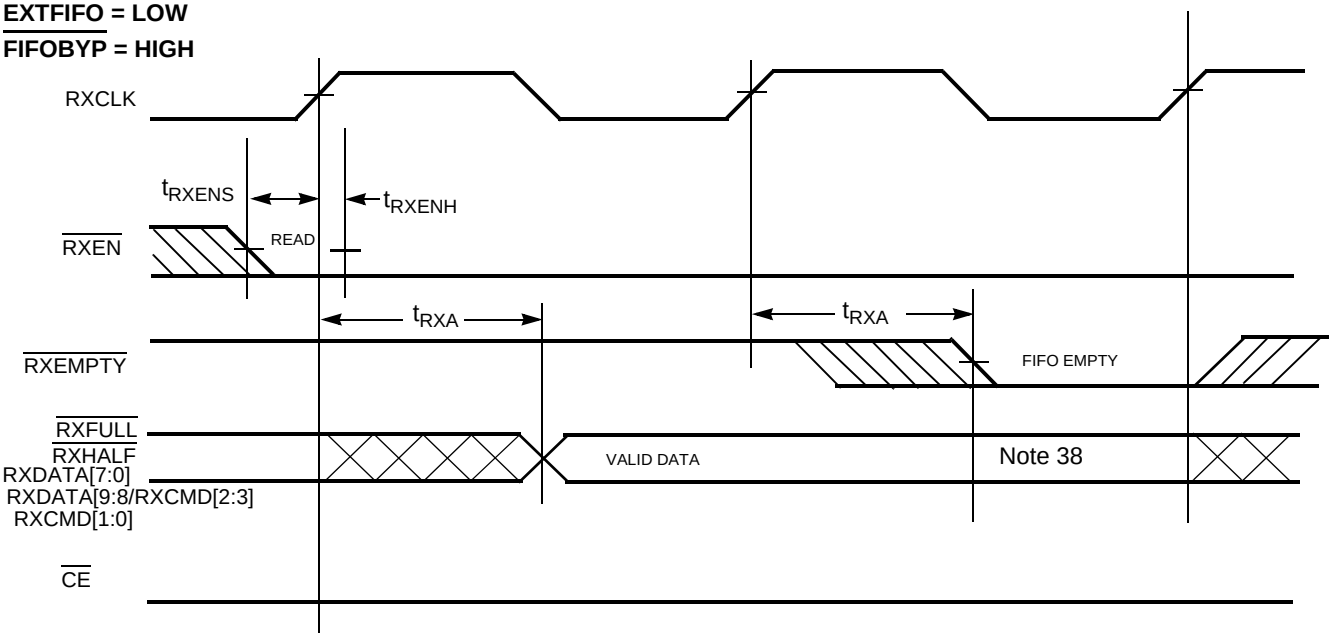


CY7C9689A HOTLink Receiver Switching Waveforms

Read Cycle
Asynchronous (FIFO) Interface
EXTFIFO = HIGH
$\overline{\text{FIFOBYP}}$ = HIGH



Read Cycle
Asynchronous (FIFO) Interface
EXTFIFO = LOW
$\overline{\text{FIFOBYP}}$ = HIGH



Notes
36. When reading data from synchronous data interface, the data is captured on any clock cycle that $\overline{\text{RXEN}}$ = LOW. $\overline{\text{RXEMPTY}}$ = HIGH indicates data is available. RXEMPTY = LOW indicates that the FIFO is empty.
37. Illustrates timing only. RXEN and $\overline{\text{RXRST}}$ not usually active in same time period.
38. Receive FIFO Reads are inhibited while the outputs are High-Z.

CY7C9689A HOTLink Receiver Switching Waveforms (continued)

Output Enable Timing

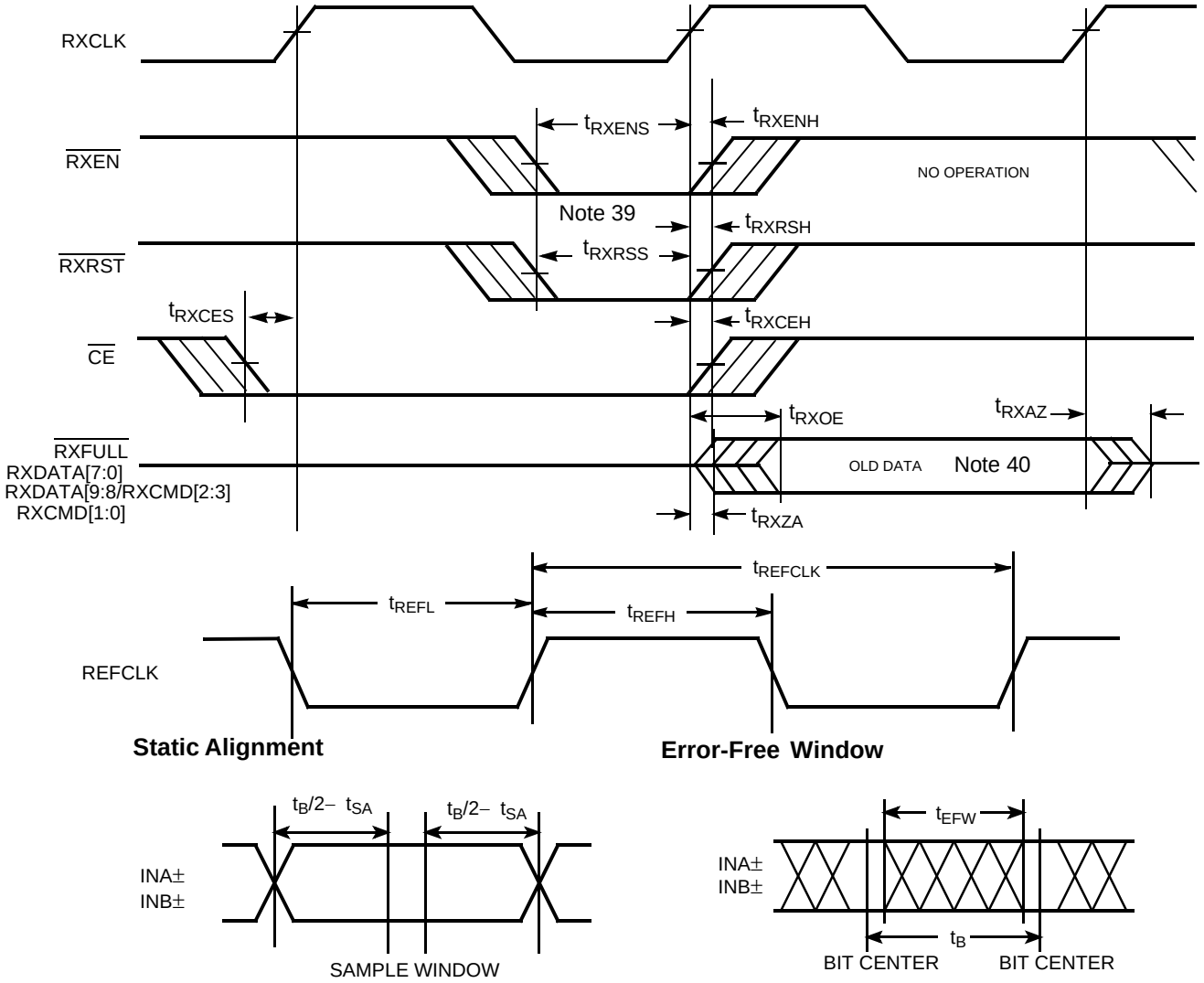


Table 7. HOTLink TAXI-compatible Encoder Patterns

4B/5B Encoder			5B/6B Encoder		
HEX Data	4-bit Binary Data[41]	5-bit Encoded Symbol[42, 43]	HEX Data	5-bit Binary Data[41]	6-bit Encoded Symbol[42, 43]
0	0000	11110	00	00000	110110
1	0001	01001	01	00001	010001

Notes

39. Binary Input Data is the parallel input data which is input to the Transmitter and output from the Receiver. Binary bits are listed from left to right in the following order: 8-Bit mode (BYTE8/10 is HIGH and TXSC/D or RXSC/D is LOW)—TXDATA/RXDATA[7], [6], [5], [4], and TXDATA/RXDATA[3], [2], [1], [0]; 10-Bit mode (BYTE8/10 is LOW and TXSC/D or RXSC/D is LOW)—TXDATA/RXDATA[8], [7], [6], [5], [4], and TXDATA/RXDATA[9], [3], [2], [1], [0].
40. The ENCODED Symbols are shown here as “ones and zeros”, but are converted to and from an NRZI stream at the transmitter output and receiver input. NRZI represents a “one” as a state transition (either LOW-to-HIGH or HIGH-to-LOW) and a “zero” as no transition within the bit interval.
41. Encoded Serial Symbol bits are shifted out with the most significant bit (Left-most) of the most significant nibble coming out first.
42. Binary CMD is the parallel input data which is input to the Transmitter and output from the Receiver. Binary bits are listed from left to right in the following order: 8-Bit mode (BYTE8/10 is HIGH and TXSC/D or RXSC/D is HIGH)—TXCMD/RXCMD[3], [2], [1], [0]; 10-Bit mode (BYTE8/10 is LOW and TXSC/D or RXSC/D is HIGH)—TXCMD/RXCMD[1], [0].
43. While these Commands are legal data and will not disrupt normal operation if used occasionally, they may cause data errors if grouped into recurrent fields. Normal PLL operation cannot be guaranteed if one or more of these commands is continuously repeated.

Table 7. HOTLink TAXI-compatible Encoder Patterns (continued)

4B/5B Encoder			5B/6B Encoder		
HEX Data	4-bit Binary Data[41]	5-bit Encoded Symbol[42, 43]	HEX Data	5-bit Binary Data[41]	6-bit Encoded Symbol[42, 43]
2	0010	10100	02	00010	100100
3	0011	10101	03	00011	100101
4	0100	01010	04	00100	010010
5	0101	01011	05	00101	010011
6	0110	01110	06	00110	010110
7	0111	01111	07	00111	010111
8	1000	10010	08	01000	100010
9	1001	10011	09	01001	110001
A	1010	10110	0A	01010	110111
B	1011	10111	0B	01011	100111
C	1100	11010	0C	01100	110010
D	1101	11011	0D	01101	110011
E	1110	11100	0E	01110	110100
F	1111	11101	0F	01111	110101
–	–	–	10	10000	111110
–	–	–	11	10001	011001
–	–	–	12	10010	101001
–	–	–	13	10011	101101
–	–	–	14	10100	011010
–	–	–	15	10101	011011
–	–	–	16	10110	011110
–	–	–	17	10111	011111
–	–	–	18	10001	101010
–	–	–	19	11001	101011
–	–	–	1A	11010	101110
–	–	–	1B	11011	101111
–	–	–	1C	11100	111010
–	–	–	1D	11101	111011
–	–	–	1E	11110	111100
–	–	–	1F	11111	111101

Table 8. HOTLink TAXI Compatible Command Symbols

CY7C9689A (Transmitter)				CY7C9689A (Receiver)	
Command Input TXCMD[3:0]				Command Output RXCMD[3:0]	
HEX	Binary CMD[44]	Encoded Symbol[42, 43]	Mnemonic	HEX	Binary CMD[44]
8-bit mode (BYTE8/10 is HIGH)					
0	0000	11000 10001	JK (8-bit SYNC)	0	0000

Note
44. Signals labeled in italics are internal to the CY7C9689A.

Table 8. HOTLink TAXI Compatible Command Symbols (continued)

CY7C9689A (Transmitter)				CY7C9689A (Receiver)	
Command Input TXCMD[3:0]				Command Output RXCMD[3:0]	
1	0001	11111 11111	II	1	0001
2	0010	01101 01101	TT	2	0010
3	0011	01101 11001	TS	3	0011
4	0100	11111 00100	IH	4	0100
5	0101	01101 00111	TR	5	0101
6	0110	11001 00111	SR	6	0110
7	0111	11001 11001	SS	7	0111
8[45]	1000	00100 00100	HH	8	1000
9[45]	1001	00100 11111	HI	9	1001
A[45]	1010	00100 00000	HQ	A	1010
B	1011	00111 00111	RR	B	1011
C	1100	00111 11001	RS	C	1100
D[45]	1101	00000 00100	QH	D	1101
E[45]	1110	00000 11111	QI	E	1110
F[45]	1111	00000 00000	QQ	F	1111
10-bit mode (BYTE8/10 is LOW)					
0	00	011000 100011	LM (10-bit SYNC)	0	00
1	01	111111 111111	I'I'	1	01
2	10	011101 011101	T'T'	2	10
3	11	011101 111001	T'S'	3	11

Functional Description

The interconnection of two or more CY7C9689A Transceivers forms a general-purpose communications subsystem capable of transporting user data at up to 20 MBytes per second over several types of serial interface media. The CY7C9689A is highly configurable with multiple modes of operation.

In the transmit section of the CY7C9689A, data moves from the input register, through the Transmit FIFO, to the 4B/5B Encoder. The encoded data is then shifted serially out the OUTx± differential PECL compatible drivers. The bit-rate clock is generated internally from a 2.5x, 5x, or 10x PLL clock multiplier. A more complete description is found in the section *CY7C9689A HOTLink Transmit-Path Operating Mode Description*.

In the receive section of the CY7C9689A, serial data is sampled by the receiver on one of the INx± differential line receiver inputs. The receiver clock and data recovery PLL locks onto the selected serial bit stream and generates an internal bit-rate sample clock. The bit stream is deserialized, decoded, and presented to the Receive FIFO, along with a character clock. The data in the FIFO can then be read either slower or faster than the incoming character rate. A more complete description is found in the section *CY7C9689A HOTLink Receive-Path Operating Mode Description*.

The Transmitter and Receiver parallel interface timing and functionality can be configured to Cascade directly to external FIFOs for depth expansion, couple directly to registers, or couple directly to state machines. These interfaces can accept or output either:

- 8-bit characters
- 10-bit characters
- 10-bit pre-encoded characters (pre-scrambled or pre-encoded)
- 12-bit pre-encoded characters (pre-scrambled or pre-encoded).

The bit numbering and content of the parallel transmit interface is shown in Table 1. When operated with the 4B/5B, 5B/6B Encoder bypassed, the TXSC/$\overline{D}$ and RXSC/$\overline{D}$ bits are ignored.

The HOTLink Transceiver serial interface provides a seamless interface to various types of media. A minimal number of external passive components are required to properly terminate transmission lines and provide LVPECL loads. For power supply decoupling, a single capacitor (in the range of 0.02 μF to 0.1 μF) is required per power/ground pair. Additional information on interfacing these components to various media can be found in the *HOTLink Design Considerations* application note.

Note
45. Signals shown as dotted lines represent the differences in timing and active state of signals when operated in Cascade Timing.

CY7C9689A TAXI HOTLink Transmit-Path Operating Mode Descriptions

The TAXI HOTLink Transmitter can be configured into several operating modes, each providing different capabilities and fitting different transmission needs. These modes are selected using the FIFOBYP, ENCBYP and BYTE8/10 inputs on the CY7C9689A Transceiver. These modes can be reduced to five primary classes:

- Synchronous Encoded
- Synchronous Pre-encoded
- Asynchronous Encoded
- Asynchronous Pre-encoded.

Synchronous Encoded

In this mode, the Transmit FIFO is bypassed, while the 4B/5B, 5B/6B encoder is enabled. One character is accepted at the Transmit Input Register at the rising edge of REFCLK, and passed to the Encoder where it is encoded for serial transmission. The Serializer operates synchronous to REFCLK, which is multiplied by 10 or 5 to generate the serial data bit-clock. In this mode the TXRST and TXHALT inputs are not interpreted and may be tied either HIGH or LOW. To place the CY7C9689A into synchronous modes, FIFOBYP must be LOW.

This mode is usually used for products that must meet specific predefined protocol requirements, and cannot tolerate the uncontrolled insertion of SYNC fill characters. The host system is required to provide new data at every rising edge of REFCLK (along with TXEN) to maintain the data stream. If TXEN is not asserted, the Encoder is loaded with JK or LM sync characters.

Input Register Mapping

In Encoded modes, the bits of the TXDATA input bus are mapped into characters (as shown in Table 1), including a TXSV bit, eight bits of data, and a TXSC/D bit to select either Special Character codes or Data characters.

The TXSC/D bit controls the encoding of the TXDATA[7:0] or TXDATA[9:0] bits of each character. It is used to identify if the input character represents a Data Character or a Special Character code. If TXSC/D is LOW, the character appeared on the TXDATA bus is encoded using the Data Character codes listed in Table 7. If TXSC/D is HIGH, the character on the TXCMD bus is encoded using the Special Character codes listed in Table 8.

Synchronous Pre-encoded

In synchronous pre-encoded mode, both the Transmit FIFO and the 4B/5B encoder are bypassed, and data passes directly from the Transmit Input Register to the Serializer. The Serializer operates synchronous to REFCLK, which is multiplied by 10 or 5 when BYTE8/10 is HIGH (as selected by the SPDSEL and RANGESEL inputs) to generate the serial data bit-clock. In this mode, part of the TXCMD bus inputs are used as part of the data input bus. To place the CY7C9689A into synchronous modes, FIFOBYP must be LOW.

This mode is usually used for products containing external encoders or scramblers, that must meet specific protocol requirements. The host system is required to provide new data at every rising edge of the REFCLK (along with TXEN) to maintain the data stream. If TXEN is not asserted, the Serializer is loaded with JK or LM sync characters.

In this mode the LSB of each input character (TXDATA[0]) is shifted out first, followed sequentially by TXDATA[1] through TXDATA[9] (TXDATA[11] when BYTE8/10 is LOW).

Asynchronous Encoded

In Asynchronous Encoded mode, both the Transmit FIFO and the Encoder are enabled. This provides 256 characters of data buffering. The Serializer operates synchronous to REFCLK, which is multiplied by 2.5, 5, or 10 to generate the serial data bit-clock (as selected by SPDSEL and RANGESEL). In this mode the TXRST and TXHALT inputs are interpreted.

This mode supports the same Input Register mapping as Synchronous Encoded mode. Because both the Transmit FIFO and Encoder are enabled, the input FIFO may be loaded at any rate supported by the FIFO (up to 50 MHz), without generating any decoder errors at the receive end of the link.

CY7C9689A TAXI HOTLink Receive-Path Operating Mode Descriptions

The HOTLink Receiver can be configured into several operating modes, each providing different capabilities and fitting different reception needs. These modes are selected using the FIFOBYP, ENCBYP, BYTE8/10 inputs on the CY7C9689A Transceiver. These modes can be reduced to four primary classes:

- Synchronous Decoded
- Synchronous Undecoded
- Asynchronous Decoded
- Asynchronous Undecoded.

In all these modes, serial data is received at one of the differential line receiver inputs and routed to the Deserializer and Framer. The PLL in the clock and data recovery block is used to extract a bit-rate clock from the transitions in the data stream, and uses that clock to capture bits from the serial stream. These bits are passed to the Deserializer where they are formed into 10- or 12-bit characters.

To align the incoming bit stream to the proper character boundaries, the Framer must be enabled by asserting RFEN HIGH. The Framer logic-block checks the incoming bit stream for the unique pattern that defines the character boundaries. This logic filter looks for the JK or LM (when BYTE8/10 is LOW) sync character. Once a sync character is found, the Framer captures the offset of the data stream from the present character boundaries, and resets the boundary to reflect this new offset, thus framing the data to the correct character boundaries.

Since noise induced errors can cause the incoming data to be corrupted, and since many combinations of corrupt and legal data can create an aliased sync character, the framer may also be disabled by deasserting RFEN LOW.

Synchronous Decoded

In these modes, the Receive FIFO is bypassed, while the 5B/4B, 6B/5B Decoder is enabled. Framed characters output from the Deserializer are decoded, and passed directly to the Receive Output Register. The Deserializer operates synchronous to the recovered bit-clock, which is divided by 10, generate the output

RXCLK clock. In this mode the RXRST input is not interpreted and may be biased either HIGH or LOW.

These modes are usually used for products that must meet specific protocol requirements. New decoded characters are provided at the RXDATA outputs once every rising edge of RXCLK. If RXEMPTY is asserted LOW, the characters on the RXCMD output register is a JK or LM sync character, and the discard policy is set to non-0. Because the decoder is now enabled, all received characters are checked for compliance to the 4B/5B decoding rules.

Output Register Mapping

The RXDATA[11:0] output bus is mapped into a character consisting of eight bits of data and four bits of command, or ten bits of data and two bits of command. An accompanying RXSC/D bit identifies the character as either command or data.

The Violation (VLTN) output indicates a code violation has occurred. When the VLTN output is asserted HIGH, this indicates a transmission error is detected in the character at the current transfer clock cycle.

Synchronous Undecoded

In this mode, both the Receive FIFO and the 5B/4B, 6B/5B Decoder are bypassed, and data passes directly from the Deserializer to the output register. The Deserializer operates synchronous to the recovered bit-clock, which is divided by 10 to generate the output RXCLK clock. In this mode the RXRST input is not interpreted and may be biased either HIGH or LOW.

This mode is usually used for products containing external decoders or descramblers that must meet specific protocol requirements. New data is provided at the RXDATA outputs once every rising edge of RXCLK. Received characters are not checked for any specific coding requirements and no decoding errors are reported.

Asynchronous Decoded

In Asynchronous Decoded mode, both the Receive FIFO and the Decoder of the CY7C9689A are enabled. The deserializer operates synchronous to the recovered bit-clock, which is divided by 10 to generate the Receive FIFO write clock. Characters are read from the Receive FIFO, using the external RXCLK input, when addressed by CE and selected by RXEN. In this mode the RXRST input is interpreted.

Asynchronous Decoded mode supports the same Output Register mapping as the Synchronous Decoded mode. Because both the Receive FIFO and Decoder are enabled, the output FIFO may be read at any rate supported by the FIFO, however, if the Receive FIFO ever indicates a full condition (RXFULL is asserted), data may be lost.

Asynchronous Undecoded

In Asynchronous Undecoded modes, the Receive FIFO is enabled. This means that all characters received from the serial interface are written to the Receive FIFO before being passed to the output register. The Deserializer operates synchronous to the recovered bit-clock, which is divided by 10 (or 12) to generate the Receive FIFO write clock. Data is read from the Receive FIFO, using the RXCLK input clock, when addressed by CE and selected by RXEN.

These modes are usually used for products containing external decoders or descramblers, that must meet specific protocol requirements. New data may be read from the Receive FIFO any time that the FIFO status flags indicate a non-empty condition (RXEMPTY is deasserted). To ensure that data is not lost, the Receive FIFO must be read faster than data is loaded into the Receive FIFO.

If the receiver is to provide framed characters, it is necessary for the transmit end to include JK or LM sync characters in the data stream. This can be done by:

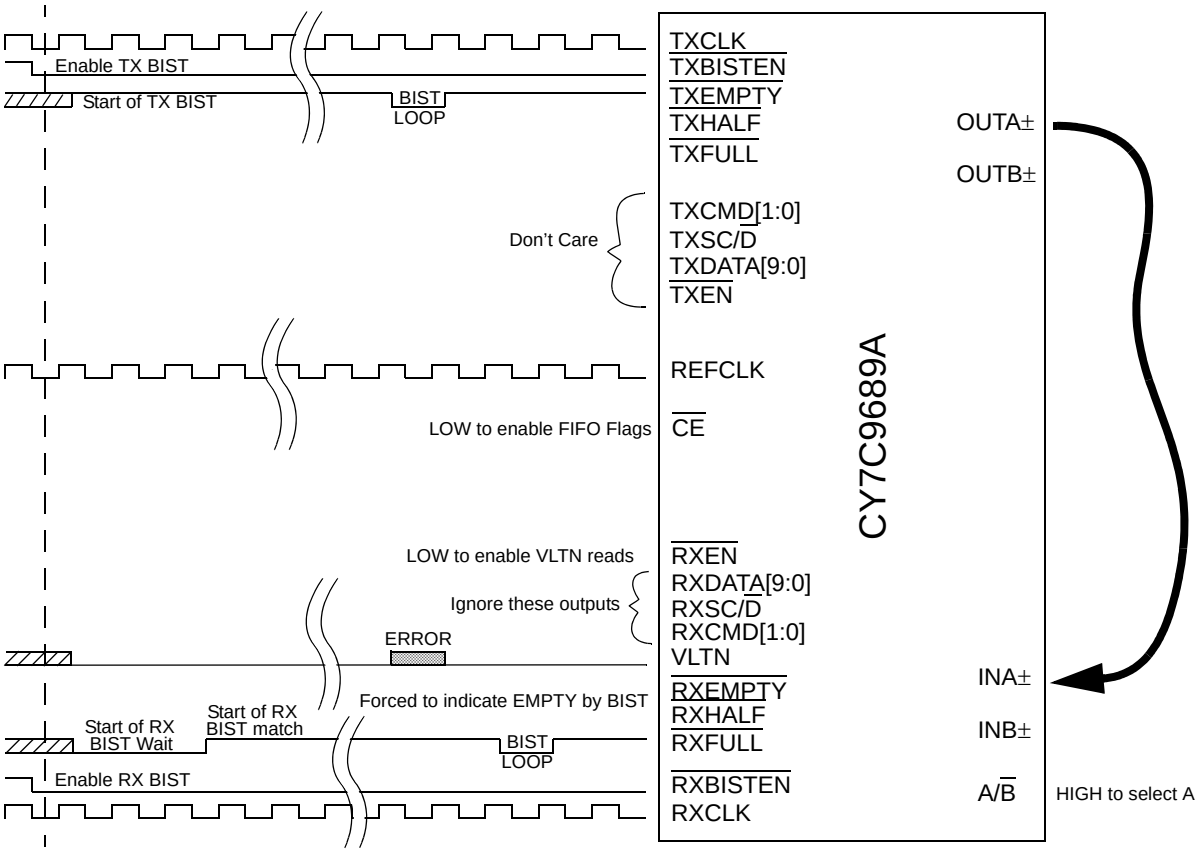
- operating the transmitter in encoded mode and writing JK or LM characters into the data stream
- operating the transmitter in pre-encoded mode and writing the 10-bit value for an encoded JK (1100010001) or LM (011000100011) character to the data stream
- not enabling the transmitter when it is operated in synchronous mode, or by allowing the transit FIFO to go empty when it is operated in asynchronous mode.

BIST Operation and Reporting

The CY7C9689ADX HOTLink Transceiver incorporates the same Built-In Self-Test (BIST) capability. This link diagnostic uses a Linear Feedback Shift Register (LFSR) to generate a 511-character repeating sequence that is compared, character-for-character, at the receiver.

BIST mode is intended to check the entire high-speed serial link at full link-speed, without the use of specialized and expensive test equipment. The complete sequence of characters used in BIST are documented in Table 4.

Figure 5. Built-In Self-Test Illustration



BIST Enable Inputs

There are separate BIST enable inputs for the transmit and receive paths of the CY7C9689A. These inputs are both active LOW; i.e., BIST is enabled in its respective section of the device when the BIST enable input is determined to be at a logic-0 level. Both BIST enable inputs are asynchronous; i.e., they are synchronized inside the CY7C9689A to the internal state machines.

BIST Transmit Path

The transmit path operation with BIST is controlled by the TXBISTEN input and overrides most other inputs (see Figure 5). When the Transmit FIFO is enabled (not bypassed) and TXBISTEN is recognized internally, all reads from the Transmit FIFO are suspended and the BIST generator is enabled to sequence out the 511 character repeating BIST sequence. If the recognition occurs in the middle of a data field, the following data is not transmitted at that time, but remains in the Transmit FIFO. Once the TXBISTEN signal is removed, the data in the Transmit FIFO is again available for transmission. To ensure proper data handling at the destination, the transmit host controller should either use TXHALT to prevent transmission of data at specific boundaries, or allow the Transmit FIFO to completely empty before enabling BIST.

With transmit BIST enabled, the Transmit FIFO remains available for loading of data. It may be written up to its normal maximum limit while the BIST operation takes place. To allow removal of stale data from the Transmit FIFO, it may also be reset during a BIST operation. The reset operation proceeds as documented, with the exception of the information presented on the TXEMPTY FIFO status flag. Since this flag is used to present BIST loop status, it continues to reflect the state of the transmit BIST loop status until TXBISTEN is no longer recognized internally. The completion of the reset operation may still be monitored through the TXFULL FIFO status flag.

The TXEMPTY flag, when used for transmit BIST progress indication, continues to reflect the active HIGH or active LOW settings determined by the UTOPIA or Cascade timing model selected by EXTFIFO; i.e., when configured for the Cascade timing model, the TXEMPTY and TXFULL FIFO flags are active HIGH, when configured for the UTOPIA timing model the TXEMPTY and TXFULL FIFO flags are active LOW. The illustration in *Figure 5* uses the UTOPIA conventions.

When TXBISTEN is first recognized, the TXEMPTY flag is clocked to a reset state, regardless of the addressed state of the Transmit FIFO (if CE is LOW or not), but is not driven out of the part unless CE has been sampled asserted (LOW). Following this, on each completed pass through the BIST loop, the TXEMPTY flag is set for one interface clock period (TXCLK or REFCLK).

The TXEMPTY flag remains set until the interface is addressed and the state of TXEMPTY has been observed. If the device is

not addressed ($\overline{CE}$ is not sampled LOW), the flag remains set internally regardless of the number of TXCLK clock cycles that are processed. If the device status is not polled on a sufficiently regular basis, it is possible for the host system to miss one or more of these BIST loop indications.

A pass through the loop is defined as that condition where the Encoder generates the 0x00 (where 0x denotes Hex number, e.g. 0x00 denotes HEX00) state. Depending on the initial state of the BIST LFSR, the first pass through the loop may occur at substantially less than 511 character periods. Following the first pass, as long as $\overline{TXBISTEN}$ remains LOW, all remaining passes are exactly 511 characters in length.

When the Transmit FIFO is bypassed, the interface is clocked by the REFCLK signal instead of TXCLK. While the active or asserted state of the $\overline{TXEMPTY}$ signal is still controlled by the EXTFIFO, the state of any completed BIST loops is no longer preserved. Instead, the $\overline{TXEMPTY}$ flag reflects the dynamic state of the BIST loop progress, and is asserted only once every 511 character periods. If the interface is not addressed at the time that this occurs, then the FIFO status flags remain in a high-Z state and the loop event is lost.

BIST Receive Path

The receive path operation in BIST is similar to that of the transmit path. While the Receive FIFO is enabled (not bypassed) and RXBISTEN is recognized internally, all writes to the Receive FIFO are suspended.

Any data present in the Receive FIFO when $\overline{RXBISTEN}$ is recognized remains in the FIFO and cannot be read until the BIST operation is complete. The data in the Receive FIFO remains valid, but is NOT available for reading through the host parallel interface. This is because the error output indicator for receive BIST operations is the VLTN signal, which is normally part of the RXDATA bus. To prevent read operations while BIST is in operation, the RXEMPTY and RXHALF flags are forced to indicate an Empty condition. Once $\overline{RXBISTEN}$ has been removed and recognized internally, the Receive FIFO status flags are updated to reflect the current content status of the Receive FIFO.

To allow removal of stale data from the Receive FIFO, it may be reset during a BIST operation. The reset operation proceeds as documented, with the exception that the RXEMPTY and RXHALF status flags already indicate an empty condition. The $\overline{RXFULL}$ flag is used to present BIST progress. The active (asserted) state on $\overline{RXFULL}$ (and $\overline{RXEMPTY}$) remain controlled by the present operating mode and interface timing model (UTOPIA or Cascade).

When $\overline{RXBISTEN}$ has been recognized, $\overline{RXFULL}$ becomes the receive BIST loop indicator (regardless of the logic state of FIFOBYP). When $\overline{RXBISTEN}$ is first recognized, the $\overline{RXFULL}$ flag is clocked to a set state, regardless of the addressed state of the Receive FIFO (if $\overline{CE}$ is sampled LOW or not). Following this, $\overline{RXFULL}$ remains set until the receiver detects the start of the BIST pattern. Then $\overline{RXFULL}$ is deasserted for the duration of the BIST pattern, pulsing asserted for one RXCLK period on the last symbol of each BIST loop. If 14 of 28 consecutive characters are received in error, $\overline{RXFULL}$ returns to the set state until the start of a BIST sequence is again detected.

Just like the BIST status flag on the transmit data path, the $\overline{RXFULL}$ flag captures the asserted states, and keeps them until they are read. This means that if the status flag is not read on a regular basis, events may be lost.

The detection of errors is presented on the VLTN output. Unlike the $\overline{RXFULL}$ FIFO status flag, the active state of this output is not controlled by the EXTFIFO input. With the Receive FIFO enabled, these outputs should operate the same as the $\overline{RXFULL}$ flag, with respect to preserving the detection state of an error until it is read.

Unlike the $\overline{RXFULL}$ flag, which only needs the CY7C9689A to be addressed ($\overline{CE}$ sampled LOW by RXCLK) to enable the $\overline{RXFULL}$ three-state driver, and an RXCLK to "read" the flag, the VLTN output requires a selection (assertion of $\overline{RXEN}$ while addressed) to enable the RXDATA bus three-state drivers. The selection process is necessary to ensure that a multi-PHY implementation does not enable multiple VLTN drivers at the same time.

When the Receive FIFO is bypassed, the interface is clocked by the RXCLK output signal. While the active or asserted state of the $\overline{RXFULL}$ signal is still controlled by the EXTFIFO input, the state of any completed BIST loops or detected errors are no longer preserved. Instead, the $\overline{RXFULL}$ flag reflects the dynamic state of the BIST loop progress, and is asserted only once every 511 character periods. If the interface is not addressed at the time that this occurs, then the FIFO status flags remain in a high-Z state and the loop event is lost. This is also true of the VLTN output, such that if the CY7C9689A receive path is not selected to enable the RXDATA bus three-state drivers, the detection of a BIST miscompare is lost.

BIST Three-state Control

When BIST is enabled on either the transmitter or the receiver, the three-state enable signals for the BIST status flags and error indicators work the same as for normal data processing. The output drivers for the BIST status that is presented on FIFO status flags are only enabled when $\overline{CE}$ has been sampled asserted (LOW) by the respective clock (TXCLK, RXCLK, or REFCLK).

To access the BIST error information, it is necessary to perform a read cycle of the addressed receiver. This means that $\overline{CE}$ must be LOW to enable the receiver (Rx_Match), and $\overline{RXEN}$ must be asserted from HIGH to LOW to select the device. Because the part is in BIST, no data is read from the FIFO, but the data bus is driven. This allows the VLTN indicator to be driven onto the RXDATA bus. So long as $\overline{RXEN}$ remains asserted, the receiver stays selected, the data bus remains driven, and VLTN has meaning.

Bus Interfacing

The parallel transmit and receive host interfaces to the CY7C9689A are configurable for either synchronous or asynchronous operation. Each of these configurations supports two selectable timing and control models of Shared Bus or Cascade.

All asynchronous bus configurations have the internal Transmit and Receive FIFOs enabled. This allows data to be written or read from these FIFOs at any rate up to the maximum 50-MHz clock rate of the FIFOs. All internal operations of the CY7C9689A do not use the external TXCLK or RXCLK, but

instead make use of synthesized derivatives of REFCLK for transmit path operations and a recovered character clock for receive path operations.

All synchronous bus configurations require the bus interface operations to be synchronous to REFCLK on the transmit path and the recovered clock (output as RXCLK) on the receive path. The internal FIFOs are bypassed in all synchronous modes.

The two supported timing and control models are Shared Bus and Cascade. The Shared Bus is based on the timing model of a FIFO with active LOW FIFO status flags and read/write enables.

The Cascade timing model is a modification of the Shared Bus model that changes the flags and FIFO read/write enables to active HIGH. This model is present primarily to allow depth expansion of the internal FIFO by direct coupling to external CY7C42x5 synchronous FIFOs. To allow this direct coupling, the cycle-to-cycle timing between the transmit and receive enables (TXEN and RXEN) are also modified to ensure correct data transfer.

These four configurations of bus operation and timing/control can all be used with or without external FIFOs. Depending on the specific mode selected, the amount of external hardware necessary to properly couple the CY7C9689A to state machines or external FIFOs is minimal in all cases, and may be zero if the proper configuration is selected.

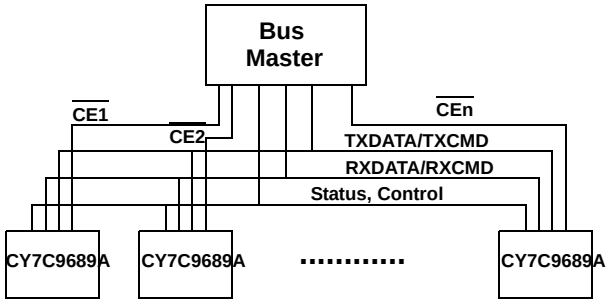
With only minor exceptions, all configurations of the CY7C9689A in the Shared Bus mode borrowed concepts from the ATM Forum's UTOPIA Bus operation. concepts of addressing and selection to control the enabled/disabled state of the output drivers, and when data can be written to or read from the part.

Shared Bus Interface Concept

The CY7C9689A Parallel Interface is designed for interfacing to a Shared Bus. The maximum TXCLK and RXCLK frequency is 50 MHz, which provides a total bandwidth of 50Million characters per second in each direction. More than two CY7C9689A can be serviced on the same bus at full serial line speed.

The CY7C9689A is designed to be the Slave in Master-Slave type of shared bus architecture. Generally, the bus Master (a Medium Access Device, MAC) is a higher layer device that sources out going data/command and sinks incoming data/command to/from Slaves (CY7C9689A) on the shared bus (see Figure 6)

Figure 6. Shared Bus Architecture



The data bus (TXDATA, RXDATA), command bus (TXCMD, RXCMD) and FIFO status flags (TXFULL, RXEMPTY, etc.) of each CY7C9689A on the shared bus can be connected together respectively. Each Slave can be assigned an address. The address of each Slave can be decoded by a decoder which drives the CE input of each Slave. The bus Master will poll each Slave by selecting (or "Addressing") the device, and sample the FIFO flags. Depending on the FIFOs status on each Slave device, the Master can schedule read accesses to Slaves which have data in the RXFIFOs, and write accesses to Slaves which have room in the TXFIFOs. While data is being transferred on the data/command bus, the bus Master can continue to poll each Slave device independently.

Device Selection

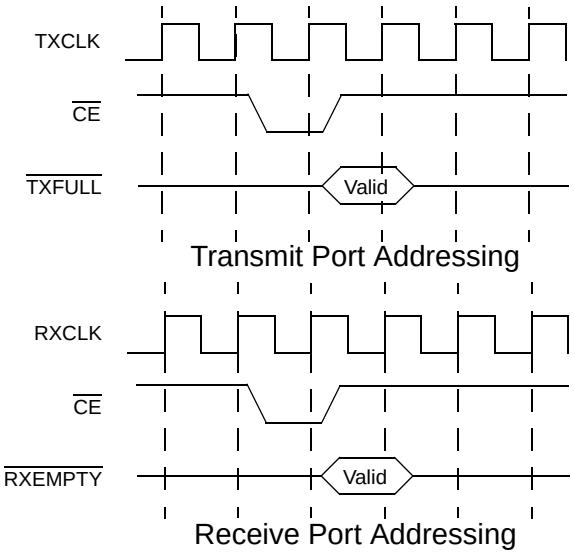
All actions on the Shared Bus interface are controlled by the Chip Enable and selection states of the interface. These states control the read and write access to the Receive and Transmit FIFOs, access to the FIFO status flags, reset of the Transmit and Receive FIFOs, and read and write access to the Serial Address Register. The CY7C9689A supports the concept of an "address match" through a single Chip Enable (CE) input.

Address Match and FIFO Flag Access

The CY7C9689A makes use of a single active-LOW Chip Enable (CE) to generate address-match conditions. This allows multiple CY7C9689A devices to share a common bus, with device output three-state controls being managed by either an address match condition (CE sampled LOW), or by a selection state.

The Transmit and Receive FIFO flag output drivers are enabled in any TXCLK, REFCLK, or RXCLK cycle following CE being sampled asserted (LOW) by the rising edge of the respective clock. The CE input is sampled separately by the clocks for the transmit and receive interfaces, which allows these clocks to be both asynchronous to each other, and to operate at different clock rates. An example of both Transmit and Receive FIFO flag access is shown in Figure 7

Figure 7. FIFO Flag Driver Enables.



When the Transmit FIFO is enabled ($\overline{\text{FIFOBYP}}$ is HIGH) and $\overline{\text{CE}}$ is sampled LOW by the rising edge of TXCLK, the output drivers for the TXFULL and TXEMPTY FIFO flags are enabled. When $\overline{\text{CE}}$ is sampled HIGH by the rising edge of TXCLK, these same output drivers are disabled.

When the Transmit FIFO is bypassed ($\overline{\text{FIFOBYP}}$ is LOW and not in byte-packed mode) and $\overline{\text{CE}}$ is sampled LOW by the rising edge of REFCLK, the output drivers for the TXFULL and TXEMPTY FIFO flags are enabled. When $\overline{\text{CE}}$ is sampled HIGH by the rising edge of REFCLK, the FIFO flag output drivers are disabled.

When $\overline{\text{CE}}$ is sampled LOW by the rising edge of RXCLK (input or output), the output drivers for the RXFULL and RXEMPTY FIFO flags are enabled. When $\overline{\text{CE}}$ is sampled HIGH by the rising edge of RXCLK, the FIFO flag output drivers are disabled.

Device Selection

The concept of selection is used to control the access to the transmit and receive parallel-data ports of the device. There are three primary types of selection:

- Transmit data selection (with and without internal Transmit FIFO)
- Receive data selection (with and without internal Receive FIFO)
- Continuous selection (for either or both transmit and receive interfaces).

In addition to these normal selection types, there are two additional sequences that are used to control the internal Transmit and Receive FIFOs reset operations, and to control read/write access to the Serial Address Register:

- Transmit reset sequence
- Receive reset sequence.

Of these operations, the transmit data selection and transmit reset sequence are mutually exclusive and cannot exist at the same time. The receive data selection and receive reset sequence are also mutually exclusive and cannot exist at the same time. Either transmit operation can exist at the same time as either receive operation.

All normal forms of selection require that an Chip Enable must be asserted ($\overline{\text{CE}}$ sampled LOW) either at the same time as the selection control signal being sampled asserted, or one or more clock cycles prior to the selection control signal being sampled asserted.

Transmit Data Selection

Asynchronous With Shared Bus Timing and Control (Transmit FIFO Enabled)

When $\overline{\text{CE}}$ is sampled LOW and $\overline{\text{TXRST}}$ is sampled HIGH by the rising edge of TXCLK, a Tx_Match condition is generated. This Tx_Match condition continues until $\overline{\text{CE}}$ is sampled HIGH or $\overline{\text{TXRST}}$ is sampled LOW at the rising edge of TXCLK. When a Tx_Match (or Tx_RstMatch) condition is present, the $\overline{\text{TXEMPTY}}$ and $\overline{\text{TXFULL}}$ output drivers are enabled. When a Tx_Match (or Tx_RstMatch) condition is not present, these same drivers are disabled (High-Z).

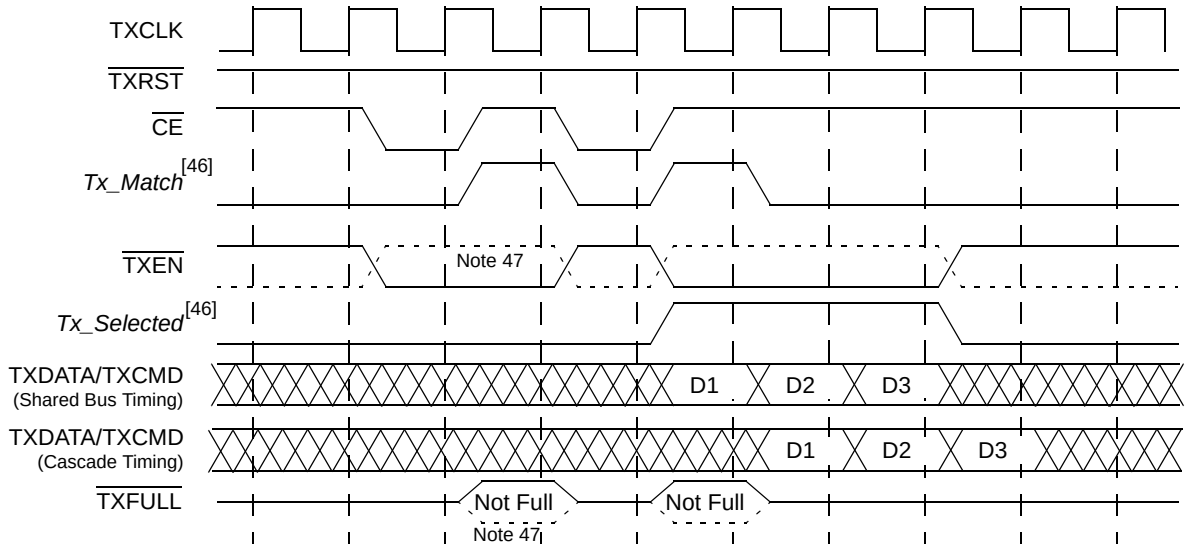
The selection state of the Transmit FIFO is entered when a Tx_Match condition is present, and $\overline{\text{TXEN}}$ transitions from HIGH to LOW. Once selected, the Transmit FIFO remains selected until $\overline{\text{TXEN}}$ is sampled HIGH by the rising edge of TXCLK. In the selected state, data present on the TXDATA inputs is captured and stored in the Transmit FIFO. This transmit interface selection process is shown in Figure 8.

Synchronous With Shared Bus Timing and Control (Transmit FIFO Bypassed)

When the Transmit FIFO is bypassed ($\overline{\text{FIFOBYP}}$ is LOW and not in byte-packed mode), the CY7C9689A must still be selected to write data into the Transmit Input Register.

When $\overline{\text{CE}}$ is sampled LOW and $\overline{\text{TXRST}}$ is sampled HIGH by the rising edge of REFCLK, a Tx_Match condition is generated. This Tx_Match condition continues until $\overline{\text{CE}}$ is sampled HIGH or $\overline{\text{TXRST}}$ is sampled LOW at the rising edge of REFCLK. When a Tx_Match (or Tx_RstMatch) condition is present, the $\overline{\text{TXEMPTY}}$ and $\overline{\text{TXFULL}}$ output drivers are enabled (with the Transmit FIFO bypassed, the status flags normally indicate an Empty condition). When a Tx_Match (or Tx_RstMatch) condition is not present, these same drivers are disabled (High-Z).

Figure 8. Transmit Selection with Transmit FIFO Enabled



The selection state of the Transmit Input Register is entered when a Tx_Match condition is present, and TXEN transitions from HIGH to LOW. Once selected, the transmit input register remains selected until TXEN is sampled HIGH by the rising edge of REFCLK. In the selected state, data present on the TXDATA inputs is captured in the Transmit Input Register and passed to the Serializer or Encoder (as selected by the ENCBYP input). This transmit interface selection process is shown in Figure 9.

When the 4B/5B Encoder is enabled and data is not written to the Transmit Input Register, the data stream is automatically padded with JK or LM SYNC characters. When the 4B/5B, 5B/6B Encoder is disabled and no data is written to the Transmit Input Register, JK or LM SYNC characters are also automatically padded with SYNC characters.

Receive Data Selection

Asynchronous With Shared Bus Timing and Control (Receive FIFO Enabled)

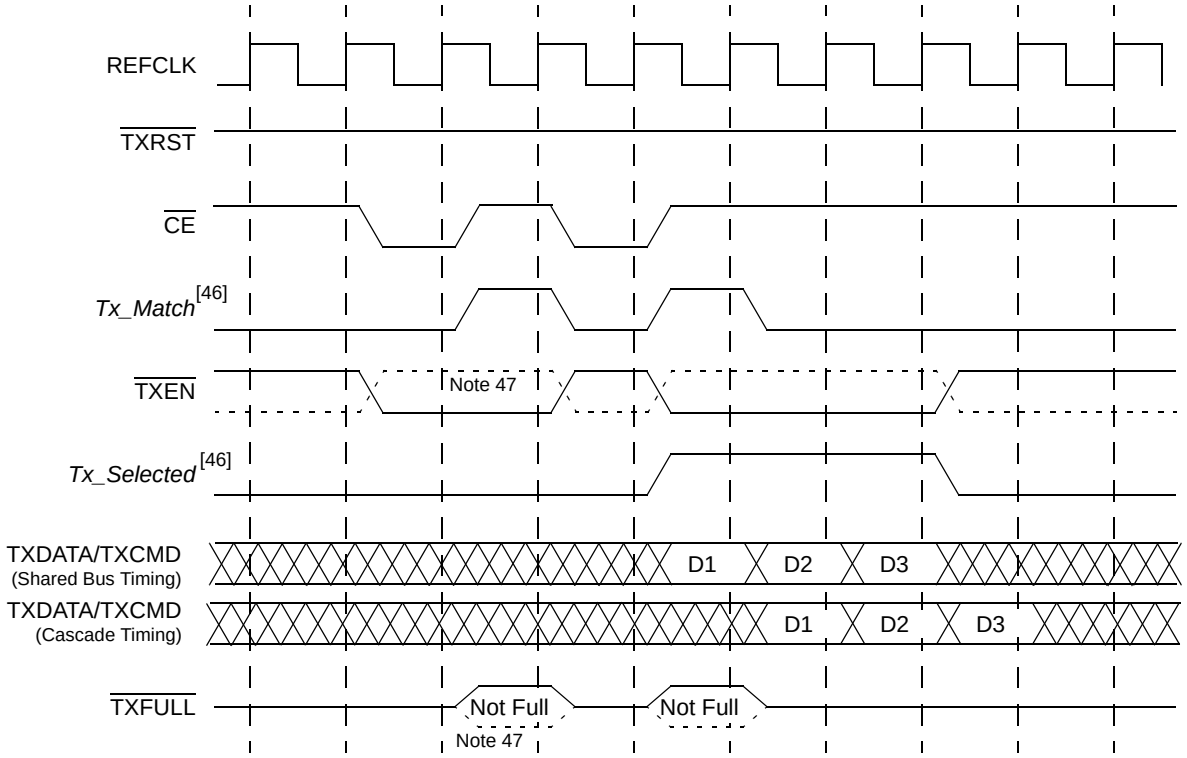
When CE is sampled LOW and RXRST is sampled HIGH by the rising edge of RXCLK input, an Rx_Match condition is generated. This Rx_Match condition continues until CE is sampled HIGH or RXRST is sampled LOW at the rising edge of RXCLK input. When an Rx_Match (or Rx_RstMatch) condition is present, the RXEMPTY and RXFULL output drivers are enabled.

When an Rx_Match (or Rx_RstMatch) condition is not present, these same drivers are disabled (High-Z).

The selection state of the Receive FIFO is entered when an Rx_Match condition is present, and RXEN transitions from HIGH to LOW. Once selected, the Receive FIFO remains selected until RXEN is sampled HIGH by the rising edge of RXCLK input. The selected state initiates a read cycle from the Receive FIFO and enables the Receive FIFO data onto the RXDATA bus. This receive interface selection process is shown in Figure 10

Notes
46. Signal names listed in italics are internal signals, shown for reference only.
47. Signals shown as dotted lines indicate timing and levels when configured for external FIFOs (EXTFIFO is HIGH).

Figure 9. Transmit Selection with Transmit FIFO Bypassed



Synchronous With UTOPIA Timing and Control (Receive FIFO Bypassed)

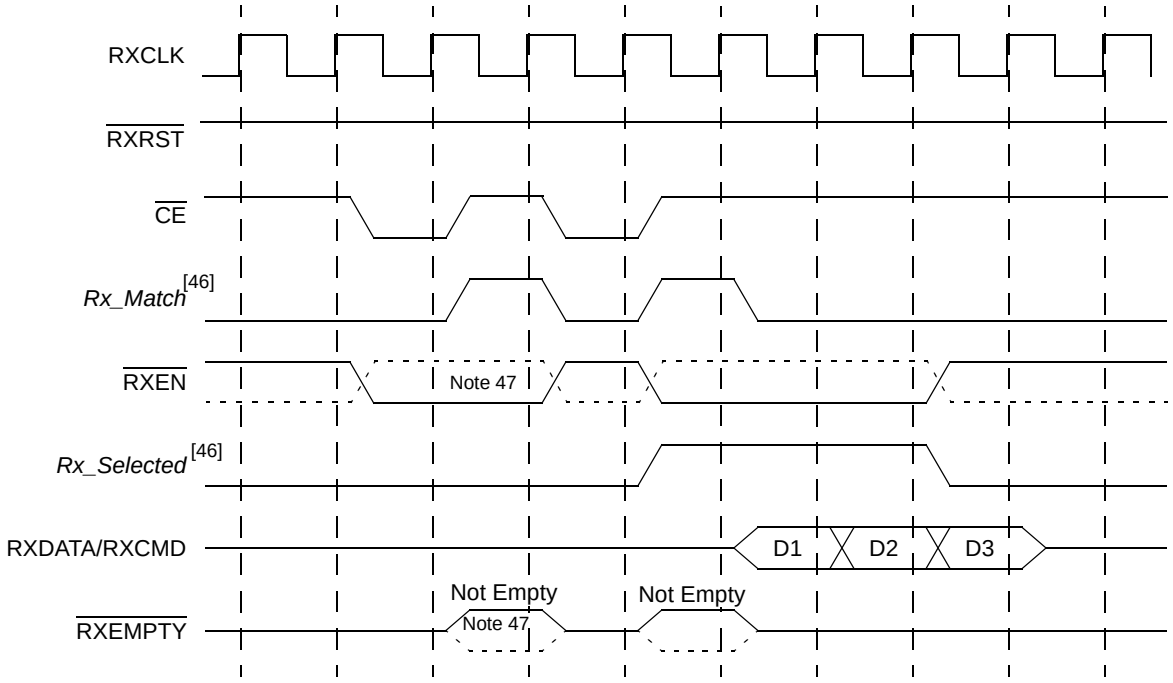
When the Receive FIFO is bypassed ($\overline{\text{FIFOBYP}}$ is LOW), the CY7C9689A must still be selected to enable the output drivers for the RXDATA bus. With the Receive FIFO bypassed, RXCLK becomes a synchronous output clock operating at the character rate.

When $\overline{\text{CE}}$ is sampled LOW and $\overline{\text{RXRST}}$ is sampled HIGH by the rising edge of RXCLK output, an Rx_Match condition is generated. This Rx_Match condition continues until $\overline{\text{CE}}$ is sampled HIGH or $\overline{\text{RXRST}}$ is sampled LOW at the rising edge of RXCLK.

When an Rx_Match (or Rx_RstMatch) condition is present, the $\overline{\text{RXEMPTY}}$ and $\overline{\text{RXFULL}}$ output drivers are enabled. With the Receive FIFO bypassed, these flags normally indicate a non-empty condition but may indicate empty if a JK or LM SYNC character is present in the output register and the receiver discard policy is non-0. When an Rx_Match (or Rx_RstMatch) condition is not present, these same drivers are disabled (High-Z).

The selection state of the Receive Output Register is entered when an Rx_Match condition is present, and $\overline{\text{RXEN}}$ transitions from HIGH to LOW. Once selected, the Receive Output Register remains selected until $\overline{\text{RXEN}}$ is sampled HIGH by the rising edge of RXCLK output. In the selected state, the output drivers for the RXDATA outputs are enabled, and new data is presented to the RXDATA bus on every clock cycle

Figure 10. Receive Selection with Receive FIFO Enabled



Continuous Selection

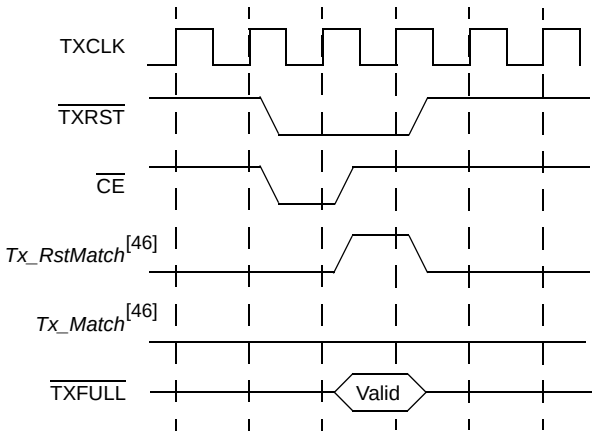
Continuous Selection is a specialized form of selection which does not require sequenced assertion of CE and TXEN or RXEN to select the device for data transfers. In this Continuous Selection mode, the CE and associated TXEN or RXEN enable signal must be asserted when the device is powered up or during assertion of RESET. So long as these signals remain asserted, the device remains selected and data is accepted and presented on every clock cycle. **Note**: The use of continuous selection makes it impossible to reset the respective internal FIFOs, or to access the Serial Address Register.

FIFO Reset Address Match

When CE and TXRST are both LOW, and this condition is sampled by the rising edge of TXCLK, a Tx_RstMatch condition is generated. This Tx_RstMatch condition continues until CE or TXRST is sampled HIGH by the rising edge of TXCLK. When a Tx_RstMatch (or Tx_Match) condition is present, the TXEMPTY and TXFULL output drivers are enabled (just as in a normal Tx_Match condition). When a Tx_RstMatch (or Tx_Match) condition is not present, these same drivers are disabled (High-Z). The Transmit FIFO reset Address Match is shown in Figure 11. Note that although TXRST remains LOW for more than one clock cycle, the Tx_RstMatch does not because the CE signal is no longer asserted (LOW).

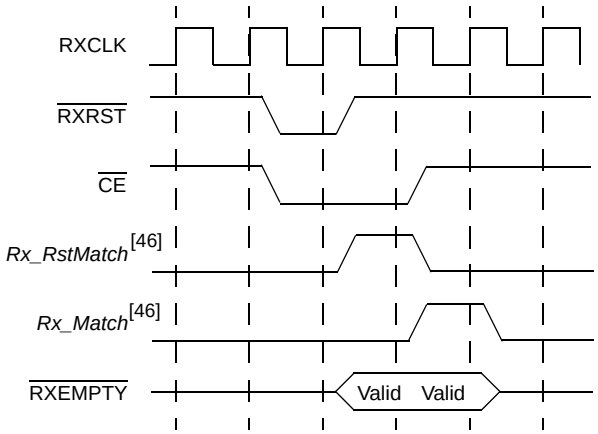
When CE and RXRST are both LOW, and this condition is sampled by the rising edge of RXCLK, an Rx_RstMatch condition is generated. This Rx_RstMatch condition continues until CE or RXRST is sampled HIGH, at the rising edge of

Figure 11. Transmit FIFO Reset Address Match



RXCLK. When an Rx_RstMatch (or Rx_Match) condition is present, the RXEMPTY and RXFULL output drivers are enabled. When an Rx_RstMatch (or Rx_Match) condition is not present, these same drivers are disabled (High-Z). The Receive FIFO reset Address Match is shown in Figure 12. Note that while the FIFO flags remain asserted for more than one clock cycle, this is due to an Rx_Match condition, not a continuation of the Rx_RstMatch.

Figure 12. Receive FIFO Reset Address Match



FIFO Reset Sequence

On power-up, the Transmitter and Receiver FIFOs are cleared automatically. If the usage of the FIFOs in specific operating modes results in stale or unwanted data, this data can be cleared by resetting the respective FIFO. Data in the Transmit FIFO will empty automatically if it is enabled to read the FIFO (assuming TXHALT is not LOW). Stale received data can be “flushed” by reading it, or the Receive FIFO can be reset to remove the unwanted data.

The Transmit and Receive FIFOs are reset when the Tx_RstMatch or Rx_RstMatch condition remains present for eight consecutive clock cycles. Any disruption of the reset sequence prior to reaching the eight cycle count, either by removal of CE or the respective TXRST or RXRST, or assertion of the associated TXEN or RXEN, terminates the sequence and does not reset the FIFO. Because CE must remain asserted during the reset sequence, the addressed FIFO flags remain driven during the entire sequence.

Transmit FIFO Reset Sequence

The Transmit FIFO reset sequence (see Figure 15) is started when TXRST and CE are first sampled LOW by the rising edge of TXCLK. Because a Tx_RstMatch condition is present, the Transmit FIFO flags are asserted and can be used to track the status of any Transmit FIFO reset in progress. Once the reset sequence has reached its maximum count (eight TXCLK cycles), the Transmit FIFO flags are asserted to indicate a FULL condition (TXEMPTY is deasserted, and both TXHALF and TXFULL are asserted). This indicates that the Transmit FIFO reset has been recognized by the Transmit Control State Machine and that a reset has been started. However, if the TXEN is asserted prior to or during the assertion and sampling of TXRST, the reset sequence is inhibited until TXEN is removed. **Note**: The FIFO FULL state forced by the reset operation is different from a FULL state caused by normal FIFO data writes. For normal FIFO write operations, when FULL is first asserted, the Transmit FIFO must still accept up to four additional writes of data. When a FULL state is asserted due to a Transmit FIFO reset operation, the FIFO will not accept any additional data.

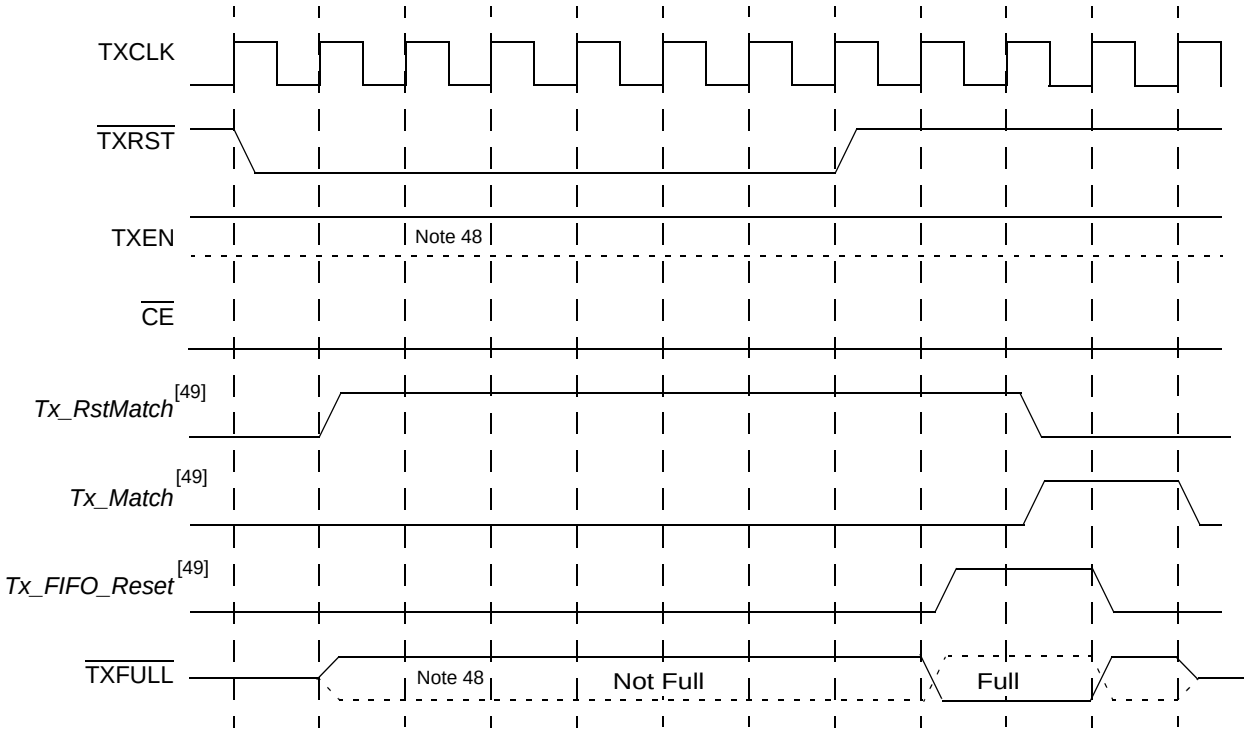
The Transmit FIFO reset does not complete until the external reset condition is removed. This can be removed by deassertion of either TXRST or CE. If CE is deasserted (HIGH) to remove the reset condition, the Transmit FIFO flag’s drivers are disabled, and the Transmit FIFO must be addressed at a later time to validate completion of the Transmit FIFO reset. If TXRST is deasserted (HIGH) to remove the reset condition, the Tx_RstMatch is changed to a Tx_Match, and the Transmit FIFO status flags remain driven. The Transmit FIFO reset operation is complete when the Transmit FIFO flags indicate an EMPTY state (TXEMPTY is asserted and both TXHALF and TXFULL are deasserted). A valid Transmit FIFO reset sequence is shown in Figure 15.

Here the TXRST and CE are asserted (LOW) at the same time. When these signals are both sampled LOW by TXCLK, a Tx_RstMatch condition is present. With TXEN deasserted (HIGH), the Transmit FIFO is not selected for data transfers. This Tx_RstMatch condition must remain for eight TXCLK cycles to initiate the Tx_FIFO_Reset. Following this the TXFULL FIFO status flag is asserted to indicate that the Transmit FIFO reset sequence has completed and that a Transmit FIFO reset is in progress.

When the TXRST signal is deasserted (HIGH), CE remains LOW to allow the FIFO status flags to be driven. This allows the completion of the reset operation to be monitored. To allow better multi-tasking on multi-PHY implementations, it is possible to deassert CE (HIGH) as soon as the FULL state is indicated. The FIFO reset operation will complete and the EMPTY state (indicating completion of the reset operation) can be detected during a separate polling operation.

For those links implemented with a single PHY, it is possible to hardwire CE LOW and still perform normal accesses and reset operations. In a single-PHY implementation, a Transmit FIFO reset can never be initiated with TXEN asserted at the same time as TXRST. Since CE is always LOW, any assertion of TXEN causes the Transmit FIFO to be selected, clearing the reset counter.

Figure 13. Transmit FIFO Reset Sequence with Constant $\overline{CE}$



Notes
48. Signals shown as dotted lines indicate timing and levels when configured for external FIFOs (EXTFIFO is HIGH).
49. Signal names listed in italics are internal signals, shown for reference only.

Figure 14. Invalid Transmit FIFO Reset Sequence with $\overline{\text{TXEN}}$ Asserted

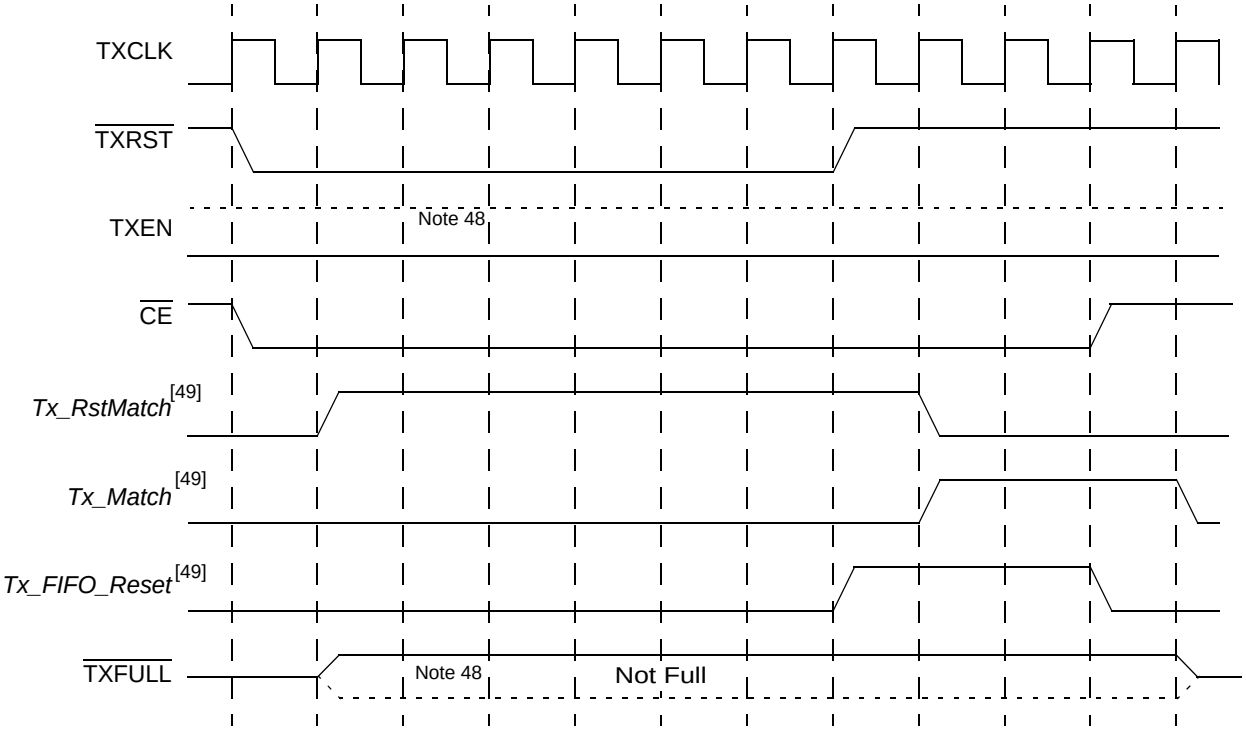


Figure 15. Transmit FIFO Reset Sequence

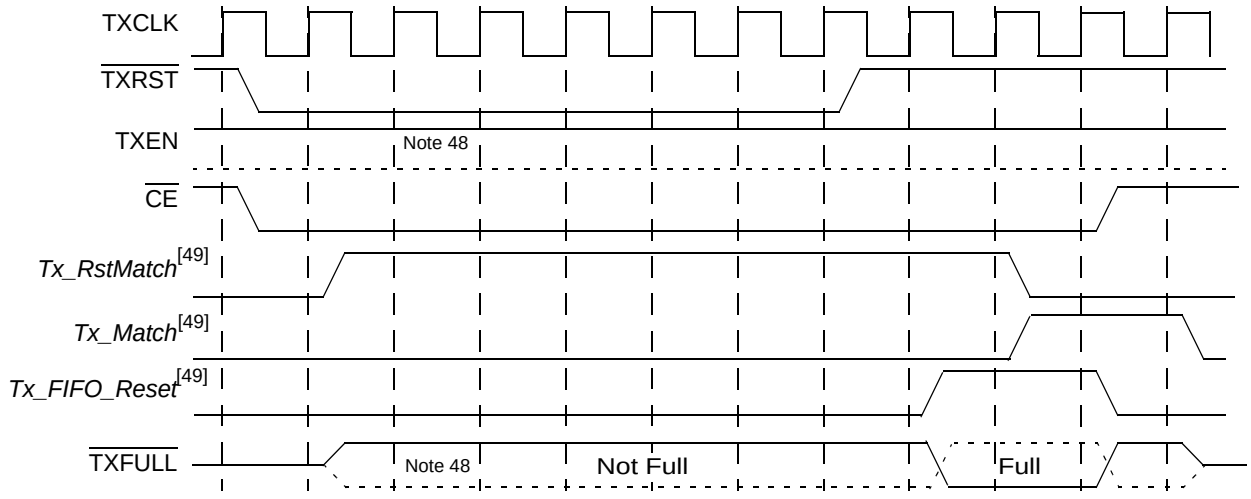
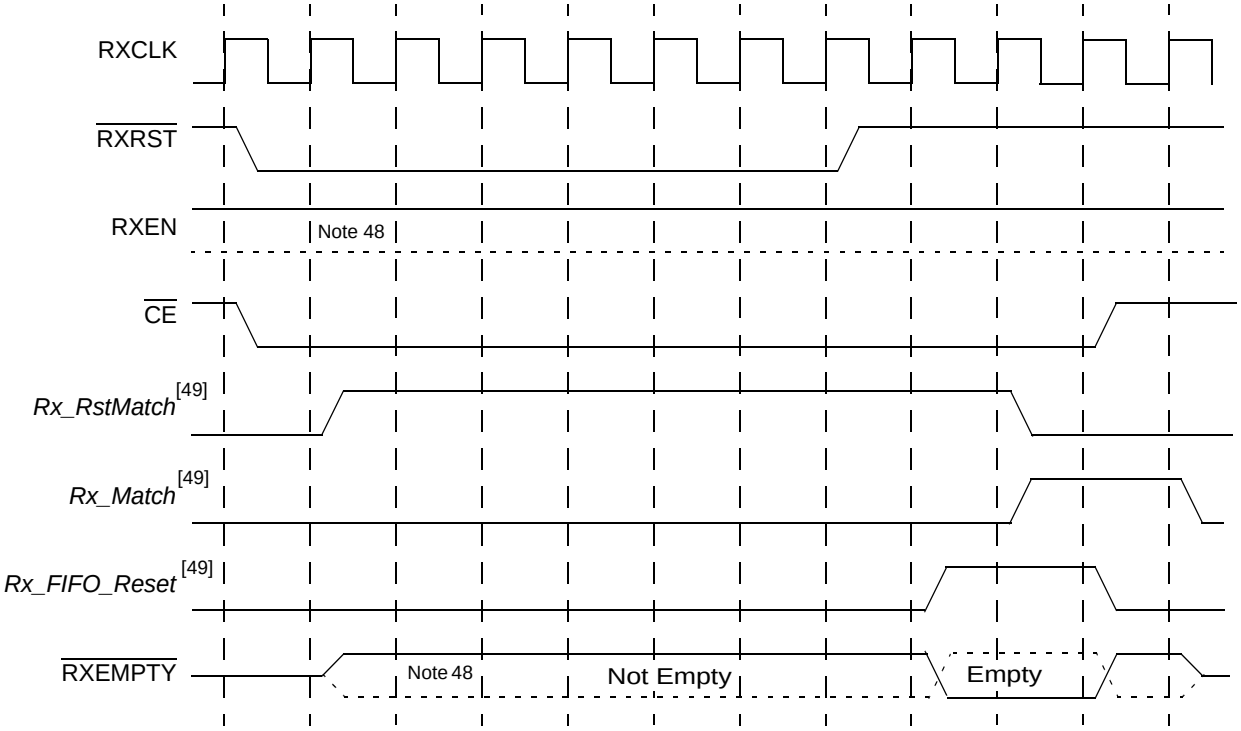


Figure 14 shows a sequence of input signals which will not produce a FIFO reset. In this case TXEN was asserted to select a Transmit FIFO for data transfers. Because TXEN remains active, the assertion of $\overline{\text{CE}}$ and $\overline{\text{TXRST}}$ does not initiate a reset operation. This is shown by the $\overline{\text{TXFULL}}$ flag remaining HIGH (deasserted) following what would be the normal expiration of the seven-state reset counter.

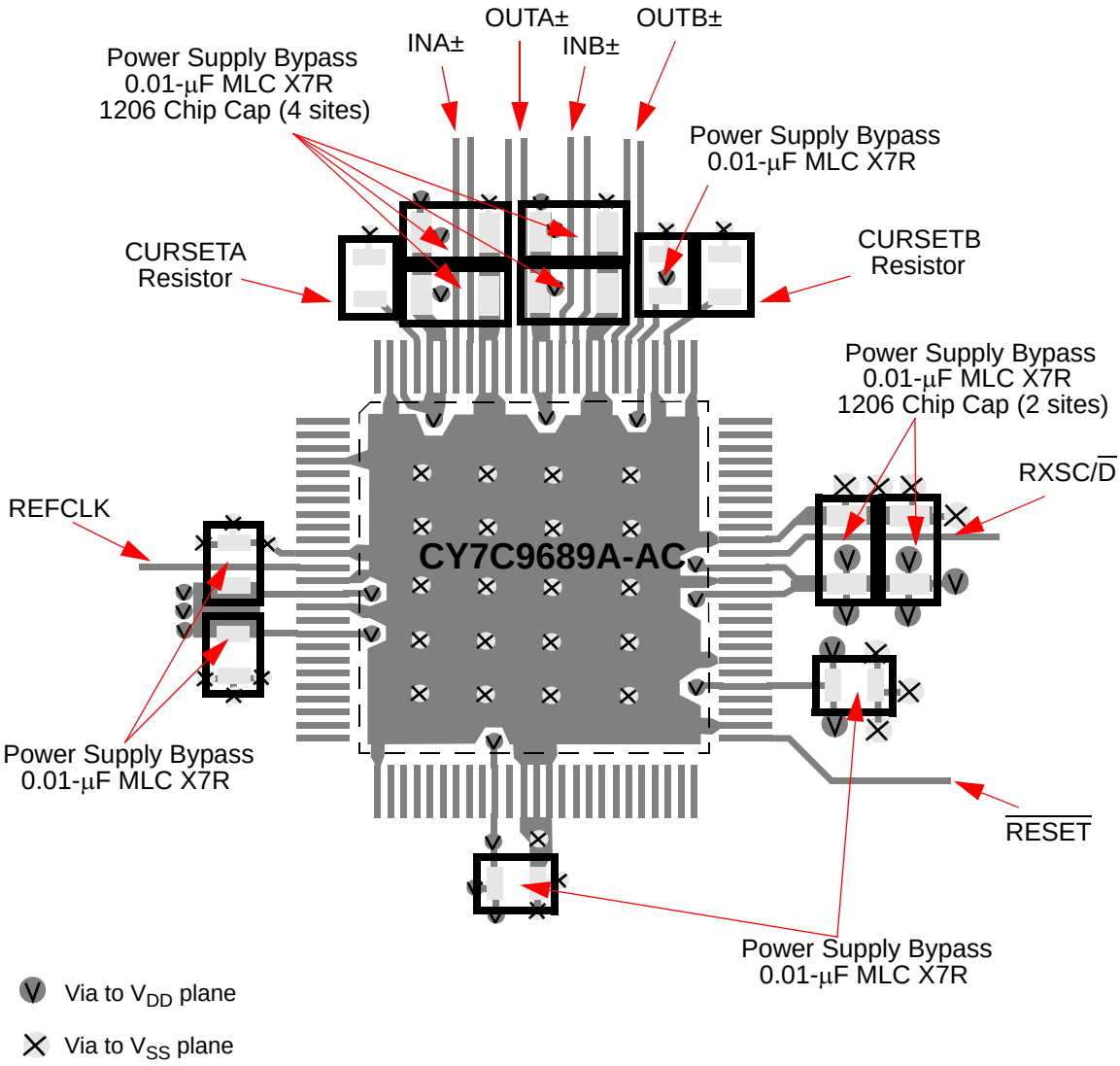
Receive FIFO Reset Sequence

The Receive FIFO reset sequence operates (for the most part) the same as the Transmit FIFO reset sequence. The same requirements exist for the assertion state of RXRST and selection of the interface. A sample Receive FIFO reset sequence is shown in Figure 16. Upon recognition of a Receive FIFO reset, the Receive FIFO flags are forced to indicate an EMPTY state to prohibit additional reads from the FIFO. Unlike the Transmit FIFO, where the internal completion of the reset operation is shown by first going FULL and later going EMPTY when the internal reset is complete, there is no secondary indication of the completion of the internal reset of the Receive FIFO. The Receive FIFO is usable as soon as new data is placed into it by the Receive Control State Machine

Figure 16. Receive FIFO Reset Sequence.



Printed Circuit Board Layout Suggestions

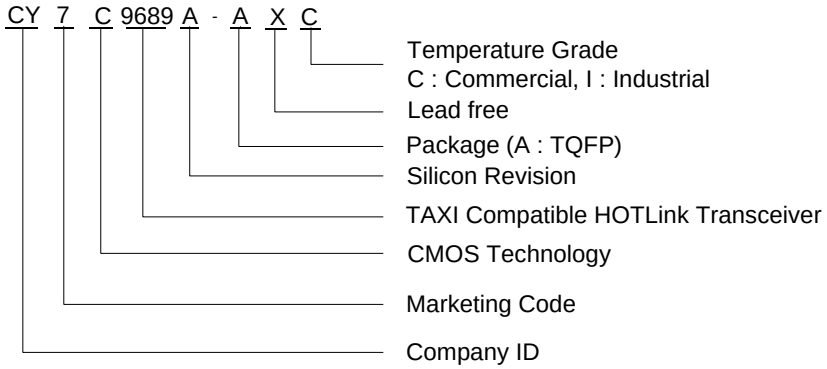


This is a typical printed circuit board layout showing example placement of power supply bypass components and other components mounted on the same side as the CY7C9689A. Other layouts, including cases with components mounted on the reverse side would work as well

Ordering Information

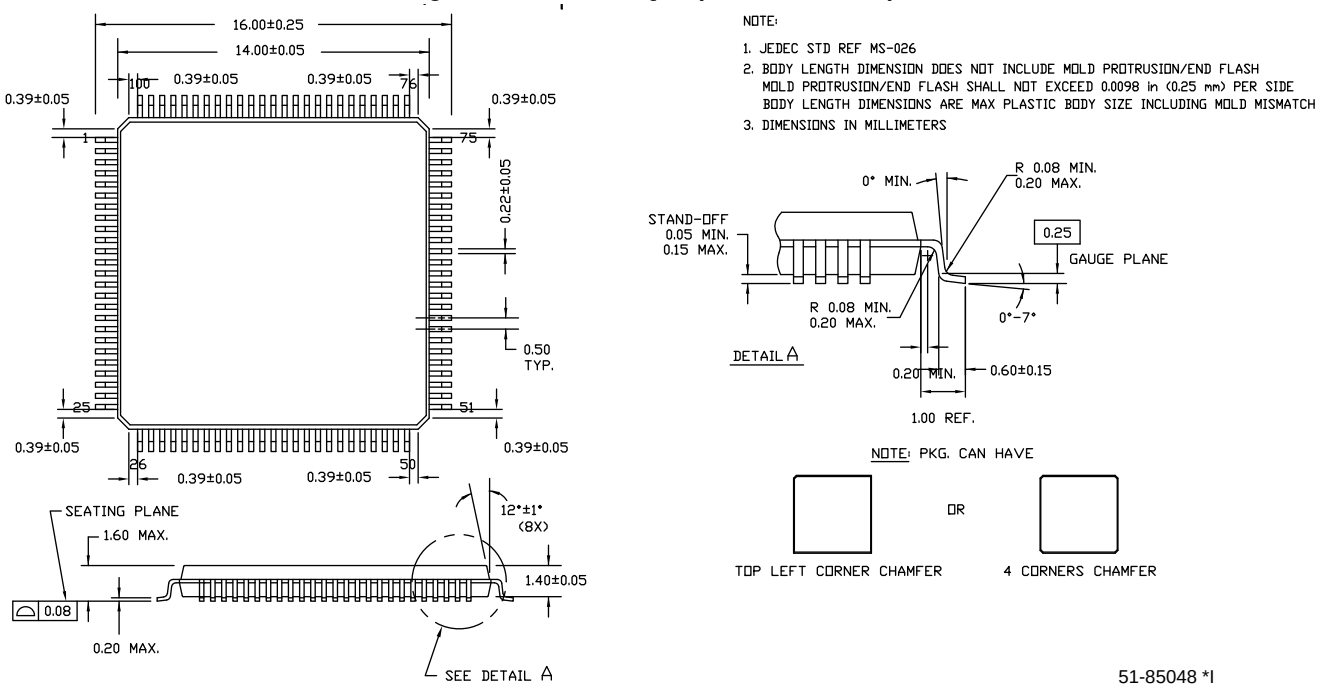
Ordering Code	Package Name	Package Type	Operating Range
CY7C9689A-AXC	A100	Pb-Free 100-lead Thin Quad Flat Pack	Commercial
CY7C9689A-AXI	A100	Pb-Free 100-lead Thin Quad Flat Pack	Industrial

Ordering Code Definitions



Package Diagram

Figure 17. 100-Pin TQFP (14 × 14 ×1.4 mm)



Acronyms

Table 9. Acronyms Used in this Document

Acronym	Description
AC	alternating current
BIST	built-in self-test
CDR	clock/data recovery
CML	current mode logic
DC	direct current
DVB	digital video broadcasting
ECL	emitter coupled logic
I/O	input/output
JTAG	joint test action group
LFI	link fault indicator
LFSR	linear feedback shift register
LPEN	local loopback input
PECL	positive-ECL
PLL	phase-locked loop
TTL	transistor-transistor logic
VCO	voltage controlled oscillator

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Mbps	megabits per second
MHz	megahertz
µA	microamperes
µs	microseconds
mA	milliamperes
mm	millimeters
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohms
pp	peak-to-peak
pF	picofarads
ps	picoseconds
sps	samples per second
V	volts

Document History Page

Document Title: CY7C9689A TAXI™-compatible HOTLink® Transceiver Document Number: 38-02020				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106249	04/20/01	SZV	Changed from Spec number: 38-00758 to 38-02020
*A	107695	06/28/01	SPN	Changed part number: CY7C9689 to CY7C9689A
*B	113563	04/10/02	REV	Removed parity reference Deleted mention of Byte-packer Fixed formatting to change mF to μF
*C	118318	11/08/02	REV	Changed pins 23 and 29 to RXDATA[11:10]/RXCMD[1:0] LFI was changed from “three state” to just output pin Fixed flip flop to Q as output and D as input Font problem with up-arrow symbols corrected
*D	506290	See ECN	PCX	Added Pb-Free part numbers to ordering information
*E	2896245	03/19/10	CGX	Updated ordering information and package diagram.
*F	3383795	09/26/11	SAAC	Template update Added Ordering Code Definitions Updated Package Diagram Added Contents, Acronyms, Units of Measure
*G	4421000	06/26/2014	LISZ	Updated pin 12 description. Updated Write Cycle, synchronous interface diagram on page 31 to add the timing specification.

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