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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

May 2014

FQB7N60 / FQI7N60

N-Channel QFET® MOSFET

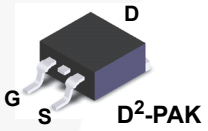
600 V, 7.4 A, 1.0 Ω

Description

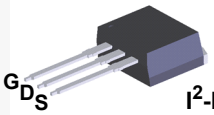
This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

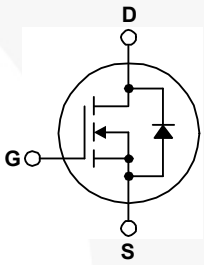
- 7.4 A, 600 V, $R_{DS(on)}$ = 1.0 Ω (Max.) @V_{GS} = 10 V, I_D = 3.7 A
- Low Gate Charge (Typ. 29 nC)
- Low Crss (Typ. 16 pF)
- 100% Avalanche Tested



D^2-PAK



I^2-PAK



Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FQB7N60TM FQB7N60TM_WS FQI7N60TU	Unit
V_{DSS}	Drain-Source Voltage		600	V
I_D	Drain Current - Continuous (T_C = 25°C)		7.4	A
	- Continuous (T_C = 100°C)		4.7	A
I_{DM}	Drain Current - Pulsed	(Note 1)	29.6	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	580	mJ
I_{AR}	Avalanche Current	(Note 1)	7.4	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	14.2	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_A = 25°C) *		3.13	W
	Power Dissipation (T_C = 25°C)		142	W
	- Derate above 25°C		1.14	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FQB7N60TM FQB7N60TM_WS FQI7N60TU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.88	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (*1 in^2 Pad of 2-oz Copper), Max.	40	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQB7N60TM	FQB7N60	D^2-PAK	Tape and Reel	330 mm	24 mm	800 units
FQB7N60TM_WS	FQB7N60S	D^2-PAK	Tape and Reel	330 mm	24 mm	800 units
FQI7N60TU	FQI7N60	I^2-PAK	Tube	N/A	N/A	50 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	600	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.67	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	--	--	10	μA
		V_{DS} = 480 V, T_C = 125°C	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 3.7 A	--	0.8	1.0	Ω
g_{FS}	Forward Transconductance	V_{DS} = 50 V, I_D = 3.7 A	--	6.4	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	1100	1430	pF
C_{oss}	Output Capacitance		--	135	175	pF
C_{rss}	Reverse Transfer Capacitance		--	16	21	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 300 V, I_D = 7.4 A, R_G = 25 Ω (Note 4)	--	30	70	ns
t_r	Turn-On Rise Time		--	80	170	ns
$t_{d(off)}$	Turn-Off Delay Time		--	65	140	ns
t_f	Turn-Off Fall Time		--	60	130	ns
Q_g	Total Gate Charge	V_{DS} = 480 V, I_D = 7.4 A, V_{GS} = 10 V (Note 4)	--	29	38	nC
Q_{gs}	Gate-Source Charge		--	7	--	nC
Q_{gd}	Gate-Drain Charge		--	14.5	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	7.4	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	29.6	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 7.4 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 7.4 A, dI_F / dt = 100 A/μs	--	320	--	ns
Q_{rr}	Reverse Recovery Charge		--	2.4	--	μC

Notes:
1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. L = 19.5 mH, I_{AS} = 7.4 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 7.4 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Essentially independent of operating temperature.

Typical Characteristics

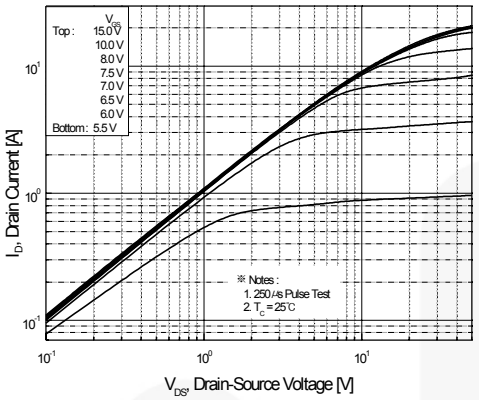


Figure 1. On-Region Characteristics

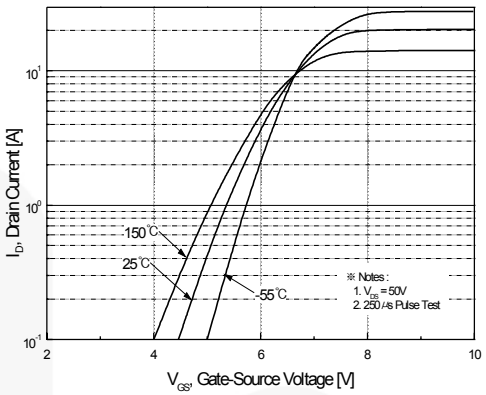


Figure 2. Transfer Characteristics

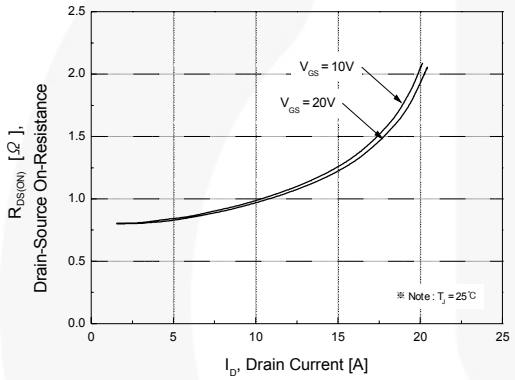


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

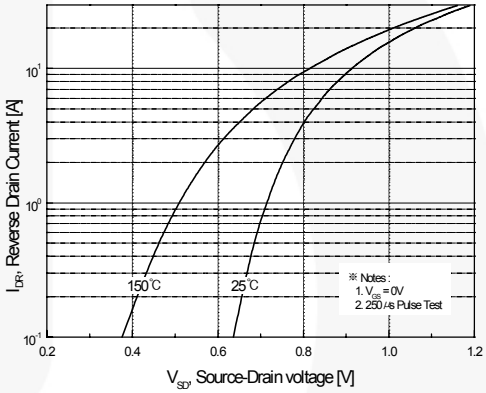


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

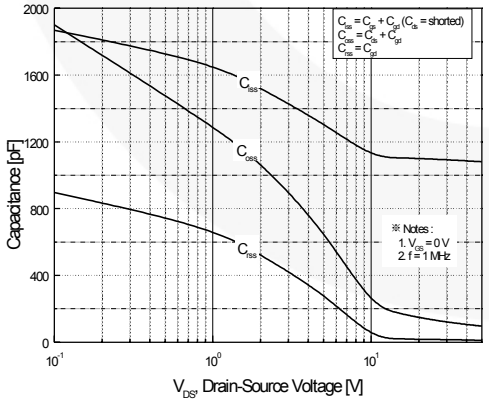


Figure 5. Capacitance Characteristics

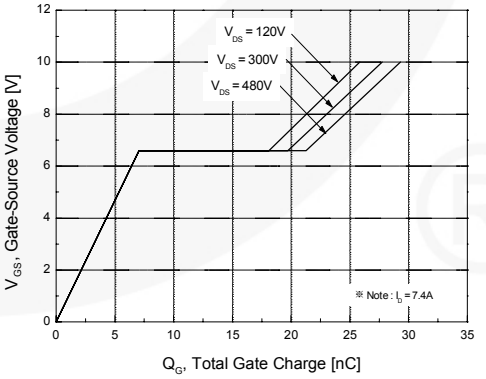


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

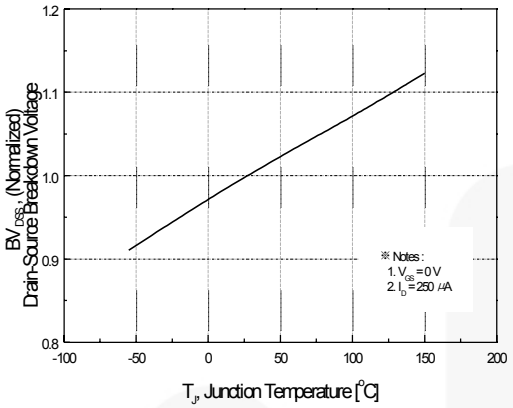


Figure 7. Breakdown Voltage Variation vs. Temperature

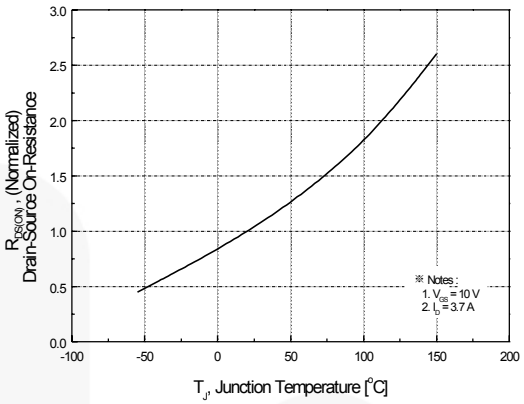


Figure 8. On-Resistance Variation vs. Temperature

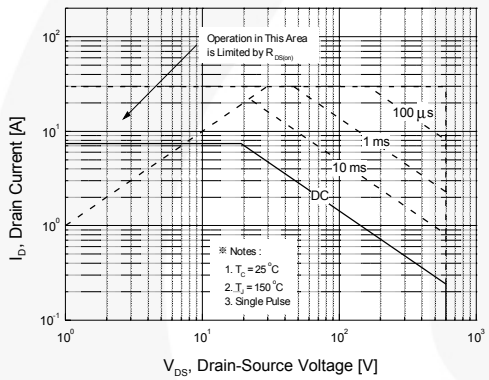


Figure 9. Maximum Safe Operating Area

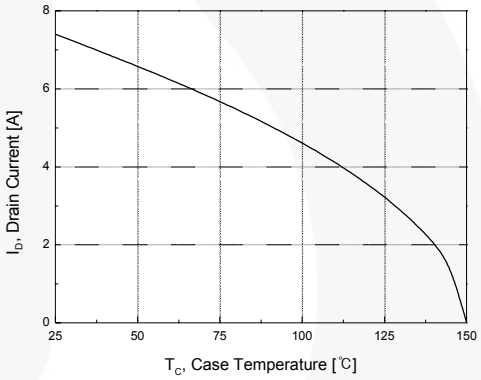


Figure 10. Maximum Drain Current vs. Case Temperature

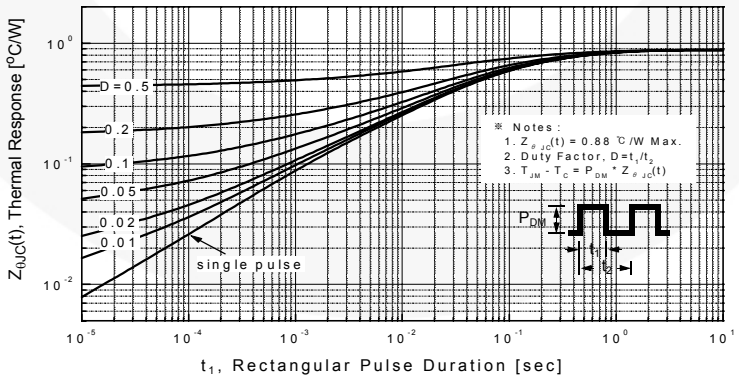


Figure 11. Transient Thermal Response Curve

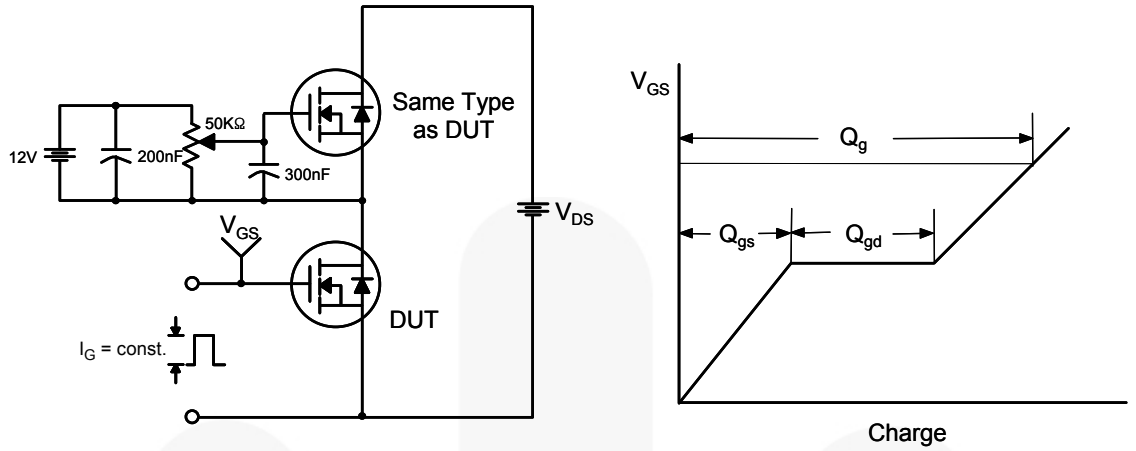


Figure 12. Gate Charge Test Circuit & Waveform

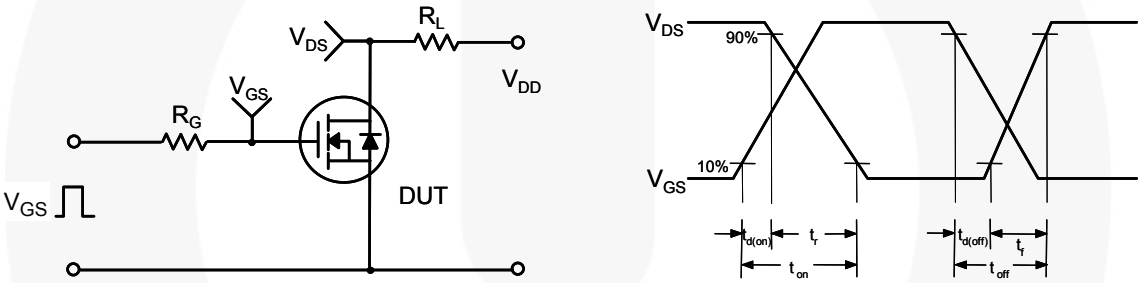


Figure 13. Resistive Switching Test Circuit & Waveforms

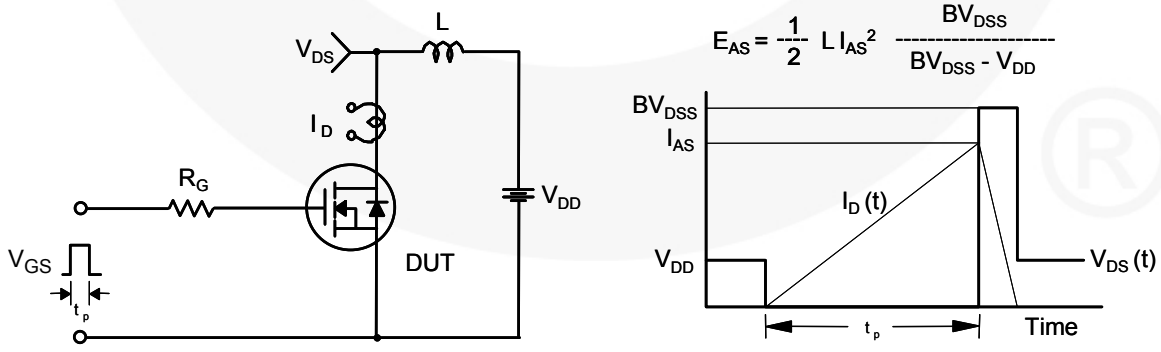


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

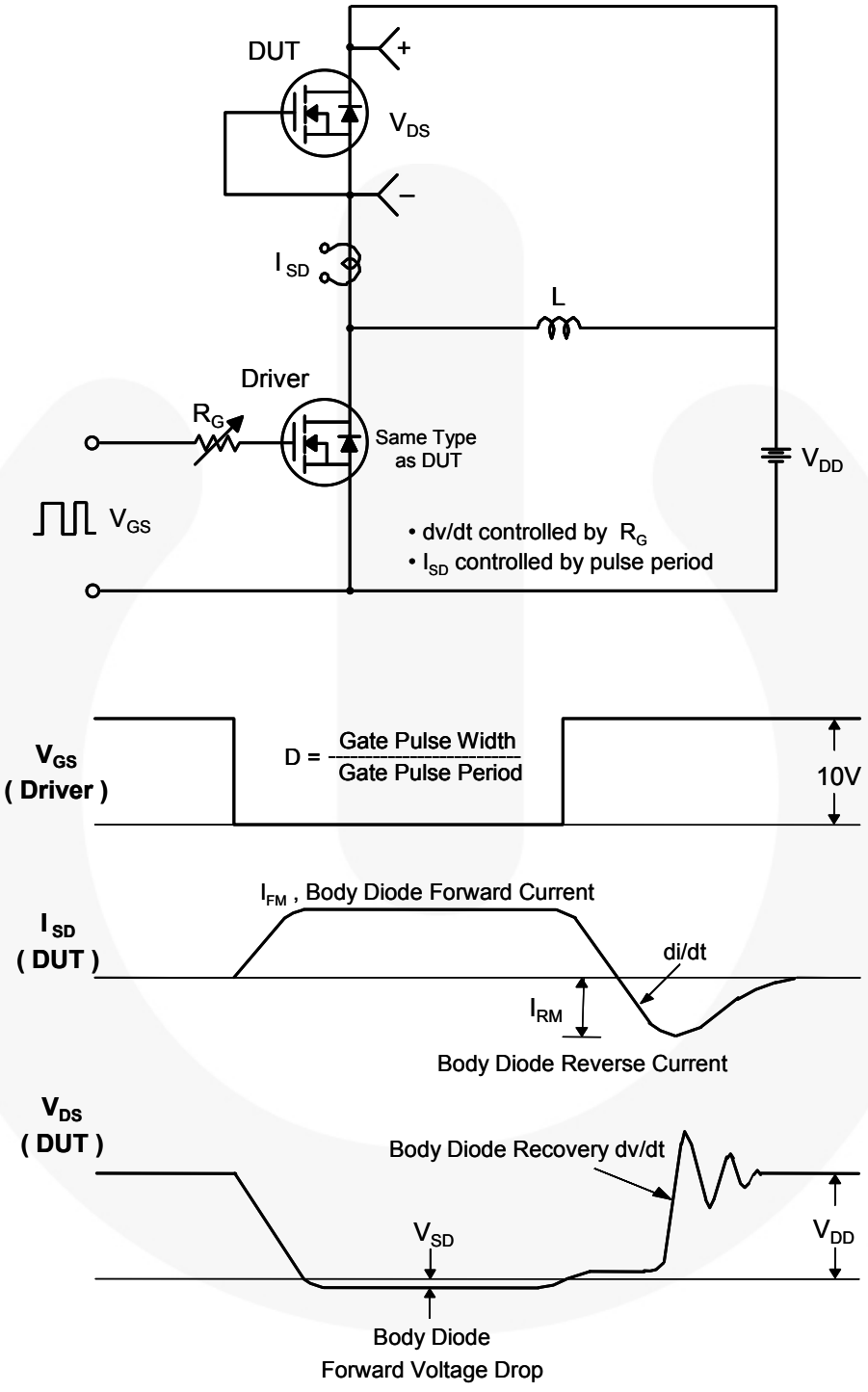


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

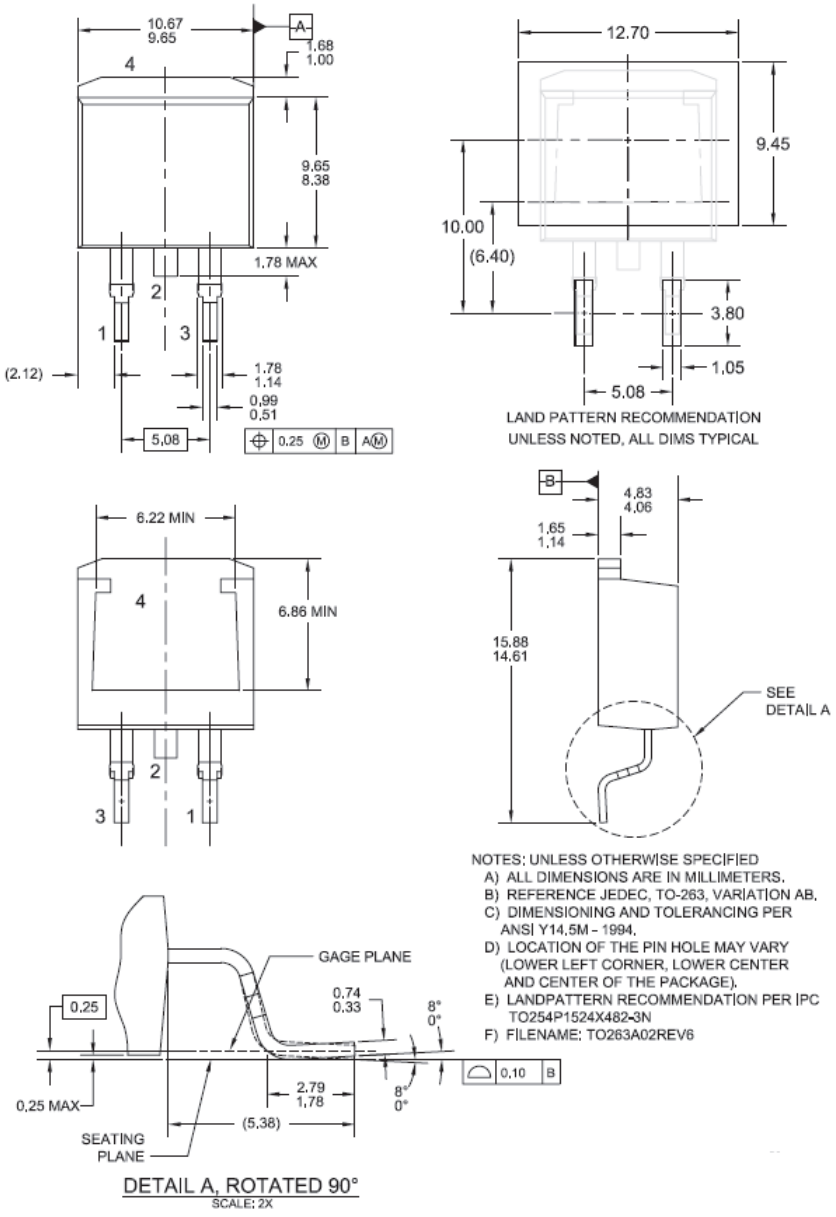


Figure 16. TO263 (D^2PAK), Molded, 2-Lead, Surface Mount

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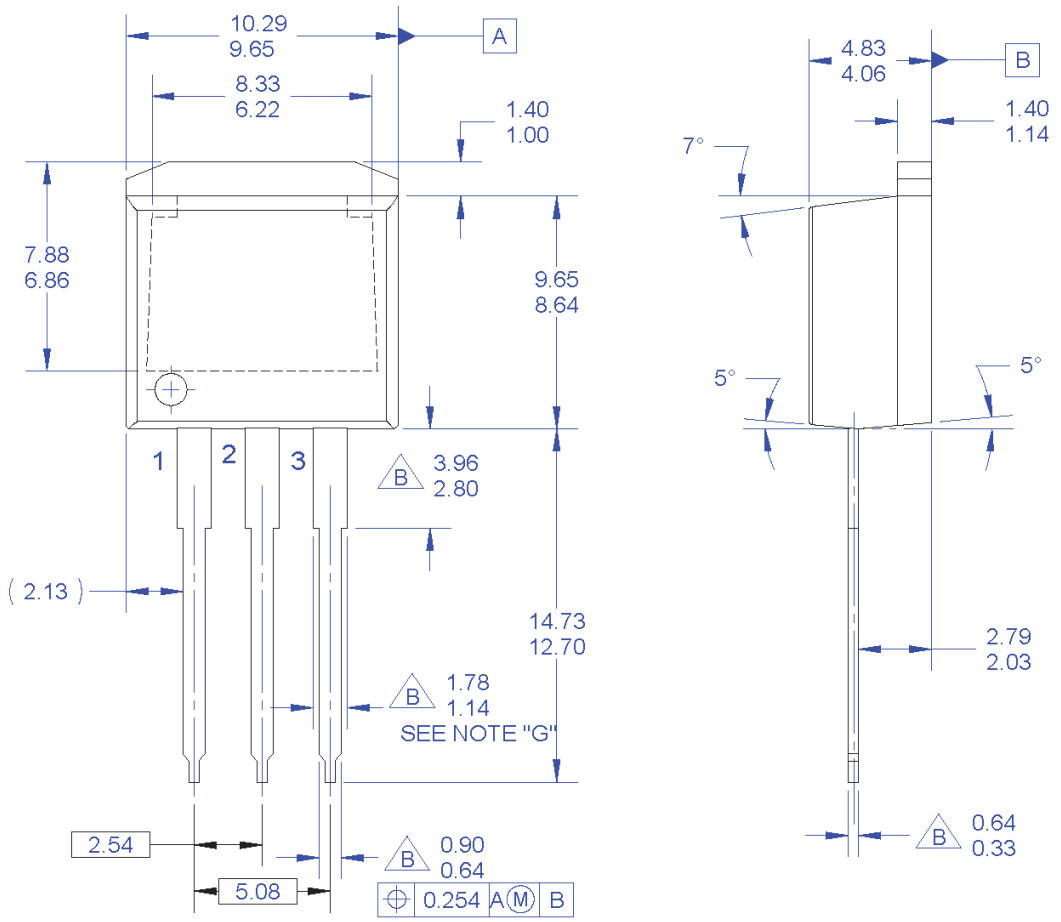
Mechanical Dimensions



NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.
B. DOES NOT COMPLY JEDEC STD. VALUE.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)
G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.
H. DRAWING FILE NAME: TO262A03REV5

Figure 17. TO262 (I^2PAK), Molded, 3-Lead, Jedec Variation AA

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I68

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