

SN54LS112A, SN54S112, SN74LS112A, SN74S112A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

D2661, APRIL 1982—REVISED MARCH 1988

SDLS011

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset and clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54LS112A and SN54S112 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS112A and SN74S112A are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each flip-flop)

| INPUTS | | | | | OUTPUTS | |
|--------|-----|-----|---|---|----------------|----------------|
| PRE | CLR | CLK | J | K | Q | \bar{Q} |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H [†] | H [†] |
| H | H | ↓ | L | L | Q ₀ | \bar{Q}_0 |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | TOGGLE | |
| H | H | H | X | X | Q ₀ | \bar{Q}_0 |

[†] The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} minimum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

SN54LS112A, SN54S112 . . . J OR W PACKAGE
SN74LS112A, SN74S112A . . . D OR N PACKAGE

(TOP VIEW)



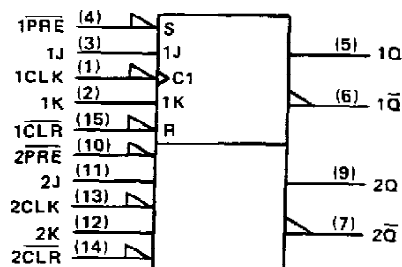
SN54LS112A, SN54S112 . . . FK PACKAGE

(TOP VIEW)



NC—No internal connection

logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

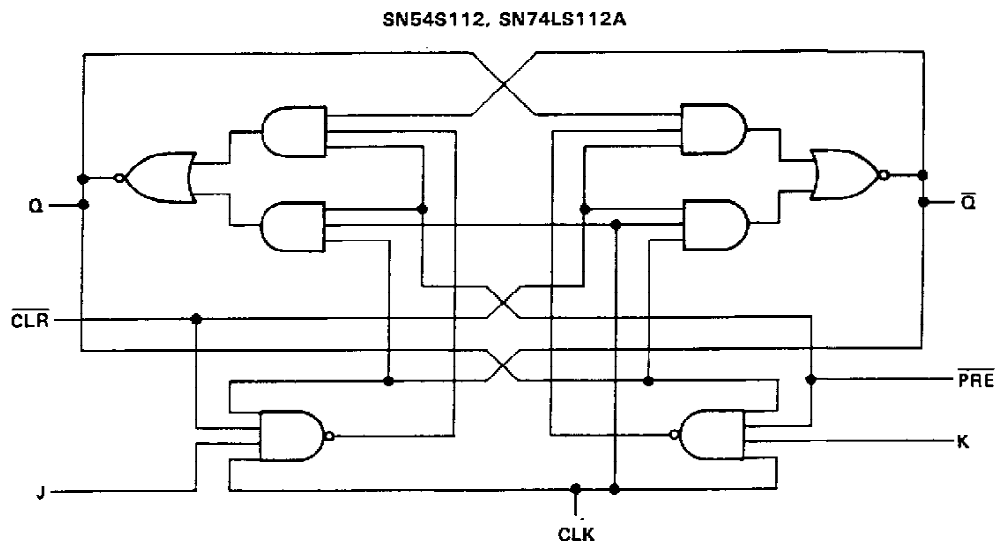
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SN54LS112A, SN54S112, SN74LS112A, SN74S112A

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

logic diagrams (positive logic)



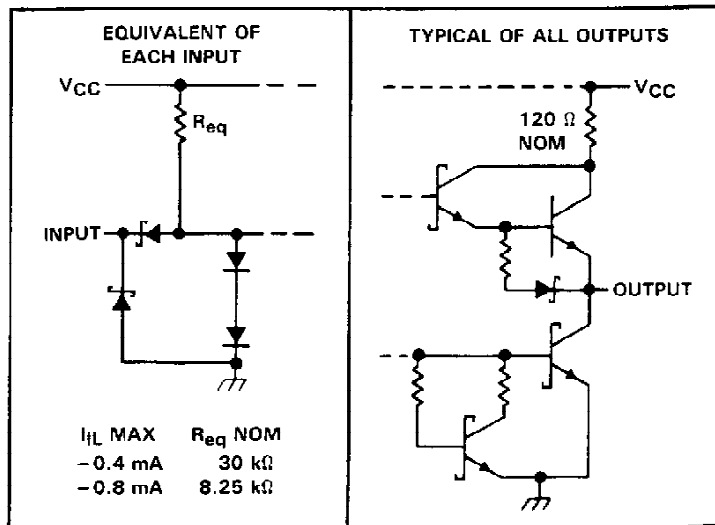
TEXAS
INSTRUMENTS

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SN54LS112A, SN54S112, SN74LS112A, SN74S112A
DUAL J-K NEGATIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET AND CLEAR

schematics of inputs and outputs

'LS112A



SN54S112, SN74S112A



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage: 'LS112A | 7 V |
| SN54LS112, SN74LS112A | 5.5 V |
| Operating free-air temperature range: SN54' | -55°C to 125°C |
| SN74' | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

SN54LS112A, SN74LS112A

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

| | | SN54LS112A | | | SN74LS112A | | | UNIT |
|-------------|--------------------------------|------------------|-----|------|------------|-----|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.7 | | | 0.8 | V |
| I_{OH} | High-level output current | | | -0.4 | | | -0.4 | mA |
| I_{OL} | Low-level output current | | | 4 | | | 8 | mA |
| f_{clock} | Clock frequency | 0 | | 30 | 0 | | 30 | MHz |
| t_w | Pulse duration | CLK high | | 20 | | | 20 | ns |
| | | PRE or CLR low | | 25 | | | 25 | |
| t_{su} | Set up time-before CLK↓ | Data high or low | | 20 | | | 20 | ns |
| | | CLR inactive | | 25 | | | 25 | |
| | | PRE inactive | | 20 | | | 20 | |
| t_h | Hold time-data after CLK↓ | 0 | | | 0 | | | ns |
| T_A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54LS112A | | SN74LS112A | | UNIT |
|------------------|------------|-------------------------|---|------------|------|------------|------|---------------|
| | | | | MIN | TYP‡ | MAX | MIN | |
| V_{IK} | | $V_{CC} = \text{MIN}$, | $I_I = -18 \text{ mA}$ | | | -1.5 | -1.5 | V |
| V_{OH} | | $V_{CC} = \text{MIN}$, | $V_{IH} = 2 \text{ V}$, $V_{IL} = \text{MAX}$, | 2.5 | 3.4 | | | V |
| V_{OL} | | $V_{CC} = \text{MIN}$, | $V_{IL} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, | 0.25 | 0.4 | | | V |
| | | $V_{CC} = \text{MIN}$, | $V_{IL} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, | | | | 0.35 | |
| I_I | J or K | $V_{CC} = \text{MAX}$, | $V_I = 7 \text{ V}$ | | | 0.1 | 0.1 | mA |
| | CLR or PRE | | | | | 0.3 | 0.3 | |
| | CLK | | | | | 0.4 | 0.4 | |
| I_{IH} | J or K | $V_{CC} = \text{MAX}$, | $V_I = 2.7 \text{ V}$ | | | 20 | 20 | μA |
| | CLR or PRE | | | | | 60 | 60 | |
| | CLK | | | | | 80 | 80 | |
| I_{IL} | J or K | $V_{CC} = \text{MAX}$, | $V_I = 0.4 \text{ V}$ | | | -0.4 | -0.4 | mA |
| | All other | | | | | -0.8 | -0.8 | |
| I_{OS}^{\S} | | $V_{CC} = \text{MAX}$, | see Note 2 | -20 | -100 | -20 | -100 | mA |
| I_{CC} (Total) | | $V_{CC} = \text{MAX}$, | see Note 3 | 4 | 6 | 4 | 6 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTES: 2. For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with $V_O = 2.25 \text{ V}$ and 2.125 V for the '54 family and the '74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

3. With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

TEXAS
INSTRUMENTS

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SN54LS112A, SN74LS112A
DUAL J-K NEGATIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET AND CLEAR

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Note 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|------------|--|----------------------------|---|-----|-----|-----|------|----|
| f_{\max} | | | $R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$ | 30 | 45 | | MHz | |
| t_{PLH} | $\overline{\text{CLR}}$, $\overline{\text{PRE}}$ or CLK | Q or $\overline{\text{Q}}$ | | | 15 | 20 | | ns |
| t_{PHL} | | | | | 15 | 20 | | ns |

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

SN54S112, SN74S112A
DUAL J-K NEGATIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

| | | SN54S112 | | | SN74S112A | | | UNIT |
|-----------------|--------------------------------|------------------|-----|-----|-----------|-----|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} | Low-level input voltage | 0.8 | | | 0.8 | | | V |
| I _{OH} | High-level output current | -1 | | | -1 | | | mA |
| I _{OL} | Low-level output current | 20 | | | 20 | | | mA |
| t _w | Pulse duration | CLK high | | 6 | 6 | | ns | |
| | | CLK low | | 6.5 | 6.5 | | | |
| | | PRE or CLR low | | 8 | 8 | | | |
| t _{su} | Set up time-before CLK↓ | Data high or low | | 7 | 7 | | ns | |
| t _h | Hold time-data after CLK↓ | 0 | | | 0 | | | ns |
| T _A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54S112 | | | SN74S112A | | | UNIT |
|-------------------|-----------|---|--|----------|------|-----|-----------|------|-----|------|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V _{IK} | | V _{CC} = MIN, I _I = -18 mA | | -1.2 | | | -1.2 | | | V |
| V _{OH} | | V _{CC} = MIN, I _{OH} = -1 mA, V _{IH} = 2 V, V _{IL} = MAX, | | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| V _{OL} | | V _{CC} = MIN, I _{OL} = 20 mA, V _{IH} = 2 V, V _{IL} = 0.8 V, | | 0.5 | | | 0.5 | | | V |
| I _I | | V _{CC} = MAX, V _I = 5.5 V | | 1 | | | 1 | | | mA |
| I _{IH} | J or K | V _{CC} = MAX, V _I = 2.7 V | | 50 | | | 50 | | | μA |
| | All other | | | 100 | | | 100 | | | |
| I _{IL} | J or K | V _{CC} = MAX, V _I = 0.5 V | | -1.6 | | | -1.6 | | | mA |
| | CLR‡ | | | -7 | | | -7 | | | |
| | PRE‡ | | | -7 | | | -7 | | | |
| | CLK | | | -4 | | | -4 | | | |
| I _{OS} † | | V _{CC} = MAX | | -40 | -100 | | -40 | -100 | mA | |
| I _{CC} # | | V _{CC} = MAX, see Note 3 | | 15 | 25 | | 15 | 25 | mA | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Clear is tested with preset high and preset is tested with clear high.

¶ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

Values are average per flip-flop.

NOTE 3: With all outputs open, I_{CC} is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.



SN54S112, SN74S112A
DUAL J-K NEGATIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET AND CLEAR

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Note 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------|---|---------------------|--|-----|-----|-----|------|
| f_{\max} | | | $R_L = 280\ \Omega, \quad C_L = 15\ \text{pF}$ | 80 | 125 | | MHz |
| t_{PLH} | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or \overline{Q} | | | 4 | 7 | ns |
| t_{PHL} | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ (CLK high) | \overline{Q} or Q | | | 5 | 7 | ns |
| | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ (CLK low) | | | | 5 | 7 | |
| t_{PLH} | CLK | Q or \overline{Q} | | | 4 | 7 | ns |
| t_{PHL} | | | | | 5 | 7 | ns |

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.



PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| JM38510/07102BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| JM38510/07102BFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| JM38510/30103B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| JM38510/30103BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| JM38510/30103BFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| M38510/07102BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| M38510/07102BFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| M38510/30103B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| M38510/30103BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| M38510/30103BFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SN54LS112AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SN54S112J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SN74LS112AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS112ADE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS112ADG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS112ADR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS112ADRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS112ADRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS112AN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74LS112AN3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | |
| SN74LS112ANE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74LS112ANSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS112ANSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|-----------------------------|
| SN74LS112ANSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74S112AD | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | |
| SN74S112AN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74S112AN3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | |
| SN74S112ANE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SNJ54LS112AFK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| SNJ54LS112AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SNJ54LS112AW | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SNJ54S112FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| SNJ54S112J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SNJ54S112W | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54LS112A, SN74LS112A :

- Catalog: [SN74LS112A](#)
- Military: [SN54LS112A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS112ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LS112ANSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS112ADR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74LS112ANSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



4040180-3/D 07/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN





4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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