

## Dual Auto-Zeroed Operational Amplifiers

### Features:

- First Monolithic Dual Auto-Zeroed Operational Amplifier
- Chopper Amplifier Performance Without External Capacitors:
  - $V_{OS}$ : 15  $\mu\text{V}$  Max.
  - $V_{OS}$ : Drift; 0.15  $\mu\text{V}/^\circ\text{C}$  Max.
  - Saves Cost of External Capacitors
- SOIC Packages Available
- High DC Gain; 120dB
- Low Supply Current; 650  $\mu\text{A}$
- Low Input Voltage Noise:
  - 0.65  $\mu\text{V}_{P-P}$  (0.1 Hz to 10 Hz)
- Wide Common Mode Voltage Range:
  - $V_{SS}$  to  $V_{DD} - 2\text{V}$
- High Common Mode Rejection; 116dB
- Dual or Single Supply Operation:
  - $\pm 3.3\text{V}$  to  $\pm 8.3\text{V}$
  - $+6.5\text{V}$  to  $+16\text{V}$
- Excellent AC Operating Characteristics:
  - Slew Rate; 2.5V/ $\mu\text{sec}$
  - Unity-Gain Bandwidth; 1.5 MHz
- Pin Compatible with LM358, OP-14, MC1458, ICL7621, TL082, TLC322

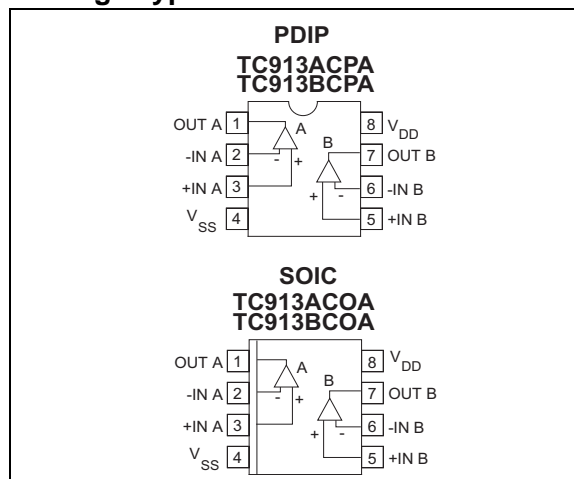
### Applications:

- Instrumentation
- Medical Instrumentation
- Embedded Control
- Temperature Sensor Amplifier
- Strain Gage Amplifier

### Device Selection Table

Part Number	Package	Temp. Range	Offset Voltage
TC913ACOA	8-Pin SOIC	0°C to +70°C	15 $\mu\text{V}$
TC913ACPA	8-Pin PDIP	0°C to +70°C	15 $\mu\text{V}$
TC913BCOA	8-Pin SOIC	0°C to +70°C	30 $\mu\text{V}$
TC913BCPA	8-Pin PDIP	0°C to +70°C	30 $\mu\text{V}$

### Package Type



### General Description:

The TC913 is the world's first complete monolithic, dual auto-zeroed operational amplifier. The TC913 sets a new standard for low-power, precision dual-operational amplifiers. Chopper-stabilized or auto-zeroed amplifiers offer low offset voltage errors by periodically sampling offset error, and storing correction voltages on capacitors. Previous single amplifier designs required two user-supplied, external 0.1  $\mu\text{F}$  error storage correction capacitors — much too large for on-chip integration. The unique TC913 architecture requires smaller capacitors, making on-chip integration possible. Microvolt offset levels are achieved and **external capacitors are not required**.

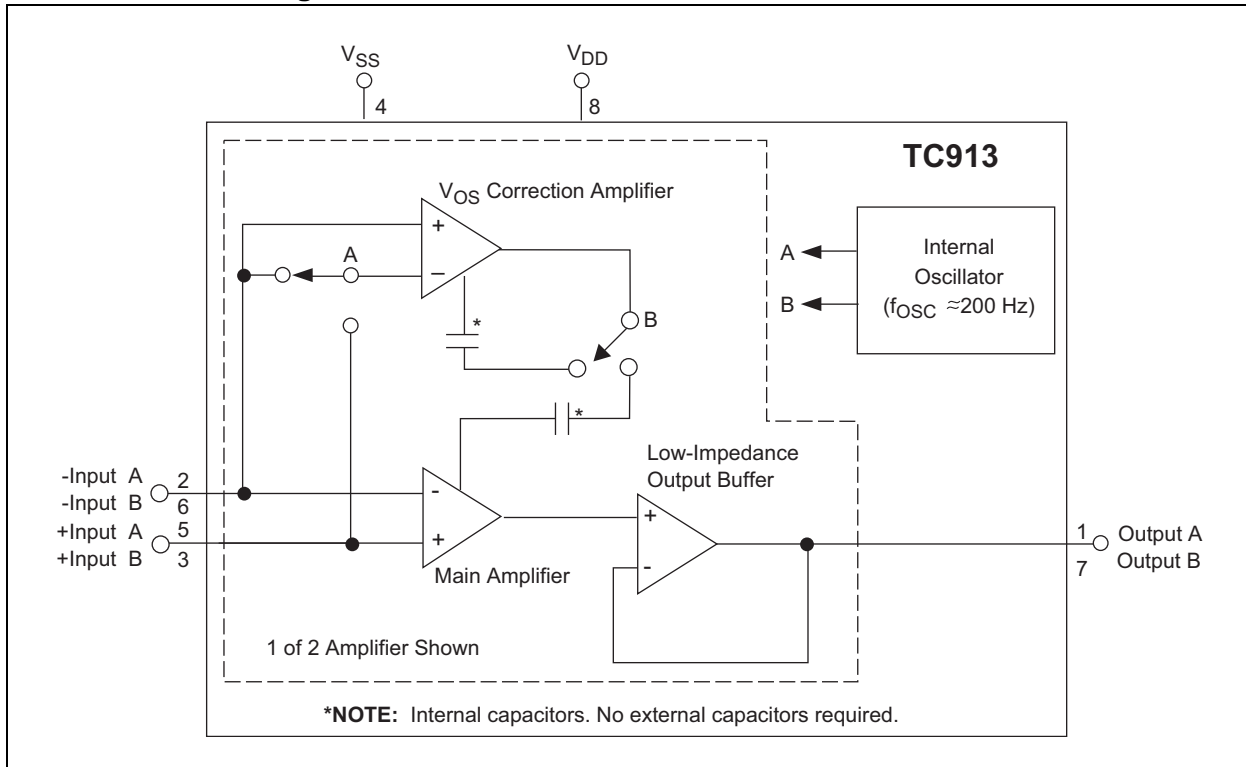
The TC913 system benefits are apparent when contrasted with a TC7650 chopper amplifier circuit implementation. A single TC913 replaces two TC7650's and four capacitors. Five components and assembly steps are eliminated.

The TC913 pinout matches many popular dual-operational amplifiers: OP-04, TLC322, LM358, and ICL7621 are typical examples. In many applications, operating from dual 5V power supplies or single supplies, the TC913 offers superior electrical performance, and can be a functional drop-in replacement; printed circuit board rework is not necessary. The TC913's low offset voltage error eliminates offset voltage trim potentiometers often needed with bipolar and low accuracy CMOS operational amplifiers.

The TC913 takes full advantage of Microchip's proprietary CMOS technology. Unity gain bandwidth is 1.5 MHz and slew rate is 2.5V/ $\mu\text{sec}$ .

# TC913A/TC913B

## Functional Block Diagram



# TC913A/TC913B

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings\*

Total Supply Voltage ( $V_{DD}$ to $V_{SS}$ ) .....	+18V
Input Voltage .....	( $V_{DD} + 0.3V$ ) to ( $V_{SS} - 0.3V$ )
Current Into Any Pin .....	10 mA
While Operating .....	100 $\mu$ A
Package Power Dissipation ( $T_A = 70^\circ\text{C}$ )	
Plastic DIP .....	730 mW
Plastic SOIC .....	470 mW
Operating Temperature Range	
C Device .....	0°C to +70°C
Storage Temperature Range .....	-65°C to +150°C

\*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

## TC913A AND TC913B ELECTRICAL SPECIFICATIONS

Electrical Characteristics: $V_S = \pm 5V$ , $T_A = +25^\circ\text{C}$ , unless otherwise indicated.									
			TC913A			TC913B			
Symbol	Parameter	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
$V_{OS}$	Input Offset Voltage	—	5	15	—	15	30	$\mu$ V	$T_A = +25^\circ\text{C}$
$TCV_{OS}$	Average Temp. Coefficient of Input Offset Voltage	—	0.05	0.15	—	0.1	0.25	$\mu\text{V}/^\circ\text{C}$	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
		—	0.05	0.15	—	0.1	0.25	$\mu\text{V}/^\circ\text{C}$	$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ (Note 1)
$I_B$	Average Input Bias Current	—	—	90	—	—	120	$\mu$ A	$T_A = +25^\circ\text{C}$
		—	—	3	—	—	4	nA	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
		—	—	4	—	—	6	nA	$-25^\circ\text{C} \leq T_A \leq +85^\circ$
$I_{OS}$	Average Input Offset Current	—	5	20	—	10	40	$\mu$ A	$T_A = +25^\circ\text{C}$
		—	—	1	—	—	1	nA	$T_A = +85^\circ\text{C}$
$e_N$	Input Voltage Noise	—	0.6	—	—	0.6	—	$\mu\text{V}_{P-P}$	0.1 to 1 Hz, $R_S \leq 100\Omega$
		—	11	—	—	11	—	$\mu\text{V}_{P-P}$	0.1 to 10 Hz, $R_S \leq 100\Omega$
CMRR	Common Mode Rejection Ratio	110	116	—	100	110	—	dB	$V_{SS} \leq V_{CM} \leq V_{DD} - 2.2$
CMVR	Common Mode Voltage Range	$V_{SS}$	—	$V_{DD} - 2$	$V_{SS}$	—	$V_{DD} - 2$	V	
$A_{OL}$	Open-Loop Voltage Gain	115	120	—	110	120	—	dB	$R_L = 10\text{ k}\Omega$ , $V_{OUT} = \pm 4V$
$V_{OUT}$	Output Voltage Swing	$V_{SS} + 0.3$	—	$V_{DD} - 0.9$	$V_{SS} + 0.3$	—	$V_{DD} - 0.9$	V	$R_L = 10\text{ k}\Omega$
BW	Closed Loop Bandwidth	—	1.5	—	—	1.5	—	MHz	Closed Loop Gain = +1
SR	Slew Rate	—	2.5	—	—	2.5	—	V/ $\mu$ sec	$R_L = 10\text{ k}\Omega$ , $C_L = 50\text{ pF}$
PSRR	Power Supply Rejection Ratio	110	—	—	100	—	—	dB	$\pm 3.3V$ to $\pm 5.5V$
$V_S$	Operating Supply Voltage Range	$\pm 3.5$	—	$\pm 8.3$	$\pm 3.5$	—	$\pm 8.3$	V	Split Supply
		7.0	—	16	7.0	—	16	V	Single Supply
$I_S$	Quiescent Supply Current	—	0.65	0.85	—	—	1.1	mA	$V_S = \pm 5V$

Note 1: Characterized; not 100% tested.

# TC913A/TC913B

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## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

**TABLE 2-1: PIN FUNCTION TABLE**

Pin No. (8-Pin PDIP) (8-Pin SOIC)	Symbol	Description
1	OUT A	Output
2	-IN A	Inverting Input
3	+IN A	Non-inverting Input
4	$V_{SS}$	Negative Power Supply
5	+IN B	Non-inverting Input
6	-IN B	Inverting Input
7	OUT B	Output
8	$V_{DD}$	Positive Power Supply

## 3.0 DETAILED DESCRIPTION

### 3.1 Theory of Operation

Each of the TC913's two Op Amps actually consists of two amplifiers. A main amplifier is always connected from the input to the output. A separate nulling amplifier alternately nulls its own offset and then the offset of the amplifier. Since each amplifier is continuously being nulled, offset voltage drift with time, temperature and power supply variations is greatly reduced.

All nulling circuitry is internal and the nulling operation is transparent to the user. Offset nulling voltages are stored on two internal capacitors. An internal oscillator and control logic, shared by the TC913's two amplifiers, control the nulling process.

### 3.2 Pin Compatibility

The TC913 pinout is compatible with OP-14, LM358, MC1458, LT1013, TLC322, and similar dual Op Amps. In many circuits operating from single or  $\pm 5V$  supplies, the TC913 is a drop-in replacement offering DC performance rivaling that of the best single Op Amps.

The TC913's amplifiers include a low-impedance class AB output buffer. Some previous CMOS chopper amplifiers used a high-impedance output stage which made open-loop gain dependent on load resistance. The TC913's open-loop gain is not dependent on load resistance.

### 3.3 Overload Recovery

The TC913 recovers quickly from output saturation. Typical recovery time from positive output saturation is 20 msec. Negative output saturation recovery time is typically 5 msec.

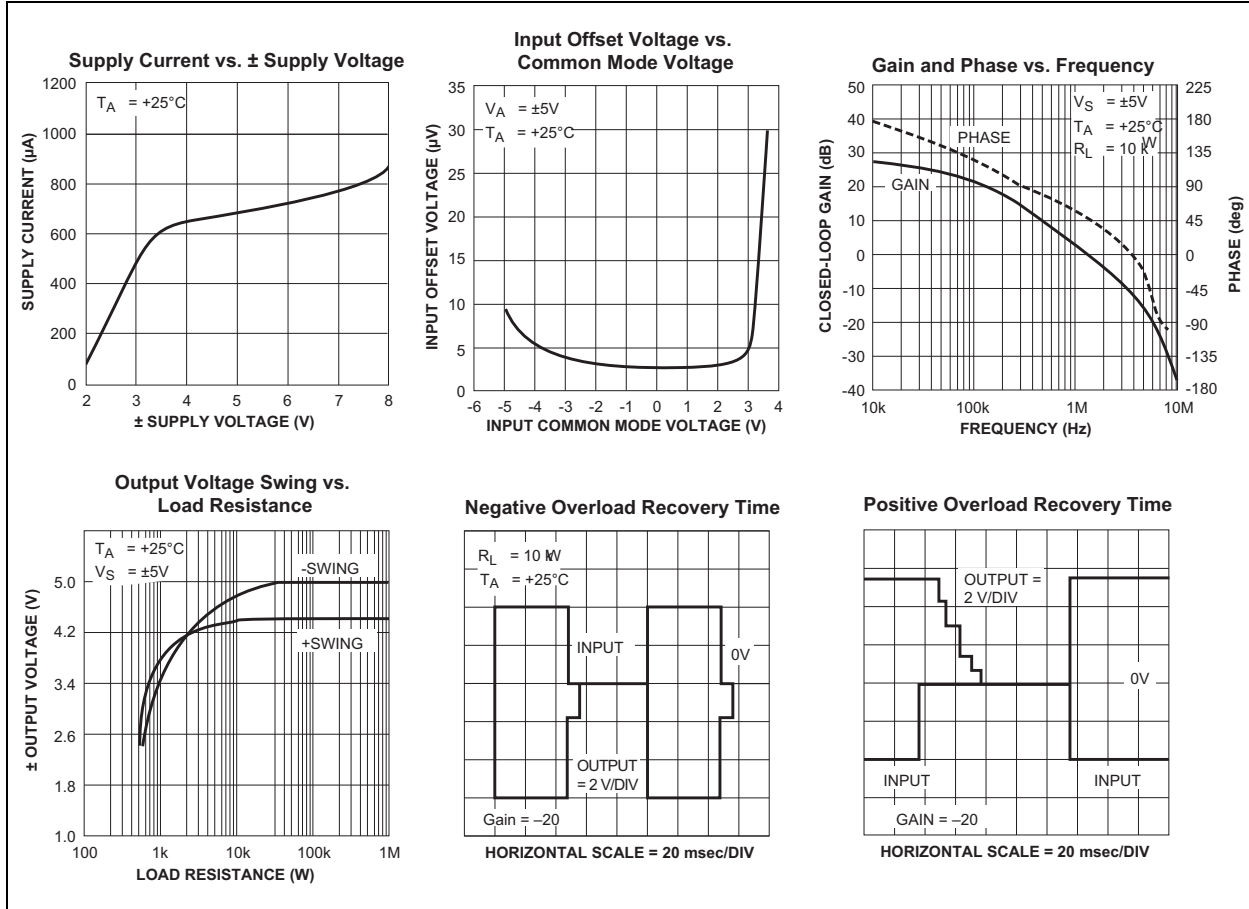
### 3.4 Avoiding Latch-up

Junction-isolated CMOS circuits inherently contain a parasitic p-n-p-n transistor circuit. Voltages exceeding the supplies by 0.3V should not be applied to the device pins. Larger voltages can turn the p-n-p-n device on, causing excessive device power supply current and power dissipation. The TC913's power supplies should be established at the same time or before input signals are applied. If this is not possible, input current should be limited to 0.1 mA to avoid triggering the p-n-p-n structure.

# TC913A/TC913B

## 4.0 TYPICAL CHARACTERISTICS

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

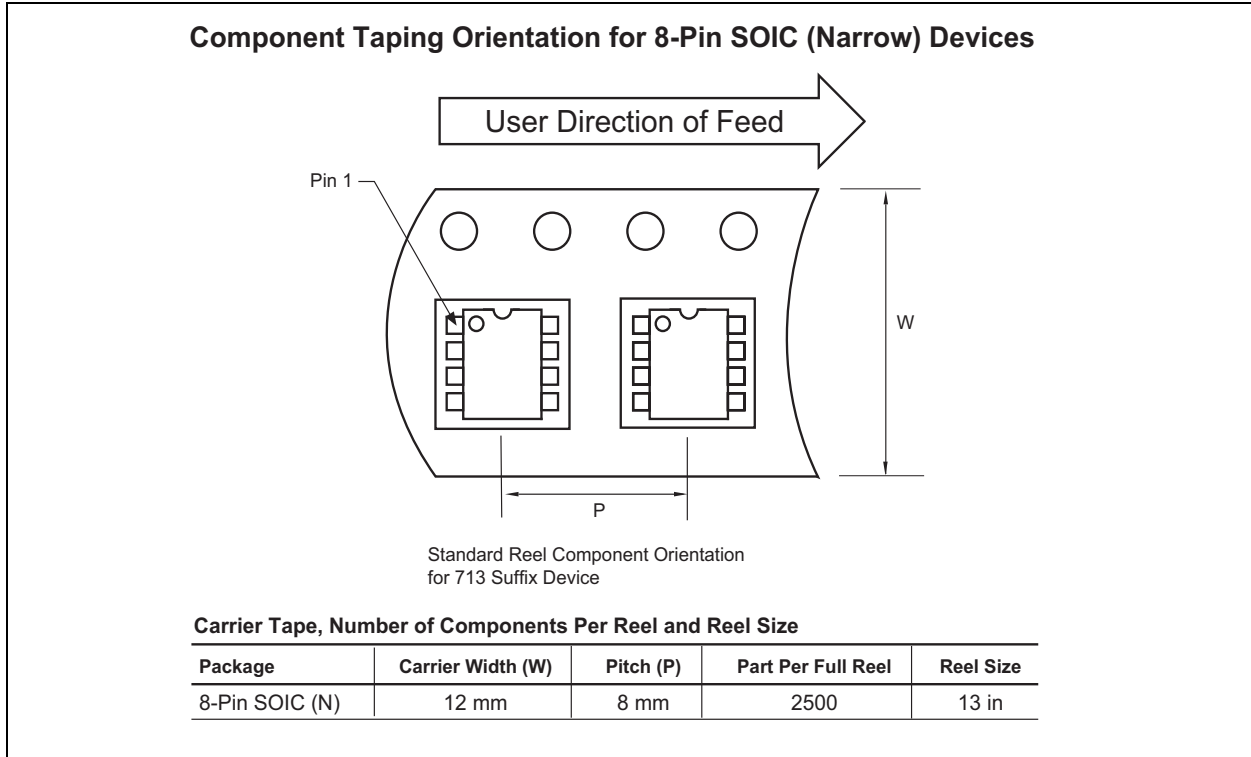


## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

Package marking data not available at this time.

### 5.2 Taping Form

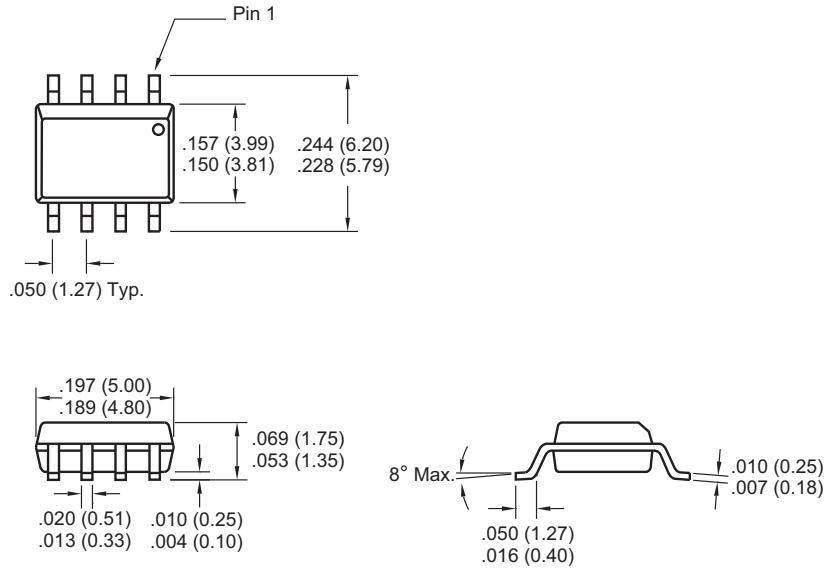


# TC913A/TC913B

## 5.3 Package Dimensions

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

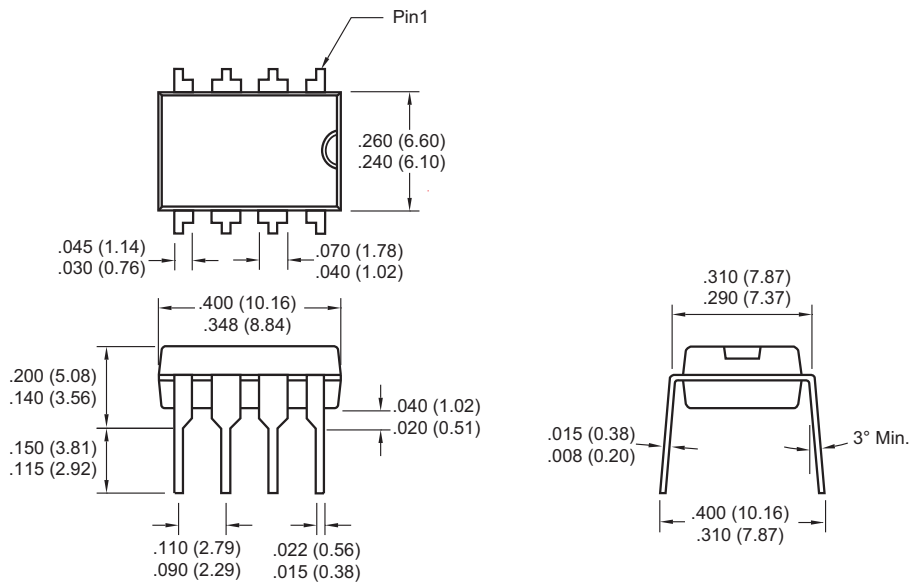
### 8-Pin SOIC



Dimensions: inches (mm)

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### 8-Pin Plastic DIP



Dimensions: inches (mm)



## 6.0 REVISION HISTORY

### Revision D (December 2012)

Added a note to each package outline drawing.

# TC913A/TC913B

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NOTES:

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### Наши контакты:

**Телефон:** +7 812 627 14 35

**Электронная почта:** [sales@st-electron.ru](mailto:sales@st-electron.ru)

**Адрес:** 198099, Санкт-Петербург,  
Промышленная ул, дом № 19, литера Н,  
помещение 100-Н Офис 331