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#### FDT457N

#### N-Channel Enhancement Mode Field Effect Transistor

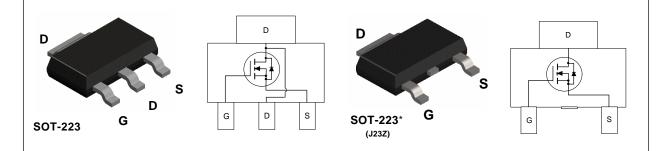
#### **General Description**

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance. These products are well suited to low voltage, low current applications such as notebook computer power management, battery powered circuits, and DC motor control.

#### **Features**

- $\begin{tabular}{ll} & \bullet & 5~A,~30~V.~R_{\rm DS(ON)} = 0.06~\Omega~@~V_{\rm GS} = 10~V \\ & R_{\rm DS(ON)} = 0.090~\Omega~@~V_{\rm GS} = 4.5~V. \\ \end{tabular}$
- High density cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handling capability in a widely used surface mount package.





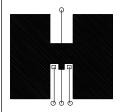
#### **Absolute Maximum Ratings** $T_A = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter		FDT457N	Units
V <sub>DSS</sub>	Drain-Source Voltage		30	V
V <sub>GSS</sub>	Gate-Source Voltage - Continuous		±20	V
I <sub>D</sub>	Maximum Drain Current - Continue	OUS (Note 1a)	5	А
	- Pulsed		16	
P <sub>D</sub>	Maximum Power Dissipation	(Note 1a)	3	W
		(Note 1b)	1.3	
		(Note 1c)	1.1	
T <sub>J</sub> ,T <sub>STG</sub>	Operating and Storage Temperature Range		-65 to 150	°C
THERMA	L CHARACTERISTICS			·
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)		42	°C/W
R <sub>euc</sub>	Thermal Resistance, Junction-to-C	Case (Note 1)	12	°C/W

<sup>\*</sup> Order option J23Z for cropped center drain lead.

Symbol	Parameter	Conditions		Min	Тур	Max	Units
OFF CHAR	ACTERISTICS	·					
3V <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		30			V
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25 °C			35		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V				1	μA
			T <sub>J</sub> =55°C			10	μA
GSSF	Gate - Body Leakage, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$				100	nA
GSSR	Gate - Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
ON CHARA	CTERISTICS (Note 2)	·					
/ <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		1	1.6	3	V
$\Delta V_{GS(th)}/\Delta T_{J}$	Gate Threshold Voltage Temp.Coefficient	I <sub>D</sub> = 250 μA, Referenced to	25 °C		-4.2		mV/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_{D} = 5 \text{ A}$			0.043	0.06	Ω
			T <sub>J</sub> =125°C		0.065	0.1	
		$V_{GS} = 4.5 \text{ V}, I_D = 3.8 \text{ A}$			0.071	0.09	
D(ON)	On-State Drain Current	$V_{GS} = 10 \text{ V}, V_{DS} = 5 \text{ V}$		5			Α
] <sub>FS</sub>	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_{D} = 5 \text{ A}$			5		S
OYNAMIC (	CHARACTERISTICS						
ciss	Input Capacitance	$V_{DS} = 15 \text{ V}, \ V_{GS} = 0 \text{ V},$ $f = 1.0 \text{ MHz}$			235		pF
oss	Output Capacitance				145		pF
C <sub>rss</sub>	Reverse Transfer Capacitance				50		pF
WITCHING	G CHARACTERISTICS (Note 2)						
D(on)	Turn - On Delay Time	$V_{DD} = 10 \text{ V}, I_{D} = 1 \text{ A},$			5	10	ns
	Turn - On Rise Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$			12	22	ns
O(off)	Turn - Off Delay Time				12	22	ns
	Turn - Off Fall Time				3	8	ns
$Q_g$	Total Gate Charge	$V_{DS} = 10 \text{ V}, \ I_{D} = 5 \text{ A}, \ V_{GS} = 5 \text{ V}$			4.2	5.9	nC
$Q_{gs}$	Gate-Source Charge				1.3		nC
$\mathbf{Q}_{ ext{gd}}$	Gate-Drain Charge				1.7		nC
RAIN-SOL	JRCE DIODE CHARACTERISTICS AND MA	XIMUM RATINGS					
6	Maximum Continuous Drain-Source Diode Forward Current					2.5	Α
/ <sub>SD</sub>	Drain-Source Diode Forward Voltage $V_{GS} = 0 \text{ V}, I_S = 2.5 \text{ A} \text{ (Note 2)}$		2)		0.85	1.2	V

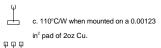
the drain pins.  $R_{\theta^{JC}}$  is



a. 42°C/W when mounted on a 1 in² pad of 2oz Cu.



b. 95°C/W when mounted on a 0.066 in<sup>2</sup> pad of 2oz Cu.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width  $\leq$  300 $\mu$ s, Duty Cycle  $\leq$  2.0%

<sup>1.</sup> R<sub>gui</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of guaranteed by design while  $\mathbf{R}_{\scriptscriptstyle{\theta \text{CA}}}$  is determined by the user's board design.

#### **Typical Electrical Characteristics**

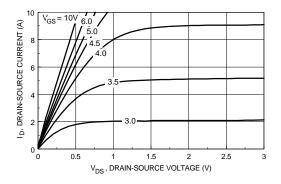


Figure 1. On-Region Characteristics.

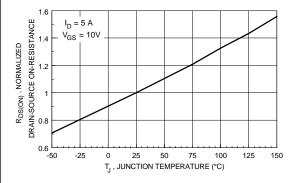


Figure 3. On-Resistance Variation with Temperature.

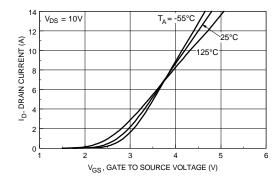


Figure 5. Transfer Characteristics.

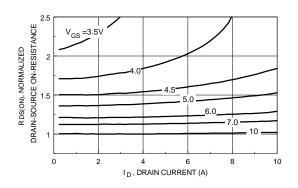


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

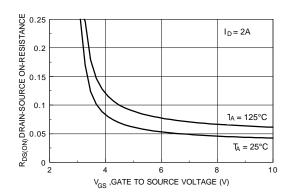


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

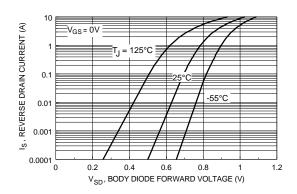


Figure 6. Body Diode Forward Voltage
Variation with Source Current
and Temperature.

#### **Typical Electrical Characteristics**

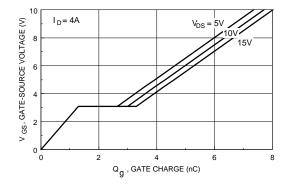


Figure 7. Gate Charge Characteristics.

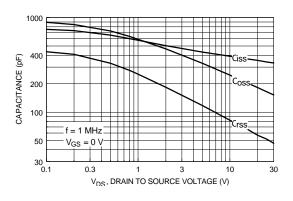


Figure 8. Capacitance Characteristics.

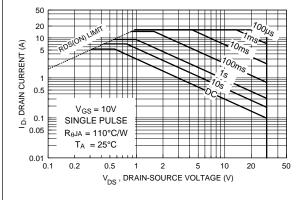


Figure 9. Maximum Safe Operating Area.

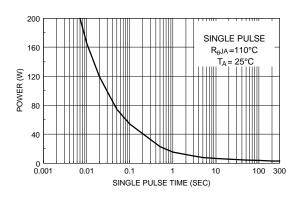


Figure 10. Single Pulse Maximum Power Dissipation.

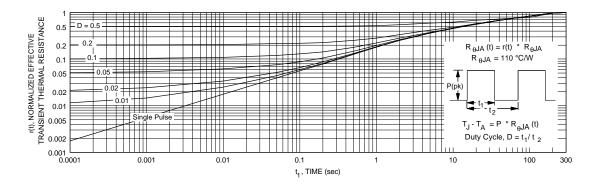


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

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