1 Gbps to 4.25 Gbps Limiting Amplifier With LOS and RSSI

FEATURES

- **Multi-Rate Operation from 1 Gbps up to 4.25 Gbps**
- **89-mW Power Consumption**
- **Input Offset Cancellation**
- **High Input Dynamic Range**
- **Output Disable**
- **CML Data Outputs**
- **Receive Signal Strength Indicator (RSSI)**
- **Loss of Signal Detection**
- **Polarity Select**
- **Single 3.3-V Supply**
- **Surface Mount Small Footprint 3-mm × 3-mm 16-Pin QFN Package**

APPLICATIONS

- **Cable Driver and Receiver**
- **1.0625 Gbps, 2.125 Gbps, and 4.25 Gbps Fibre Channel Receivers**
- **Gigabit Ethernet Receivers**

DESCRIPTION

The ONET4251PA is a versatile high-speed limiting amplifier for copper cable and fiber optic applications with data rates up to 4.25 Gbps.

This device provides a gain of about 50 dB, which ensures a full 800-mV_{p-p} differential output swing over its wide input signal dynamic range.

The high input signal dynamic range ensures low jitter output signals even when overdriven with input signal swings as high as 1200 mV_{p-p}.

The ONET4251PA comprises a loss of signal detection as well as a received signal strength indicator.

The part is available in a small footprint 3-mm × 3-mm 16-pin QFN package. It requires a single 3.3-V supply.

This power efficient limiting amplifier dissipates less than 89 mW typical. It is characterized for operation from –40°C to 85°C.

BLOCK DIAGRAM

A simplified block diagram of the ONET4251PA is shown in Figure 1.

This compact 3.3 V, low power 4.25 Gbps limiting amplifier consists of a high-speed data path with offset cancellation block, a loss of signal and RSSI detection block, and a bandgap voltage reference and bias current generation block.

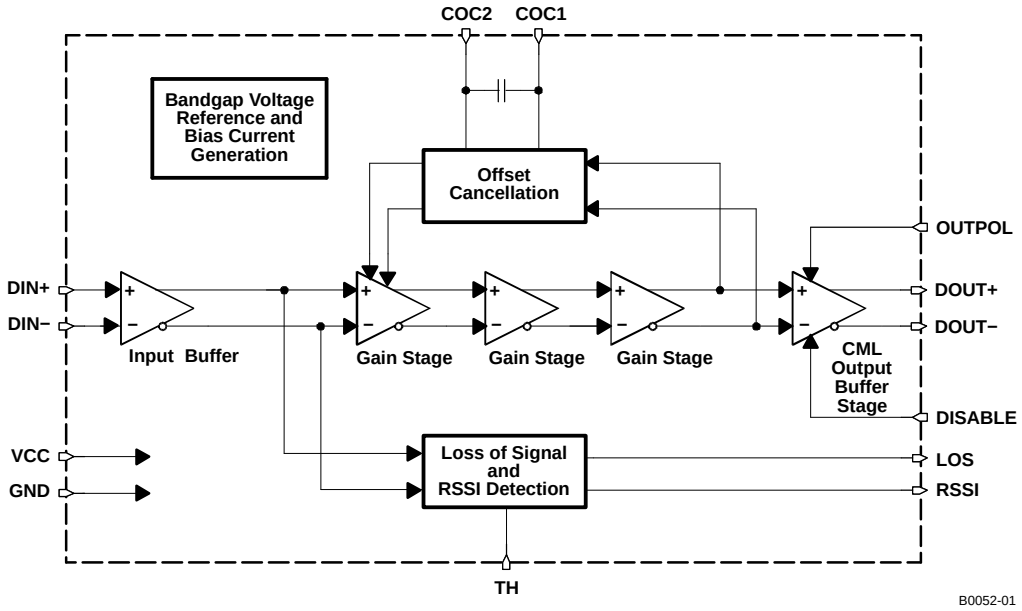


Figure 1. Simplified Block Diagram of the ONET4251PA

HIGH SPEED DATA PATH

The high-speed data signal is applied to the data path by means of the input signal pins DIN+/DIN–. The data path consists of the input stage with $2 \times 50\text{-}\Omega$ on-chip line termination to VCC, three gain stages, which provide the required typical gain of about 50 dB, and a CML output stage. The amplified data output signal is available at the output pins DOUT+/DOUT–, which provide $2 \times 50\text{-}\Omega$ back-termination to VCC. The output stage also includes a data polarity switching function, which is controlled by the OUTPOL input, and a disable function, controlled by the signal applied to the *DISABLE* input pin.

An offset cancellation compensates for internal offset voltages and thus ensures proper operation even for very small input data signals.

The low frequency cutoff is typically as low as 50 kHz with the built-in filter capacitor.

For applications which require even lower cutoff frequencies, an additional external filter capacitor may be connected to the COC1/COC2 pins.

LOSS OF SIGNAL AND RSSI DETECTION

The output signal of the input buffer is monitored by the loss of signal and RSSI detection circuitry. In this block, a signal is generated that is linear proportional to the input amplitude over a wide input voltage range. This signal is available at the RSSI output pin.

Furthermore, this circuit block compares the input signal to a threshold which can be programmed by means of an external resistor connected to the TH pin. If the input signal falls below the specified threshold, a loss of signal is indicated at the LOS pin.

The relation between the LOS assert voltage V_{AST} (in $mV_{p\text{-}p}$) and the external resistor R_{TH} (in $k\Omega$) connected to the TH pin can be approximated as given below:

$$R_{TH} \approx \frac{22.4\ k\Omega}{\left(V_{AST}/mV_{p-p} - 1\right)} + 560\ \Omega \quad (1)$$

$$V_{AST} \approx \frac{22.4\ mV_{p-p}}{R_{TH}/k\Omega - 0.56} + 1\ mV_{p-p} \quad (2)$$

BANDGAP VOLTAGE AND BIAS GENERATION

The ONET4251PA limiting amplifier is supplied by a single 3.3-V ±10% supply voltage connected to the VCC pins. This voltage is referred to ground (GND).

An on-chip bandgap voltage circuitry generates a supply voltage independent reference from which all other internally required voltages and bias currents are derived.

PACKAGE

For the ONET4251PA a small footprint 3-mm × 3-mm 16-pin QFN package, with a lead pitch of 0,5 mm is used. The pin out is shown in Figure 2.

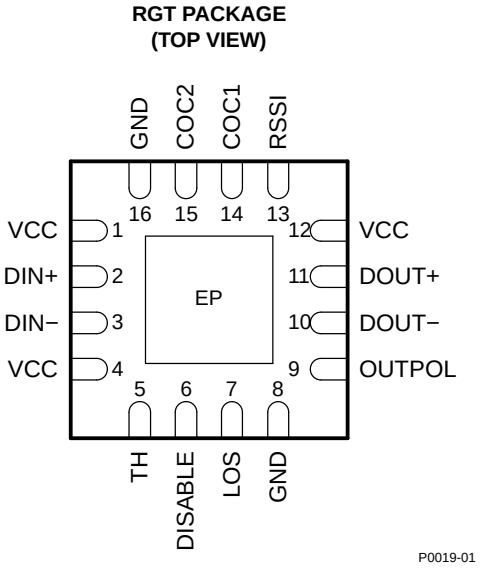


Figure 2. Pinout of ONET4251PA in a 3 mm x 3 mm 16-Pin QFN Package (Top View)

TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NO.	NAME		
1, 4, 12	VCC	supply	3.3-V ±10% supply voltage
2	DIN+	analog-in	Non-inverted data input. On-chip 50-Ω terminated to VCC.
3	DIN-	analog-in	Inverted data input. On-chip 50-Ω terminated to VCC.
5	TH	analog-in	LOS threshold adjustment with resistor to GND.
6	DISABLE	CMOS-in	Disables CML output stage when set to high level.
7	LOS	CMOS-out	High level indicates that the input signal amplitude is below the programmed threshold level.
8, 16, EP	GND	supply	Circuit ground. Exposed die pad (EP) must be grounded.
9	OUTPOL	CMOS-in	Output data signal polarity select (internally pulled high). Setting to a high level or leaving the pin open selects normal polarity. Low level selects inverted polarity.
10	DOUT-	CML-out	Inverted data output. On-chip 50-Ω back-terminated to VCC.
11	DOUT+	CML-out	Non-inverted data output. On-chip 50-Ω back-terminated to VCC

TERMINAL FUNCTIONS (continued)

TERMINAL		TYPE	DESCRIPTION
NO.	NAME		
13	RSSI	analog-out	Analog output voltage proportional to the input data amplitude. Indicates the strength of the received signal (RSSI).
14	COC1	analog	Offset cancellation filter capacitor terminal 1. Connect an additional filter capacitor between this pin and COC2 (pin 15). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15).
15	COC2	analog	Offset cancellation filter capacitor terminal 2. Connect an additional filter capacitor between this pin and COC1 (pin 14). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE/UNIT
V_{CC}	Supply voltage (2)	–0.3 V to 4 V
V_{DIN+}, V_{DIN-}	Voltage at DIN+, DIN–(2)	0.5 V to 4 V
V_{TH}, $V_{DISABLE}$, V_{LOS}, V_{OUTPOL}, V_{DOUT+}, $V_{DOUT–}$, V_{RSSI}, V_{COC1}, V_{COC2}	Voltage at TH, DISABLE, LOS, OUTPOL, DOUT+, DOUT-, RSSI, COC1, COC2 (2)	–0.3 V to 4 V
$V_{COC,DIFF}$	Differential voltage between COC1 and COC2	±1 V
$V_{DIN,DIFF}$	Differential voltage between DIN+ and DIN–	±2.5 V
I_{LOS}	Current into LOS	– 1 to 9 mA
I_{DIN+}, $I_{DIN–}$, I_{DOUT+}, $I_{DOUT–}$	Continuous current at inputs and outputs	–25 mA to 25 mA
ESD	ESD rating at all pins	2 kV (HBM)
$T_{J(max)}$	Maximum junction temperature	125°C
T_{STG}	Storage temperature range	–65 to 85°C
T_A	Characterized free-air operating temperature range	–40 to 85°C
T_{LEAD}	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	3.0	3.3	3.6	V
T_A	Operating free-air temperature	–40		85	°C
V_{IH}	CMOS input high voltage	2.1			V
V_{IL}	CMOS input low voltage			0.6	V

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
I_{VCC}	Supply current	*DISABLE* = low (excludes CML output current)		27	40	mA
V_{OD}	Differential data output voltage swing	DISABLE = high		0.25	10	mV_{p-p}
		DISABLE = low	600	760	1200	
R_{IN}, R_{OUT}	Data input/output resistance	Single-ended		50		Ω
V_{RSSI}	RSSI output voltage	Input = 8 mV_{p-p}, $R_{RSSI} \geq 10$ kΩ		180		mV
		Input = 80 mV_{p-p}, $R_{RSSI} \geq 10$ kΩ		1900		
	RSSI Linearity	8 $mV_{p-p} \leq V_{IN} \leq 80$ mV_{p-p}		±3%		
$V_{IN(MIN)}$	Minimum data input voltage				50	mV_{p-p}
$V_{IN(MAX)}$	Data input overload		1200			mV_{p-p}
	LOS high voltage	I_{SOURCE} = 30 µA	2.4			V
	LOS low voltage	I_{SINK} = 1 mA			0.4	V

AC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted), typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Low frequency –3 dB bandwidth	C_{OC} = open		50		kHz
		C_{OC} = 0.1 µF		0.8		
	Data rate		4.25			Gb/s
v_{NI}	Input referred noise			230		$µV_{RMS}$
DJ	Deterministic jitter	K28.5 pattern at 4.25 Gbps		6	19	ps_{p-p}
		K28.5 pattern at 2.125 Gbps		8	22	
		K28.5 pattern at 1.0625 Gbps		11	28	
RJ	Random jitter	Input = 50 mVpp		1		ps_{RMS}
t_r	Output rise time	20% to 80%		35	70	ps
t_f	Output fall time	20% to 80%		35	70	ps
	LOS hysteresis	K28.5 pattern at 4.25 Gbps	2.5	4.5		dB
R_{TH}	LOS threshold adjustment resistor	See (1)		4		kΩ
V_{AST}	LOS assert voltage	R_{TH} = 4 kΩ K28.5 pattern at 4.25 Gbps	3	7		mV_{p-p}
V_{DEA}	LOS deassert voltage	R_{TH} = 4 kΩ K28.5 pattern at 4.25 Gbps		11	50	mV_{p-p}
t_{LOS}	LOS assert/deassert time		2		100	µs
t_{DIS}	Disable response time			20		ns

(1) For a given external resistor connected to the TH pin, the LOS assert voltage value may vary due to part-to-part variations. If high precision is required, adjustment of this resistor for each device is mandatory.

TYPICAL CHARACTERISTICS

Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted).

OUTPUT EYE-DIAGRAM AT 4.25 GBPS AND MINIMUM INPUT VOLTAGE (50 mV_{p-p})

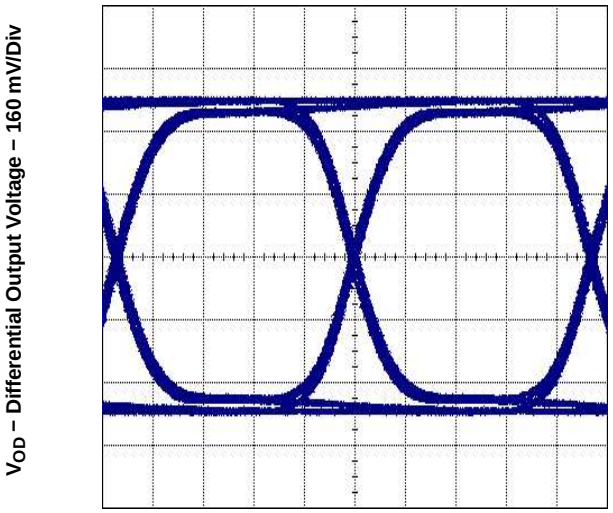


Figure 3.

OUTPUT EYE-DIAGRAM AT 4.25 GBPS AND MAXIMUM INPUT VOLTAGE (1200 mV_{p-p})

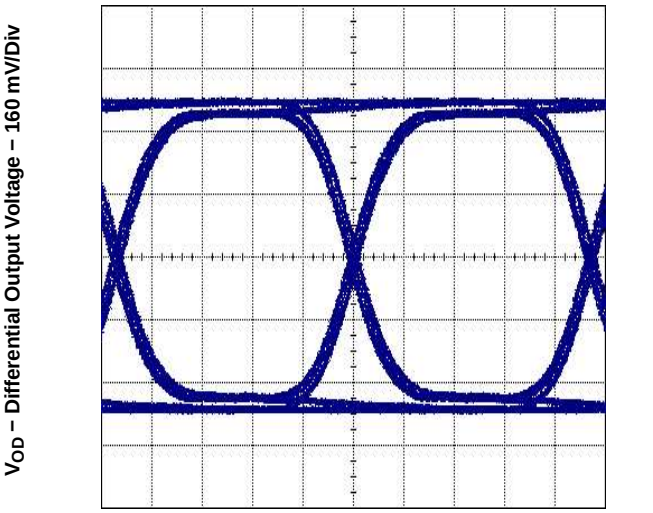


Figure 4.

OUTPUT EYE-DIAGRAM AT 4.25 GBPS AND 85°C AND MINIMUM INPUT VOLTAGE (50 mV_{p-p})

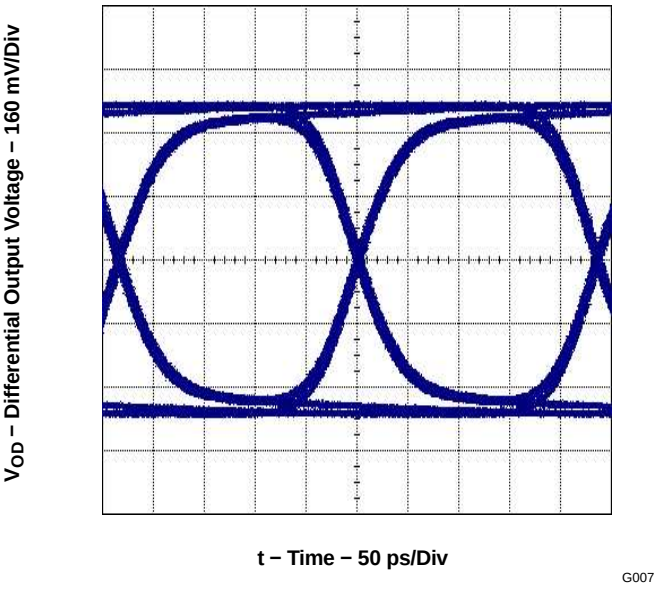


Figure 5.

FREQUENCY RESPONSE

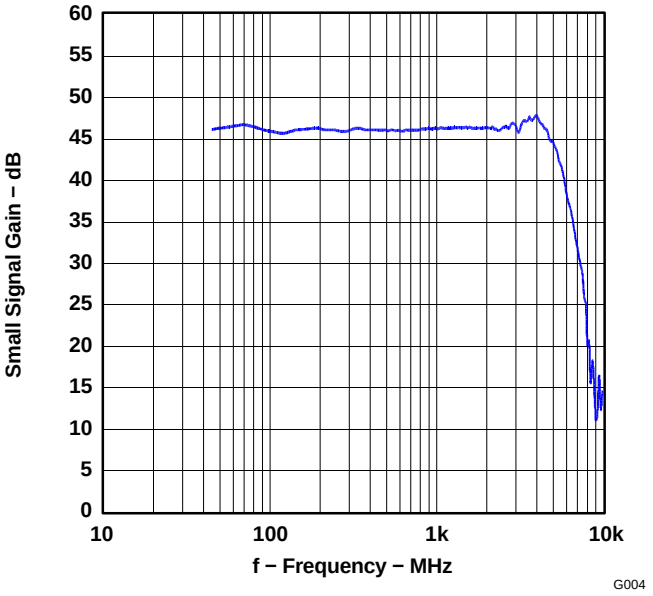


Figure 6.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted).

OUTPUT EYE-DIAGRAM AT 2.125 GBPS AND MINIMUM INPUT VOLTAGE (50 mV_{p-p})

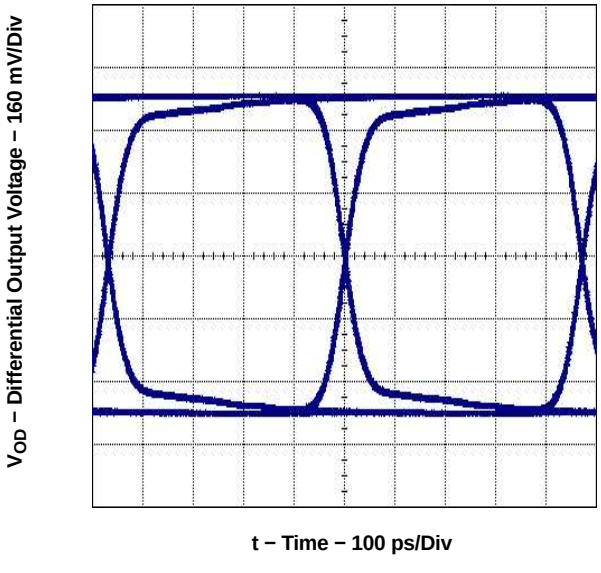


Figure 7.

OUTPUT EYE-DIAGRAM AT 2.125 GBPS AND MAXIMUM INPUT VOLTAGE (1200 mV_{p-p})

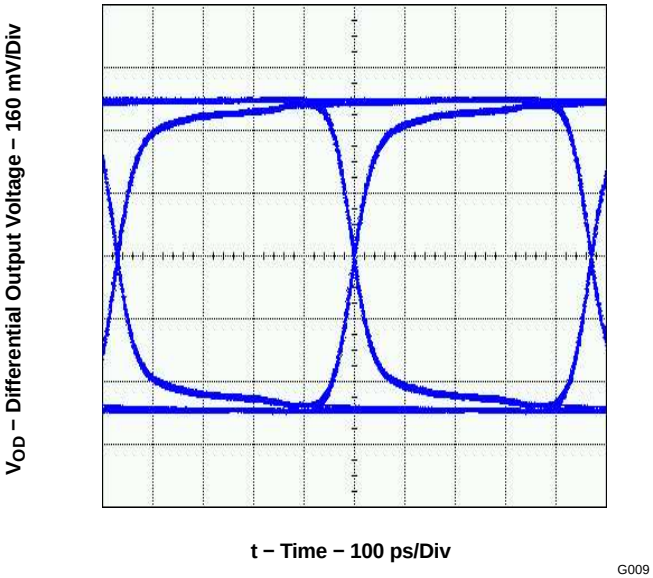


Figure 8.

OUTPUT EYE-DIAGRAM AT 1.0625 GBPS AND MINIMUM INPUT VOLTAGE (50 mV_{p-p})

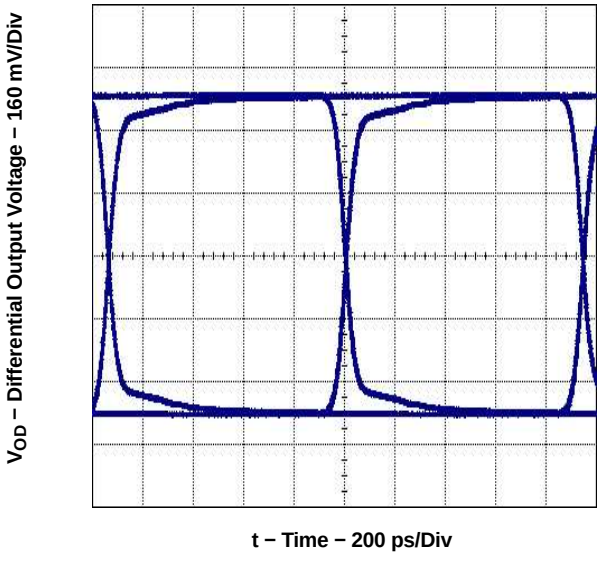


Figure 9.

OUTPUT EYE-DIAGRAM AT 1.0625 GBPS AND MAXIMUM INPUT VOLTAGE (1200 mV_{p-p})

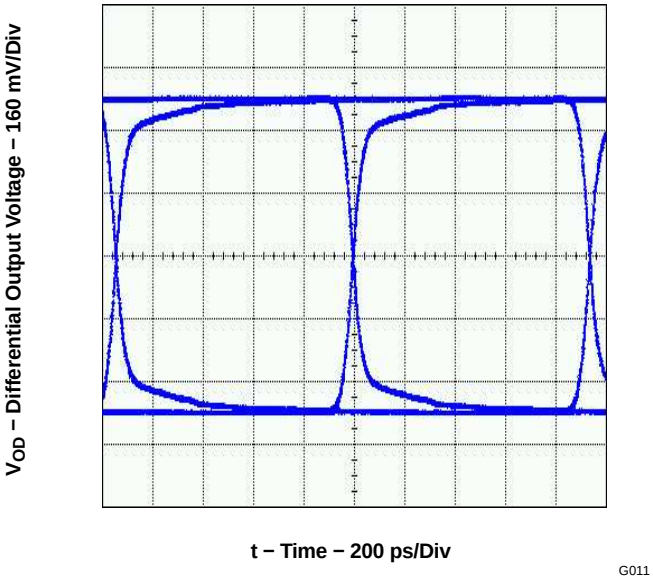


Figure 10.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted).

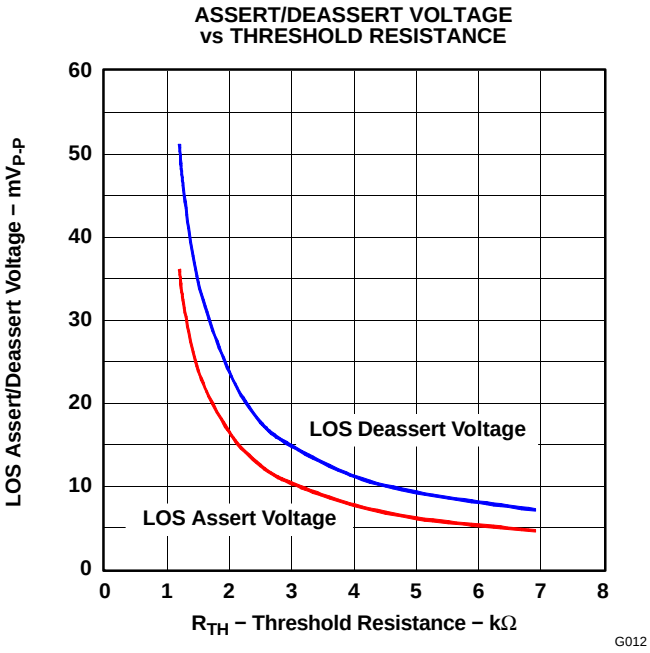


Figure 11.

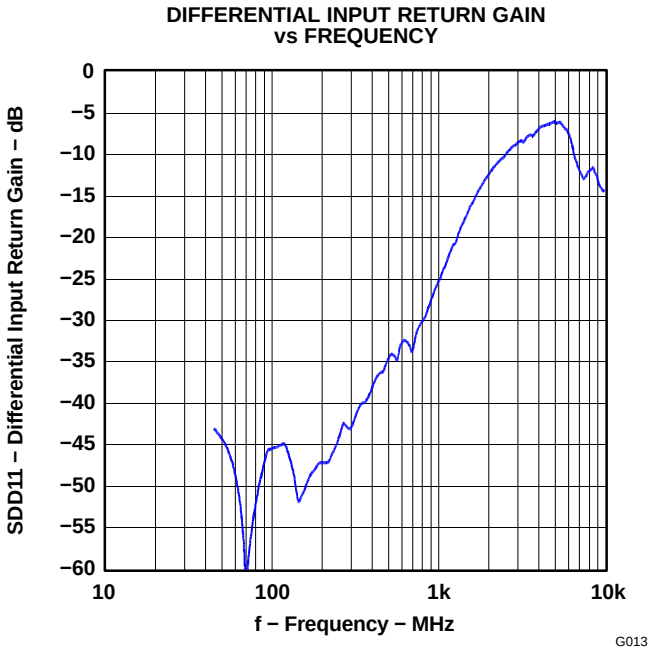


Figure 12.

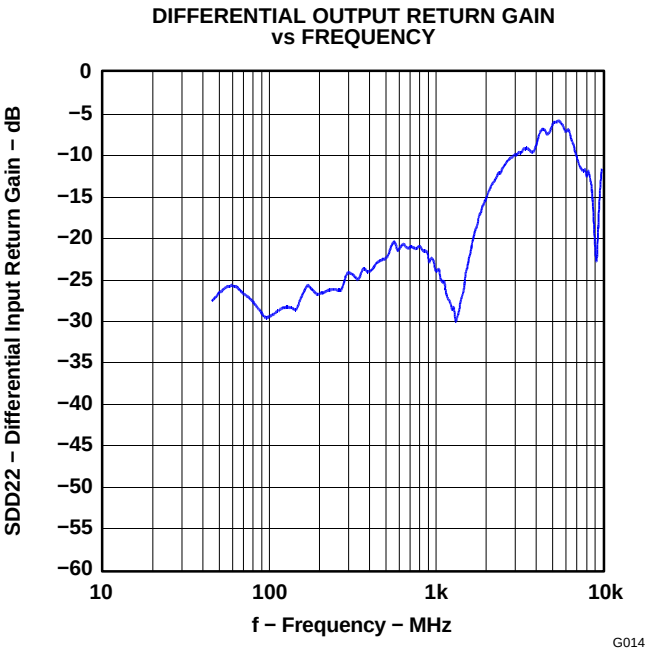


Figure 13.

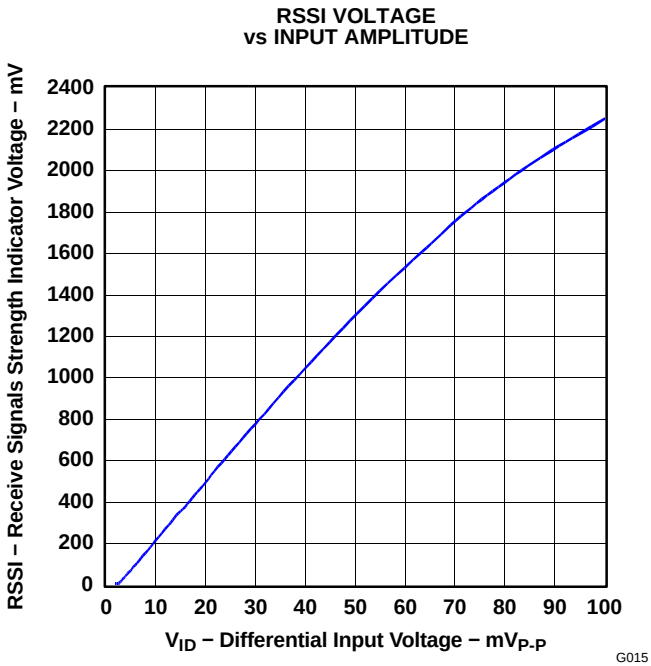


Figure 14.

APPLICATION INFORMATION

Figure 15 shows the ONET4251PA connected with an ac-coupled interface to the data signal source as well as to the output load.

Besides the ac-coupling capacitors C_1 through C_4 in the input and output data signal lines, the only required external component is the LOS threshold setting resistor R_{TH}. In addition, if a low cutoff frequency is required, as an option, an external filter capacitor C_{OC} may be used.

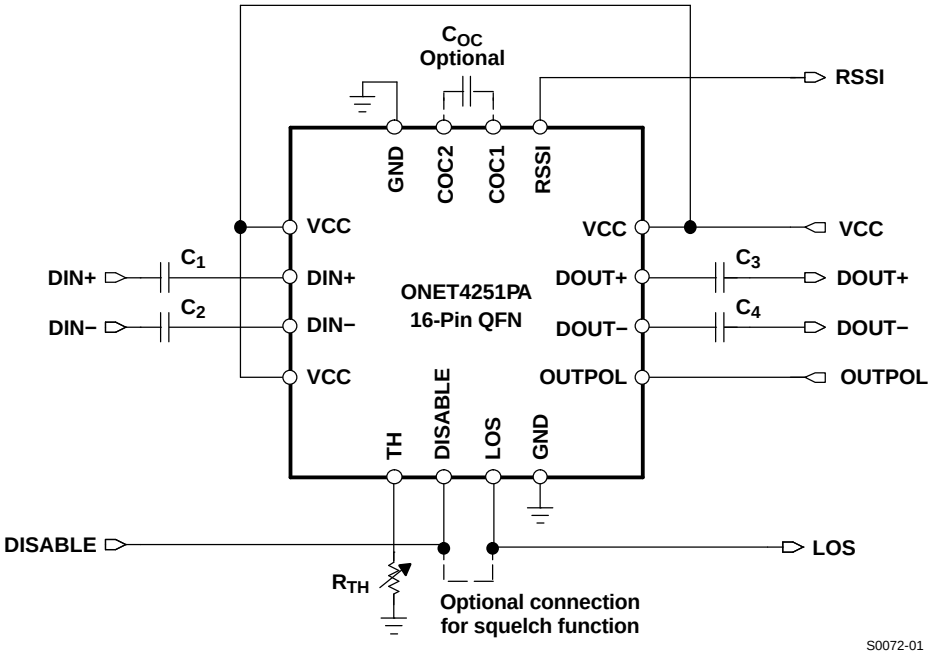


Figure 15. Basic Application Circuit With AC Coupled I/Os

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ONET4251PARGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ONET4251PARGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ONET4251PARGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ONET4251PARGTTG4	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

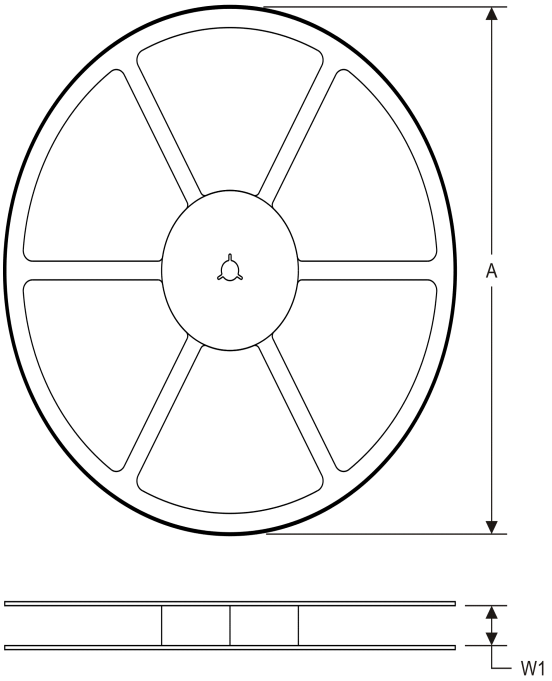
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

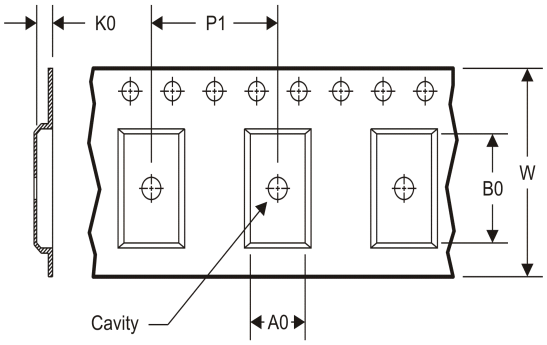
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



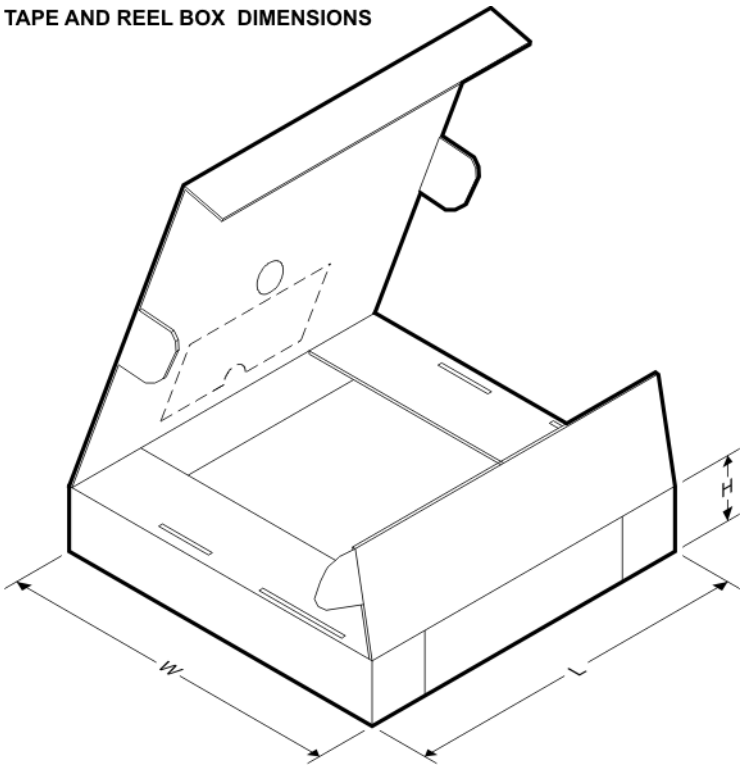
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ONET4251PARGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ONET4251PARGTT	QFN	RGT	16	250	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

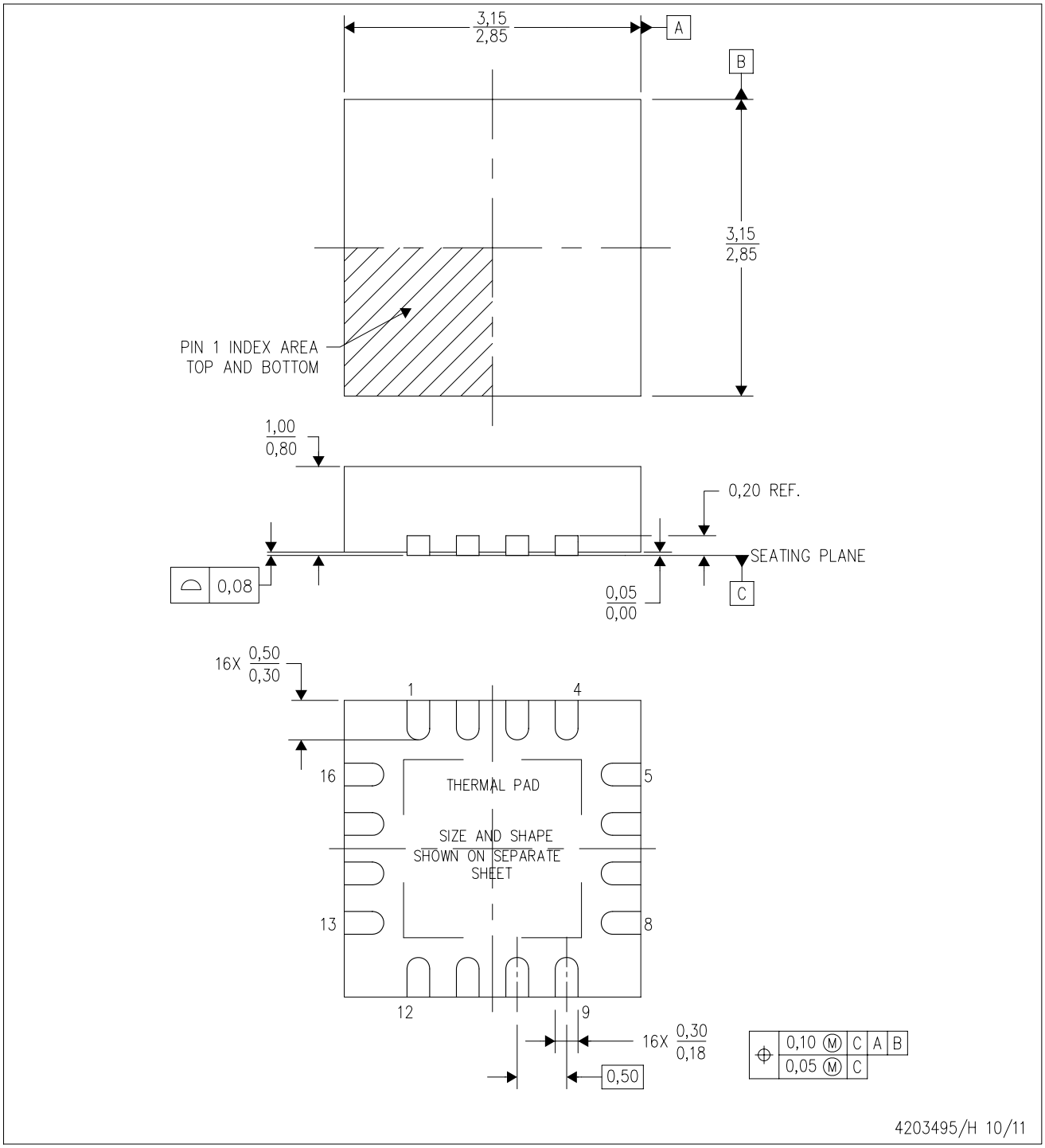
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ONET4251PARGTR	QFN	RGT	16	3000	338.1	338.1	20.6
ONET4251PARGTT	QFN	RGT	16	250	338.1	338.1	20.6

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

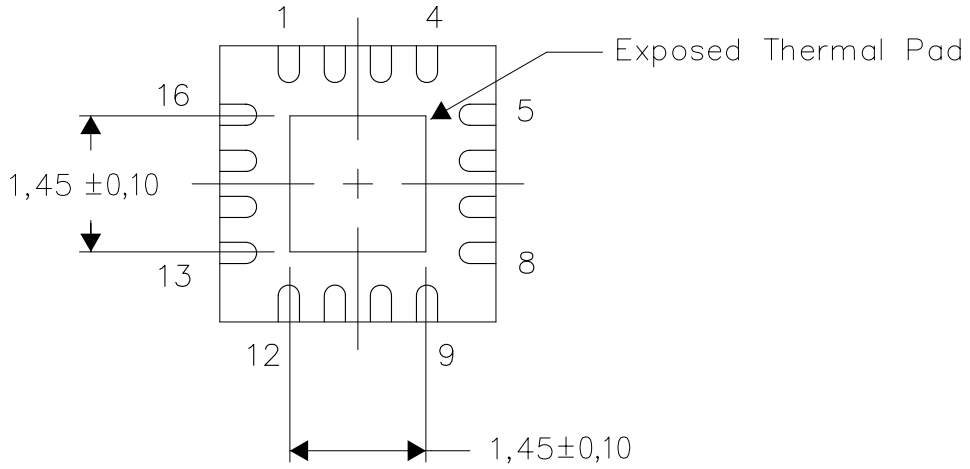
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



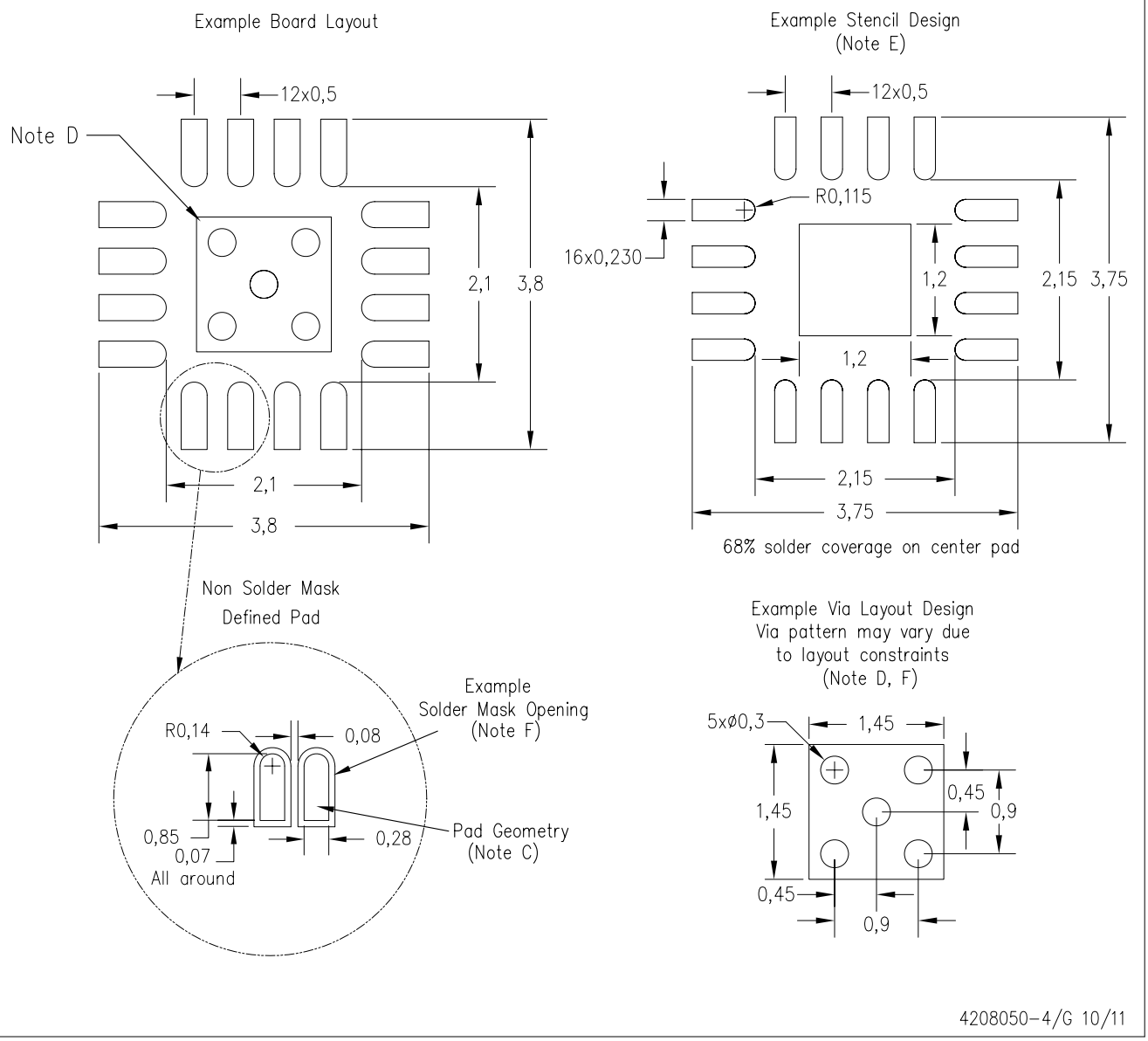
Bottom View

Exposed Thermal Pad Dimensions

4206349–2/Q 10/11

NOTE: All linear dimensions are in millimeters

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург, Промышленная ул, дом № 19, литера Н, помещение 100-Н Офис 331