

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## 74HC/HCT564

Octal D-type flip-flop; positive-edge trigger; 3-state; inverting

Product specification  
File under Integrated Circuits, IC06

December 1990

# Octal D-type flip-flop; positive-edge trigger; 3-state; inverting

## 74HC/HCT564

### FEATURES

- 3-state inverting outputs for bus oriented applications
- 8-bit positive-edge triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT564 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT564 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ( $\overline{OE}$ ) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When  $\overline{OE}$  is LOW, the contents of the 8 flip-flops are available at the outputs.

When  $\overline{OE}$  is HIGH, the outputs go to the high impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

The "564" is functionally identical to the "574" but has inverting outputs. The "564" is functionally identical to the "534", but has a different pinning.

### QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

| SYMBOL                              | PARAMETER                                   | CONDITIONS                                    | TYPICAL |     | UNIT |
|-------------------------------------|---------------------------------------------|-----------------------------------------------|---------|-----|------|
|                                     |                                             |                                               | HC      | HCT |      |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay CP to $\overline{Q}_n$    | C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V | 15      | 16  | ns   |
| f <sub>max</sub>                    | maximum clock frequency                     |                                               | 127     | 62  | MHz  |
| C <sub>I</sub>                      | input capacitance                           |                                               | 3.5     | 3.5 | pF   |
| C <sub>PD</sub>                     | power dissipation capacitance per flip-flop | notes 1 and 2                                 | 27      | 27  | pF   |

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>; for HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

### ORDERING INFORMATION

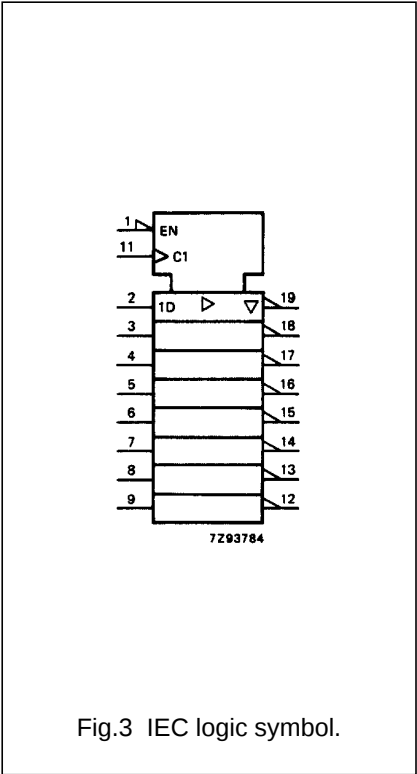
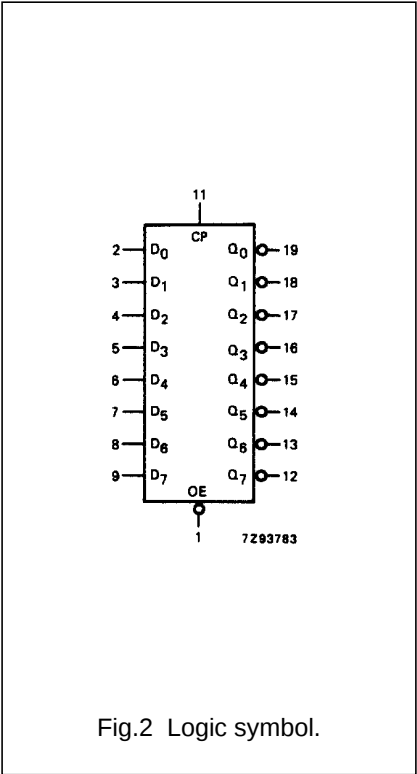
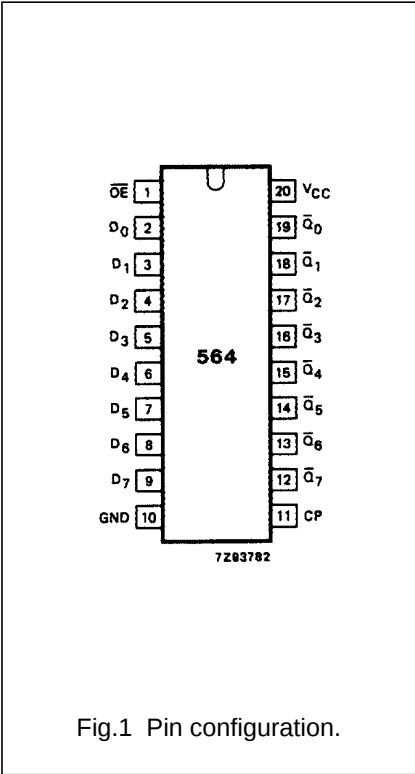
See "74HC/HCT/HCU/HCMOS Logic Package Information".

Octal D-type flip-flop; positive-edge trigger;  
3-state; inverting

74HC/HCT564

PIN DESCRIPTION

| PIN NO.                        | SYMBOL                               | NAME AND FUNCTION                         |
|--------------------------------|--------------------------------------|-------------------------------------------|
| 1                              | $\overline{OE}$                      | 3-state output enable input (active LOW)  |
| 2, 3, 4, 5, 6, 7, 8, 9         | D <sub>0</sub> to D <sub>7</sub>     | data inputs                               |
| 10                             | GND                                  | ground (0 V)                              |
| 11                             | CP                                   | clock input (LOW-to-HIGH, edge-triggered) |
| 19, 18, 17, 16, 15, 14, 13, 12 | $\overline{Q_0}$ to $\overline{Q_7}$ | 3-state flip-flop outputs                 |
| 20                             | V <sub>CC</sub>                      | positive supply voltage                   |



Octal D-type flip-flop; positive-edge trigger;  
3-state; inverting

74HC/HCT564

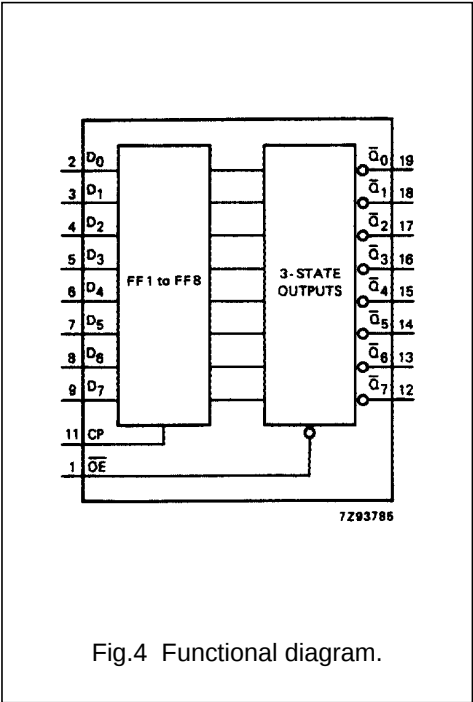


Fig.4 Functional diagram.

FUNCTION TABLE

| OPERATING<br>MODES                   | INPUTS          |    |                | INTERNAL<br>FLIP-FLOPS | OUTPUTS                              |
|--------------------------------------|-----------------|----|----------------|------------------------|--------------------------------------|
|                                      | $\overline{OE}$ | CP | D <sub>n</sub> |                        | $\overline{Q_0}$ to $\overline{Q_7}$ |
| load and read<br>register            | L               | ↑  | l              | L                      | H                                    |
|                                      | L               | ↑  | h              | H                      | L                                    |
| load register and<br>disable outputs | H               | ↑  | l              | L                      | Z                                    |
|                                      | H               | ↑  | h              | H                      | Z                                    |

Notes

- 1. H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
L = LOW voltage level  
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
Z = high impedance OFF-state  
↑ = LOW-to-HIGH clock transition

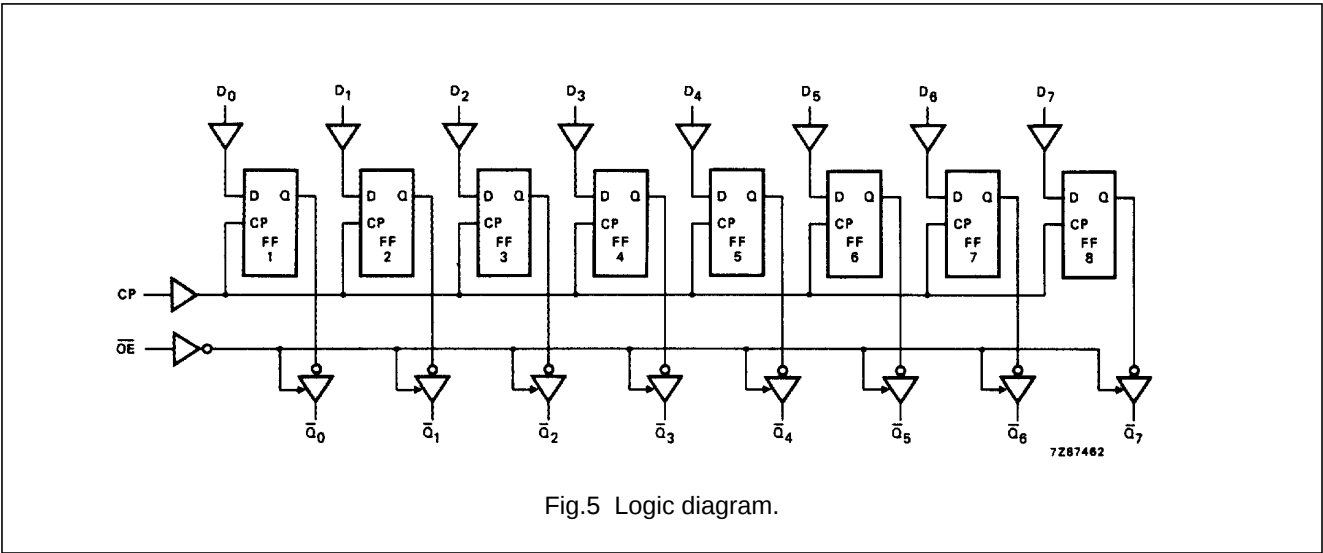


Fig.5 Logic diagram.

# Octal D-type flip-flop; positive-edge trigger; 3-state; inverting

74HC/HCT564

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER                                              | T <sub>amb</sub> (°C) |                  |                 |                 |                 |                 |                 | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|--------------------------------------------------------|-----------------------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|------|------------------------|-----------|
|                                     |                                                        | 74HC                  |                  |                 |                 |                 |                 |                 |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |                                                        | +25                   |                  |                 | −40 to +85      |                 | −40 to +125     |                 |      |                        |           |
|                                     |                                                        | min.                  | typ.             | max.            | min.            | max.            | min.            | max.            |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>CP to Q <sub>n</sub>              |                       | 50<br>18<br>14   | 165<br>33<br>28 |                 | 205<br>41<br>35 |                 | 250<br>50<br>43 | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |
| t <sub>PZH</sub> / t <sub>PZL</sub> | 3-state output enable<br>time<br>OE to Q <sub>n</sub>  |                       | 44<br>16<br>13   | 140<br>28<br>24 |                 | 175<br>35<br>30 |                 | 210<br>42<br>36 | ns   | 2.0<br>4.5<br>6.0      | Fig.8     |
| t <sub>PHZ</sub> / t <sub>PLZ</sub> | 3-state output disable<br>time<br>OE to Q <sub>n</sub> |                       | 50<br>18<br>14   | 135<br>27<br>23 |                 | 170<br>34<br>29 |                 | 205<br>41<br>35 | ns   | 2.0<br>4.5<br>6.0      | Fig.8     |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                                 |                       | 14<br>5<br>4     | 60<br>12<br>10  |                 | 75<br>15<br>13  |                 | 90<br>18<br>15  | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |
| t <sub>W</sub>                      | clock pulse width<br>HIGH or LOW                       | 80<br>16<br>14        | 14<br>5<br>4     |                 | 100<br>20<br>17 |                 | 120<br>24<br>20 |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |
| t <sub>su</sub>                     | set-up time<br>D <sub>n</sub> to CP                    | 60<br>12<br>10        | 6<br>2<br>2      |                 | 75<br>15<br>13  |                 | 90<br>18<br>15  |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>h</sub>                      | hold time<br>D <sub>n</sub> to CP                      | 5<br>5<br>5           | 0<br>0<br>0      |                 | 5<br>5<br>5     |                 | 5<br>5<br>5     |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| f <sub>max</sub>                    | maximum clock pulse<br>frequency                       | 6.0<br>30<br>35       | 38<br>115<br>137 |                 | 4.8<br>24<br>28 |                 | 4.0<br>20<br>24 |                 | MHz  | 2.0<br>4.5<br>6.0      | Fig.6     |

# Octal D-type flip-flop; positive-edge trigger; 3-state; inverting

74HC/HCT564

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT                            | UNIT LOAD COEFFICIENT |
|----------------------------------|-----------------------|
| $\overline{OE}$                  | 0.80                  |
| D <sub>0</sub> to D <sub>7</sub> | 0.25                  |
| CP                               | 1.00                  |

## AC CHARACTERISTICS FOR 74HCT

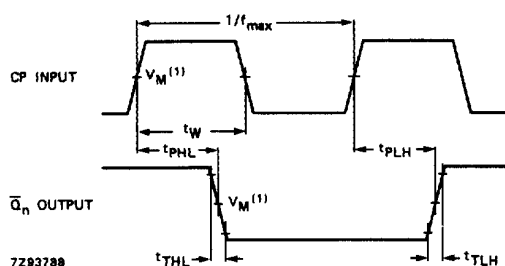
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER                                                          | T <sub>amb</sub> (°C) |      |      |            |      |             |      | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|--------------------------------------------------------------------|-----------------------|------|------|------------|------|-------------|------|------|------------------------|-----------|
|                                     |                                                                    | 74HCT                 |      |      |            |      |             |      |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |                                                                    | +25                   |      |      | −40 to +85 |      | −40 to +125 |      |      |                        |           |
|                                     |                                                                    | min.                  | typ. | max. | min.       | max. | min.        | max. |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>CP to $\overline{Q}_n$                        |                       | 19   | 35   |            | 44   |             | 53   | ns   | 4.5                    | Fig.6     |
| t <sub>PZH</sub> / t <sub>PZL</sub> | 3-state output enable<br>time $\overline{OE}$ to $\overline{Q}_n$  |                       | 19   | 35   |            | 44   |             | 53   | ns   | 4.5                    | Fig.8     |
| t <sub>PHZ</sub> / t <sub>PLZ</sub> | 3-state output disable<br>time $\overline{OE}$ to $\overline{Q}_n$ |                       | 19   | 30   |            | 38   |             | 45   | ns   | 4.5                    | Fig.8     |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                                             |                       | 5    | 12   |            | 15   |             | 18   | ns   | 4.5                    | Fig.6     |
| t <sub>W</sub>                      | clock pulse width<br>HIGH or LOW                                   | 18                    | 8    |      | 23         |      | 27          |      | ns   | 4.5                    | Fig.6     |
| t <sub>su</sub>                     | set-up time<br>D <sub>n</sub> to CP                                | 12                    | 3    |      | 15         |      | 18          |      | ns   | 4.5                    | Fig.7     |
| t <sub>h</sub>                      | hold time<br>D <sub>n</sub> to CP                                  | 3                     | −2   |      | 3          |      | 3           |      | ns   | 4.5                    | Fig.7     |
| f <sub>max</sub>                    | maximum clock pulse<br>frequency                                   | 27                    | 56   |      | 22         |      | 18          |      | MHz  | 4.5                    | Fig.6     |

# Octal D-type flip-flop; positive-edge trigger; 3-state; inverting

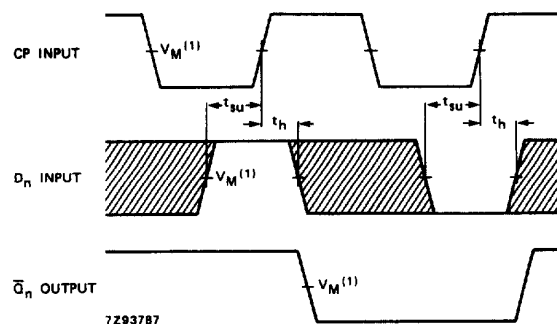
74HC/HCT564

## AC WAVEFORMS



- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

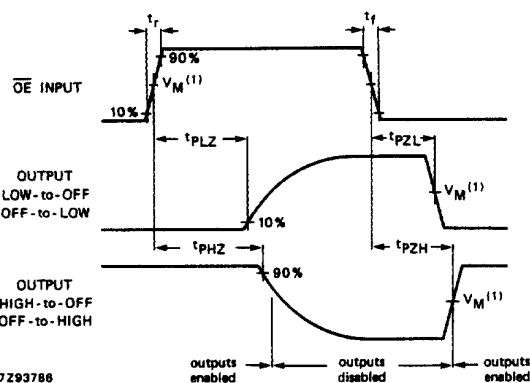
Fig.6 Waveforms showing the clock (CP) to output ( $\overline{Q}_n$ ) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.



The shaded areas indicate when the input is permitted to change for predictable output performance.

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.7 Waveforms showing the data set-up and hold times for the data input ( $D_n$ ).



- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.8 Waveforms showing the 3-state enable and disable times.

## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".



**Стандарт  
Электрон  
Связь**

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

**Наши контакты:**

**Телефон:** +7 812 627 14 35

**Электронная почта:** [sales@st-electron.ru](mailto:sales@st-electron.ru)

**Адрес:** 198099, Санкт-Петербург,  
Промышленная ул, дом № 19, литера Н,  
помещение 100-Н Офис 331