DEMO9S08DZ60

Demonstration Board for Freescale MC9S08DZ60

Axiom Manufacturing • 2813 Industrial Lane • Garland, TX 75041
Email: Sales@axman.com Web: http://www.axman.com

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REVISION

Date	Rev	Comments
December 2, 2006	A	Initial Release

CAUTIONARY NOTES

1) Electrostatic Discharge (ESD) prevention measures should be used when handling this product. ESD damage is not a warranty repair item.

2) Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

3) 3) EMC Information on the DEMO9S08DZ60 board:

   a) This product as shipped from the factory with associated power supplies and cables, has been verified to meet with requirements of CE and the FCC as a CLASS A product.

   b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

   c) In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate prevention measures.

   d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may effect its performance and cause interference with nearby electronic equipment. If such interference is detected, suitable mitigating measures should be taken.

TERMINOLOGY

This development module utilizes option select jumpers to configure default board operation. Terminology for application of the option jumpers is as follows:

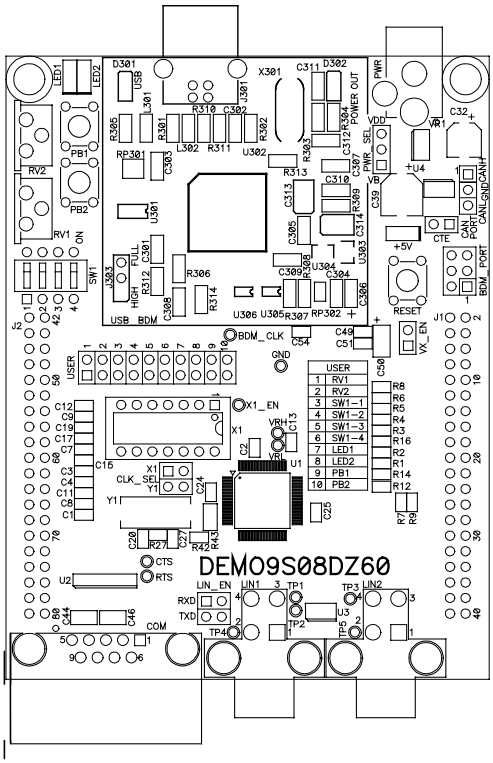
Jumper – a plastic shunt that connects 2 terminals electrically

Jumper on, in, or installed - jumper is installed such that 2 pins are connected together

Jumper off, out, or idle - jumper is installed on 1 pin only. It is recommended that jumpers be idled by installing on 1 pin so they will not be lost.

FEATURES

The DEMO9S08DZ60 is a demonstration board for the MC9S08DZ60 microcontroller. Application development is quick and easy with the integrated USB-BDM, sample software tools, and examples. An optional BDM_PORT port is also provided to allow use of a BDM_PORT cable. Two, 40-pin connectors provide access to all IO signals on the target MCU.



- MC9S08DZ60, 64 LQFP
- 32K Bytes Flash
- 4K Bytes RAM
- 2K Bytes EEPROM
- Timing Sources
- 4 MHz XTAL
- OSC socket
- BNC connector
- Integrated P&E USB-BDM
- BDM_PORT header for BDM cable support (not installed)
- LIN PHY w/ 2, 4-pos Molex connectors
- HS-CAN PHY w/ 3-pos pin header connector
- LP Filters on ADC inputs
- 2 ea., MCU_PORT socket headers for access to MCU IO signals
- On-board +5V regulator
- Optional Power from USB-BDM or MCU_PORT connector
- Power Input Selection Jumpers
- Power input from USB-BDM
- Power input from on-board regulator
- Power input from Connector J1
- Optional Power output through Connector J1
- User Components Provided
- 3 Push Switches; 2 User, 1 Reset
- 1 4-pos DIP Switch
- 7 LED Indicators; 4 User, VDD, USB Power, USB Power Out
- 2ea. 5K ohm POTs w /LP Filter
- Jumpers
- Power Select
- VSEL
- VX_EN
- USER_EN
- Connectors
- 2 40-pin MCU I/O Connector
- 2.0mm Barrel Connector
- BDM_PORT
- USB Connectors
- DB9 Connector

Specifications:
Board Size 3.5” x 4.0”

Power Input: +6VDC to +18VDC

NOTE: LIN functionality supported when powered from PWR connector only

REFERENCES

Reference documents are provided on the support CD in Acrobat Reader format.

DEMO9S08DZ60_UG.pdf	DEMO9S08DZ60 User Guide (this document)
DEMO9S08DZ60_QSG.pdf	DEMO9S08DZ60 Quick Start Guide
DEMO9S08DZ60 _SCH_B.pdf	DEMO9S08DZ60 Schematic Rev. B
DEMO9S08DZ60_Silk_B.pdf	DEMO9S08DZ60 Top Silk, Rev B

GETTING STARTED

To get started quickly, please refer to the DEMO9S08DZ60 Quick Start Guide. This quick start will show the user how to connect the board to the PC, install the correct version of CodeWarrior Development Studio, and run a simple LED test program.

OPERATING MODES

The DEMO9S08DZ60 board operates in two operating modes: Run Mode, or Debug Mode. Run Mode executes the user application from Power-On or Reset. Debug Mode supports the development and debug of applications. See the related sections below for quickly starting the board in the desired operation mode.

RUN MODE

Run mode executes the user application when power is applied to the board or the RESET button is pressed. Use the following settings to configure the DEMO9S08DZ60 board for RUN Mode to get started quickly.

1. Connect auxiliary equipment to board as required by application.

2. Configure the board option jumpers for run mode.

Table 1: Run Mode Setup

PWR_SEL	Pin1 – Pin2 (VB)
CLK_SEL	Pin1 – Pin2 (Y1)
VX_EN	As Required
USER	As Required
LIN_EN	As Required

NOTE: See Power section below to configure power input from PWR connector or from J1 connector.

3. Apply power to the board.

4. The programmed application will begin to execute.

Debug Mode

Debug Mode supports application development and debug. Debug mode is available to the user through the integrated USB-Multilink BDM or through the use of an external HCS12/HCS08 BDM cable. Use of the integrated USB-Multilink BDM requires only a host PC with an available USB port and an A/B type USB cable. A 6-pin BDM interface header (BDM_PORT) supports the use of an external HCS12 BDM cable. The BDM_PORT header is not installed in default configuration. The steps below describe using the integrated USB-Multilink BDM.

1. Connect auxiliary equipment to board as required by application.
2. Install and launch P&E PKGHCS08Z tool set, CodeWarrior Development Studio, or other software capable of communicating with the HCS12/HCS08 MCU.
3. Configure the board option jumpers for DEBUG mode.

Table 2: BDM Mode Setup

PWR_SEL	Pin1 – Pin2 (VB)
CLK_SEL	Pin1 – Pin2 (Y1)
VX_EN	As Required
USER	As Required
LIN_EN	As Required

NOTE: Refer to the Development Support section below for details on using an external HCS12 BDM cable.

4. Connect the supplied USB cable between an available USB port on the host PC and the USB connector on the board.
5. Hosting development software will establish DEBUG communication.
6. Refer to BDM cable documentation for details on use of BDM.

MEMORY MAP

The table below shows the default memory map for the MC9S08DZ60 immediately out of reset.

Table 3: Memory Map

$0000 - $007F	REGISTERS	128 bytes
$0080 - $107F	RAM	4096 bytes
$1080 - $13FF	FLASH	896 bytes
$1400 - $17FF	EEPROM	2 x 1024 bytes
$1800 - $18FF	High Page Registers	256
$1900 - $FFFF	FLASH	59136 bytes

SOFTWARE DEVELOPMENT

Software development requires the use of an assembler or compiler supporting the HCS08 instruction set and a host PC operating a debug interface. CodeWarrior Development Studio and Axiom IDE for Windows for Debugging and Flash programming are supplied with this board.

DEVELOPMENT SUPPORT

Application development and debug for the target MC9S08DZ60 is supported through a background debug mode (BDM) interface. The BDM interface consists of an integrated USB-Multilink BDM and a 6-pin interface header (BDM_PORT) to connect a HCS12/HCS08 BDM cable.

Integrated BDM

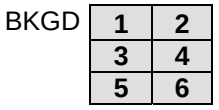
The DEMO9S08DZ60 board features an integrated USB-Multilink BDM from P&E Microcomputer Systems. The integrated USB-Multilink BDM supports application development and debugging via background debug mode. All necessary signals are provided by the integrated USB-Multilink BDM. A USB, type B, connector provides connection from the target board to the host PC.

The integrated USB-Multilink BDM provides +5V power and ground to target board eliminating the need to power the board externally. Power from the USB-Multilink BDM is derived from the USB bus; therefore, total current consumption for the target board, and connected circuitry, **must not exceed 500mA**. This current limit describes the current supplied by the USB cable to the BDM circuit, the target board, and any connected circuitry. Excessive current drain will violate the USB specification causing the bus to disconnect. Damage to the host PC USB hub or the target board may result.

BDM_PORT Header

A compatible HCS12 BDM cable can also attach to the 6-pin BDM interface header (BDM_PORT). This header is not installed in default configuration. The figure below shows the pin-out for the DEBUG header

Figure 1: BDM_PORT Header



See the HC(S)08 Reference Manual for complete DEBUG documentation

NOTE: This header is not installed in default configuration.

POWER

The DEMO9S08DZ60 is designed to allow the user to power the board through the USB-Multilink BDM during application development. A 2.0-mm barrel connector has been applied to support stand-alone operation and to support LIN functionality. The board may also be powered through connector J1. This connection may also be used to supply power from the board to external circuitry.

During application development, the board may be powered from either the USB-BDM or the PWR connector. To utilize LIN functionality, the board must be powered from PWR connector with a typical input voltage of +12VDC.

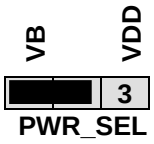
POWER SELECT

Power may be applied to the board through the integrated USB-Multilink BDM circuitry, a 2.0mm barrel connector, or through connector J1. Power selection is achieved using 2 selection headers: PWR_SEL option header and the VX_EN option header.

PWR_SEL

The PWR_SEL option header selects power input either from the integrated USB-Multilink BDM circuitry or from the on-board voltage regulator. The figure below details the PWR_SEL header connections.

Figure 2: PWR_SEL Option Header



CONFIGURATION

1 – 2: Selects power input from USB-ML12
2 – 3: Selects power input from on-board regulator or J1

NOTE: Set PWR_SEL jumper to VB during application development. Use barrel connector input (PWR) to support LIN functionality if needed.

Power from the integrated BDM is drawn from the USB bus and is limited to **500 mA**. This current limit accounts for the total current supplied over the USB cable to the BDM circuit, the target board, and any connected circuitry. Current drain in excess of 500 mA will violate the USB specification and will cause the USB bus to disconnect. Damage to the host PC or the target board may also result.

The on-board voltage regulator (VR1) accepts power input through a 2.0mm barrel connector (PWR). Input voltage may range from +6V to +18V. The voltage regulator (VR1) provides a +5V fixed output limited to 250mA. Over-temperature and over-current limit built into the voltage regulator provides protection from excessive stress. The user must consider the maximum output current limit of VR1 when attempting to power off-board circuitry through connector J1.

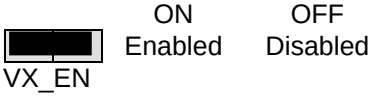
If powered from the PWR connector, the integrated BDM may still be used to develop and debug application code. Alternately, the board may be powered from the integrated BDM while the LIN bus is powered from the PWR connector.

VX_EN

The VX_EN option header is a 2-pin jumper that connects or disconnects input J1-1 directly to the target board +5V voltage rail. J1-3 is directly connected to the ground plane. Use of this feature requires a regulated +5V input power source. This power input is decoupled to minimize noise but is not regulated. Care should be exercised when using this feature; no protection is applied on this input and damage to the target board may result if over-driven. Also, do not attempt to power the target board through this connector while also applying power through the USB-Multilink BDM or the PWR connector; damage to the board may result.

Power may also be sourced to off-board circuitry through the J1 connector. The current supplied from the USB bus or the on-board regulator limits current output to external circuitry. Excessive current drain may damage the target board, the host PC USB hub, or the on-board regulator. The figure below details the VX_EN header connections.

Figure 3: VX_EN Option Header



CAUTION: Do not exceed available current supply from USB-Multilink BDM or on-board regulator, when sourcing power through connector J1 to external circuitry.

RESET SWITCH

The RESET switch provides a method to apply an asynchronous RESET to the MCU. The RESET switch is connected directly to the RESET* input on the MCU. Pressing the RESET switch applies a low voltage level to the RESET* input. A pull-up bias resistor allows normal MCU operation. Shunt capacitance ensures an adequate input pulse width.

LOW VOLTAGE RESET

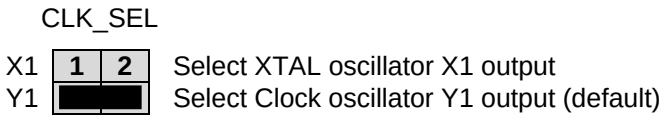
The MC9S08DZ60 utilizes an internal Low Voltage Detect (LVD) circuit. The LVD holds the MCU in reset until applied voltage reaches an appropriate level. The LVD also protect against under-voltage conditions. Consult the MC9S08DZ60 reference manual for details LVD operation.

TIMING

The DEMO9S08DZ60 provide 1 internal and 2 external timing sources. The 32 kHz internal timing source, with ±0.2% resolution, is active out of RESET. An external crystal with ±50ppm resolution is also provided. A full-size socket allows alternate square-wave clock inputs to be applied. The target MCU must be configured to select either external timing input source. Refer to the target MCU documentation for details on configuring external timing inputs.

The CLK_SEL option header selects the on-board XTAL oscillator, or the optional CLOCK oscillator socket. The figure below shows settings for CLK_SEL option header.

Figure 4: CLK_SEL Option Header



COMMUNICATIONS

The DEMO9S08DZ60 board applies two Serial Communications Interface (SCI) ports. SCI0 is applied to RS-232 serial communications (COM) on the target board. SCI1 is applied to LIN communications on the target board. RS-232 communications are supported through a DB9 connector. LIN communications are supported through a pair of 4-pin Molex connectors.

RS-232

An RS-232 translator provides RS-232 to TTL/CMOS logic level translation on the COM connector. The COM connector is a 9-pin Dsub, right-angle connector. A ferrite bead on shield ground provides conducted immunity protection. Communication signals TXD1 and RXD1 are routed from the transceiver to the MCU. Hardware flow control signals RTS and CTS are available on the logic side of the transceiver. These signals are routed to vias located near the transceiver. RTS has been biased properly to support 2-wire RS-232 communications.

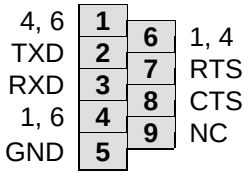
Table 4: COM Connections

MCU Port	COM Signal	I/O PORT CONNECTOR
PTE0/TXD1	TXD	J1-5
PTE1/RXD1	RXD	J1-7

COM Connector

A standard 9-pin Dsub connector provides external connections for the SCI0 port. The Dsub shell is connected to board ground through a ferrite bead. The ferrite bead provides noise isolation on the RS-232 connection. The figure below details the DB9 connector.

Figure 5: COM Connector



Female DB9 connector that interfaces to the MCU internal SCI0 serial port via the RS232 transceiver. Flow control is provided at test points on the board.

Pins 1, 4, and 6 are connected together.

LIN Communications

The DEMO9S08DZ60 applies the MC33661D Local Interconnect Interface (LIN) physical layer (PHY) for use in developing automotive control applications. The MC33661D physical layer interface (PHY) supports LIN bus functionality for input voltages between +6V and +18V. Only power applied to the PWR connector will enable the LIN bus. Two, 4-pin, Molex connectors provide off-board connectivity. The figure below shows the pin-out of the LIN connector looking into the connector.

Figure 6: LIN Connector

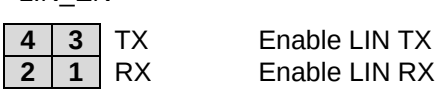
REF: Mating Connector, Molex P/N,
39-01-2040, Housing
39-00-0039, Socket

NOTE: +12V must be applied to the PWR connector when using the LIN functionality.

LIN_EN

The LIN_EN option header connects or disconnects the LIN PHY to SCI1.

Figure 7: LIN_EN Option Header

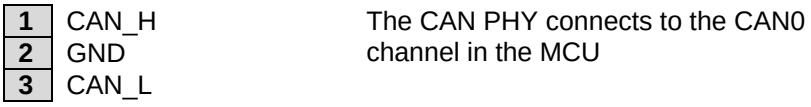


NOTE: +12V must be applied to the PWR connector when using the LIN functionality.

CAN Communications

The DEMO9S08DZ60 provides a high-speed CAN physical layer interface (PHY). A 3-pin connector provides connectivity to the off-board CAN bus. The CAN PHY connects to the CAN0 channel on the MCU. The PHY supports data rates up to 1 MBPS with edge-rate control to reduce EMI/RFI. The figure below shows the pin-out of the CAN_PORT connector.

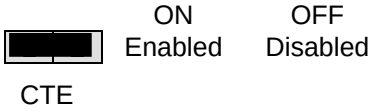
Figure 8: CAN_PORT Connector



CAN Termination

The DEMO9S08DZ60 applies a 121 ohm differential termination to the CAN bus. An option jumper allows the user to selectively apply termination. Installing the CTE option jumper applies termination to the differential CAN bus. Removing the CTE option jumper removes the CAN termination.

Figure 9: CTE Option Header



VRH/VRL

MCU inputs VRH and VRL provide the upper and lower voltage reference for the analog to digital (ATD) converter. By default, VRH is tied to VDD and VRL is tied to ground. Adequate filtering has been added to provide a voltage reference with minimal ripple. Either, or both, references may be isolated to provide alternate ATD input references. A test point via on each signal, labeled VRH, or VRL, provides a convenient attach point.

A 0-ohm configuration resistor allows isolation of each reference voltage. Removing R25 isolates VRH while removing R26 isolates VRL. Install 0805 sized 0-ohm resistors in these locations to restore the board to default configuration.

Care must be exercised when using alternate input references. The associated isolation resistor must be removed before applying an alternate voltage reference or the board may be damaged. The table below summarizes the changes necessary to use alternate VRH and/or VRL.

Table 5: ATD Reference Voltage

	Installed (Default)	Removed
R25	VRH = VDD	VRH provided by user
R26	VRL = GND	VRL provided by user

NOTE: Damage to the board may result if an alternate reference voltage is attached without first removing the associated configuration resistor.

USER I/O

User I/O includes 2 potentiometers, 1 4-position DIP switch, 2 push button switches, and 2 green LEDs for user I/O. The User option header block enables or disables each User I/O individually.

POT

The DEMO9S08DZ60 target board provides 2 5K ohm trimmer potentiometers (POT) have been provided to simulate analog input. Both parts are decoupled to minimize noise during adjustment. Potentiometer RV1 connects to analog input PTB4/ADP12. Potentiometer RV2 connects to analog input PTB5/ADP13. . The figure below shows the USER enable position and associated signal for the potentiometer.

SWITCHES

The DEMO9S08DZ60 target board provides 2 push button switches and one 4-position DIP switch for user input. Each push button switch is an active low input with a pull-up resistor bias to prevent indeterminate input conditions. Pressing a push-button switch causes a low logic input on the associated input.

Each DIP switch position is an active low input. Use of the DIP switches requires enabling the associated, internal PORTG pull-ups on the MCU prevent indeterminate input conditions. Moving a DIP switch position to ON causes a low logic level on the associated input. The figure below shows the USER enable position and associated signal for each user switch.

LED's

The DEMO9S08DZ60 target board provides 2 green LEDs for output indication. Each LED is an active low output. Writing a low logic level to an LED output causes the associated LED to turn on. A series, current-limit resistor prevents excessive diode current. The figure below shows the USER enable position and associated signal for each user LED.

User Signals

The following table shows the connections for each user I/O device.

Table 6: User I/O

USER	Ref Des	Signal	Device
1	RV1	PTB4/ADP12	Potentiometer
2	RV2	PTB5/ADP13	Potentiometer
3	SW1-1	PTG2	4-pos DIP Switch
4	SW1-2	PTG3	4-pos DIP Switch
5	SW1-3	PTG4	4-pos DIP Switch
6	SW1-4	PTG5	4-pos DIP Switch
7	LED1	PTC5/ADP21	Green LED
8	LED2	PTB3/ADP11	Green LED
9	SW1	PTB6/ADP14	Push Button Switch
10	SW2	PTB7/ADP15	Push Button Switch

User Enable

The User option header block enables or disables each User I/O device individually. User I/O includes 4 green LEDs, 2 push button switches, one 4-position DIP switch, a Light Sensor, and a potentiometer. Installing a shunt enables the associated option. Removing a shunt disables the associated option. The table below shows the configuration option for each USER I/O.

Figure 10: USER Option Header

		Shunt		
	USER	Installed	Removed	Description
1		Enable	Disable	Potentiometer
2		Enable	Disable	Potentiometer
3		Enable	Disable	DIP Switch Position 1
4		Enable	Disable	DIP Switch Position 2
5		Enable	Disable	DIP Switch Position 3
6		Enable	Disable	DIP Switch Position 4
7		Enable	Disable	LED 1
8		Enable	Disable	LED 2
9		Enable	Disable	Push Button Switch 1
10		Enable	Disable	Push Button Switch 2

MCU I/O PORT

The MCU I/O PORT connectors (J1 and J2) provide access to the MC9S08DZ60 I/O signals. The figures below show the pin-out for each MCU I/O connector.

Figure 11: MCU I/O PORT – J1

	J1		
VX	**1**	**2**	PTA7/PIA7/ADP7/IRQ
VSS	**3**	**4**	RESET*
PTE0/TXD1	**5**	**6**	BKGD/MS
PTE1/RXD1	**7**	**8**	PTF7
PTG2	**9**	**10**	PTA0/PIA0/ADP0/MCLK
PTG3	**11**	**12**	PTA1/PIA1/ADP1/ACMP1+
PTD2/PID2/TPM1CH0	**13**	**14**	PTA2/PIA2/ADP2/ACMP1-
PTD3/PID3/TPM1CH1	**15**	**16**	PTA3/PIA3/ADP3/ACMP1O
PTE4/SCL/MOSI	**17**	**18**	PTA4/PIA4/ADP4
PTE5/SDA/MISO	**19**	**20**	PTA5/PIA5/ADP5
PTE3/SPSCK	**21**	**22**	PTA6/PIA6/ADP6
PTE2/SS*	**23**	**24**	PTB0/PIB0/ADP8
PTG4	**25**	**26**	PTE6/TXD2/TXCAN
PTG5	**27**	**28**	PTE7/RXD2/RXCAN
PTF3/TMP2CLK/SDA	**29**	**30**	PTB1/PIB1/ADP9
PTF2/TPM1CLK/SCL	**31**	**32**	PTB2/PIB2/ADP10
PTD4/PID4/TPM1CH2	**33**	**34**	PTD0/PID0/TPM2CH0
PTD5/PID5/TPM1CH3	**35**	**36**	PTD1/PID1/TPM2CH1
PTD6/PID6/TPM1CH4	**37**	**38**	PTC0/ADP16
PTD7/PID7/PTM1CH5	**39**	**40**	PTC1/ADP17

Figure 12: MCU I/O PORT – J2

	J2		
NC	**41**	**42**	PTF0/TXD2
NC	**43**	**44**	PTF1/RXD2
NC	**45**	**46**	PTB3/PIB3/ADP11
NC	**47**	**48**	PTB4/PIB4/ADP12
NC	**49**	**50**	PTB5/PIB5/ADP13
NC	**51**	**52**	PTB6/PIB6/ADP14
NC	**53**	**54**	PTB7//PIB7/ADP15
NC	**55**	**56**	PTC2/ADP18
NC	**57**	**58**	PTC3/ADP19
NC	**59**	**60**	PTC4/ADP20
NC	**61**	**62**	PTC5/ADP21
NC	**63**	**64**	PTC6/ADP22
NC	**65**	**66**	PTC7/ADP23
NC	**67**	**68**	NC
NC	**69**	**70**	NC
NC	**71**	**72**	NC
NC	**73**	**74**	NC
NC	**75**	**76**	PTF4/ACMP2+
NC	**77**	**78**	PTF5/ACMP2-
NC	**79**	**80**	PTF6/ACMP2O

Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

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Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург,
Промышленная ул, дом № 19, литера Н,
помещение 100-Н Офис 331