

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT273**

**Octal D-type flip-flop with reset;  
positive-edge trigger**

Product specification  
File under Integrated Circuits, IC06

September 1993

# Octal D-type flip-flop with reset; positive-edge trigger

## 74HC/HCT273

### FEATURES

- Ideal buffer for MOS microprocessor or memory
- Common clock and master reset
- Eight positive edge-triggered D-type flip-flops
- See “377” for clock enable version
- See “373” for transparent latch version
- See “374” for 3-state version
- Output capability; standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT273 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT273 have eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset ( $\overline{MR}$ ) inputs load and reset (clear) all flip-flops simultaneously.

The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q<sub>n</sub>) of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the  $\overline{MR}$  input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

### QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	15	15	ns
	$\overline{MR}$ to Q <sub>n</sub>		15	20	ns
f <sub>max</sub>	maximum clock frequency		66	36	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per flip-flop	notes 1 and 2	20	23	pF

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

### ORDERING INFORMATION

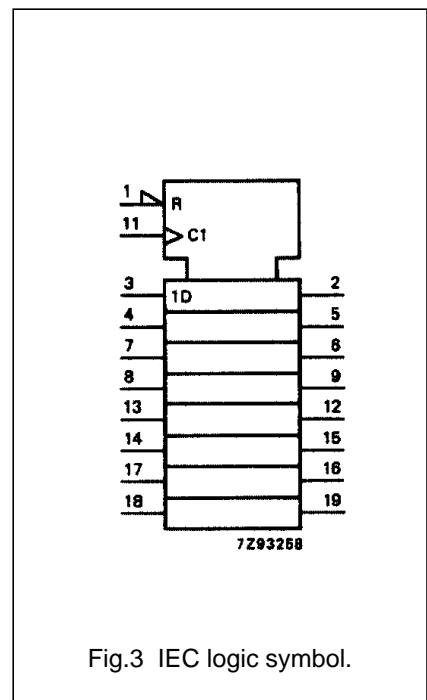
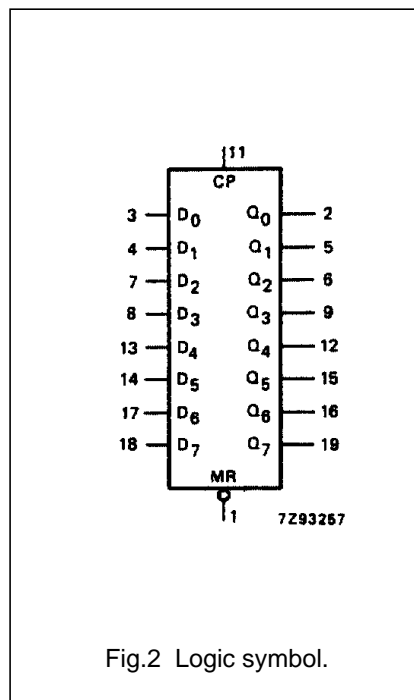
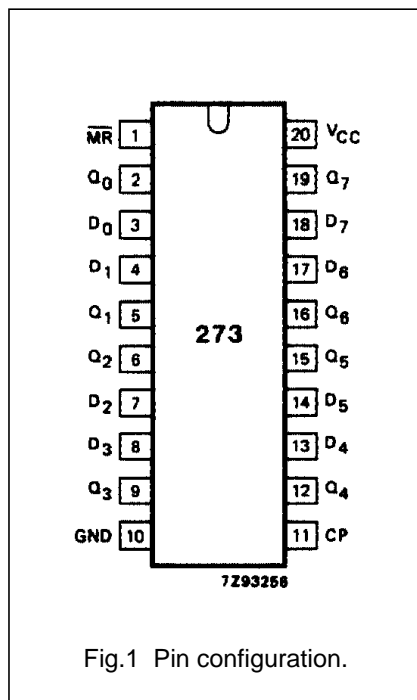
See “74HC/HCT/HCU/HCMOS Logic Package Information”.

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	master reset input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	$Q_0$ to $Q_7$	flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	$D_0$ to $D_7$	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	$V_{CC}$	positive supply voltage



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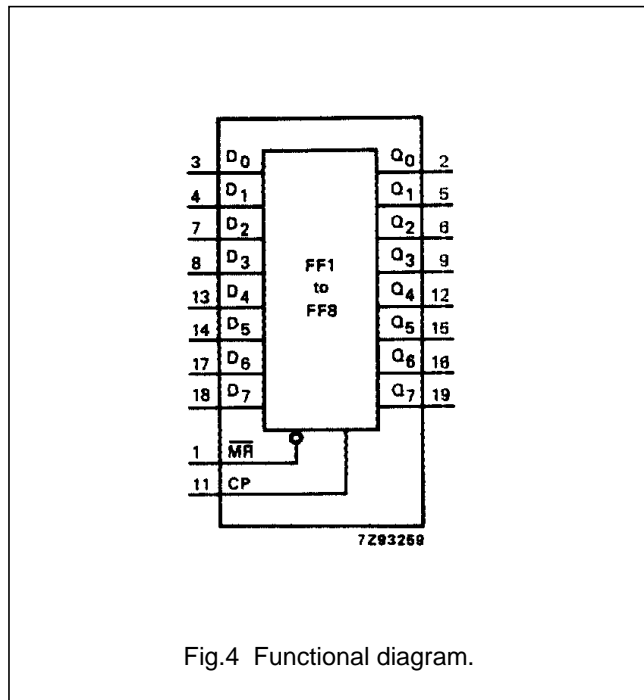


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{MR}$	CP	$D_n$	$Q_n$
reset (clear)	L	X	X	L
load "1"	H	↑	h	H
load "0"	H	↑	l	L

Note

- H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
L = LOW voltage level  
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
↑ = LOW-to-HIGH transition  
X = don't care

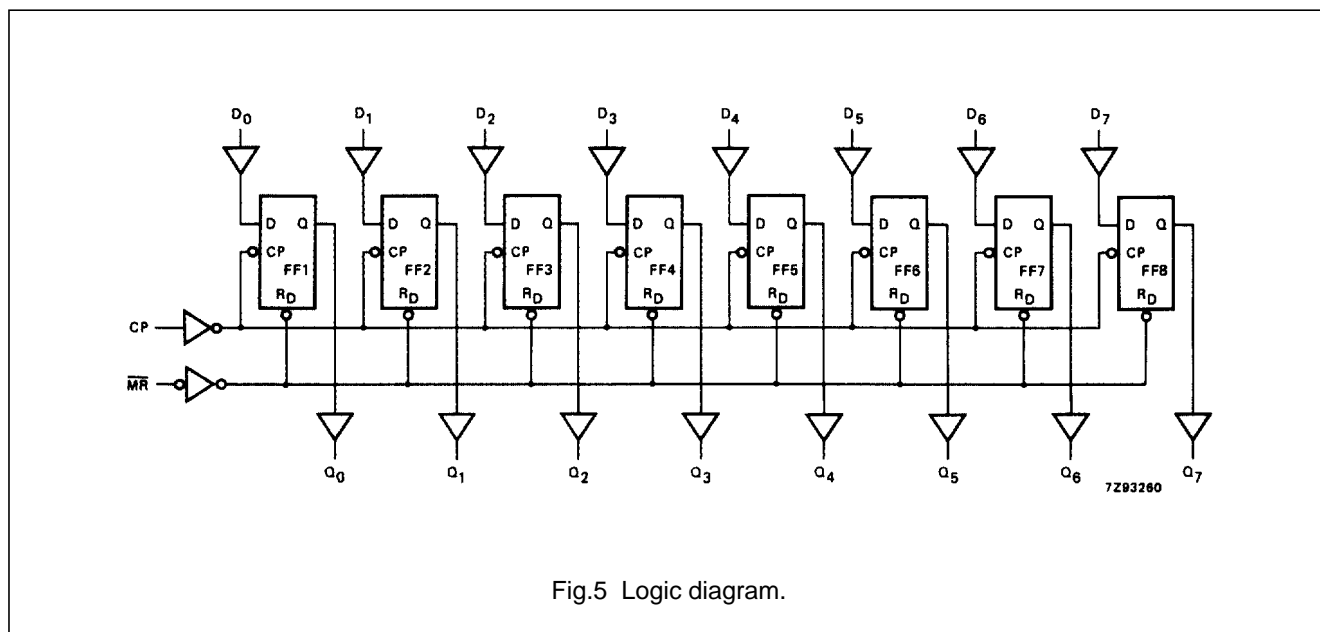


Fig.5 Logic diagram.

# Octal D-type flip-flop with reset; positive-edge trigger

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## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		41 15 13	150 30 26		185 37 31		225 45 38	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		44 16 14	150 30 26		185 37 31		225 45 38	ns	2.0 4.5 6.0	Fig.7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 15		110 22 19	ns	2.0 4.5 6.0	Fig.6
t <sub>w</sub>	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t <sub>w</sub>	master reset pulse width LOW	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.7
t <sub>rem</sub>	removal time MR to CP	50 10 9	-6 -2 -2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.7
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	60 12 10	11 4 3		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.8
t <sub>h</sub>	hold time D <sub>n</sub> to CP	3 3 3	-6 -2 -2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig.8
f <sub>max</sub>	maximum clock pulse frequency	6.0 30 35	20.6 103 122		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.6

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## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{MR}$	1.00
CP	1.75
D <sub>n</sub>	0.15

## AC CHARACTERISTICS FOR 74HCT

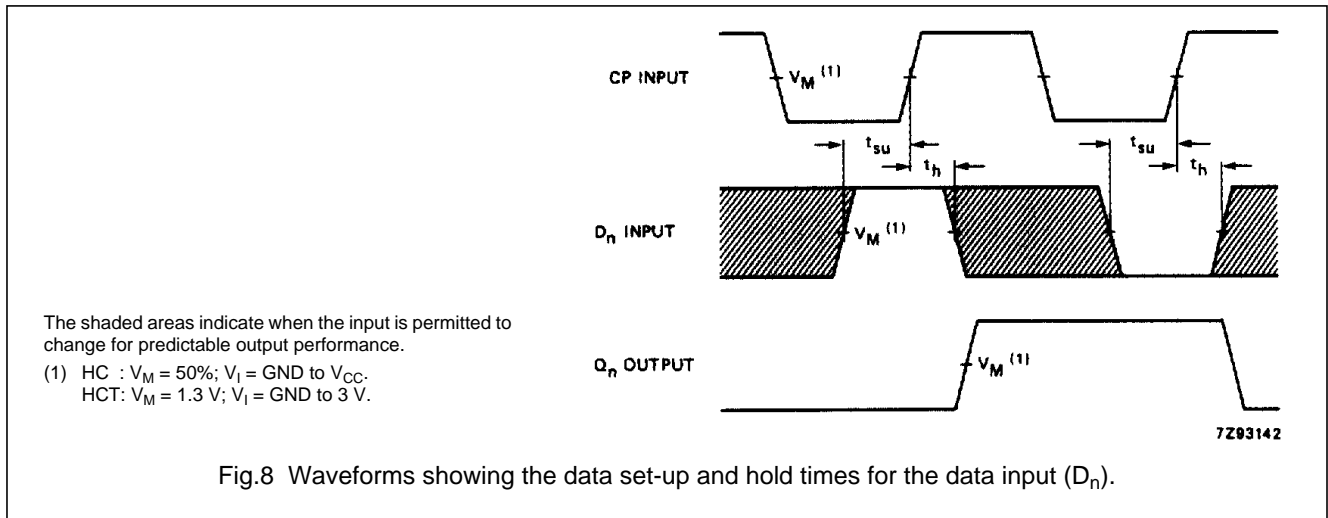
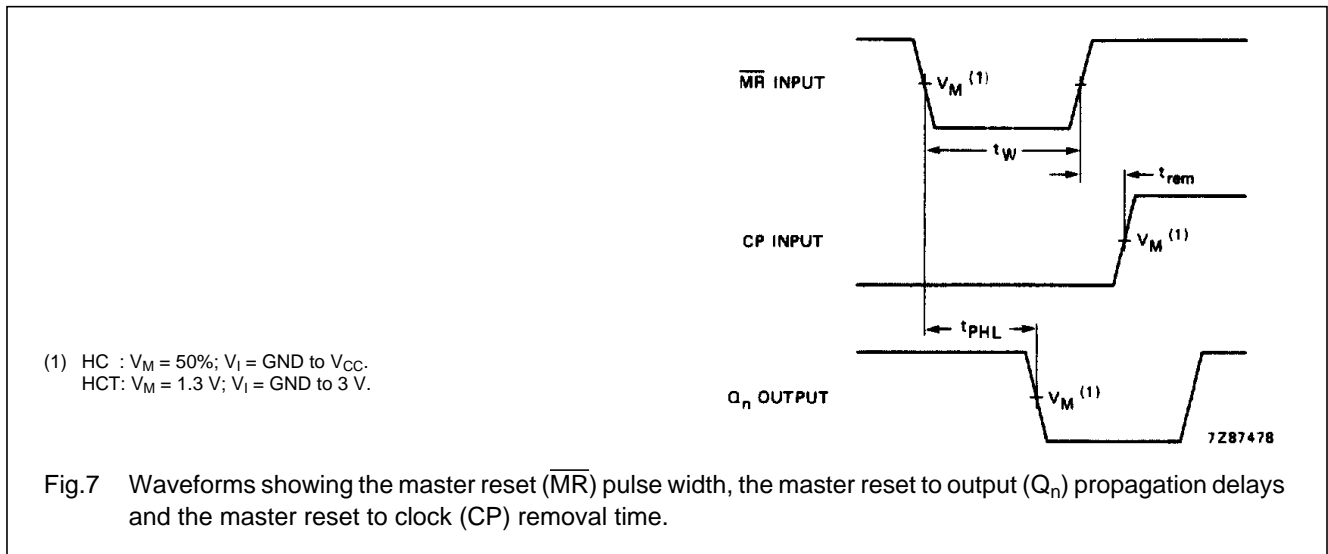
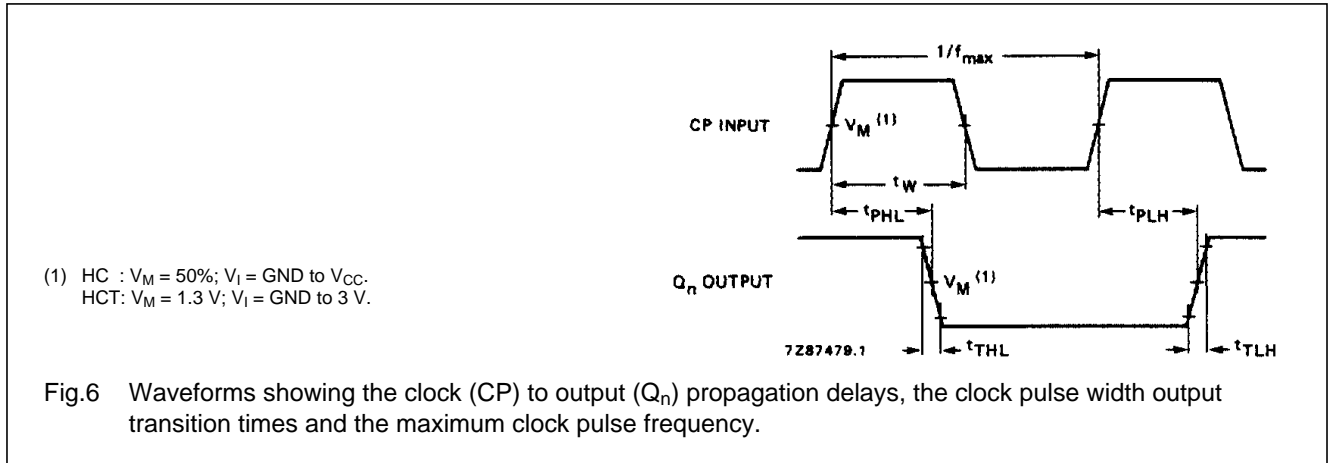
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HCT									V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		16	30		38		45	ns	4.5	Fig.6	
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		23	34		43		51	ns	4.5	Fig.7	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.6	
t <sub>w</sub>	clock pulse width HIGH or LOW	16	9		20		24		ns	4.5	Fig.6	
t <sub>w</sub>	master reset pulse width LOW	16	8		20		24		ns	4.5	Fig.7	
t <sub>rem</sub>	removal time $\overline{MR}$ to CP	10	-2		13		15		ns	4.5	Fig.7	
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	12	5		15		18		ns	4.5	Fig.8	
t <sub>h</sub>	hold time D <sub>n</sub> to CP	3	-4		3		3		ns	4.5	Fig.8	
f <sub>max</sub>	maximum clock pulse frequency	30	56		24		20		MHz	4.5	Fig.6	

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### AC WAVEFORMS



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**PACKAGE OUTLINES**

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.





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