Ordering number : ENA1968

SANYO

SANYO Semiconductors
DATA SHEET

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LV5216CS — Bi-CMOS IC LED Driver

Overview

The LV5216CS is 10ch LED driver IC for the cell phones with built-in charge pump circuit.

Features

- LED driver ×10 channels (MAIN, 3-color, 1-color) and charge pump circuit incorporated.
- Each LED driver current value adjusted by serial bus.
- Main LED automatic luminance control with illumination sensor incorporated.
- Usable both the LOG type and the linear type illumination sensor.
- Output level changeover possible for illumination sensor ON/OFF control output.
- Ringing tone and 3-color LEDs synchronization function incorporated.
- Gradation function incorporated (3-color LEDs)

Function

- Charge pump circuit ((One time and automatic switch method of 1.5 times) 5.0V time fixed output 1.5 times)
- LED driver
  - Main LCD backlight LED driver ×6 with automatic luminance control
    - LED current 5-bit changeover (0.6 to 19.2mA)
    - Fade IN / OUT function.
    - External brightness control function.
    - MLED5 and MLED6 independently controllable. Full ON possible.
    - Dim mode 3-bit changeover (0.2mA to 1.6mA)
  - 3-color LEDs driver ×1
    - LED current 5-bit changeover (0.6 to 19.2mA)
    - Gradation function
    - Ringing tone synchronization function (Forced to operate at SCTL: H)
  - 1-color LED driver ×1
    - LED current 5-bit changeover (0.6 to 19.2mA)
    - 2-fold current mode available

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		4.5	V
Maximum pin voltage	V1 max	LED driver, charge pump circuit	6	V
Allowable power dissipation	Pd max	* Mounted on a circuit board	850	mW
Operating temperature	Topr		-30 to +75	°C
Storage temperature	Tstg		-40 to +125	°C

* Specified board: 40mm × 50mm × 0.8mm, glass epoxy board. (2S2P (4-layer board))

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_{BAT}		3.0 to 4.5	V
Supply voltage 2	V_{DD}		1.7 to V_{BAT}	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 5.0V

Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
Consumption current						
Consumption current	$I_{CC}1$	RESET:L (standby mode)		0	5	μA
	$I_{CC}2$	RESET:H (sleep mode)		0.3	5.0	μA
	$I_{CC}3$	charge pump: ON		4	7	mA
Charge pump block						
Output voltage	V_O1	I_O=50mA One time		3.65		V
	V_O2	I_O=50mA 1.5 times		5.0		V
Resistance current	I_{LM}	1.5 times mode V_{BAT}=3.4V >4V	170			mA
Charge pump change voltage						
Threshold voltage	V_D1	When you set the voltage of the LED pin and the MAIN current value 19.2mA		0.25	0.35	V
Charge pump clock block						
Clock frequency	F_{OSC}		400	500	600	kHz
LED driver block						
Minimum output current value	$I_{MIN}1$	MAIN LED driver, Serial data=#00, V_O=0.5V	0.2	0.6	1.7	mA
	$I_{MIN}2$	3+1-color LED driver, Serial data=#00, V_O=0.5V	0.2	0.6	1.7	mA
	$I_{MIN}3$	1-color LED driver, Serial data=#00, V_O=0.5V, 2 times current mode	0.4	1.2	3.4	mA
Maximum output current value	$I_{MAX}1$	MAIN LED driver, Serial data=#FF, V_O=0.5V	18.0	19.2	20.4	mA
	$I_{MAX}2$	3+1-color LED driver, Serial data=#FF, V_O=0.5V	18.0	19.2	20.4	mA
	$I_{MAX}3$	1-color LED driver, Serial data=#FF, V_O=0.5V, 2 times current mode	36.0	38.4	40.8	mA
Non-linearity error	LE	*1	-2		2	LSB
Differential linearity error	DLE	*2	-2		2	LSB
Maximum output current	ΔIL1	MAIN LED driver Maximum current setting V_O=2 or 0.2V	-10			%
	ΔIL2	3+1-color LED driver Maximum current setting V_O=4 to0.35V	-10			%
Leakage current	IL1	MAIN LED driver, LED driver: OFF, V_O=5V			1	μA
	IL2	3+1-color LED driver, LED driver: OFF, V_O=5V			1	μA
External CTL current	$V_{EM}1$	MLED fixed current mode current value, MICTL pin voltage =1.8V, RT2=100kΩ, Serial MISW: Difference current with turning OFF, MICTLC:01h	-0.05	0	0.05	mA
	$V_{EM}2$	MLED fixed current mode current value, MICTL pin voltage =0.98V, RT2=100kΩ, Serial MISW: Ratio to current value when turning it OFF, MICTLC:01h	45	50	55	%

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
External CTL current	$V_{EM}3$	MLED fixed current mode current value, MICTL pin voltage =0V, RT2=100kΩ, MICTLC: 01h * Operation to erase LED by 0V impression is NG as for the MICTL pin.		0	0.5	mA
ON resistance for SW mode	FONR	MLED5 and 6: SW mode, I_L=-30mA		10		Ω
Illuminance sensor information input circuit (LOG type)						
PTD pin thresh voltage 1	VPLG1	Voltage of change PTD pin of 1 in brightness and 2 in brightness, Serial TAD=0.42V, TAU=0.84 setting	0.197	0.247	0.297	V
PTD pin thresh voltage 2	VPLG15	Voltage of change PTD pin of 15 in brightness and 16 in brightness, Serial TAD=0.42V, TAU=0.84 setting	0.752	0.843	0.920	V
PTD pin thresh voltage difference 1	ΔVPLG	Difference of voltage of change PTD pin of change voltage of PTD pin, brightness n+2, and n+1 in brightness of brightness n+1 and n in brightness	VPLGn+1-VPLGn›0 (1≤n≤14)			V
Illuminance sensor information input circuit (Linear type)						
PTD pin thresh voltage 3	VPLN1	Voltage of change PTD pin of 1 in brightness and 2 in brightness, Serial TAU=0.84 setting	0.01	0.03	0.05	V
PTD pin thresh voltage 4	VPLN9A	Voltage of change PTD pin of 9 in brightness and 10 in brightness, Serial TAU=0.84 setting, PTGSW: open	0.84	0.99	1.14	V
PTD pin thresh voltage difference 2	ΔVPLNL	Difference of voltage of change PTD pin of change voltage of PTD pin, brightness n+2, and n+1 in brightness of brightness n+1 and n in brightness	VPLNn+1-VPLNn›0 (1≤n≤8)			V
PTD pin thresh voltage 5	VPLN8B	Voltage of change PTD pin of 8 in brightness and 9 in brightness, Serial TAU=0.84 setting, PTGSW: ON	0.04	0.06	0.08	V
PTD pin thresh voltage 6	VPLN15	Voltage of change PTD pin of 15 in brightness and 16 in brightness, Serial TAU=0.84 setting	1.08	1.23	1.38	V
PTD pin thresh voltage difference 3	ΔVPLNH	Difference of voltage of change PTD pin of change voltage of PTD pin, brightness n+2, and n+1 in brightness of brightness n+1 and n in brightness	VPLNn+1-VPLNn›0 (8≤n≤14)			V
Control circuit block						
H level 1	$V_{IN}H1$	Input H level Serial	$V_{DD} \times 0.8$			V
L level 1	$V_{IN}L1$	Input L level Serial	0		$V_{DD} \times 0.2$	V
H level 2	$V_{IN}H2$	Input H level RESET SCTL	1.5			V
L level 2	$V_{IN}L2$	Input L level RESET SCTL	0		0.3	V
H output level 1	$V_{HO}1$	Output H level PTEN I_L=1mA Serial PTENH:V_{BAT} setting	V_{BAT} - 0.3			V
H output level 2	$V_{HO}2$	Output H level PTEN I_L=1mA Serial PTENH:V_{DD} setting	V_{DD} - 0.3			V
L output level 1	$V_{LO}1$	Output L level PTEN I_L=1mA	0		0.3	V

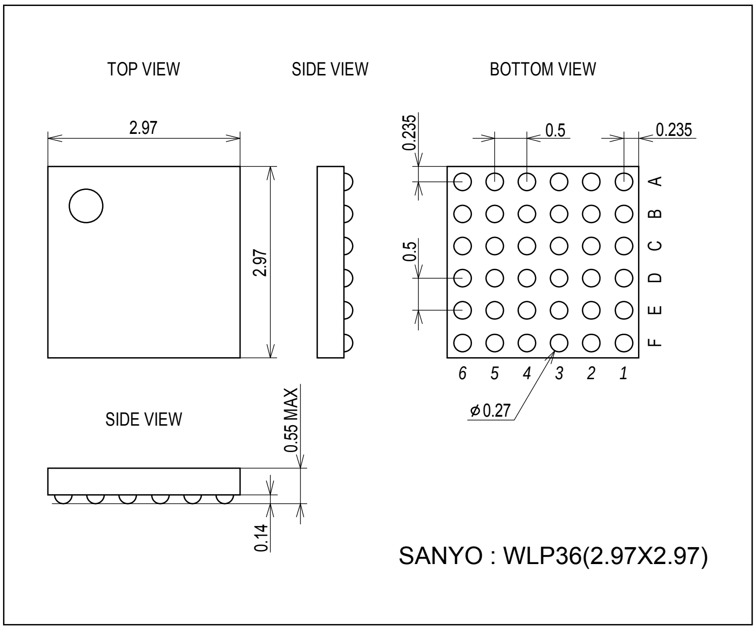
*1. Non-linearity error: The difference between the actual and ideal current values.

*2. Differential linearity error: The difference between the actual and ideal increment when one low-order bi value is added.

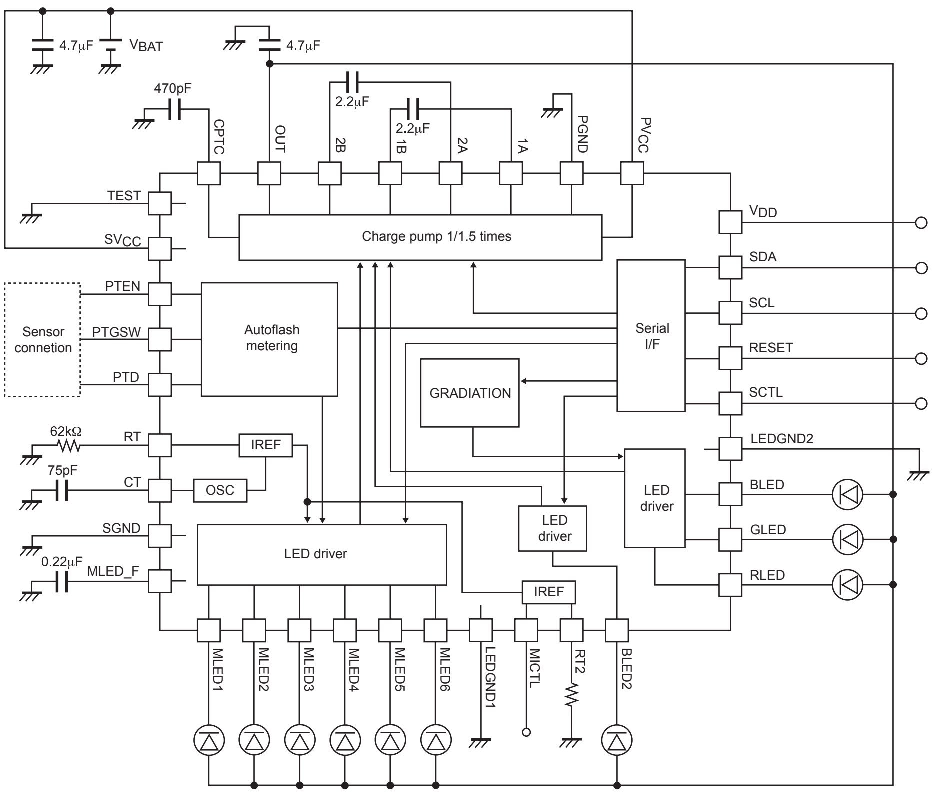
Package Dimensions

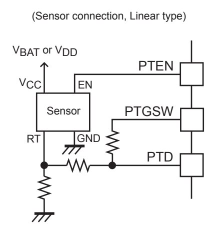
unit : mm (typ)

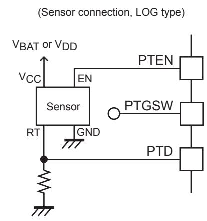
3412



Block Diagram & Pin arrangement drawing

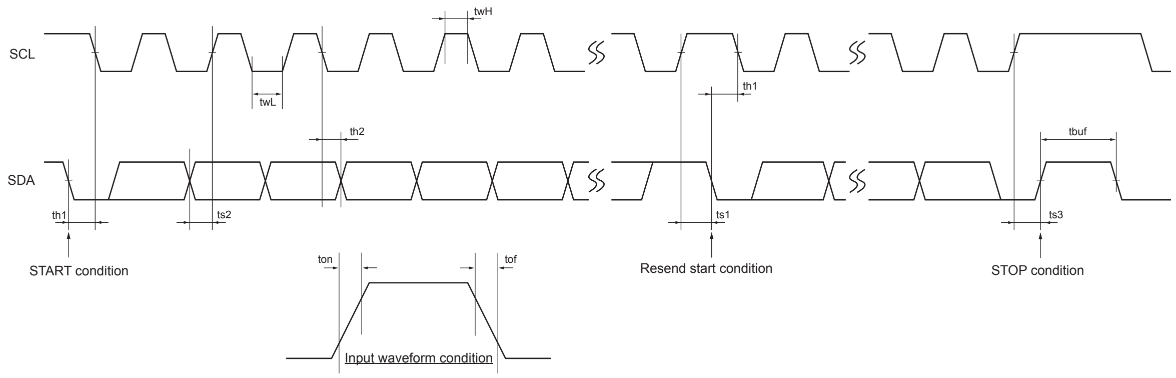






Serial Bus Communication Specifications

1) I²C serial transfer timing conditions



Standard mode

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCL clock frequency	fsc1	SCL clock frequency	0	-	100	kHz
Data setup time	ts1	SCL setup time relative to the fall of SDA	4.7	-	-	μs
	ts2	SDA setup time relative to the rise of SCL	250	-	-	ns
	ts3	SCL setup time relative to the rise of SDA	4.0	-	-	μs
Data hold time	th1	SCL hold time relative to the fall of SDA	4.0	-	-	μs
	th2	SDA hold time relative to the fall of SCL	0	-	-	μs
Pulse width	twL	SCL pulse width for the L period	4.7	-	-	μs
	twH	SCL pulse width for the H period	4.0	-	-	μs
Input waveform conditions	ton	SCL and SDA (input) rise time	-	-	1000	ns
	tof	SCL and SDA (input) fall time	-	-	300	ns
Bus free time	tbuf	Time between STOP condition and START condition	4.7	-	-	μs

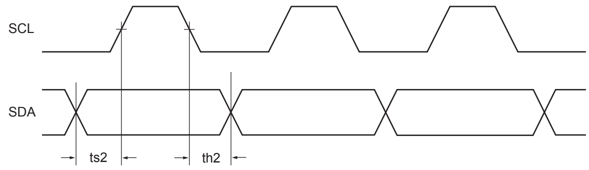
High-speed mode

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCL clock frequency	fsc1	SCL clock frequency	0	-	400	kHz
Data setup time	ts1	SCL setup time relative to the fall of SDA	0.6	-	-	μs
	ts2	SDA setup time relative to the rise of SCL	100	-	-	ns
	ts3	SCL setup time relative to the rise of SDA	0.6	-	-	μs
Data hold time	th1	SCL hold time relative to the fall of SDA	0.6	-	-	μs
	th2	SDA hold time relative to the fall of SCL	0	-	-	μs
Pulse width	twL	SCL pulse width for the L period	1.3	-	-	μs
	twH	SCL pulse width for the H period	0.6	-	-	μs
Input waveform conditions	ton	SCL and SDA (input) rise time	-	-	300	ns
	tof	SCL and SDA (input) fall time	-	-	300	ns
Bus free time	tbuf	Time between STOP and START conditions	1.3	-	-	μs

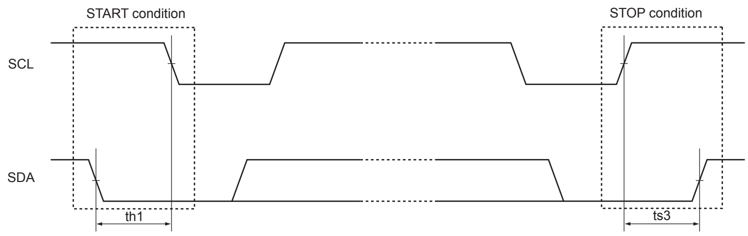
2) I^{2}C bus transfer method

Start and stop conditions

During data transfer operation using the I^{2}C bus, SDA must basically be kept in constant state while SCL is “H” as shown below.



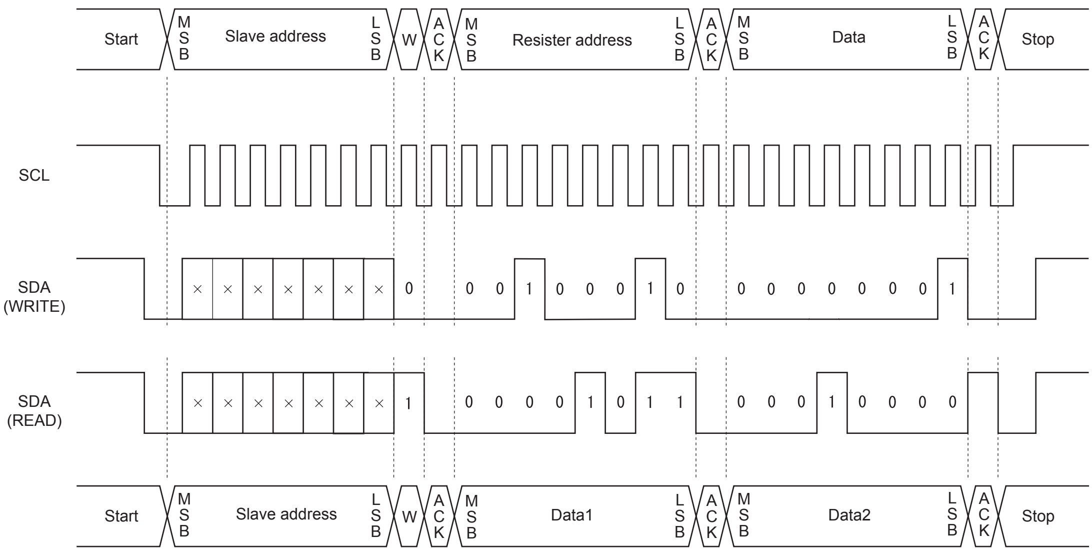
When data is not being transferred, both SCL and SDA are set in the “H” state.
When SCL=SDA is “H,” the start condition is established when SDA is changed from “H” to “L,” and access is started.
When SCL is “H,” the stop condition is established when SDA is changed from “L” to “H,” and access is ended.



Data transfer and acknowledgement response

After the start condition has been established, the data is transferred one byte (8 bits) at a time.
Any number of bytes of data can be transferred continuously.
Each time the 8-bit data is transferred, the ACK signal is sent from the receive side to the send side. The ACK signal is issued when SDA on the send side is released and SDA on the receive side is set to “L” immediately after fall of the clock pulse at the SCL eighth bit of data transfer to “L.”
When the next 1-byte transfer is left in the receive state after sending the ACK signal from the receive side, the receive side releases SDA at the fall of the SCL ninth clock.
In the I^{2}C bus, there is no CE signal. In its place, a 7-bit slave address is assigned to each device, and the first byte of transfer is assigned to the command (R/W) representing the 7-bit address and subsequent transfer direction. Note that only write is valid in this IC. The 7-bit address is transferred sequentially starting with MSB, and the eighth bit is set to “L” which indicates a write.

In the LV5216CS the slave address is specified as "1110100"



Data transfer writing format

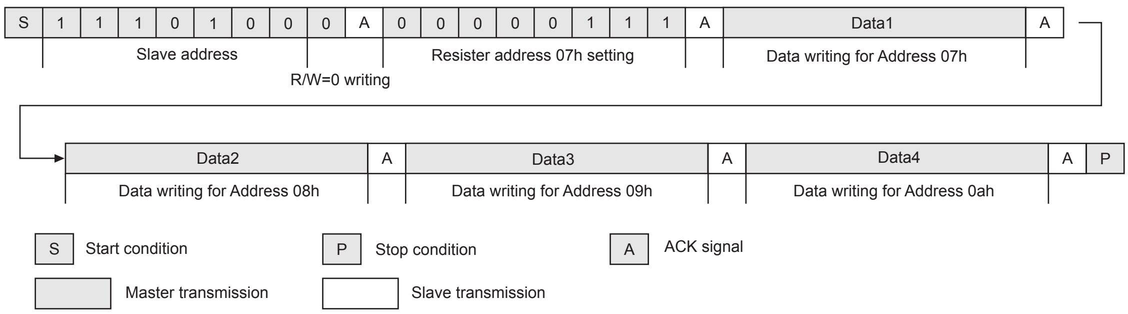
In the first one byte, the slave address and the Write command are allocated, and the following one byte specifies the register address in the cereal map.

The register address is done after the fourth byte be to do the data transfer to the address specified in the register address written in the third byte and the 2nd byte, and to continue data after that and the increment is done by the automatic operation.

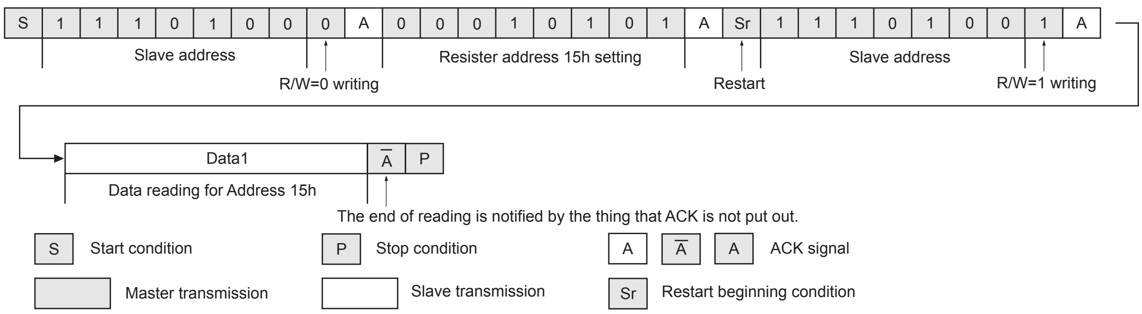
As a result, a data continuous sending from a specified address becomes possible.

However, when the address becomes 3fh, the forwarding address of the following byte becomes 00h.

Example of writing data



Example of reading data



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