

NTS4173P

Power MOSFET

–30 V, –1.3 A, Single P–Channel, SC–70

Features

- –30 V BV_{DS} , Low $R_{DS(on)}$ in SC–70 Package
- Low Threshold Voltage
- Fast Switching Speed
- This is a Halide–Free Device
- This is a Pb–Free Device

Applications

- Load Switch
- Low Current Inverter and DC–DC Converters
- Power Switch for Printers, Communication Equipment

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain–to–Source Voltage		V_{DS}	–30	V
Gate–to–Source Voltage		V_{GS}	± 12	V
Continuous Drain Current (Note 1)	Steady State	I_D	$T_A = 25^\circ\text{C}$	A
			$T_A = 85^\circ\text{C}$	
	$t \leq 5 \text{ s}$		$T_A = 25^\circ\text{C}$	
Power Dissipation (Note 1)	Steady State	P_D	$T_A = 25^\circ\text{C}$	W
	$t \leq 5 \text{ s}$			
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM}	–5.0	A
Operating Junction and Storage Temperature		T_J, T_{stg}	–55 to 150	$^\circ\text{C}$
Source Current (Body Diode)		I_S	–1.0	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction–to–Ambient – Steady State (Note 1)	$R_{\theta JA}$	425	$^\circ\text{C}/\text{W}$
Junction–to–Ambient – $t \leq 5 \text{ s}$ (Note 1)	$R_{\theta JA}$	360	

1. Surface–mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)

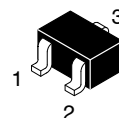
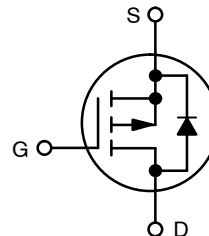


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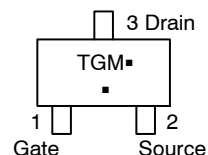
$V_{(BR)DS}$	$R_{DS(on)}$ MAX	I_D MAX
–30 V	150 m Ω @ –10 V	–1.2 A
	200 m Ω @ –4.5 V	–1.0 A
	280 m Ω @ –2.5 V	–0.9 A

SC–70/SOT–323 (3 LEADS)



SC–70/SOT–323
CASE 419
STYLE 8

MARKING DIAGRAM/ PIN ASSIGNMENT



TG = Specific Device Code
M = Date Code*
▪ = Pb–Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTS4173PT1G	SC–70 (Pb–Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

* Date code orientation may vary depending upon manufacturing location

NTS4173P

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -24\text{ V}, T_J = 25^\circ\text{C}$ $V_{GS} = 0\text{ V}, V_{DS} = -24\text{ V}, T_J = 85^\circ\text{C}$			-1.0 -5.0	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 0.1	μA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	-0.7	-1.15	-1.5	V
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -1.2\text{ A}$		90	150	$\text{m}\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -1.0\text{ A}$		110	200	
		$V_{GS} = -2.5\text{ V}, I_D = -0.9\text{ A}$		165	280	
Forward Transconductance	g_{FS}	$V_{DS} = -5\text{ V}, I_D = -1.2\text{ A}$		3.6		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz},$ $V_{DS} = -15\text{ V}$		430		pF
Output Capacitance	C_{oss}			55		
Reverse Transfer Capacitance	C_{rss}			40		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -15\text{ V},$ $I_D = -1.2\text{ A}$		4.8		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.6		
Gate-to-Source Charge	Q_{GS}			1.1		
Gate-to-Drain Charge	Q_{GD}			1.5		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -10\text{ V}, V_{DS} = -15\text{ V},$ $I_D = -1.2\text{ A}$		10.1		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.6		
Gate-to-Source Charge	Q_{GS}			1.1		
Gate-to-Drain Charge	Q_{GD}			1.5		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -15\text{ V},$ $I_D = -1.2\text{ A}, R_G = 3\text{ }\Omega$		7.7		ns
Rise Time	t_r			5.2		
Turn-Off Delay Time	$t_{d(off)}$			16.2		
Fall Time	t_f			6.7		
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -10\text{ V}, V_{DS} = -15\text{ V},$ $I_D = -1.2\text{ A}, R_G = 3\text{ }\Omega$		5.3		ns
Rise Time	t_r			6.7		
Turn-Off Delay Time	$t_{d(off)}$			19.9		
Fall Time	t_f			7.1		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -1.0\text{ A}$		-0.8	-1.0	V
Reverse Recovery Time	t_{RR}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, I_S = -1.0\text{ A},$ $dI_{SD}/dt = 100\text{ A}/\mu\text{s}$		12		ns
Charge Time	t_a			10		
Discharge Time	t_b			2.0		
Reverse Recovery Charge	Q_{RR}			7.0		nC

2. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
3. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$
4. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

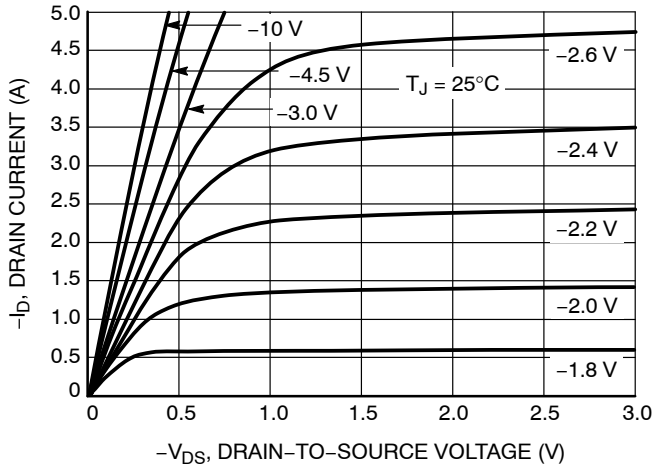


Figure 1. On-Region Characteristics

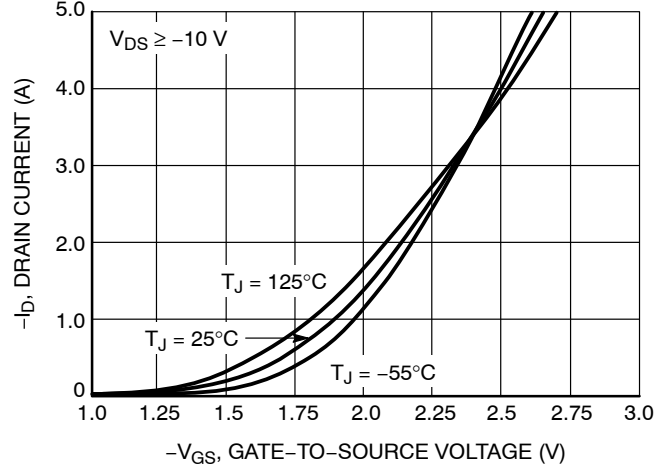


Figure 2. Transfer Characteristics

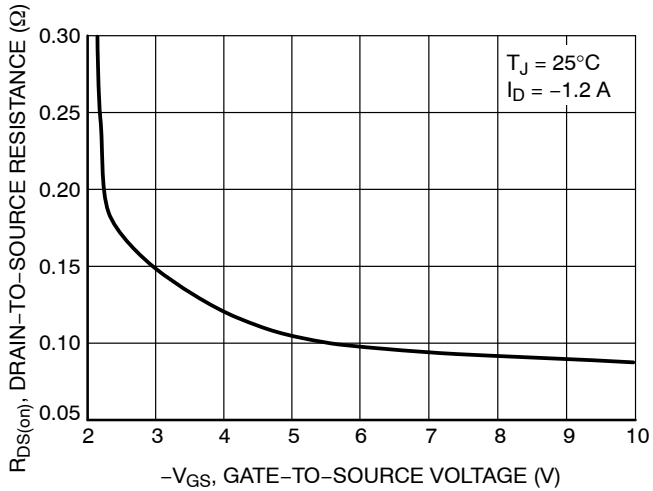


Figure 3. On-Resistance vs. Gate Voltage

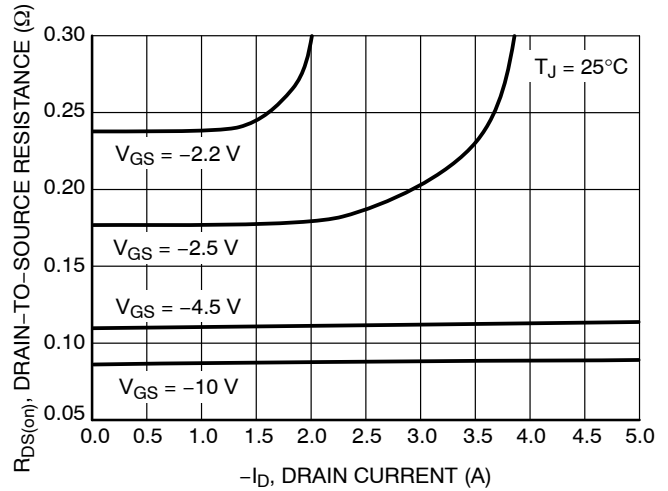


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

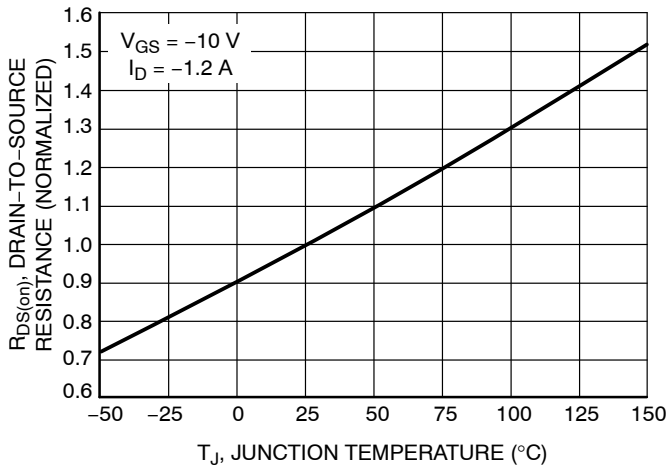


Figure 5. On-Resistance Variation with Temperature

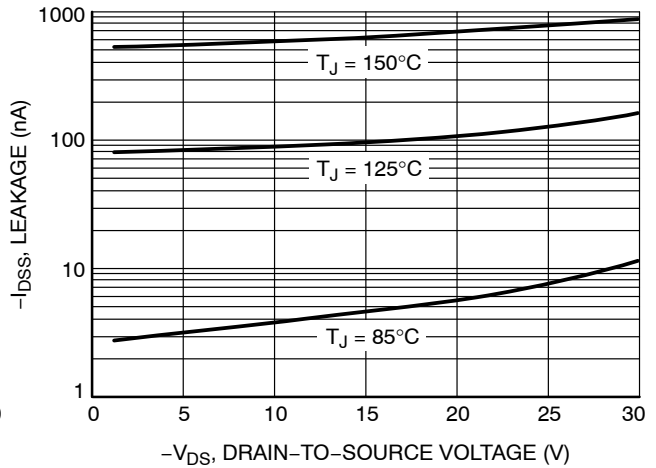


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

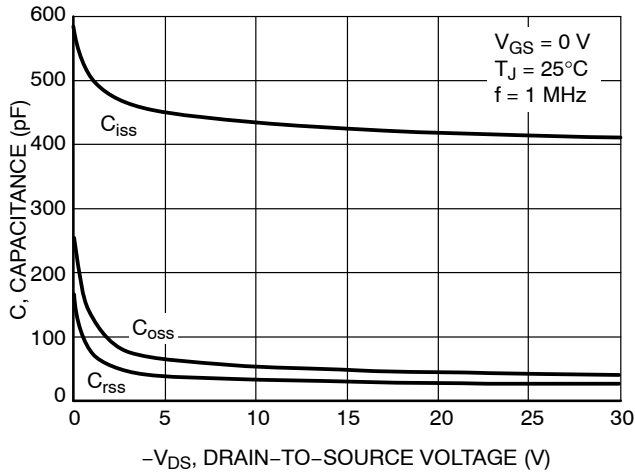


Figure 7. Capacitance Variation

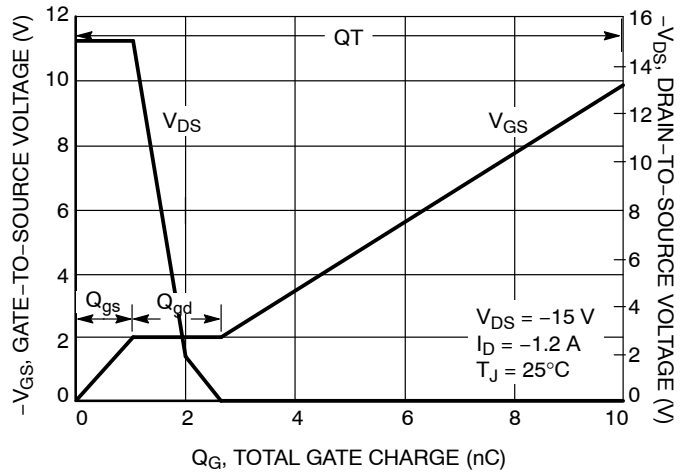


Figure 8. Gate-to-Source Voltage vs. Total Charge

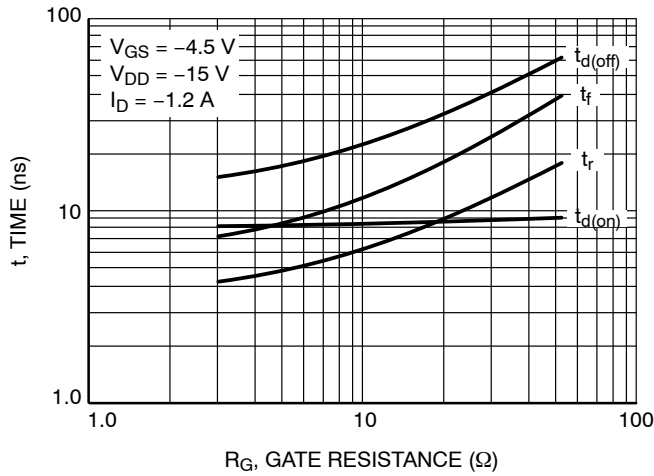


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

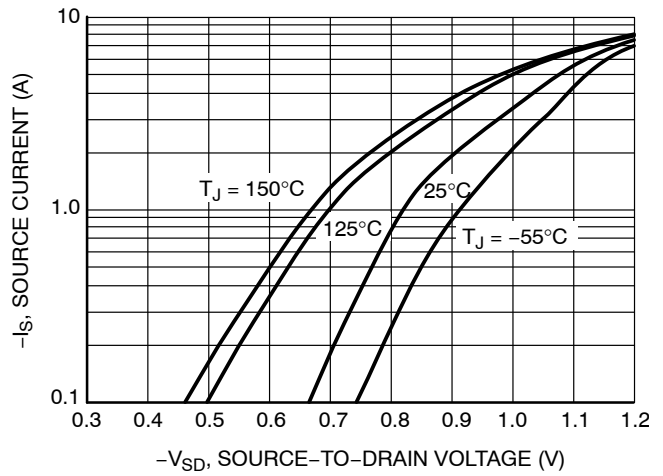


Figure 10. Diode Forward Voltage vs. Current

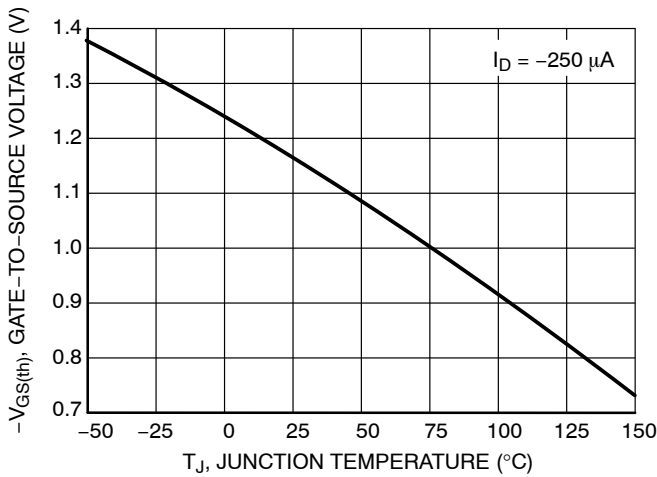


Figure 11. Threshold Voltage

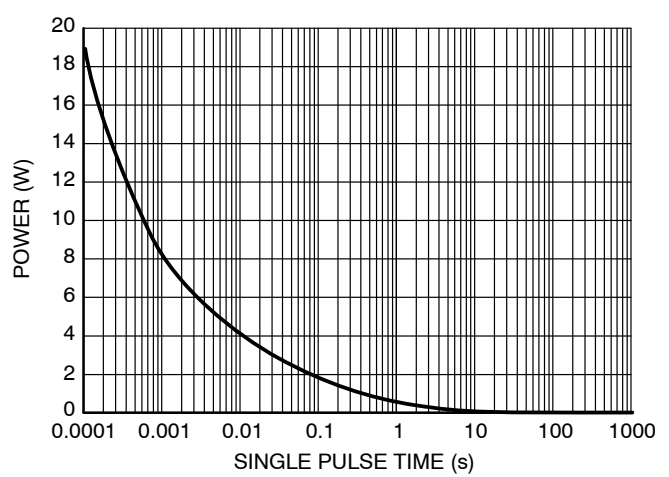


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL PERFORMANCE CURVES

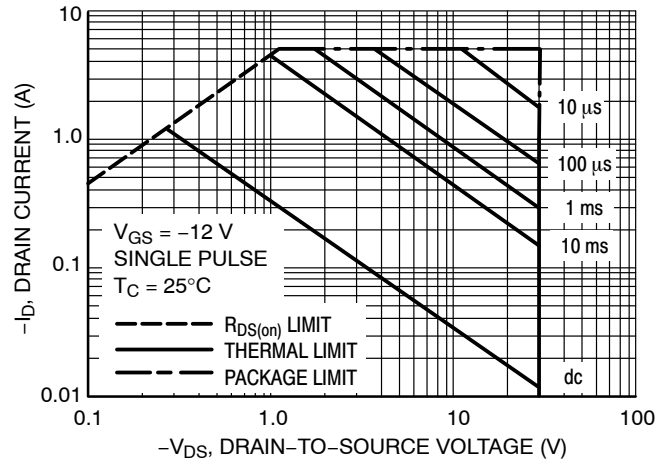


Figure 13. Maximum Rated Forward Biased Safe Operating Area

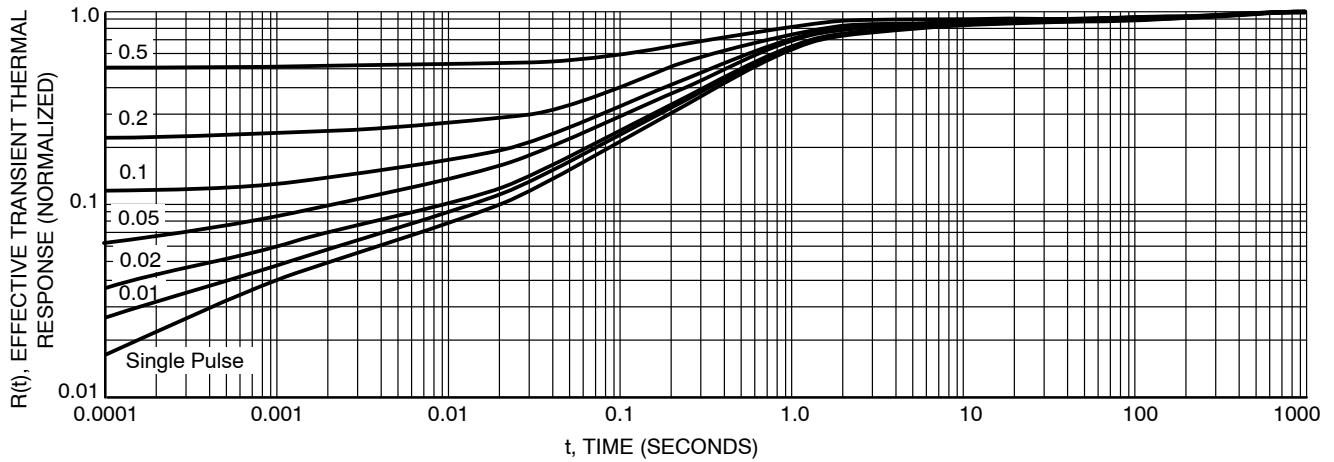
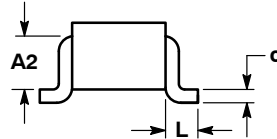
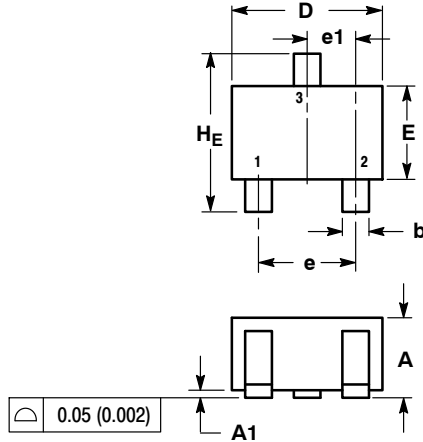


Figure 14. FET Thermal Response

NTS4173P

PACKAGE DIMENSIONS

SC-70 (SOT-323) CASE 419-04 ISSUE M



NOTES:

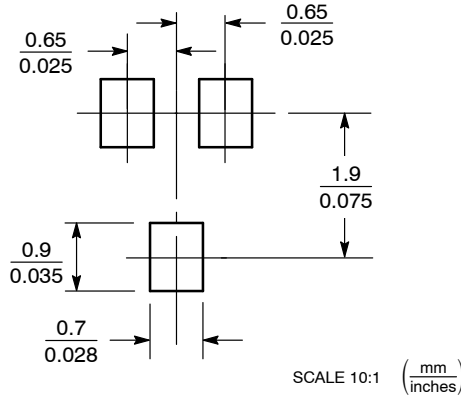
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2		0.7 REF			0.028 REF	
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1		0.65 BSC			0.026 BSC	
L		0.425 REF			0.017 REF	
HE	2.00	2.10	2.40	0.079	0.083	0.095

STYLE 8:

- PIN 1. GATE
- SOURCE
- DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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