



GaAs PHEMT MMIC MODULATOR DRIVER AMPLIFIER, DC - 20 GHz

Typical Applications

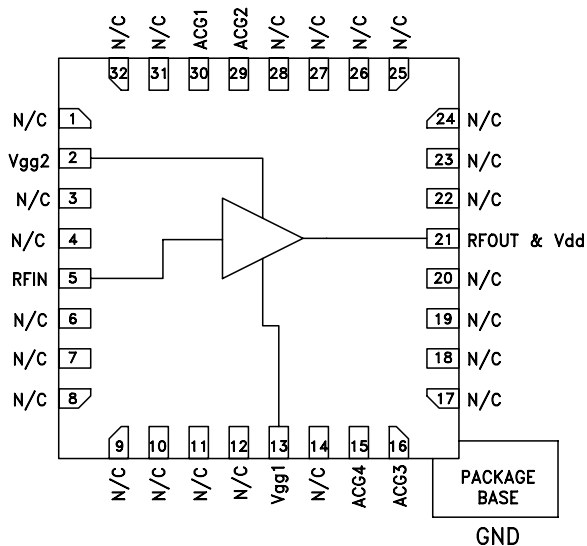
The HMC465LP5(E) wideband driver is ideal for:

- OC192 LN/MZ Modulator Driver
- Microwave Radio & VSAT
- Test Instrumentation
- Military EW, ECM & C³I

Features

- Gain: 15 dB
- Output Voltage to 10Vpk-pk
- +24 dBm Saturated Output Power
- Supply Voltage: +8V @160 mA
- 50 Ohm Matched Input/Output
- 32 Lead 5x5 mm QFN Package: 25 mm²

Functional Diagram



General Description

The HMC465LP5(E) is a GaAs MMIC PHEMT Distributed Driver Amplifier packaged in leadless 5x5 mm surface mount package which operate between DC and 20 GHz. The amplifier provides 15 dB of gain, 3 dB noise figure and +25 dBm of saturated output power while requiring only 160 mA from a +8V supply. Gain flatness is excellent at ±0.5 dB as well as ±4 deg deviation from linear phase from DC - 10 GHz making the HMC465LP5(E) ideal for OC192 fiber optic LN/MZ modulator driver amplifiers as well as test equipment applications. The HMC465LP5(E) amplifiers I/Os are internally matched to 50 Ohms.

Electrical Specifications, $T_A = +25^\circ C$, $V_{dd} = 8V$, $V_{gg2} = 1.5V$, $I_{dd} = 160 mA^*$

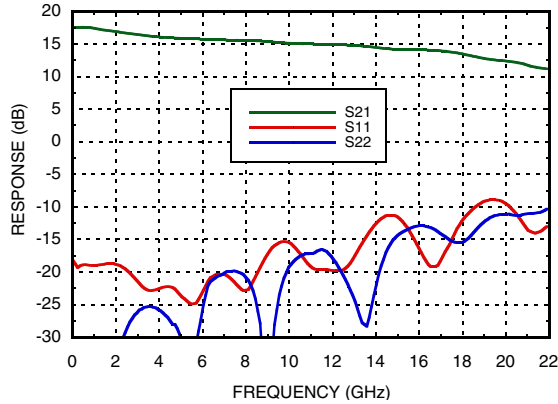
| Parameter | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Units |
|--|--------|-------|------|------------|-------|-------|-------------|-------|-------|--------|
| Frequency Range | DC - 6 | | | 6.0 - 12.0 | | | 12.0 - 20.0 | | | GHz |
| Gain | 13 | 16 | | 12 | 15 | | 9.5 | 12.5 | | dB |
| Gain Flatness | | ±0.75 | | | ±0.25 | | | ±1.5 | | dB |
| Gain Variation Over Temperature | | 0.015 | 0.02 | | 0.020 | 0.025 | | 0.035 | 0.045 | dB/ °C |
| Noise Figure | | 3.0 | | | 3.0 | | | 4.0 | | dB |
| Input Return Loss | | 20 | | | 15 | | | 8 | | dB |
| Output Return Loss | | 22 | | | 17 | | | 12 | | dB |
| Output Power for 1 dB Compression (P1dB) | 21 | 24 | | 20 | 23 | | 16 | 20 | | dBm |
| Saturated Output Power (Psat) | | 25.5 | | | 25 | | | 23 | | dBm |
| Output Third Order Intercept (IP3) | | 32 | | | 28 | | | 24 | | dBm |
| Saturated Output Voltage | | 10 | | | 10 | | | 8 | | Vpk-pk |
| Group Delay Variation | | ±15 | | | ±15 | | | | | pSec |
| Supply Current (Idd) (Vdd= 8V, Vgg1= -0.6V Typ.) | | 160 | | | 160 | | | 160 | | mA |

* Adjust Vgg1 between -2 to 0V to achieve Idd= 160 mA typical.

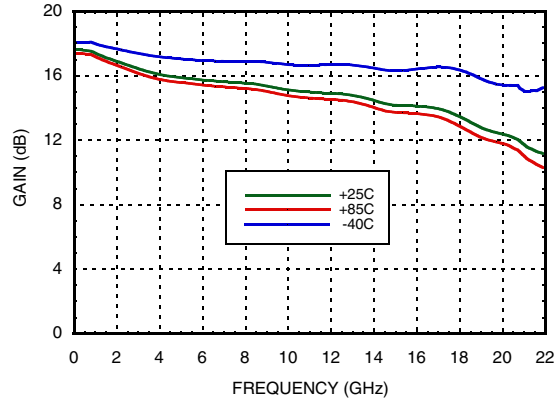


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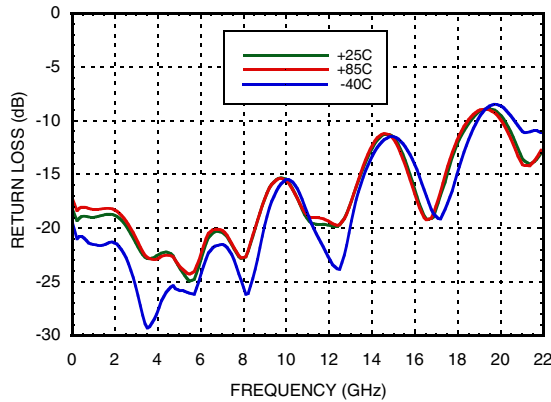
Gain & Return Loss



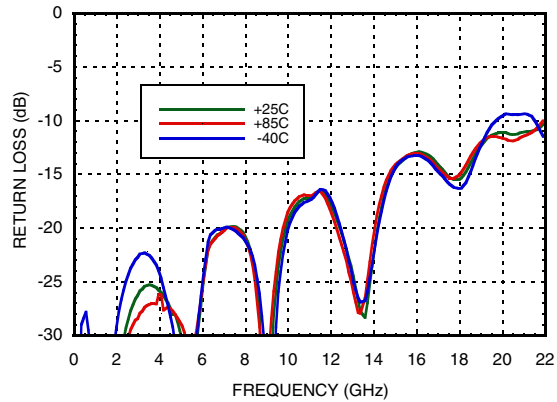
Gain vs. Temperature



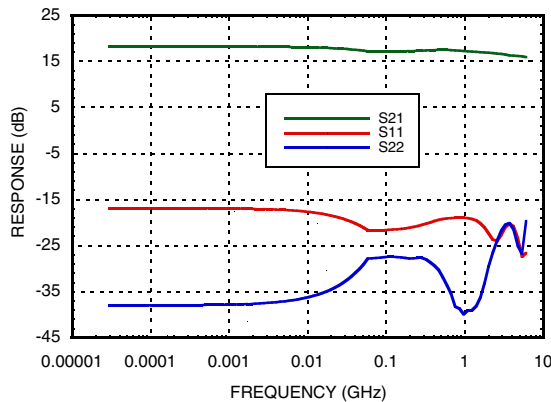
Input Return Loss vs. Temperature



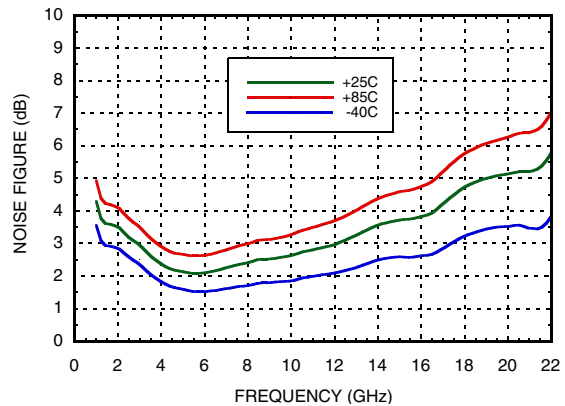
Output Return Loss vs. Temperature



Low Frequency Gain & Return Loss



Noise Figure vs. Temperature

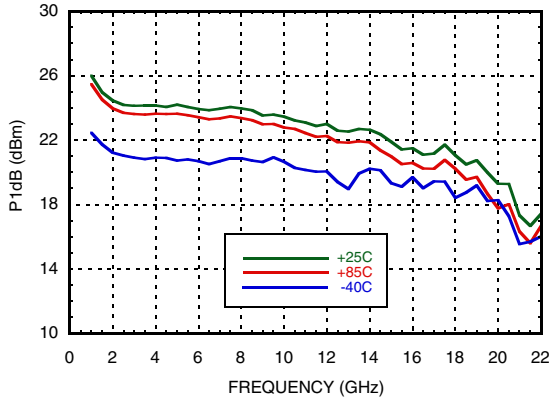




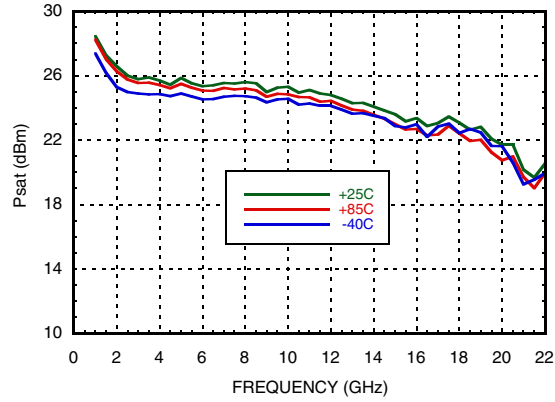
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AMPLIFIERS - DRIVER & GAIN BLOCK - SMT

P1dB vs. Temperature



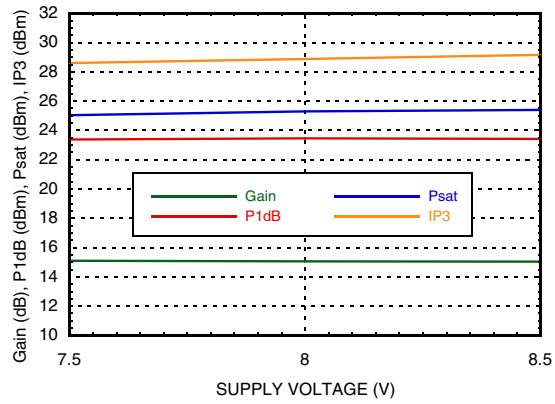
Psat vs. Temperature



Output IP3 vs. Temperature



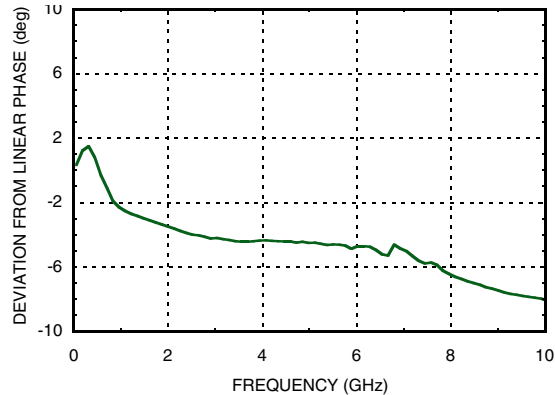
Gain, Power & Output IP3 vs. Supply Voltage @ 10 GHz, I_{dd} = 160mA



Group Delay



Deviation from Linear Phase





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Absolute Maximum Ratings

| | |
|---|------------------------|
| Drain Bias Voltage (Vdd) | +9 Vdc |
| Gate Bias Voltage (Vgg1) | -2 to 0 Vdc |
| Gate Bias Current (Igg1) | +3.2mA |
| Gate Bias Voltage (Vgg2) | (Vdd -8) Vdc to +3 Vdc |
| Gate Bias Current (Igg2) | +3.2mA |
| RF Input Power (RFIN)(Vdd = +8 Vdc) | +23 dBm |
| Channel Temperature | 150 °C |
| Continuous Pdiss (T = 85 °C) (derate 24 mW/°C above 85 °C) | 1.56 W |
| Thermal Resistance (channel to ground paddle) | 41.5 °C/W |
| Storage Temperature | -65 to +150 °C |
| Operating Temperature | -40 to +85 °C |

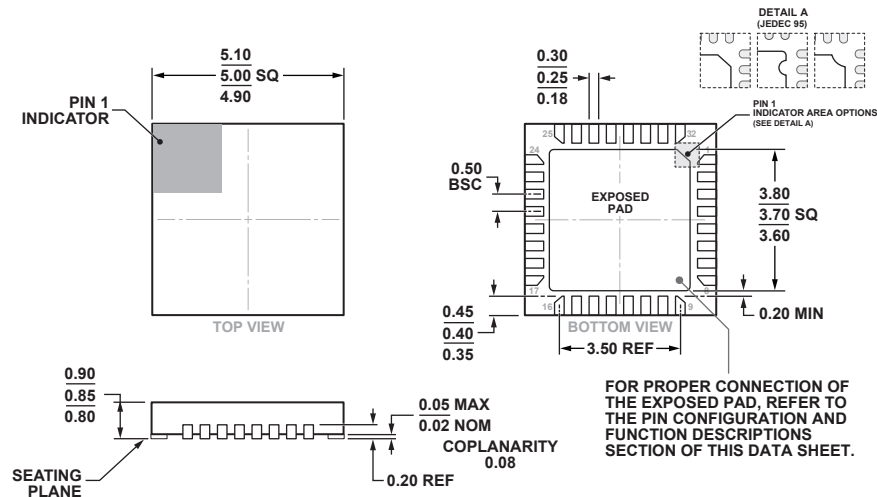
Typical Supply Current vs. Vdd

| Vdd (V) | Idd (mA) |
|---------|----------|
| +7.5 | 161 |
| +8.0 | 160 |
| +8.5 | 159 |



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-4.

32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm x 5 mm and 0.85 mm Package Height
(HCP-32-1)

Dimensions shown in millimeters.

Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking ^[3] |
|-------------|--|---------------|---------------------|--------------------------------|
| HMC465LP5 | Low Stress Injection Molded Plastic | Sn/Pb Solder | MSL1 ^[1] | H465 XXXX |
| HMC465LP5E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 ^[2] | H465 XXXX |

[1] Max peak reflow temperature of 235 °C

[2] Max peak reflow temperature of 260 °C

[3] 4-Digit lot number XXXX

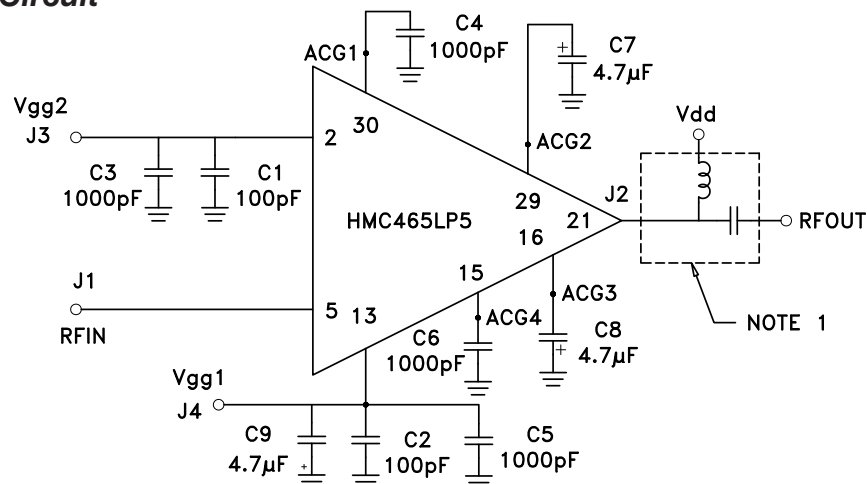


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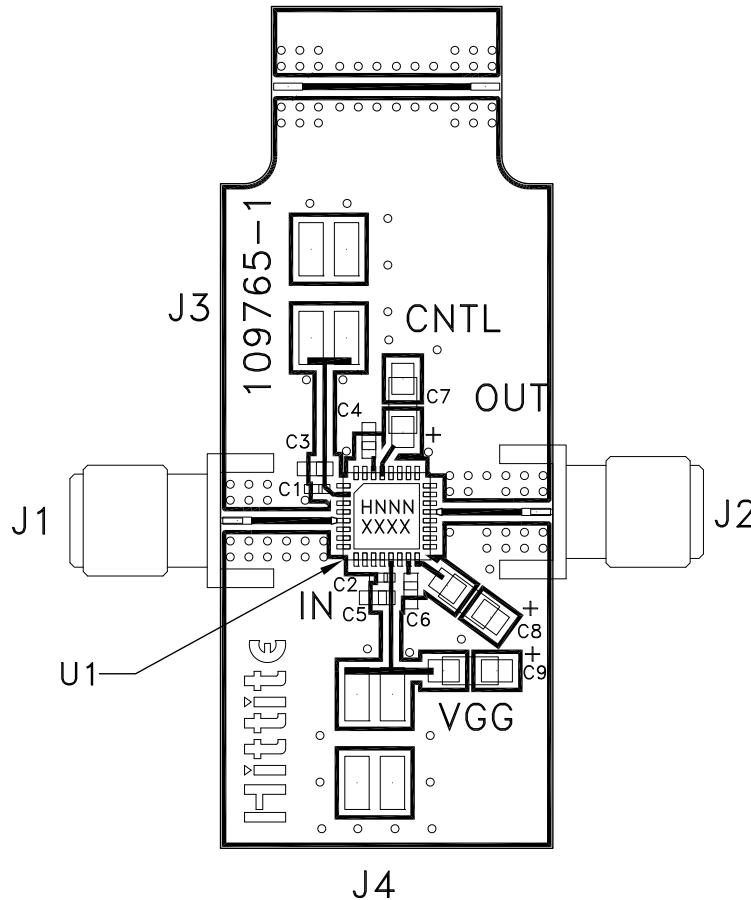
Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|--|-------------|--|---------------------|
| 1, 3, 4, 6 - 12, 14, 17, 18, 19, 20, 22 - 28, 31, 32 | N/C | The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally. | |
| 2 | Vgg2 | Gate Control 2 for amplifier. +1.5V should be applied to Vgg2 for nominal operation. | |
| 5 | RFIN | This pad is DC coupled and matched to 50 Ohms. | |
| 13 | Vgg1 | Gate Control 1 for amplifier. | |
| 15 | ACG4 | Low frequency termination. Attach bypass capacitor per application circuit herein. | |
| 16 | ACG3 | | |
| 21 | RFOUT & Vdd | RF output for amplifier. Connect the DC bias (Vdd) network to provide drain current (Idd). See application circuit herein. | |
| 29 | ACG2 | Low frequency termination. Attach bypass capacitor per application circuit herein. | |
| 30 | ACG1 | | |
| Ground Paddle | GND | Ground paddle must be connected to RF/DC ground. | |

Application Circuit



NOTE 1: Drain Bias (Vdd) must be applied through a broadband bias tee or external bias network.

**GAAS PHEMT MMIC MODULATOR DRIVER
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Evaluation PCB

List of Materials for Evaluation PCB 108347 [1]

| Item | Description |
|---------|---------------------------------|
| J1 - J2 | SRI K Connector |
| J3 - J4 | 2mm Molex Header |
| C1, C2 | 100 pF Capacitor, 0402 Pkg. |
| C3 - C6 | 1000 pF Capacitor, 0603 Pkg. |
| C7 - C9 | 4.7 μ F Capacitor, Tantalum |
| U1 | HMC465LP5 / HMC465LP5E |
| PCB [2] | 109765 Evaluation PCB |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and package bottom should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Analog Devices, upon request.

**GAAS PHEMT MMIC MODULATOR DRIVER
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These devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

The input to this device should be AC-coupled. To provide the typical 8Vp-p output voltage swing, a 1.2Vp-p AC-coupled input voltage swing is required.

Device Power Up Instructions

1. Ground the device
 2. Set V_{gg} to -2V (no drain current)
 3. Set V_{ctl} to +1V (no drain current)
 4. Set V_{dd} to +5V (no drain current)
 5. Adjust V_{gg} for I_{dd} = 140mA
- V_{gg} may be varied between -1V and 0V to provide the desired eye crossing point percentage (i.e. 50% crosspoint) and a limited cross point control capability.
 - V_{dd} may be increased to +8V if required to achieve greater output voltage swing.
 - V_{ctl} may be adjusted between +2V and +0V to vary the output voltage swing.

Device Power Down Instructions

1. Reverse the sequence identified above in steps 1 through 4.



HMC465LP5 / 465LP5E

v07.0418

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Notes:



Стандарт Электрон Связь

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