

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ max}$	$I_D \text{ MAX}$ $T_A = +25^\circ\text{C}$
-12V	0.8 Ω @ $V_{GS} = -4.5\text{V}$	-0.2A
	1.1 Ω @ $V_{GS} = -2.5\text{V}$	
	3.0 Ω @ $V_{GS} = -1.8\text{V}$	
	5.0 Ω @ $V_{GS} = -1.5\text{V}$	

Description

This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Load Switch
- Power Management Functions
- Portable Power Adaptors

Features

- 0.4mm Ultra Low Profile Package for Thin Application
- 0.48mm² Package Footprint, 16 Times Smaller than SOT23
- Low On-Resistance
- Low Input Capacitance
- ESD Protected Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

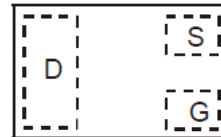
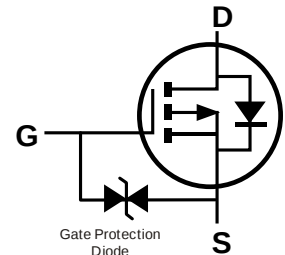
Mechanical Data

- Case: X2-DFN0806-3
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 ^(e4)
- Weight: 0.00043 grams (Approximate)

X2-DFN0806-3



Bottom View


 Top View
 Package Pin Configuration


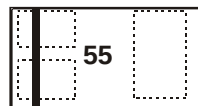
Internal Schematic

Ordering Information (Note 4)

Part Number	Case	Packaging
DMP1555UFA-7B	X2-DFN0806-3	10,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information


 Top View
 Bar Denotes Gate
 and Source Side

55 = Product Type Marking Code

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	-12	V
Gate-Source Voltage	V _{GSS}	±8	
Continuous Drain Current (V _{GS} = -4.5V)	I _D	-0.2	A
Pulsed Drain Current	I _{DM}	-1.5	A

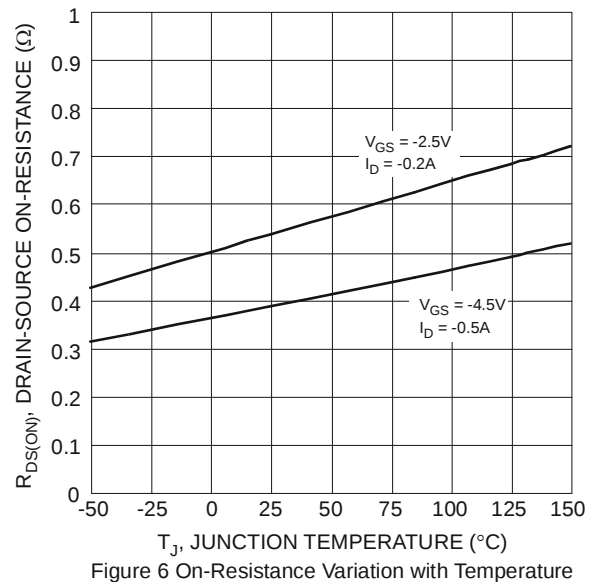
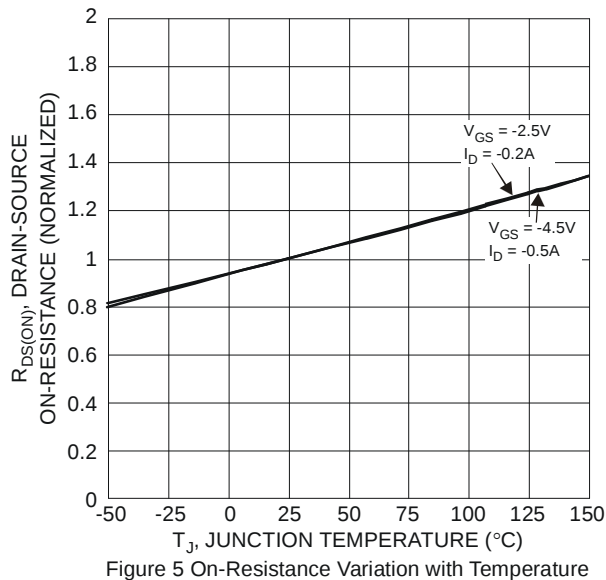
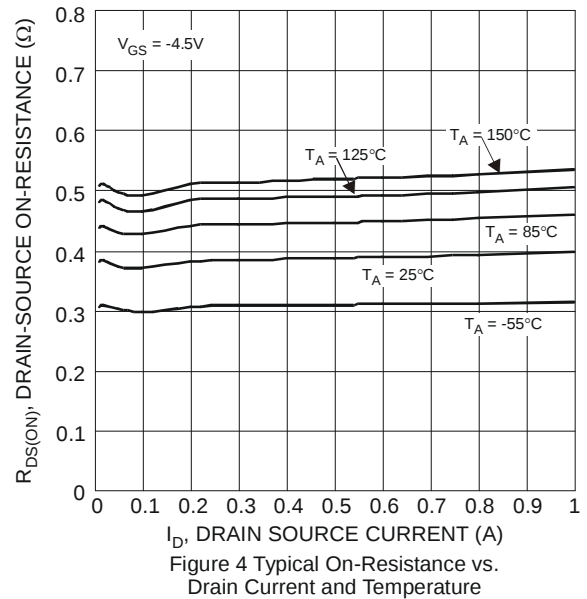
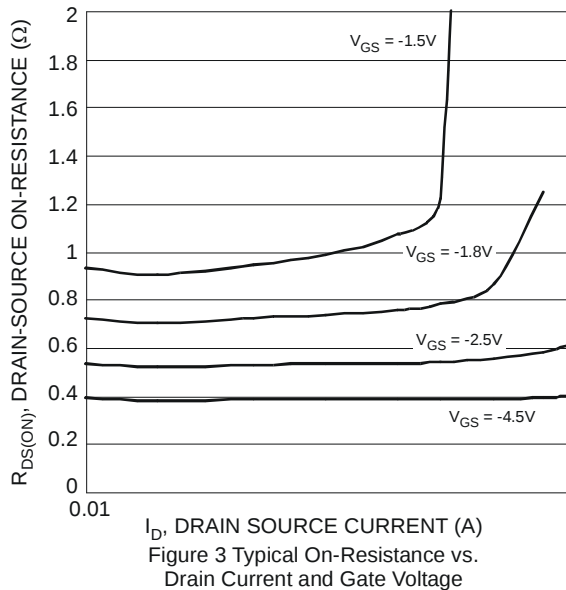
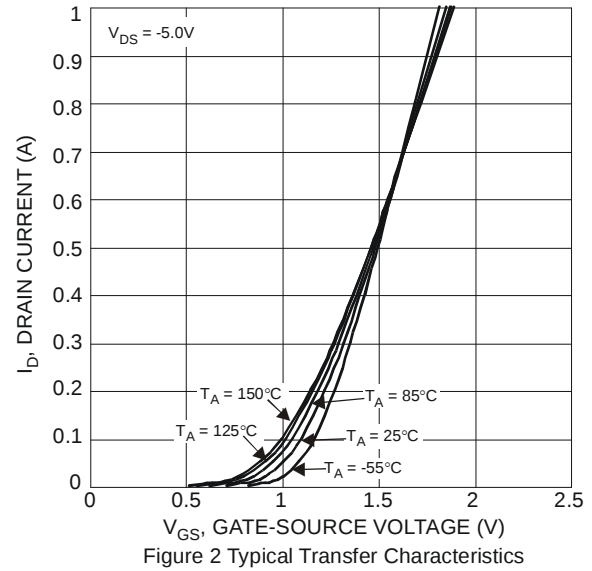
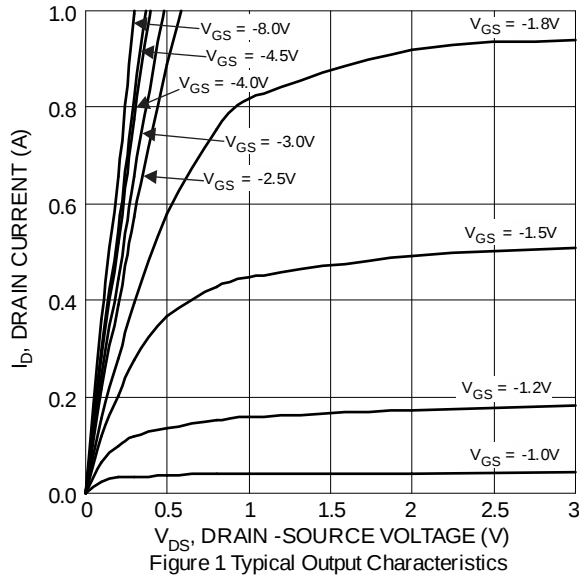
Thermal Characteristics

Characteristic	Symbol	Value	Units
Total Power Dissipation	P _D	0.36	W
Thermal Resistance, Junction to Ambient	R _{θJA}	353	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to 150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	-12	—	—	V	V _{GS} = 0V, I _D = -250μA
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	—	—	-1	μA	V _{DS} = -10V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±10	μA	V _{GS} = ±8V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(th)}	-0.4	—	-1.0	V	V _{DS} = V _{GS} , I _D = -250μA
Static Drain-Source On-Resistance	R _{DS(on)}	—	0.4	0.8	Ω	V _{GS} = -4.5V, I _D = -0.2A
		—	0.55	1.1		V _{GS} = -2.5V, I _D = -0.1A
		—	0.75	3.0		V _{GS} = -1.8V, I _D = -0.05A
		—	1.0	5.0		V _{GS} = -1.5V, I _D = -0.01A
Diode Forward Voltage	V _{SD}	—	—	-1.2	V	V _{GS} = 0V, I _S = -0.2A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	—	55.4	—	pF	V _{DS} = -10V, V _{GS} = 0V, f = 1MHz
Output Capacitance	C _{oss}	—	14.7	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	11.9	—	pF	
Total Gate Charge (V _{GS} = 4.5V)	Q _g	—	0.84	—	nC	V _{DS} = -6V, V _{GS} = -4.5V, I _D = -0.2A
Gate-Source Charge	Q _{gs}	—	0.12	—	nC	
Gate-Drain Charge	Q _{gd}	—	0.23	—	nC	
Turn-On Delay Time	t _{D(on)}	—	16	—	ns	V _{DD} = -6V, V _{GS} = -4.5V, I _D = -0.2A, R _G = 6Ω
Turn-On Rise Time	t _r	—	62	—	ns	
Turn-Off Delay Time	t _{D(off)}	—	232	—	ns	
Turn-Off Fall Time	t _f	—	186	—	ns	

- Notes:
- Device mounted on FR-4 PCB, with minimum recommended pad layout.
 - Device mounted on minimum recommended pad layout test board, 10μs pulse duty cycle = 1%.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing.



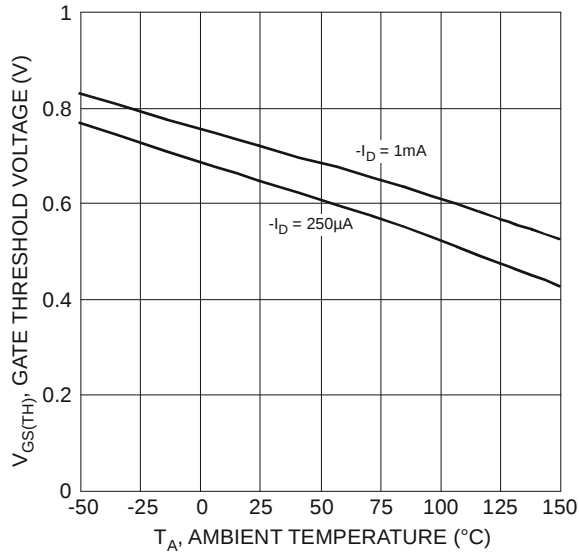


Figure 7 Gate Threshold Variation vs. Ambient Temperature

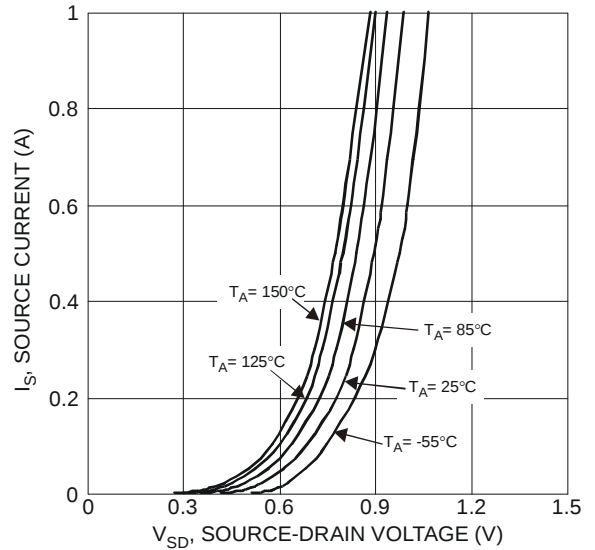


Figure 8 Diode Forward Voltage vs. Current

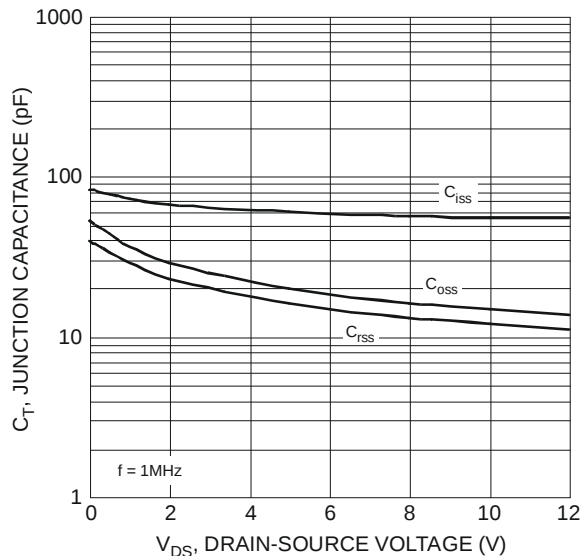


Figure 9 typical Junction Capacitance

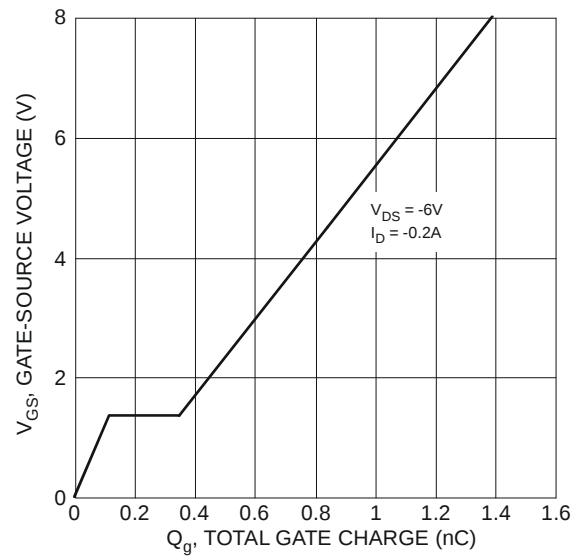


Figure 10 Gate-Charge Characteristics

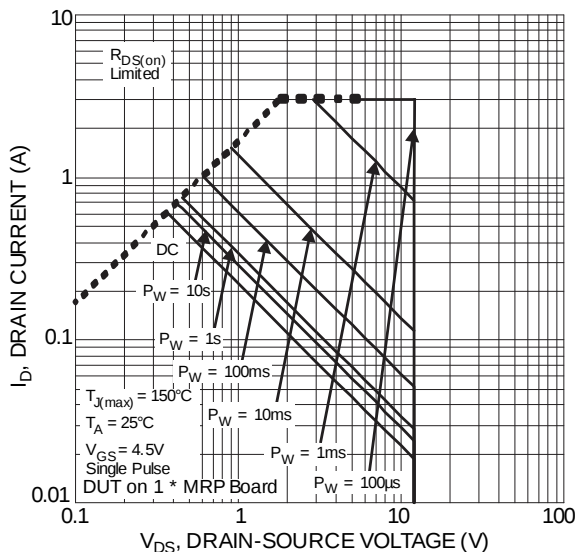
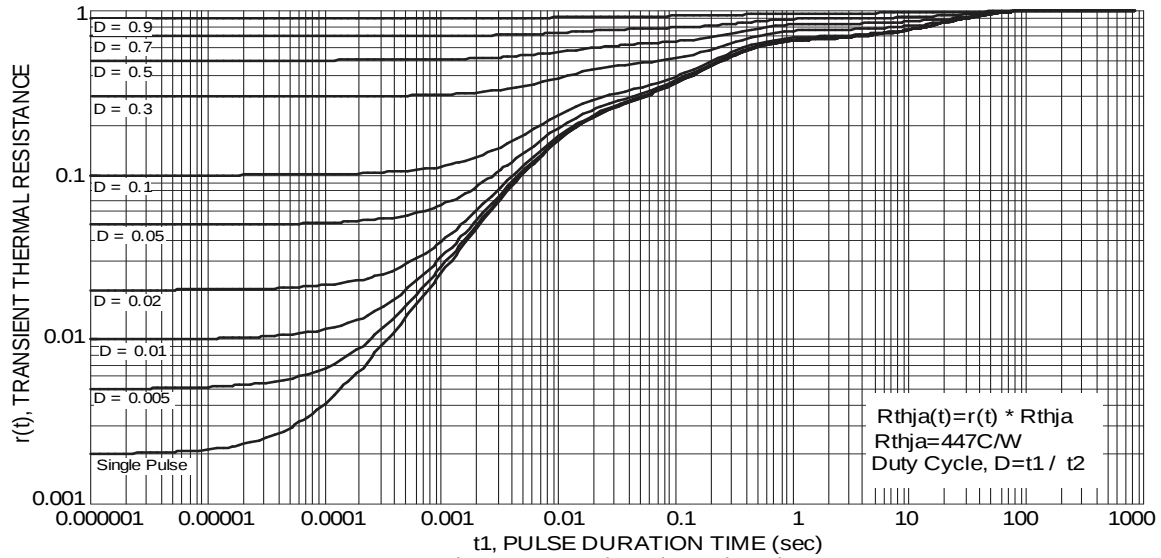
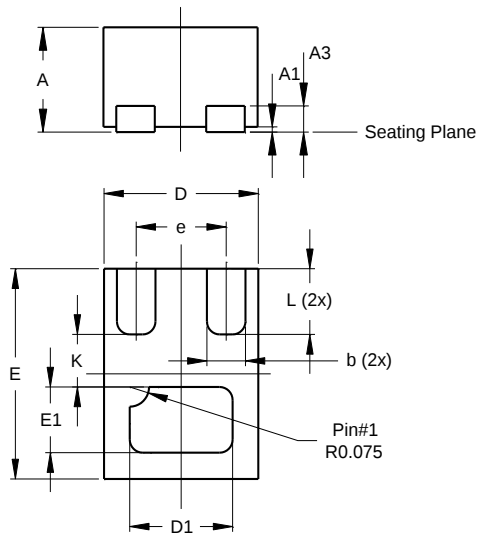


Figure 11 SOA, Safe Operation Area



Package Outline Dimensions

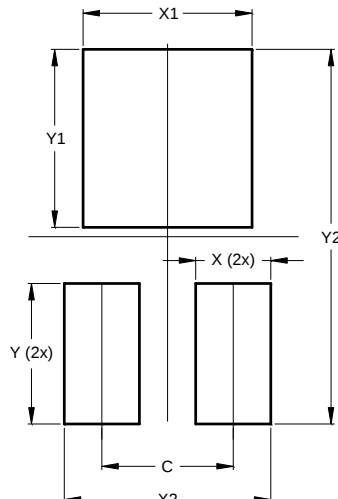
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.



X2-DFN0806-3			
Dim	Min	Max	Typ
A	0.375	0.40	0.39
A1	0	0.05	0.02
A3	-	-	0.10
b	0.10	0.20	0.15
D	0.55	0.65	0.60
D1	0.35	0.45	0.40
E	0.75	0.85	0.80
E1	0.20	0.30	0.25
e	-	-	0.35
K	-	-	0.20
L	0.20	0.30	0.25
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
C	0.350
X	0.200
X1	0.450
X2	0.550
Y	0.375
Y1	0.475
Y2	1.000

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