CS4234

4 In/5 Out CODEC with Programmable Class H Controller

DAC Features

- Advanced multibit Delta–Sigma modulator
- 24-bit resolution
- Differential or single-ended outputs
- -109 dB dynamic range (A-weighted)
- -90 dB THD+N
- 2 Vrms full-scale output into 3-kΩ AC load
- Rail-to-rail operation
- Programmable group delay in 4-channel audio output path

ADC Features

- Advanced multibit Delta–Sigma modulator
- 24-bit resolution
- Differential inputs
- -105 dB dynamic range (A-weighted)
- -88 dB THD+N
- 2 Vrms full-scale input

System Features

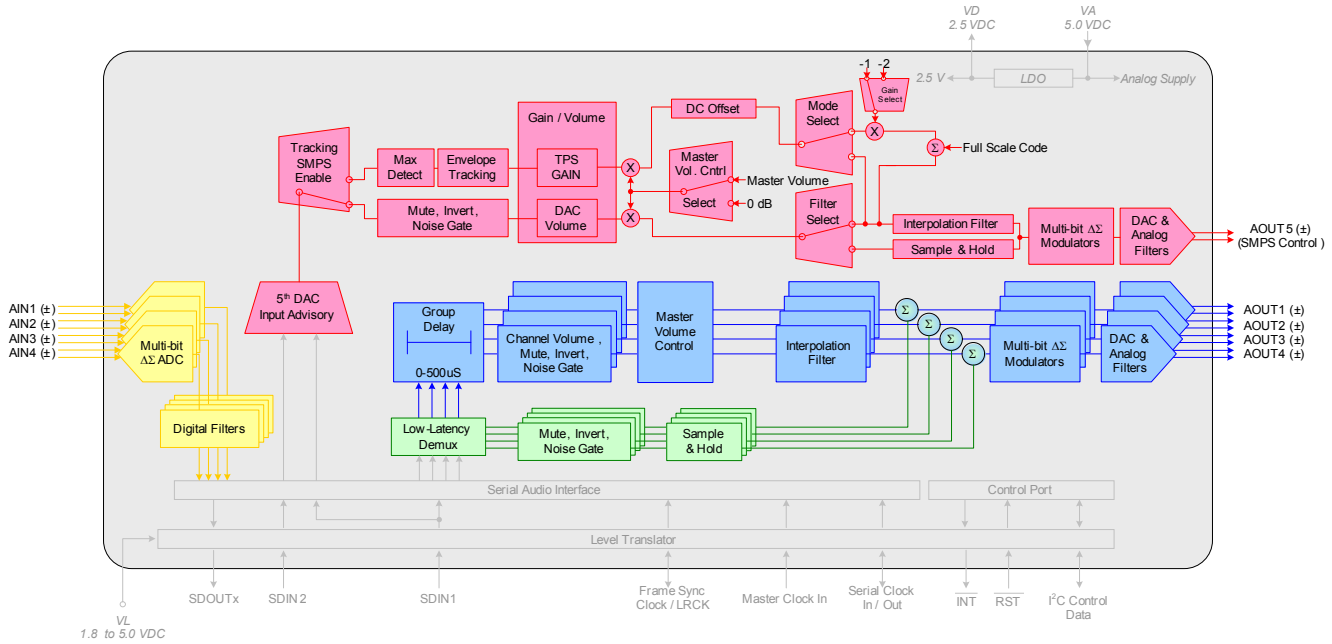
- TDM, left justified, and I^{2}S serial inputs and outputs
- Nondelayed low-latency path
- Supports sample rates up to 96 kHz

Class H Controller Features

- Can be used with any integrated Class AB amplifier IC or discrete amplifier solution.
- Increases efficiency of Class AB amplifiers
- Creates audio tracking reference signal for external switch-mode power supply
- Internal envelope tracking of up to 32 channels
- Input path for externally generated tracking signal

Common Applications

- Discrete Class H automotive audio amplifiers
- Automotive head units with internal Class H amplifiers
- Audio mixing consoles
- Audio effects processors



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General Description

The CS4234 is a highly versatile CODEC that combines 4 channels of high performance analog to digital conversion, 4 channels of high performance digital to analog conversion for audio, and 1 channel of digital to analog conversion to provide a nondelayed audio reference signal to an external Class H tracking power supply. If not used to drive a tracking power supply, the 5th DAC can instead be used as a standard audio grade DAC, with performance specifications identical to that of the 4 DACs in the audio path. Additionally, the CS4234 includes tunable group delay for each of the 4 audio DAC paths to provide lead time for the external switch-mode power supply, and a nondelayed path into the DAC outputs for input signals requiring a low-latency path to the outputs.

Targeting the automotive audio market, this controller was specifically designed to work with Apex Precision Power's CS44417 Class AB audio amplifier, but remains flexible enough to allow any standard Class AB amplifier to be operated as a Class H amplifier in order to maximize efficiency. Class H control provides significant efficiency gains over traditional Class AB amplifiers, while avoiding the increased electromagnetic interference (EMI) and cost of Class D amplifiers.

The Class H controller provides a reference signal which tracks the envelope of the maximum (on a sample by sample basis) of up to 32 channels of serial data in the TDM slots input on the SDINx lines. This reference signal is sent to the 5th DAC to create an analog reference signal for an external switch-mode power supply that supplies rail voltages to an external Class AB amplifier, thereby turning any standard Class AB amplifier into a Class H amplifier. If desired, the internal tracking power supply circuitry can be bypassed, which allows a DSP generated tracking signal to be used to control the SMPS. This feature allows an unlimited number of channels to be tracked, using a DSP to create the tracking signal.

This product is available in a 40-pin QFN package in Automotive (-40 °C to +105 °C) temperature grade. See "Ordering Information" on page 74 for complete details.

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1. PIN DESCRIPTIONS

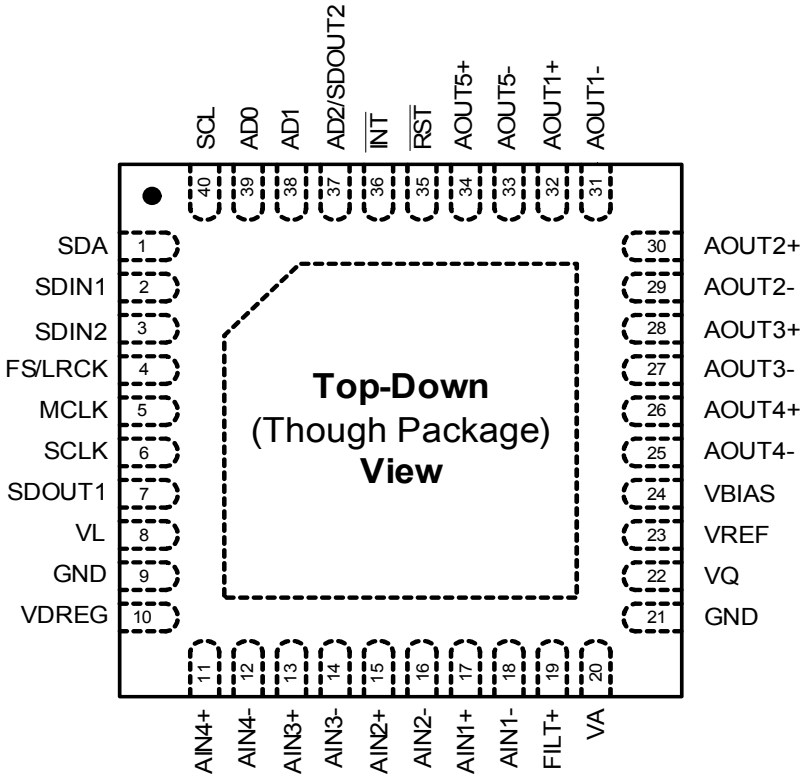


Figure 1. CS4234 Pinout

Pin Name	Pin #	Pin Description
SDA	1	**Serial Control Data** (*Input/Output*) - Bidirectional data I/O for the I²C control port.
SDINx	2,3	**Serial Data Input** (*Input*) - Input channels serial audio and low latency data.
FS/LRCK	4	**Frame Synchronization Clock/Left/Right Clock** (*Input/Output*) - Determines which channel or frame is currently active on the serial audio data line.
MCLK	5	**Master Clock** (*Input*) -Clock source for the internal logic, processing, and modulators.
SCLK	6	**Serial Clock** (*Input*/*Output*) -Serial Clock for the serial data port.
SDOUT1	7	**Serial Data Output 1** (*Output*) - ADC data output into a multi-slot TDM stream or AIN1 and AIN2 ADC data output in Left Justified and I²S modes.
VL	8	**Interface Power** (*Input*) - Positive power for the digital interface level shifters.
GND	9,21	**Ground** (*Input*) - Ground reference for the I/O and digital, analog sections.
VDREG	10	**Digital Power** (*Output*) - Internally generated positive power supply for digital section.
AINx+	11,13,15, 17	**Positive Analog Input** (*Input*) - Positive input signals to the internal analog to digital converters. The full scale analog input level is specified in the Analog Input Characteristics table.
AINx-	12,14,16, 18	**Negative Analog Input** (*Input*) - Negative input signals to the internal analog to digital converters. The full scale analog input level is specified in the Analog Input Characteristics table.
FILT+	19	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal ADCs.
VA	20	**Analog Power** (*Input*) - Positive power for the analog sections.
VQ	22	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
VREF	23	**Analog Power Reference** (*Input*) - Return pin for the VBIAS cap.

Pin Name	Pin #	Pin Description
VBIAS	24	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal DACs.
AOUTx-	25,27,29, 31, 33	**Negative Analog Output** (*Output*) - Negative output signals from the internal digital to analog converters. The full scale analog output level is specified in the Analog Output Characteristics table.
AOUTx+	26,28,30, 32, 34	**Positive Analog Output** (*Output*) - Positive output signals from the internal digital to analog converters. The full scale analog output level is specified in the Analog Output Characteristics table.
$\overline{\text{RST}}$	35	**Reset** (*Input*) - Applies reset to the internal circuitry when pulled low.
$\overline{\text{INT}}$	36	**Interrupt** (*Output*) - Sent to DSP to indicate an interrupt condition occurred.
AD2/SDOUT2	37	**I²C Address Bit 2/Serial Data Output 2** (*Input/Output*) - Sets the I²C address bit 2 at reset. Functions as Serial Data Out 2 for AIN3 and AIN4 ADC data output in Left Justified and I²S modes. High impedance in TDM mode. See Section 4.3 I²C Control Port for more details concerning this mode of operation.
AD1	38	**I²C Address Bit 1** (*Input*) - Sets the I²C address bit 1.
AD0	39	**I²C Address Bit 0** (*Input*) - Sets the I²C address bit 0.
SCL	40	**Serial Control Port Clock** (*Input*) - Serial clock for the I²C control port.
GND	-	**Thermal Pad** - The thermal pad on the bottom of the device should be connected to the ground plane via an array of vias.

1.1 I/O Pin Characteristics

Input and output levels and associated power supply voltage are shown in the table below. Logic levels should not exceed the corresponding power supply voltage.

Power Supply	Pin Name	I/O	Driver	Internal Connections (Note 1)	Receiver
VL	SCL	Input	-	Weak Pull-down (~500kΩ)	5.0 V CMOS, with Hysteresis
	SDA	Input/Output	CMOS/Open Drain	Weak Pull-down (~500kΩ)	5.0 V CMOS, with Hysteresis
	$\overline{\text{INT}}$	Output	CMOS/Open Drain	(Note 2)	-
	$\overline{\text{RST}}$	Input	-	(Note 2)	5.0 V CMOS, with Hysteresis
	MCLK	Input	-	Weak Pull-down (~500kΩ)	5.0 V CMOS, with Hysteresis
	FS/LRCK	Input/Output	5.0 V CMOS-	Weak Pull-down (~500kΩ)	5.0 V CMOS, with Hysteresis
	SCLK	Input/Output	5.0 V CMOS-	Weak Pull-down (~500kΩ)	5.0 V CMOS, with Hysteresis
	SDOUT1	Output	5.0 V CMOS	Weak Pull-down (~500kΩ)	
	SDINx	Input	-	Weak Pull-down (~500kΩ)	5.0 V CMOS, with Hysteresis
	AD0,1	Input	-	(Note 2)	5.0 V CMOS
	AD2/SDOUT2	Input/Output	5.0 V CMOS-	(Note 2)	5.0 V CMOS

Notes:

1. Internal connection valid when device is in reset.
2. This pin has no internal pull-up or pull-down resistors. External pull-up or pull-down resistors should be added in accordance with Figure 2.

2. TYPICAL CONNECTION DIAGRAM

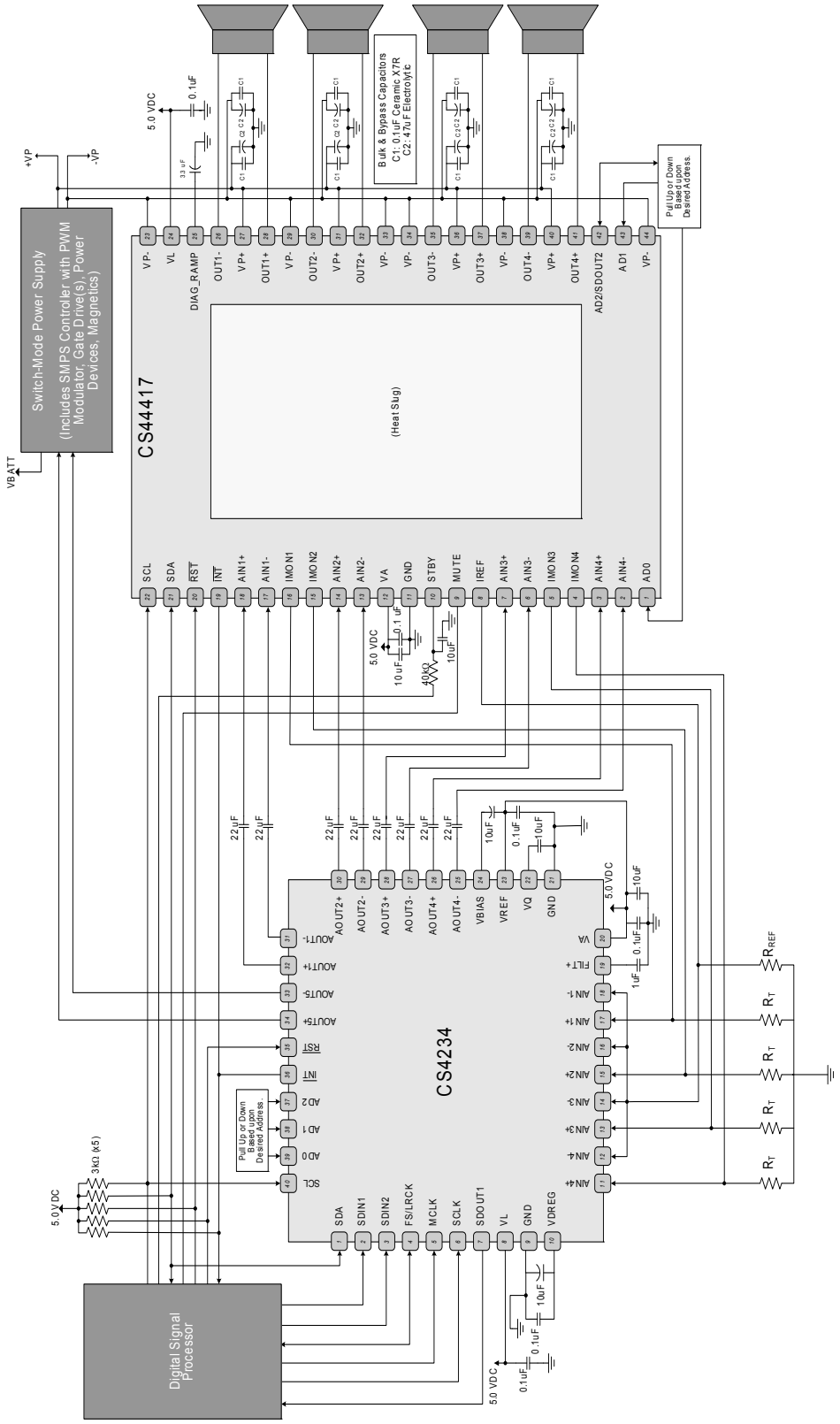


Figure 2. Typical Connection Diagram

3. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

GND = 0 V; all voltages with respect to ground. (Note 3)

Parameters	Symbol	Min	Typ	Max	Units
DC Power Supply					
Analog Core	VA	3.135 4.75	3.3 5	3.465 5.25	V V
Level Translator	VL	1.71	-	5.25	V
Temperature					
Ambient Operating Temperature - Power Applied	T_A	-40	-	+105	°C
Junction Temperature	T_J	-40	-	+150	°C

Notes: 3. Device functional operation is guaranteed within these limits. Functionality is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

ABSOLUTE MAXIMUM RATINGS

GND = 0 V; all voltages with respect to ground.

Parameters		Symbol	Min	Max	Units
DC Power Supply					
Analog Core		VA	-0.3	5.5	V
Level Translator		VL	-0.3	5.5	V
VDREG Current	(Note 4)	I_{VDREG}	-	10	µA
Inputs					
Input Current	(Note 5)	I_{in}	-	±10	mA
Analog Input Voltage	(Note 6)	V_{INA}	- 0.3	VA + 0.4	V
Logic Level Input Voltage	(Note 6)	V_{IND}	-0.3	VL + 0.4	V
Temperature					
Ambient Operating Temperature - Power Applied		T_A	-55	+125	°C
Storage Temperature		T_{stg}	-65	+150	°C

WARNING: OPERATION BEYOND THESE LIMITS MAY RESULT IN PERMANENT DAMAGE TO THE DEVICE.

Notes: 4. No external loads should be connected to the VDREG pin. Any connection of a load to this point may result in errant operation or performance degradation in the device.

5. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

6. The maximum over/under voltage is limited by the input current.

DC ELECTRICAL CHARACTERISTICS

GND = 0 V; all voltages with respect to ground.

Parameters	Min	Typ	Max	Units
VDREG (Note 7)				
Nominal Voltage	-	2.5	-	V
Output Impedance	-	0.5	-	Ω
FILT+				
Nominal Voltage	-	VA	-	V
Output Impedance	-	23	-	kΩ
DC Current Source/Sink	-	-	1	µA
VQ				
Nominal Voltage	-	0.5•VA	-	V
Output Impedance	-	77	-	kΩ
DC Current Source/Sink	-	-	0	µA

Notes:

7. No external loads should be connected to the VDREG pin. Any connection of a load to this point may result in errant operation or performance degradation in the device.

TYPICAL CURRENT CONSUMPTION

This table represents the power consumption for individual circuit blocks within the CS4234. CS4234 is configured as shown in Figure 2 on page 8. VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC; F_S = 100 kHz; MCLK = 25.6 MHz; DAC load is 3 kΩ; All input signals are zero (digital zero for SDINx inputs and AC coupled to ground for AINx inputs) .

	Functional Block	**VA/VL**	**Typical Current [mA] (unless otherwise noted)** (Note 9), (Note 12)	
			i_{VA}	i_{VL}
1	Reset Overhead (All lines held static, $\overline{RST}$ line pulled low.)	5	0.030	0.001
		3.3	0.020	0.001
2	Power Down Overhead (All lines clocks and data lines active, $\overline{RST}$ line pulled high, All PDNx bits set high.)	5	5	0.101
		3.3	5	0.101
3	PLL(Note 10) (Current drawn resulting from PLL being active. PLL is active for 256x and 384x)	5	1	-
		3.3	1	-
4	DAC Overhead (Current drawn whenever any of the five DACs are powered up.)	5	50	-
		3.3	45	-
5	DAC Channel (Note 8) (Current drawn per each DAC powered up.)	5	5	-
		3.3	4	-
6	ADC Overhead (Current drawn whenever any of the four ADCs are powered up.)	5	11	-
		3.3	11	-
7	ADC Group (Current drawn due to an ADC "group" being powered up. See (Note 11))	5	2	-
		3.3	2	-
8	ADC Channel (Current drawn per each ADC powered up.)	5	2	0.109
		3.3	2	0.066

Notes:

8. Full-scale differential output signal.
9. Current consumption increases with increasing F_S and increasing MCLK. Values are based on F_S of 100 kHz and MCLK of 25.6 MHz. Current variance between speed modes is small.
10. PLL is activated by setting the MCLK RATE bit to either 000 (operating in 256x mode) or 001 (operating in 384 kHz).
11. Internal to the CS4234, the analog to digital converters are grouped together in stereo pairs. ADC1 and ADC2 are grouped together as are ADC3 and ADC4. The ADC group current draw is the current that is drawn whenever one of these groups become active.
12. To calculate total current draw for an arbitrary amount of ADCs or DACs, the following equations apply:

Total Running Current Draw from VA Supply = *Power Down Overhead + PLL (If Applicable)+ DAC Current Draw + ADC Current Draw*

where

DAC Current Draw = DAC Overhead + (Number of DACs x DAC Channel)

ADC Current Draw = ADC Overhead + (Number of active ADC Groups x ADC Group) + (Number of active ADC Channels x ADC Channel)

and

Total Running Current Draw from VL Supply = *PDN Overhead + (Number of active ADC Channels x ADC Channel)*

ANALOG INPUT CHARACTERISTICS

Test Conditions (unless otherwise specified): Device configured as shown in Figure 2 on page 8. Input sine wave: 1 kHz; VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC.; T_A = -40 to +105 °C; Measurement Bandwidth is 20 Hz to 20 kHz unless otherwise specified; Sample Rate = 48 kHz; all Power Down ADCx bits = 0.

Parameter	VA, VREF = 3.3 V			VA, VREF = 5.0 V			Unit
	Min	Typ	Max	Min	Typ	Max	
Dynamic Range							
A-weighted	93	101	-	97	105	-	dB
unweighted	90	98	-	94	102	-	dB
Total Harmonic Distortion + Noise							
-1 dBFS	-	-95	-87	-	-88	-80	dB
-60 dBFS	-	-38	-30	-	-42	-34	dB
Other Analog Characteristics							
Interchannel Gain Mismatch	-	0.2	-	-	0.2	-	dB
Gain Drift	-	±100	-	-	±100	-	ppm/°C
Offset Error (Note 13)							
High Pass Filter On	-	0.0001	-	-	0.0001	-	% Full Scale
High Pass Filter Off	-	0.25	-	-	0.25	-	% Full Scale
Interchannel Isolation	-	90	-	-	90	-	dB
Full-scale Input Voltage (Differential Inputs)	1.58•VA	1.66•VA	1.74•VA	1.58•VA	1.66•VA	1.74•VA	Vpp
Input Impedance	-	40	-	-	40	-	kΩ
Common Mode Rejection (Differential Inputs)	-	60	-	-	60	-	dB
PSRR (Note 14) 1 kHz	-	45	-	-	45	-	dB
60 Hz	-	20	-	-	20	-	dB

Notes:

13. AINx+ connected to AINx-.
14. Valid with the recommended capacitor values on FILT+ and VQ. See Figure 4 for test configuration.

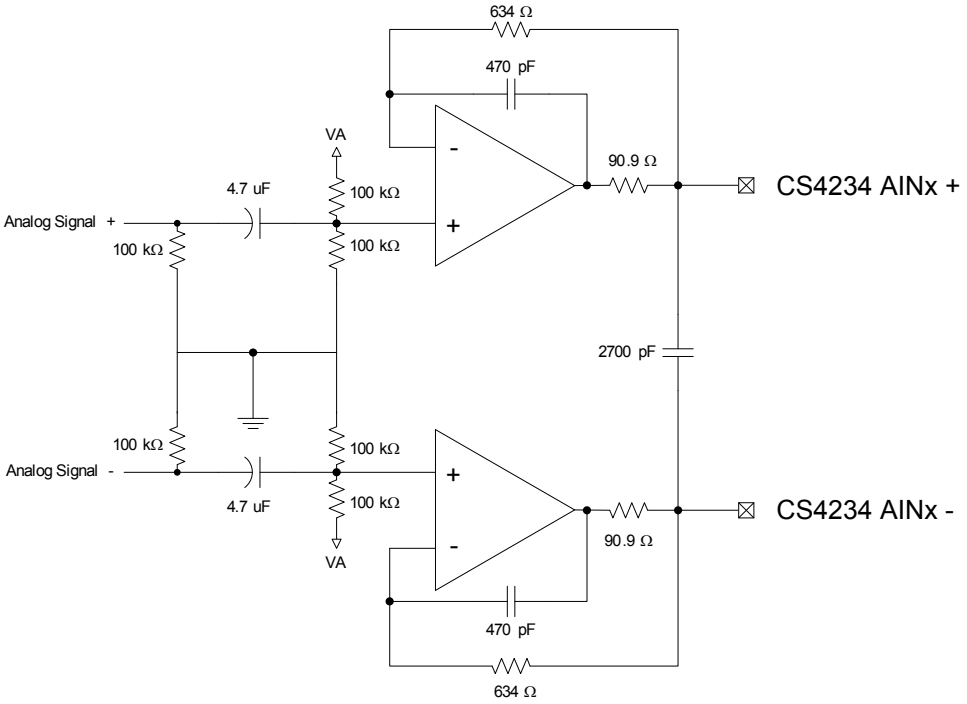


Figure 3. Test Circuit for ADC Performance Testing

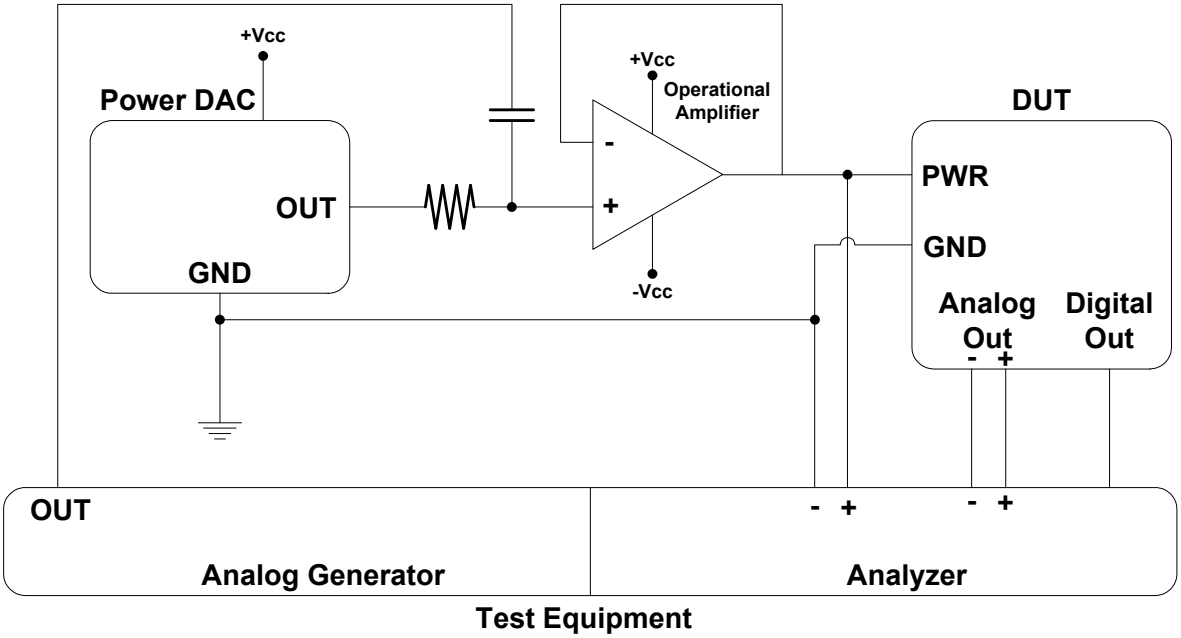


Figure 4. PSRR Test Configuration

ADC DIGITAL FILTER CHARACTERISTICS

Test Conditions (unless otherwise specified): Device configured as shown in Section 2. on page 8. Input sine wave: 1 kHz; VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC.; T_A = -40 to +105 °C; Measurement Bandwidth is 20 Hz to 20 kHz unless otherwise specified. See filter plots in Section 7. on page 70.

Parameter (Note 15)		Min	Typ	Max	Unit
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.4535	Fs
Passband Ripple		-0.09	-	0.17	dB
Stopband		0.6	-	-	Fs
Stopband Attenuation		70	-	-	dB
Single-Speed Mode					
ADC Group Delay (Note 16)		-	9.5/Fs	-	s
***High-Pass Filter Characteristics* (48 kHz Fs)**					
Frequency Response	-3.0 dB -0.13 dB	- -	2 11	- -	Hz Hz
Phase Deviation	@ 20 Hz	-	10	-	Deg
Passband Ripple		-0.09	-	0.17	dB
Filter Settling Time (Note 17)		-	25000/Fs	-	s
Double-Speed Mode					
ADC Group Delay (Note 16)		-	9.5/Fs	-	s
***High-Pass Filter Characteristics* (96 kHz Fs)**					
Frequency Response	-3.0 dB -0.13 dB	- -	4 22	- -	Hz Hz
Phase Deviation	@ 20 Hz	-	10	-	Deg
Passband Ripple		-0.15	-	0.17	dB
Filter Settling Time (Note 17)		-	25000/Fs	-	s

Note:

15. Response is clock dependent and will scale with Fs.
16. The ADC group delay is measured from the time the analog inputs are sampled on the AINx pins to the FS/LRCK rising transition after the last bit of that group of samples has been transmitted on SDOUT1.
17. The amount of time from input of half-full-scale step function until the filter output settles to 0.1% of full scale.

ANALOG OUTPUT CHARACTERISTICS

Test Conditions (unless otherwise specified): Device configured as shown in Section 2. on page 8. VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC.; T_A = -40 to +105 °C; Full-scale 1 kHz input sine wave; Sample Rate = 48 kHz; Measurement Bandwidth is 20 Hz to 20 kHz; Specifications apply to all channels unless otherwise indicated; all Power Down DACx bits = 0. See (Note 19).

Parameter		VA, VREF= 3.3 V (Differential/Single-ended) Min	Typ	Max	VA, VREF= 5.0 V (Differential/Single-ended) Min	Typ	Max	Unit
Dynamic Performance								
Dynamic Range								
18 to 24-Bit	A-weighted	98/94	106/102	-	101/97	109/105	-	dB
	unweighted	95/91	103/99	-	98/94	106/102	-	dB
16-Bit	A-weighted	87	95	-	87	95	-	dB
	unweighted	84	92	-	84	92	-	dB
Total Harmonic Distortion + Noise		-	-90/-88	-82/-80	-	-90/-88	-82/-80	dB
Full-scale Output Voltage		1.48•VA/ 0.74•VA	1.56•VA/ 0.78•VA	1.64•VA/ 0.82•VA	1.48•VA/ 0.74•VA	1.56•VA/ 0.78•VA	1.64•VA/ 0.82•VA	Vpp
Interchannel Isolation (1 kHz)		-	100	-	-	100	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)(Note 19)		3	-	-	3	-	-	kΩ
Load Capacitance (C_L)(Note 19)		-	-	100	-	-	100	pF
Parallel DC-Load Resistance(Note 20)		10	-	-	10	-	-	kΩ
Output Impedance		-	100	-	-	100	-	Ω
PSRR (Note 21)	1 kHz	-	60	-	-	60	-	dB
	60 Hz	-	60	-	-	60	-	dB

Notes:

18. One LSB of triangular PDF dither added to data.
19. Loading configuration is given in Figure 5 below.

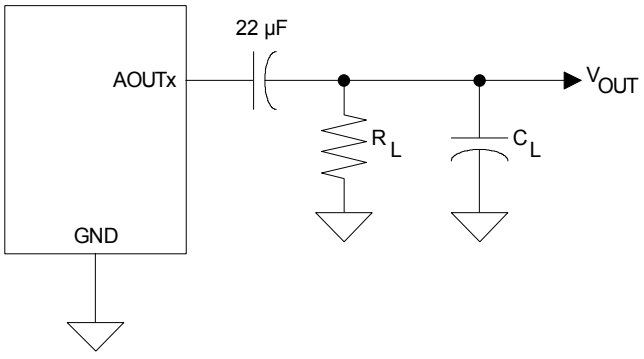


Figure 5. Equivalent Output Test Load

20. Parallel combination of all DAC DC loads. See Section 4.2.3.
21. Valid with the recommended capacitor values on FILT+ and VQ. See Figure 4 for test configuration.

COMBINED DAC INTERPOLATION AND ON-CHIP ANALOG FILTER RESPONSE

Test Conditions (unless otherwise specified): VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC. The filter characteristics have been normalized to the sample rate (F_S) and can be referenced to the desired sample rate by multiplying the given characteristic by F_S. See filter plots in Section 8. on page 71.

Parameter		Min	Typ	Max	Unit
Single-Speed Mode					
Passband (Note 22)	to -0.05 dB corner to -3 dB corner	0 0	- -	0.4780 0.4996	F_S F_S
Frequency Response 20 Hz to 20 kHz		-0.01	-	+0.12	dB
StopBand		0.5465	-	-	F_S
StopBand Attenuation	(Note 23)	102	-	-	dB
DAC1-4 Group Delay (Note 24) (Note 25)		-	11/Fs	-	s
DAC5 Group Delay (Note 25) (w/ interpolation filter) (w/ sample and hold)		 - -	 11/Fs 2/Fs	 - -	 s s
Low-Latency Group Delay (Note 25)		-	2/Fs	-	s
Double-Speed Mode					
Passband (Note 22)	to -0.1 dB corner to -3 dB corner	0 0	- -	0.4650 0.4982	F_S F_S
Frequency Response 20 Hz to 20 kHz		-0.05	-	+0.2	dB
StopBand		0.5770	-	-	F_S
StopBand Attenuation	(Note 23)	80	-	-	dB
DAC1-4 Group Delay (Note 24) (Note 25)		-	7/Fs	-	s
DAC5 Group Delay (Note 25) (w/ interpolation filter) (w/ sample and hold)		 - -	 7/Fs 2.5/Fs	 - -	 s s
Low-latency Group Delay (Note 25)		-	2.5/Fs	-	s

22. Response is clock dependent and will scale with F_S.
23. For Single-Speed Mode, the measurement bandwidth is 0.5465 F_S to 3 F_S.
    For Double-Speed Mode, the measurement bandwidth is 0.577 F_S to 1.4 F_S.
24. This specification is in addition to any delay added via the “GROUP DELAY[3:0]” bits in the "TPS Control" register.
25. The DAC group delay is measured from the FS/LRCK rising transition before the first bit of a group of samples is transmitted on the SDINx pins to the time it appears on the AOUTx pins.

DIGITAL I/O CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
High-Level Input Voltage (all input pins except $\overline{RST}$) (VL = 1.8 V)	(% of VL)	V_{IH}	75%	-	-	V
High-Level Input Voltage (all input pins except $\overline{RST}$) (VL = 2.5 V, 3.3 V, or 5 V)	(% of VL)	V_{IH}	70%	-	-	V
Low-Level Input Voltage (all input pins except $\overline{RST}$)	(% of VL)	V_{IL}	-	-	30%	V
High-Level Input Voltage ($\overline{RST}$ pin)		V_{IH}	1.2	-	-	V
Low-Level Input Voltage ($\overline{RST}$ pin)		V_{IL}	-	-	0.3	V
High-Level Output Voltage at I_o = 2 mA	(% of VL)	V_{OH}	80%	-	-	V
Low-Level Output Voltage at I_o = 2 mA	(% of VL)	V_{OL}	-	-	20%	V
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance			-	8	-	pF

SWITCHING CHARACTERISTICS - SERIAL AUDIO INTERFACE

VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC.

Parameters		Symbol	Min	Max	Units
$\overline{RST}$ pin Low Pulse Width	(Note 26)		1	-	ms
MCLK Frequency	(Note 27)		7.68	25.6	MHz
MCLK Duty Cycle			45	55	%
SCLK Duty Cycle			45	55	%
Input Sample Rate (FS/LRCK pin)	Single-Speed Mode	F_S	30	50	kHz
	Double-Speed Mode	F_S	60	100	kHz
SCLK Falling Edge to SDOUTx Valid (VL = 1.8 V)		t_{dh2}	-	31	ns
SCLK Falling Edge to SDOUTx Valid (VL = 2.5 V)		t_{dh2}	-	22	ns
SCLK Falling Edge to SDOUTx Valid (VL = 3.3 V or 5 V)		t_{dh2}	-	17	ns
TDM Slave Mode					
SCLK Frequency	(Note 28)		256x	512x	F_S
FS/LRCK High Time Pulse	(Note 29)	t_{lpw}	$1/f_{SCLK}$	$(n-1)/f_{SCLK}$ (Note 30)	ns
FS/LRCK Rising Edge to SCLK Rising Edge		t_{lcks}	5	-	ns
SDINx Setup Time Before SCLK Rising Edge		t_{ds}	3	-	ns
SDINx Hold Time After SCLK Rising Edge		t_{dh1}	5	-	ns
PCM Slave Mode					
SCLK Frequency			32x	64x	F_S
FS/LRCK Duty Cycle			45	55	%
FS/LRCK Edge to SCLK Rising Edge		t_{lcks}	5	-	ns
SDINx Setup Time Before SCLK Rising Edge		t_{ds}	3	-	ns
SDINx Hold Time After SCLK Rising Edge		t_{dh1}	5	-	ns
PCM Master Mode					
SCLK Frequency			64x	64x	F_S
FS/LRCK Duty Cycle			45	55	%
FS/LRCK Edge to SCLK Rising Edge		t_{lcks}	5	-	ns
SDINx Setup Time Before SCLK Rising Edge		t_{ds}	5	-	ns
SDINx Hold Time After SCLK Rising Edge (VL = 1.8 V)		t_{dh1}	11	-	ns
SDINx Hold Time After SCLK Rising Edge (VL = 2.5 V, 3.3 V, or 5 V)		t_{dh1}	10	-	ns

Notes:

26. After applying power to the CS4234, $\overline{RST}$ should be held low until after the power supplies and MCLK are stable.
27. MCLK must be synchronous to and scale with F_S.
28. The SCLK frequency must remain less than or equal to the MCLK frequency. For this reason, SCLK may range from 256x to 512x only in single speed mode. In double speed mode, 256x is the only ratio supported.
29. The MSB of CH1 is always aligned with the second SCLK rising edge following FS/LRCK rising edge.
30. Where “n” is equal to the MCLK to LRCK ratio (set by the Master Clock Rate register bits), i.e. in 256x mode, n = 256, in 512x mode, n = 512, etc.

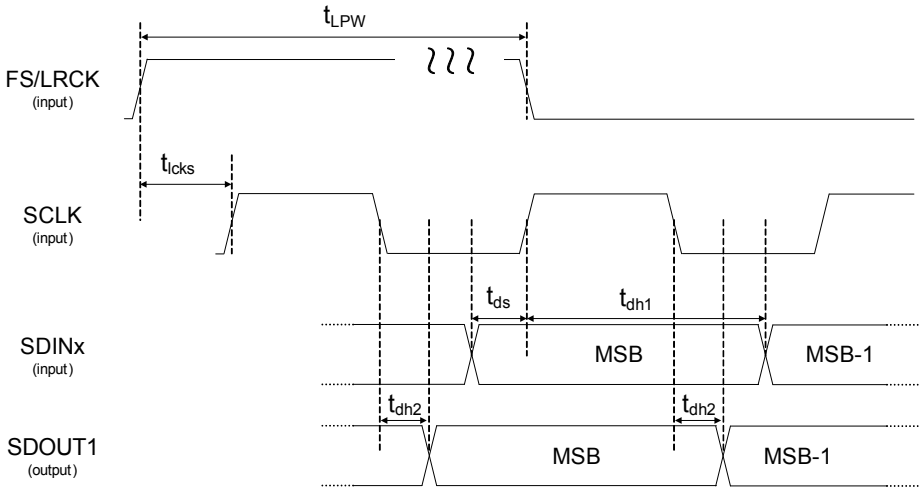


Figure 6. TDM Serial Audio Interface Timing

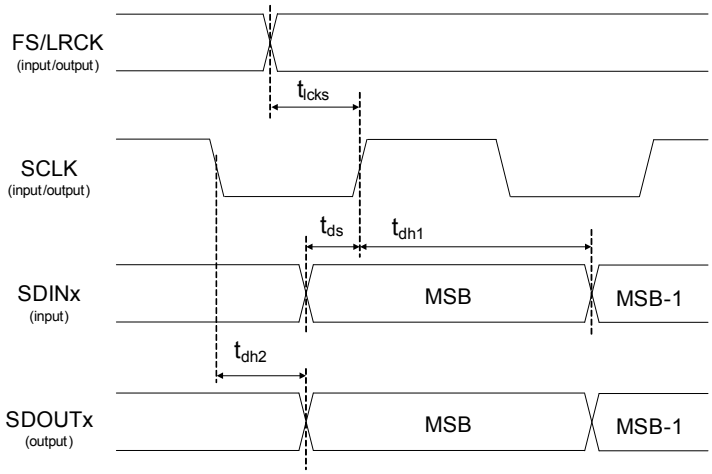


Figure 7. PCM Serial Audio Interface Timing

SWITCHING SPECIFICATIONS - CONTROL PORT

Test conditions (unless otherwise specified): Inputs: Logic 0 = GND = 0 V, Logic 1 = VL; SDA load capacitance equal to maximum value of C_b specified below (Note 31).

Parameters	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	550	kHz
$\overline{\text{RESET}}$ Rising Edge to Start	t_{irs}	(Note 32)	-	ns
Bus Free Time Between Transmissions	t_{buf}	1.3	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	0.6	-	µs
Clock Low time	t_{low}	1.3	-	µs
Clock High Time	t_{high}	0.6	-	µs
Setup Time for Repeated Start Condition	t_{sust}	0.6	-	µs
SDA Input Hold Time from SCL Falling (Note 33)	t_{hddi}	0	0.9	µs
SDA Output Hold Time from SCL Falling	t_{hddo}	0.2	0.9	µs
SDA Setup time to SCL Rising	t_{sud}	100	-	ns
Rise Time of SCL and SDA	t_r	-	300	ns
Fall Time SCL and SDA	t_f	-	300	ns
Setup Time for Stop Condition	t_{susp}	0.6	-	µs
SDA Bus Load Capacitance	C_b	-	400	pF
SDA Pull-Up Resistance	R_p	500	-	Ω

Notes:

31. All specifications are valid for the signals at the pins of the CS4234 with the specified load capacitance.
32. 2 ms + (3000/MCLK). See Section 4.2.1.
33. Data must be held for sufficient time to bridge the transition time, t_f, of SCL.

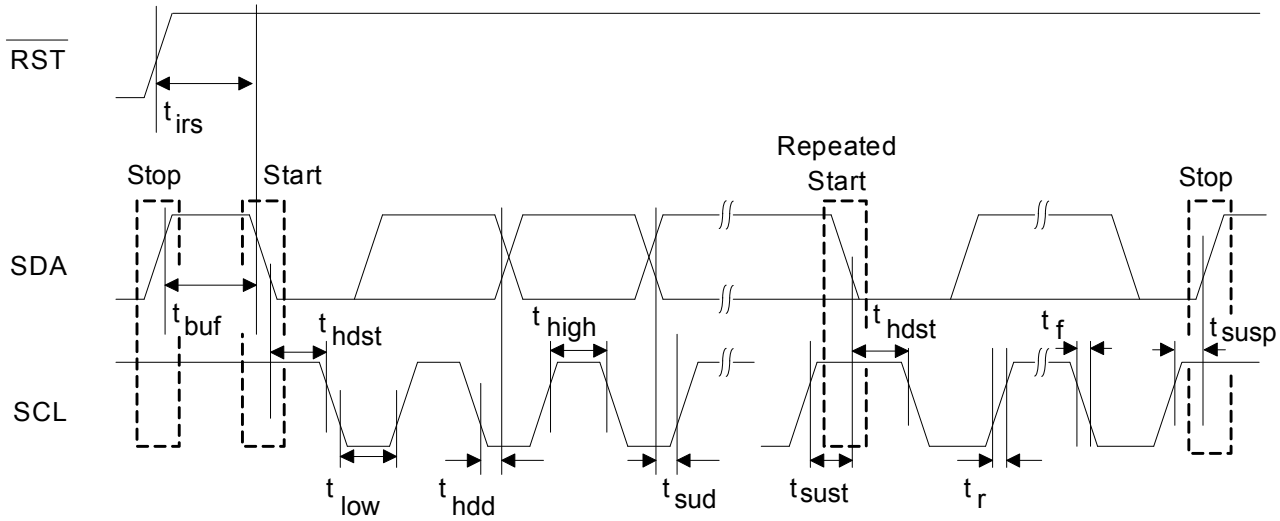


Figure 8. I²C Control Port Timing

4. APPLICATIONS

4.1 Power Supply Decoupling, Grounding, and PCB Layout

As with any high-resolution converter, the CS4234 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 2 shows the recommended power arrangements, with VA connected to clean supplies. VDREG, which powers the digital circuitry, is generated internally from an on-chip regulator from the VA supply. The VDREG pin provides a connection point for the decoupling capacitors, as shown in Figure 2.

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be as near to the pins of the CS4234 as possible. The low value ceramic capacitor should be the nearest to the pin and should be mounted on the same side of the board as the CS4234 to minimize inductance effects. All signals, especially clocks, should be kept away from the FILT+, VBIAS, and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+, VBIAS, and VQ decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from their respective pins and GND.

For optimal heat dissipation from the package, it is recommended that the area directly under the device be filled with copper and tied to the ground plane. The use of vias connecting the topside ground to the backside ground is also recommended.

4.2 Recommended Power-Up and Power-Down Sequence

The initialization and Power-Up/Down sequence flow chart is shown in Figure 9. For the CS4234 Reset is defined as all lines held static, $\overline{\text{RST}}$ line is pulled low. Power Down is defined as all lines (excluding MCLK) held static, $\overline{\text{RST}}$ line is high, all PDNx bits are ‘1’. Running is defined as $\overline{\text{RST}}$ line high, all PDNx bits are ‘0’.

4.2.1 Power-up

The CS4234 enters a reset state upon the initial application of VA and VL. When these power supplies are initially applied to the device, the audio outputs, AOUTxx, are clamped to VQ which is initially low. Additionally, the interpolation and decimation filters, delta-sigma modulators and control port registers are all reset and the internal voltage reference, multi-bit digital-to-analog and analog-to-digital converters and low-pass filters are powered down. The device remains in the reset state until the $\overline{\text{RST}}$ pin is brought high.

Once $\overline{\text{RST}}$ is brought high, the control port address is latched after 2 ms + (3000/MCLK). Until this latching transition is complete, the device will not respond to I²C reads or writes, but the I²C bus may still be used during this time. Once the latching transition is complete, the address is latched and the control port is accessible. At this point and the desired register settings can be loaded per the interface descriptions detailed in the Section 4.3 I²C Control Port. To ensure specified performance and timing, the VA_SEL must be set to “0” for VA = 3.3 VDC and “1” for VA = 5.0 VDC before audio output begins.

After the $\overline{\text{RST}}$ pin is brought high and MCLK is applied, the outputs begin to ramp with VQ towards the nominal quiescent voltage. VQ will charge to VA/2 upon initial power up. The time that it takes to charge up to VA/2 is governed by the size of the capacitor attached to the VQ pin. With the capacitor value shown in the typical connection diagram, the charge time will be approximately 250 ms. The gradual voltage ramping allows time for the external DC-blocking capacitors to charge to VQ, effectively blocking the quiescent DC voltage. Once FS/LRCK is valid, MCLK occurrences are counted over one F_S period to determine the MCLK/F_S ratio. With MCLK valid and any of the PDNx bits cleared, the internal voltage references will transition to their nominal voltage. Power is applied to the D/A converters and filters, and the analog outputs are unclamped from the quiescent voltage, VQ. Afterwards, normal operation begins.

4.2.2 Power-down

To prevent audio transients at power-down, the DC-blocking capacitors must fully discharge before turning off the power. In order to do this in a controlled manner, it is recommended that all the converters be muted to start the sequence. Next, set PDNx for all converters to 1 to power them down internally. Then, FS/LRCK and SCLK can be removed if desired. Finally, the "VQ RAMP" bit in the "DAC Control 4" register must be set to '1' for a period of 50 ms before applying reset or removing power or MCLK. During this time, voltage on VQ and the audio outputs discharge gradually to GND. If power is removed before this 50 ms time period has passed, a transient will occur and a slight click or pop may be heard. There is no minimum time for a power cycle. Power may be reapplied at any time.

It is important to note that all clocks should be applied and removed in the order specified in Figure 9. If MCLK is removed or applied before $\overline{\text{RST}}$ has been pulled low, audible pops, clicks and/or distortion can result. If either SCLK or FS/LRCK is removed or applied before all PDNx bits are set to "1", audible pops, clicks and/or distortion can result.

Note: Timings are approximate and based upon the nominal value of the passive components specified in the "Typical Connection Diagram" on page 8. See Section 4.6.6.2 for volume ramp behavior.

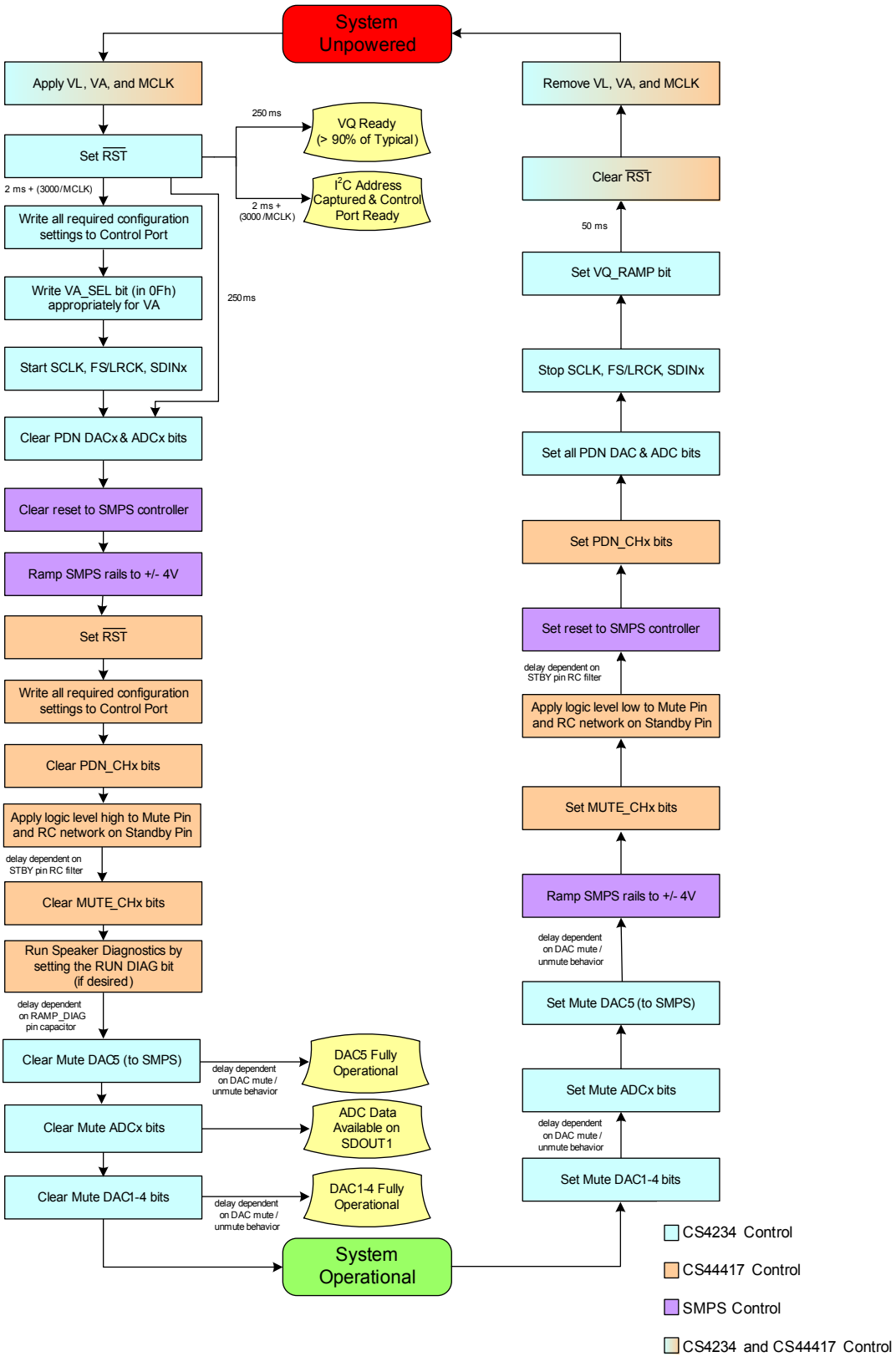


Figure 9. System Level Initialization and Power-up / Power-down Sequence

4.2.3 DAC DC Loading

Figure 10 shows the analog output configuration during power-up, with the AOUTx± pins clamped to VQ to prevent pops and clicks. Thus any DC loads (RL_x) on the output pins will be in parallel when the switches are closed. These DC loads will pull the VQ voltage down towards ground. If the parallel combination of all DC loads exceeds the specification shown in the Analog Output Characteristics table, the VQ voltage will never rise to its minimum operating voltage. If the VQ voltage never rises above this minimum operating voltage, the device will not finish the power-up sequence and normal operation will not begin.

Also note that any AOUTx± pin(s) with a DC load must remain powered up (PDN DACx = 0) to keep the VQ net at its nominal voltage during normal operation, otherwise clipping may occur on the outputs.

Note that the load capacitors (CL_x) are also in parallel during power-up. The amount of total capacitance on the VQ net during power-up will affect the amount of time it takes for the VQ voltage to rise to its nominal operating voltage after VA power is applied. The time period can be calculated using the time constant given by the internal series resistor and the load capacitors.

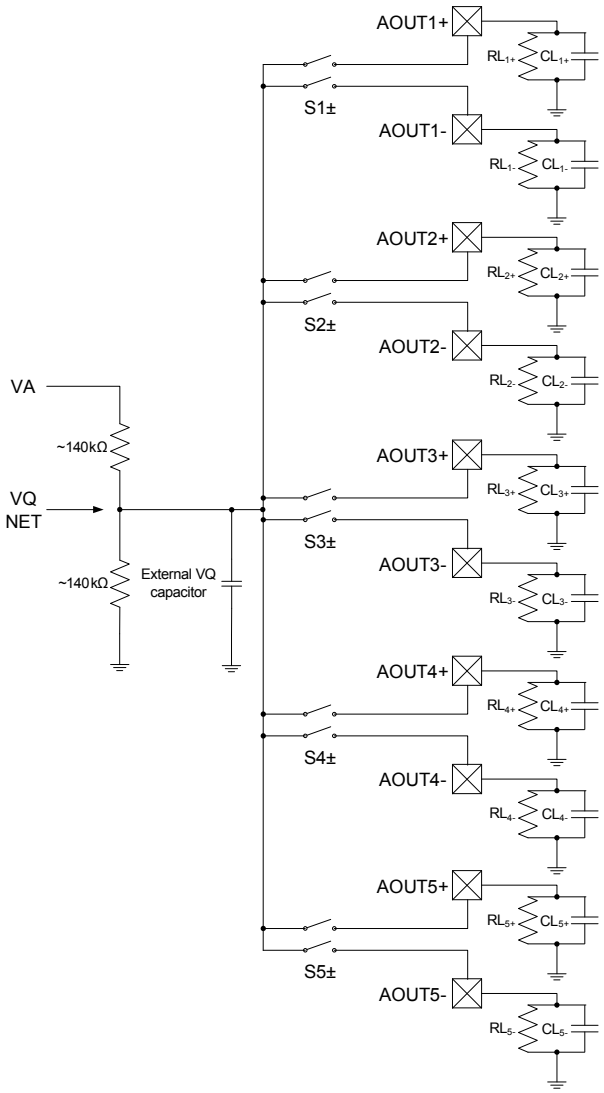


Figure 10. DAC DC Loading

4.3 I²C Control Port

All device configuration is achieved via the I²C control port registers as described in the Switching Specifications - Control Port table. The operation via the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the I²C pins should remain static if no operation is required. The CS4234 acts as an I²C slave device.

SDA is a bidirectional data line. Data is clocked into and out of the device by the clock, SCL. The ADx pins form the least significant bits of the chip address and should be connected through a resistor to VL or GND as desired. The state of these pins are sensed after the CS4234 is released from reset.

The signal timings for a read and write cycle are shown in Figure 11 and Figure 12. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS4234 after a Start condition consists of a 7-bit chip address field and a R/$\overline{W}$ bit (high for a read, low for a write). The upper 4 bits of the 7-bit address field are fixed at 0010. To communicate with a CS4234, the chip address field, which is the first byte sent to the CS4234, should match 0010 followed by the settings of the ADx pins. The eighth bit of the address is the R/$\overline{W}$ bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS4234 after each input byte is read, and is input to the CS4234 from the microcontroller after each transmitted byte.

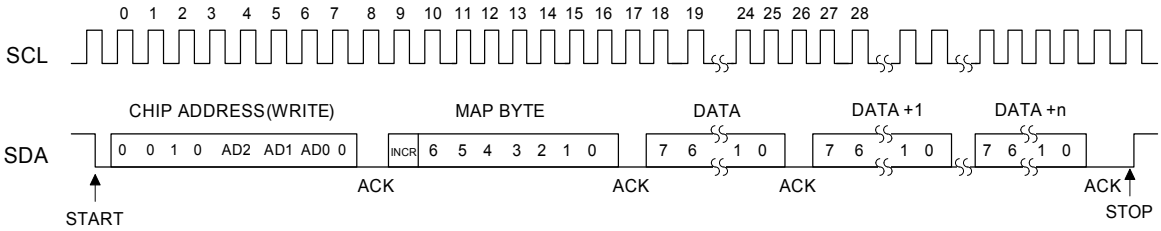


Figure 11. Timing, I²C Write

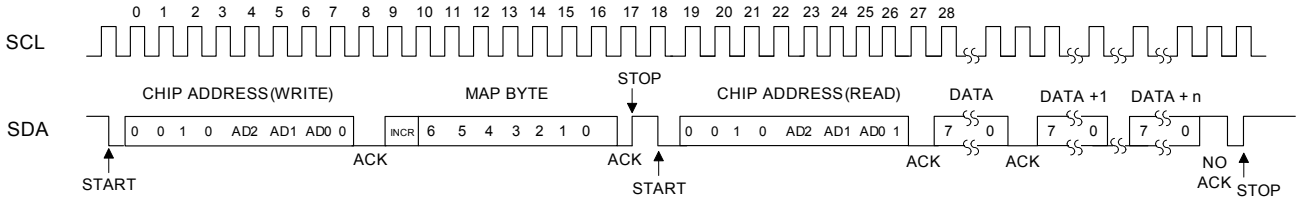


Figure 12. Timing, I²C Read

Since the read operation can not set the MAP, an aborted write operation is used as a preamble. As shown in Figure 12, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.
Send 0010xxx0 (chip address and write operation).
Receive acknowledge bit.
Send MAP byte, auto increment off.

Receive acknowledge bit.
Send stop condition, aborting write.
Send start condition.
Send 0010xxx1 (chip address and read operation).
Receive acknowledge bit.
Receive byte, contents of selected register.
Send acknowledge bit.
Send stop condition.

Setting the auto increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

4.3.1 Memory Address Pointer (MAP)

The MAP byte comes after the address byte and selects the register to be read or written. Refer to the pseudocode above for implementation details.

4.3.1.1 Map Increment (INCR)

The CS4234 has MAP auto-increment capability enabled by the INCR bit (the MSB) of the MAP. If INCR is set to '0', MAP will stay constant for successive I²C reads or writes. If INCR is set to '1', MAP will auto-increment after each byte is read or written, allowing block reads or writes of successive registers.

4.4 System Clocking

The CS4234 will operate at sampling frequencies from 30 kHz to 100 kHz. This range is divided into two speed modes as shown in Table 1.

Mode	Sampling Frequency
Single-Speed	30-50 kHz
Double-Speed	60-100 kHz

Table 1. Speed Modes

The serial port clocking must be changed while all PDNx bits are set. If the clocking is changed otherwise, the device will enter a mute state, see Section 4.8 on page 47.

4.4.1 Master Clock

The ratio of the MCLK frequency to the sample rate must be an integer. The FS/LRCK frequency is equal to F_S, the frequency at which all of the slots of the TDM stream or channels in Left Justified or I²S formats are clocked into or out of the device. The Speed Mode and Master Clock Rate bits configure the device to generate the proper clocks in Master Mode and receive the proper clocks in Slave Mode. Table 2 illustrates several standard audio sample rates and the required MCLK and FS/LRCK frequencies.

The CS4234 has an internal fixed ratio PLL. This PLL is activated when the "MCLK RATE[2:0]" bits in the "Clock and SP Sel." register are set to either 000 or 001, corresponding to 256x or 384x. When in either of these two modes, the PLL will activate to adjust the frequency of the incoming MCLK to ensure that the internal state machines operate at a nominal 24.576 MHz rate. As is shown in the Typical Current Consumption table, activation of the PLL will increase the power consumption of the CS4234.

FS/LRCK (kHz)	MCLK (MHz)				
	128x (Note 34)	192x (Note 34)	256x	384x	512x
32	-	-	8.1920	12.2880	16.3840
44.1	-	-	11.2896	16.9344	22.5792
48	-	-	12.2880	18.4320	24.5760
64	8.1920	12.2880	16.3840	-	-
88.2	11.2896	16.9344	22.5792	-	-
96	12.2880	18.4320	24.5760	-	-
Mode	**DSM**			**SSM**	

Table 2. Common Clock Frequencies

Note:

34. 128x and 192x ratios valid only in Left Justified or I²S formats.

4.4.2 Master Mode Clock Ratios

As a clock master, FS/LRCK and SCLK will operate as outputs internally derived from MCLK. FS/LRCK is equal to F_S and SCLK is equal to 64x F_S as shown in Figure 13. TDM format is not supported in Master Mode.

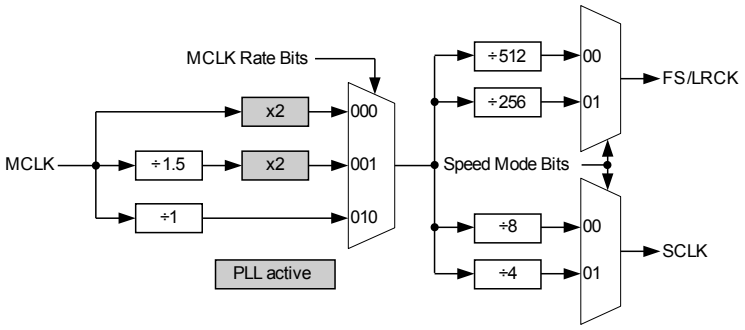


Figure 13. Master Mode Clocking

The resulting valid master mode clock ratios are shown in Table 3 below.

	SSM	DSM
MCLK/F_S	256x, 384x, 512x	128x, 192x, 256x
SCLK/F_S	64x	64x

Table 3. Master Mode Left Justified and I²S Clock Ratios

4.4.3 Slave Mode Clock Ratios

In Slave Mode, SCLK and FS/LRCK operate as inputs. The FS/LRCK clock frequency must be equal to the sample rate, F_S, and must be synchronously derived from the supplied master clock, MCLK.

The serial bit clock, SCLK, must be synchronously derived from the master clock, MCLK, and be equal to 512x, 256x, 128x, 64x, 48x or 32x F_S, depending on the desired format and speed mode. Refer to Table 4

and Table 5 for required clock ratios.

	SSM	DSM
MCLK/F_S	256x, 384x, 512x	128x, 192x, 256x
SCLK/F_S	32x, 48x, 64x, 128x	32x, 48x, 64x

Table 4. Slave Mode Left Justified and I²S Clock Ratios

(Note 35)	SSM		DSM
MCLK/F_S	256x, 384x, 512x	512x	256x
SCLK/F_S	256x	512x	256x

Table 5. Slave Mode TDM Clock Ratios

Note:

35. For all cases, the SCLK frequency must be less than or equal to the MCLK frequency.

4.5 Serial Port Interface

The serial port interface format is selected by the Serial Port Format register bits. The TDM format is available in Slave Mode only.

4.5.1 TDM Mode

The serial port of the CS4234 supports the TDM interface format with varying bit depths from 16 to 24 as shown in Figure 15. Data is clocked out of the ADC on the falling edge of SCLK and clocked into the DAC on the rising edge.

As indicated in Figure 15, TDM data is received most significant bit (MSB) first, on the second rising edge of the SCLK occurring after a FS/LRCK rising edge. All data is valid on the rising edge of SCLK. All bits are transmitted on the falling edge of SCLK. Each slot is 32 bits wide, with the valid data sample left justified within the slot. Valid data lengths are 16, 18, 20, or 24 bits.

FS/LRCK identifies the start of a new frame and is equal to the sample rate, F_S. As shown in Figure 14, FS/LRCK is sampled as valid on the rising SCLK edge preceding the most significant bit of the first data sample and must be held valid for at least 1 SCLK period.

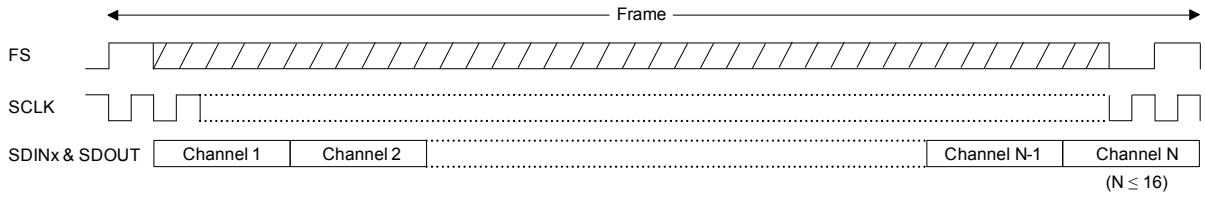


Figure 14. TDM System Clock Format

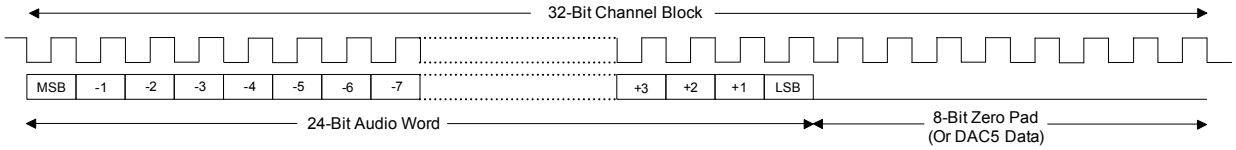


Figure 15. 32-bit Receiver Channel Block

The structure in which the serial data is coded into the TDM slots is shown in Figure 16. When using a 48 kHz sample rate with a 24.576 MHz MCLK and SCLK, a 16 slot TDM structure can be realized. When using a 48 kHz sample rate with 12.288 MHz SCLK and 24.576 MHz MCLK, or a 96 kHz sample rate with a 24.576 MHz MCLK and SCLK, an 8 slot TDM structure can be realized. The data that is coded into the TDM slots is extracted into the appropriate signal path via the settings in the Control port. Please refer to Section 4.6.1 Routing the Serial Data within the Signal Paths for more details.

MCLK = 12.288/24.576MHz FS = 48/96kHz SCLK = 12.288/24.576MHz																
	Slot 1 [31:0]		**Slot 2 [31:0]**		**Slot 3 [31:0]**		**Slot 4 [31:0]**		**Slot 5 [31:0]**		**Slot 6 [31:0]**		**Slot 7 [31:0]**		**Slot 8 [31:0]**	
SDIN1	Input Data 1.1.A [31:8]	Input Data 1.1.B [7:0]	Input Data 1.2.A [31:8]	Input Data 1.2.B [7:0]	Input Data 1.3.A [31:8]	Input Data 1.3.B [7:0]	Input Data 1.4.A [31:8]	x [7:0]	Input Data 1.5.A [31:8]	Input Data 1.5.B [7:0]	Input Data 1.6.A [31:8]	Input Data 1.6.B [7:0]	Input Data 1.7.A [31:8]	Input Data 1.7.B [7:0]	Input Data 1.8.A [31:8]	x[7:0]
SDIN2	Input Data 2.1 [31:8]	x [7:0]	Input Data 2.2 [31:8]	x [7:0]	Input Data 2.3 [31:8]	x[7:0]	Input Data 2.4 [31:8]	x [7:0]	Input Data 2.5 [31:8]	x [7:0]	Input Data 2.6 [31:8]	x[7:0]	Input Data 2.7 [31:8]	x[7:0]	Input Data 2.8 [31:8]	x[7:0]
SDOUT	ADC1 Data[31:8]	0's [7:0]	ADC2 Data [31:8]	0's [7:0]	ADC3 Data [31:8]	0's [7:0]	ADC4 Data[31:8]	0's [7:0]	0's [31:0]		0's [31:0]		0's [31:0]		0's [31:0]	
SDOUT with Sidechain	ADC1 Data[31:8]	0's [7:0]	ADC2 Data [31:8]	0's [7:0]	ADC3 Data [31:8]	0's [7:0]	ADC4 Data [31:8]	0's [7:0]	Output Data (SDIN2 Slot 1)		Output Data (SDIN2 Slot 2)		Output Data (SDIN2 Slot 3)		Output Data (SDIN2 Slot 4)	

MCLK = 24.576MHz FS = 48kHz SCLK = 24.576MHz																				
	Slot 1 [31:0]			**Slot 4 [31:0]**		**Slot 5 [31:0]**			**Slot 8 [31:0]**		**Slot 9 [31:0]**			**Slot 12 [31:0]**		**Slot 13 [31:0]**			**Slot 16 [31:0]**	
SDIN1	Input Data 1.1.A [31:8]	Input Data 1.1.B [7:0]		Input Data 1.4.A [31:8]	x [7:0]	Input Data 1.5.A [31:8]	Input Data 1.5.B [7:0]		Input Data 1.8.A [31:8]	x [7:0]	Input Data 1.9.A [31:8]	Input Data 1.9.B [7:0]		Input Data 1.12.A [31:8]	x [7:0]	Input Data 1.13.A [31:8]	Input Data 1.13.B [7:0]		Input Data 1.16.A [31:8]	x [7:0]
SDIN2	Input Data 2.1 [31:8]	x [7:0]	...→...	Input Data 2.4 [31:8]	x [7:0]	Input Data 2.5 [31:8]	x [7:0]	...→...	Input Data 2.8 [31:8]	x [7:0]	Input Data 2.9 [31:8]	x [7:0]	...→...	Input Data 2.12 [31:8]	x [7:0]	Input Data 2.13 [31:8]	x [7:0]	...→...	Input Data 2.16 [31:8]	x [7:0]
SDOUT	ADC1 Data [31:8]	0's [7:0]		ADC4 Data [31:8]	0's [7:0]	0's [31:0]			0's [31:0]		0's [31:0]			0's [31:0]		0's [31:0]			0's [31:0]	
SDOUT with Sidechain	ADC1 Data [31:8]	0's [7:0]		ADC4 Data [31:8]	0's [7:0]	Output Data (SDIN2 Slot 1)			Output Data (SDIN2 Slot 4)		Output Data (SDIN2 Slot 5)			Output Data (SDIN2 Slot 8)		Output Data (SDIN2 Slot 9)			Output Data (SDIN2 Slot 12)	

Figure 16. Serial Data Coding and Extraction Options within the TDM Streams

4.5.2 Left Justified and I²S Modes

The serial port of the CS4234 supports the Left Justified and I²S interface formats with valid bit depths of 16, 18, 20, or 24 bits for the SDOUTx pins and 24 bits for the SDINx pins. All data is valid on the rising edge of SCLK. Data is clocked out of the ADC on the falling edge of SCLK and clocked into the DAC on the rising edge. In Master Mode each slot is 32 bits wide.

In Left Justified mode (see Figure 17) the data is received or transmitted most significant bit (MSB) first, on the first rising edge of the SCLK occurring after a FS/LRCK edge. The left channel is received or transmitted while FS/LRCK is logic high.

In I²S mode (see Figure 18) the data is received or transmitted most significant bit (MSB) first, on the second rising edge of the SCLK occurring after a FS/LRCK edge. The left channel is received or transmitted while FS/LRCK is logic low.

The AIN1 and AIN2 signals are transmitted on the SDOUT1 pin; the AIN3 and AIN4 signals are transmitted on the AD2/SDOUT2 pin. The data on the SDIN1 pin is routed to AOUT1 and AOUT2; the data on the SDIN2 pin is routed to AOUT3 and AOUT4. AOUT5 is unavailable in these modes and should be placed in the powered down state by using the appropriate Power Down DACx register bit. If it is powered up in these modes, the AOUT5 output will be active and may drive an AC or DC signal.

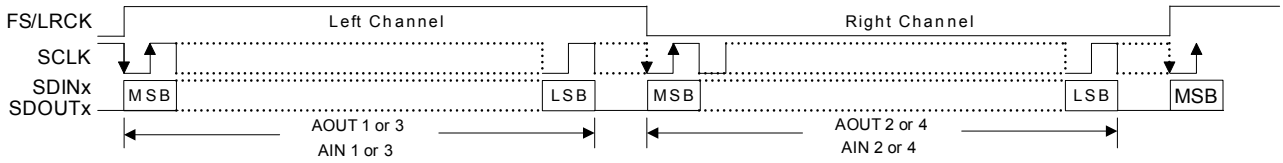


Figure 17. Left Justified Format

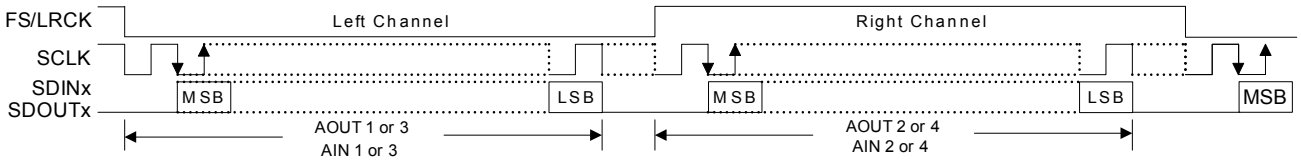


Figure 18. I²S Format

4.6 Internal Signal Path

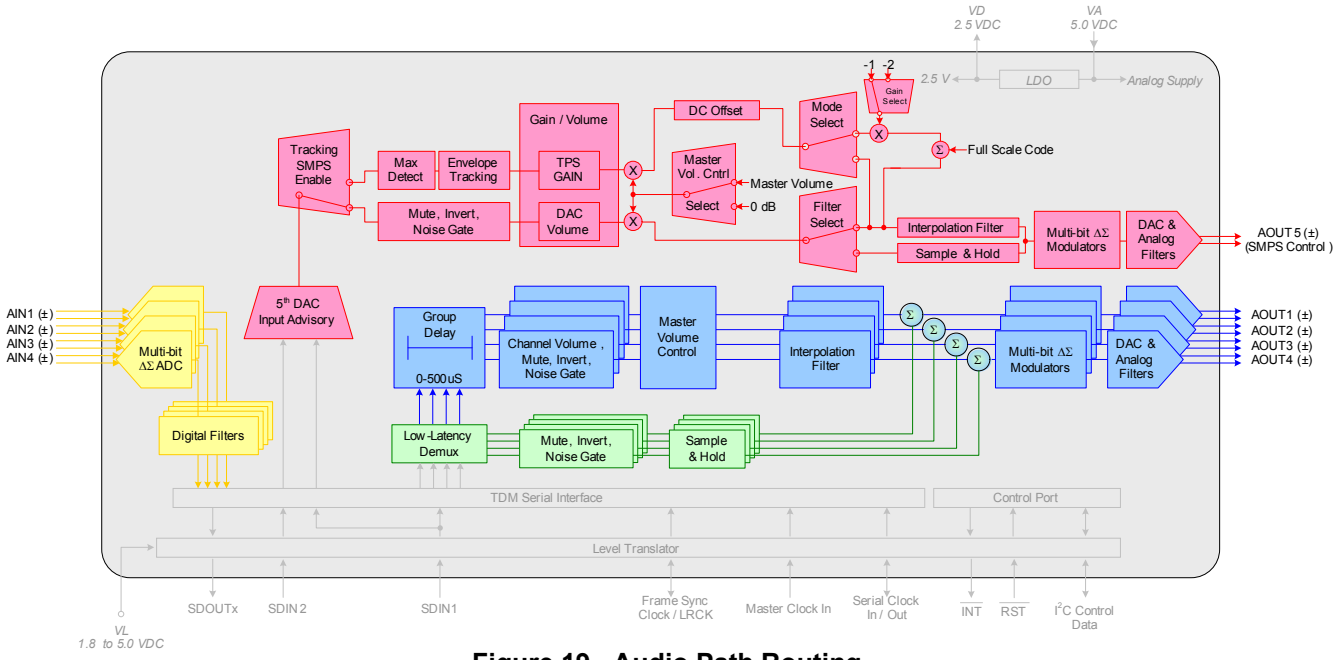


Figure 19. Audio Path Routing

The CS4234 device includes four main paths in which audio data can be routed. The analog input path, shown in yellow, allows up to four analog signals to be combined into a single TDM stream on the SDOUT1 pin or output as stereo pairs on the SDOUT1 and SDOUT2 pins. The DAC1-4 path, highlighted in blue, converts serial audio data to analog audio data. The DAC5 path is highlighted in red and can be used to create a tracking power supply signal, to convert a digital tracking power supply signal to analog, or as a standard audio CODEC with performance characteristics identical to the DACs found in the DAC1-4 path. Group delay will often be added to the DAC1-4 path to allow the tracking power supply signal to lead the audio signal. A low-latency path is provided as well to allow signals which should not be delayed to be mixed together with the output signal at a point after the group delay block. The low-latency path is shown in green.

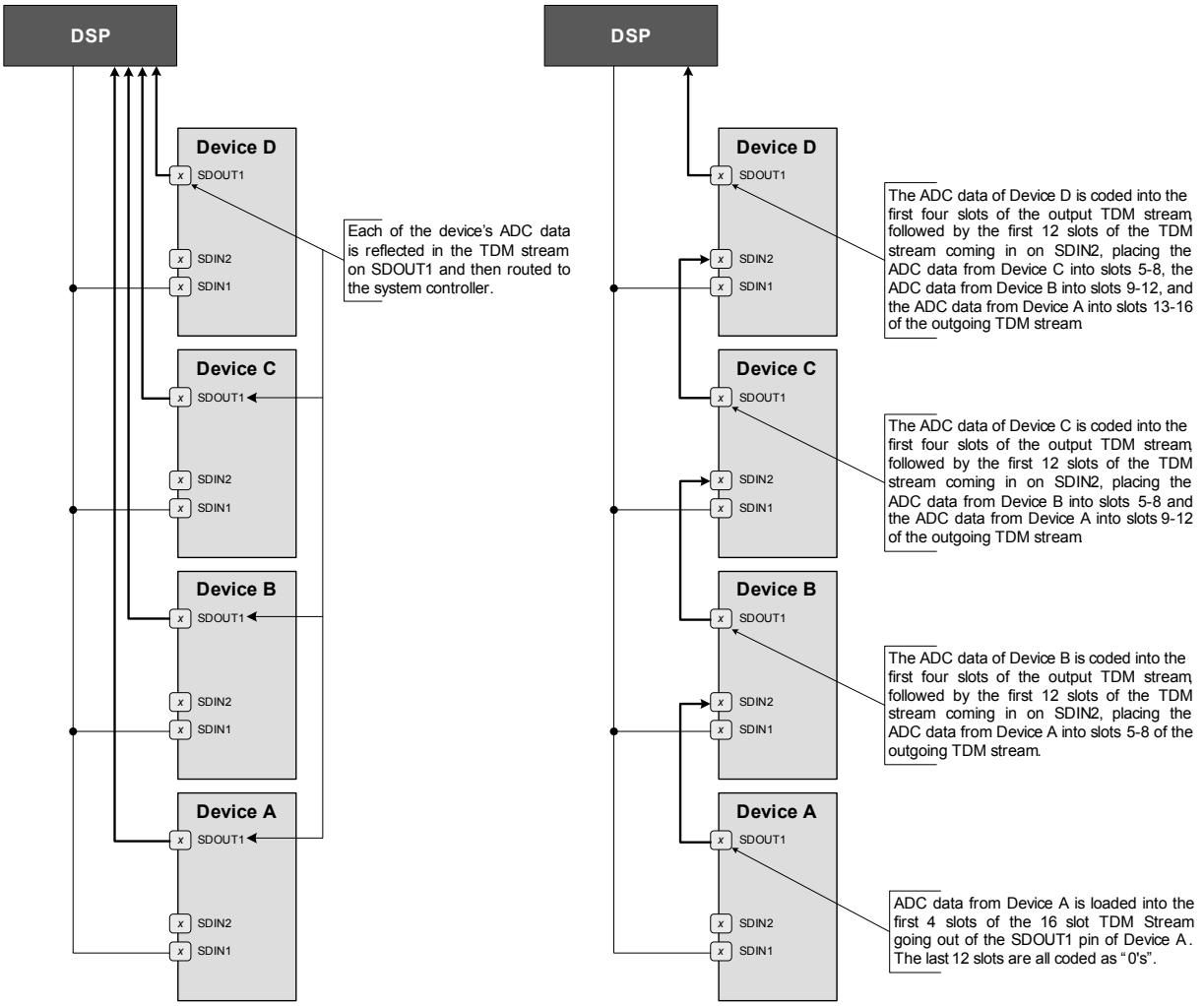
4.6.1 Routing the Serial Data within the Signal Paths

The serial port in the CS4234 is highly versatile and allows a number of ways that the serial data can be coded into and extracted out of the TDM slots on the SDINx pins. Because of its versatility, it is possible to errantly route the serial data into several of the available data paths. This mode of operation is not supported in the CS4234 and should not be used.

4.6.1.1 ADC Signal Routing

In TDM mode, the CS4234 is designed to load the first four slots of the TDM stream on the SDOUT1 pin with the internal ADC data. Additionally, in order to minimize the number of SDOUT1 lines that must be run to the system controller in a multiple IC application, the SDOUT1 data for up to 4 devices can be loaded into a single TDM stream by side chaining the devices together, as shown in Figure 20. To enable the sidechain feature, the “SDO CHAIN” bit in the "SP Control" register must be set.

In Left Justified or I²S mode, the CS4234 transmits the AIN1 and AIN2 signals on the SDOUT1 pin and the AIN3 and AIN4 signals on the SDOUT2 pin.



Note:
This diagram shows the configuration for 16 slot TDM streams. If 8 slot TDM streams are used, two separate serial data lines will need to be connected from the DSP. One would carry the serial data for Devices C&D and the other would carry the serial data for Devices A&B

Figure 20. Conventional SDOUT1 (Left) vs. Sidechain SDOUT1 (Right) Configuration

4.6.1.2 DAC1-4, DAC5, and Low-latency Signal Routing

In TDM mode, each of the 3 output paths have a collection of bits that advise the CS4234 where data for each of the paths is located within the incoming TDM streams. For the DAC1-4 path, the bits are "DAC1-4 SOURCE[2:0]" bits in the "SP Data Sel." register. For the DAC5 path, the bits are the "DAC5 SOURCE[2:0]" bits in the "SP Control" register. Finally, for the Low-Latency Path, the bits are the "LL SOURCE[2:0]" bits in the "SP Data Sel." register. Details for these registers and the setting of their respective bits can be found in Figure 21 and Figure 22.

In Left Justified or I²S mode, the CS4234 routes the data on the SDIN1 pin to DAC1 and DAC2 and the data on the SDIN2 pin to DAC3 and DAC4. DAC5 is unavailable in the PCM modes and should be placed in the powered down state by using the appropriate Power Down DACx register bit. If it is powered up in these modes, the DAC5 output will be active and may drive an AC or DC signal.

DAC1-4 Source [2:0]	DAC1-4 Data is in:
000	Slots 1-4 of SDIN1
001	Slots 5-8 of SDIN1
010	Slots 9-12 of SDIN1
011	Slots 13-16 of SDIN1
100	Slots 1-4 of SDIN2
101	Slots 5-8 of SDIN2
110	Slots 9-12 of SDIN2
111	Slots 13-16 of SDIN2

LL Source [2:0]	Low Latency Data is in:
000	Slots 1-4 of SDIN1
001	Slots 5-8 of SDIN1
010	Slots 9-12 of SDIN1
011	Slots 13-16 of SDIN1
100	Slots 1-4 of SDIN2
101	Slots 5-8 of SDIN2
110	Slots 9-12 of SDIN2
111	Slots 13-16 of SDIN2

DAC5 Source [2:0]	DAC5 Data is in:
000	Coded into the LSBs of Slots 1-3 of SDIN1
001	Coded into the LSBs of Slots 5-7 of SDIN1
010	Coded into the LSBs of Slots 9-11 of SDIN1
011	Coded into the LSBs of Slots 13-15 of SDIN1
100	Determined by the Masking bits
101	Reserved
110	Reserved
111	Reserved

MCLK= 12.288/24.576MHz FS/LRCK= 48/96kHz SCLK = 12.288/24.576MHz								
SDIN1	Slot 1 [31:0]	Slot 2 [31:0]	Slot 3 [31:0]	Slot 4 [31:0]	Slot 5 [31:0]	Slot 6 [31:0]	Slot 7 [31:0]	Slot 8 [31:0]
SDIN2	Slot 1 [31:0]	Slot 2 [31:0]	Slot 3 [31:0]	Slot 4 [31:0]	Slot 5 [31:0]	Slot 6 [31:0]	Slot 7 [31:0]	Slot 8 [31:0]

MCLK= 24.576MHz FS/LRCK= 48kHz SCLK= 24.576MHz											
SDIN1	Slot 1 [31:0]	...→...	Slot 4 [31:0]	Slot 5 [31:0]	...→..	Slot 8 [31:0]	Slot 9 [31:0]	...→..	Slot 12 [31:0]	Slot 13 [31:0]	...→..	Slot 16 [31:0]
SDIN2	Slot 1 [31:0]		Slot 4 [31:0]	Slot 5 [31:0]		Slot 8 [31:0]	Slot 9 [31:0]		Slot 12 [31:0]	Slot 13 [31:0]		Slot 16 [31:0]

Figure 21. DAC1-4, Low Latency, and DAC5 Path Serial Data Source Selection

DAC1-4 Source [2:0]	DAC1-4 Data is in:
000	Slots 1-4 of SDIN1
001	Slots 5-8 of SDIN1
010	Slots 9-12 of SDIN1
011	Slots 13-16 of SDIN1
100	Slots 1-4 of SDIN2
101	Slots 5-8 of SDIN2
110	Slots 9-12 of SDIN2
111	Slots 13-16 of SDIN2

LL Source [2:0]	Low Latency Data is in:
000	Slots 1-4 of SDIN1
001	Slots 5-8 of SDIN1
010	Slots 9-12 of SDIN1
011	Slots 13-16 of SDIN1
100	Slots 1-4 of SDIN2
101	Slots 5-8 of SDIN2
110	Slots 9-12 of SDIN2
111	Slots 13-16 of SDIN2

DAC5 Source [2:0]	DAC5 Data is in:
000	Coded into the LSBs of Slots 1-3 of SDIN1
001	Coded into the LSBs of Slots 5-7 of SDIN1
010	Coded into the LSBs of Slots 9-11 of SDIN1
011	Coded into the LSBs of Slots 13-15 of SDIN1
100	Determined by the Masking bits
101	Reserved
110	Reserved
111	Reserved

MCLK = 12.288/24.576MHz
FS/LRCK = 48/96kHz
SCLK = 12.288/24.576MHz

	Slot 1 [31:0]		Slot 2 [31:0]		Slot 3 [31:0]		Slot 4 [31:0]		Slot 5 [31:0]	Slot 6 [31:0]	Slot 7 [31:0]	Slot 8 [31:0]
SDIN1	DAC1 [23:0]	DAC5 [23:16]	DAC2 [23:0]	DAC5 [15:8]	DAC3 [23:0]	DAC5 [7:0]	DAC4 [23:0]	x	x	x	x	x
SDIN2	LL1 [23:0]	x	LL2 [23:0]	x	LL3 [23:0]	x	LL4 [23:0]	x	x	x	x	x

DAC1-4 Source [2:0]	DAC1-4 Data is in:
000	Slots 1-4 of SDIN1
001	Slots 5-8 of SDIN1
010	Slots 9-12 of SDIN1
011	Slots 13-16 of SDIN1
100	Slots 1-4 of SDIN2
101	Slots 5-8 of SDIN2
110	Slots 9-12 of SDIN2
111	Slots 13-16 of SDIN2

LL Source [2:0]	Low Latency Data is in:
000	Slots 1-4 of SDIN1
001	Slots 5-8 of SDIN1
010	Slots 9-12 of SDIN1
011	Slots 13-16 of SDIN1
100	Slots 1-4 of SDIN2
101	Slots 5-8 of SDIN2
110	Slots 9-12 of SDIN2
111	Slots 13-16 of SDIN2

DAC5 Source [2:0]	DAC5 Data is in:
000	Coded into the LSBs of Slots 1-3 of SDIN1
001	Coded into the LSBs of Slots 5-7 of SDIN1
010	Coded into the LSBs of Slots 9-11 of SDIN1
011	Coded into the LSBs of Slots 13-15 of SDIN1
100	Determined by the Masking bits
101	Reserved
110	Reserved
111	Reserved

MCLK = 12.288/24.576MHz
FS/LRCK = 48/96kHz
SCLK = 12.288/24.576MHz

	Slot 1 [31:0]		Slot 2 [31:0]	Slot 3 [31:0]	Slot 4 [31:0]	Slot 5 [31:0]		Slot 6 [31:0]		Slot 7 [31:0]		Slot 8 [31:0]	
SDIN1	DAC5 [23:0]	x	x	x	x	DAC1 [23:0]	x	DAC2 [23:0]	x	DAC3 [23:0]	x	DAC4 [23:0]	x
SDIN2	x		x	x	x	LL1 [23:0]	x	LL2 [23:0]	x	LL3 [23:0]	x	LL4 [23:0]	x

Figure 22. Example Serial Data Source Selection

As can be seen from Figure 22, setting '100' of the DAC5 Source[2:0] bits configures the DAC5 path to use the mask bits to determine which signals are routed into the DAC5 path. The CS4234 is designed to make any one of the slots of both the SDINx pins available to the 5th DAC Input Advisory block, where the mask bits for the DAC5 path are located. The configuration of the mask bits is shown in Table 6 and Table 7. In order to unmask a slot from the DAC5 path, a '0' must be written to the appropriate bit within the appropriate mask register.

Data to be Unmasked from DAC5 Path	SDIN1 Mask 1[7:0] Setting								SDIN1 Mask 2[7:0] Setting							
SDIN1 Slot 1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
SDIN1 Slot 2	x	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x
SDIN1 Slot 3	x	x	0	x	x	x	x	x	x	x	x	x	x	x	x	x
SDIN1 Slot 4	x	x	x	0	x	x	x	x	x	x	x	x	x	x	x	x
SDIN1 Slot 5	x	x	x	x	0	x	x	x	x	x	x	x	x	x	x	x
SDIN1 Slot 6	x	x	x	x	x	0	x	x	x	x	x	x	x	x	x	x
SDIN1 Slot 7	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	x
SDIN1 Slot 8	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x
SDIN1 Slot 9	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x
SDIN1 Slot 10	x	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x
SDIN1 Slot 11	x	x	x	x	x	x	x	x	x	x	0	x	x	x	x	x
SDIN1 Slot 12	x	x	x	x	x	x	x	x	x	x	x	0	x	x	x	x
SDIN1 Slot 13	x	x	x	x	x	x	x	x	x	x	x	x	0	x	x	x
SDIN1 Slot 14	x	x	x	x	x	x	x	x	x	x	x	x	x	0	x	x
SDIN1 Slot 15	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	x
SDIN1 Slot 16	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0

Table 6. Unmasking SDIN1 Data from DAC5 Path

Data to be Unmasked from DAC5 Path	SDIN2 Mask 1[7:0] Setting								SDIN2 Mask 2[7:0] Setting							
SDIN2 Slot 1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
SDIN2 Slot 2	x	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x
SDIN2 Slot 3	x	x	0	x	x	x	x	x	x	x	x	x	x	x	x	x
SDIN2 Slot 4	x	x	x	0	x	x	x	x	x	x	x	x	x	x	x	x
SDIN2 Slot 5	x	x	x	x	0	x	x	x	x	x	x	x	x	x	x	x
SDIN2 Slot 6	x	x	x	x	x	0	x	x	x	x	x	x	x	x	x	x
SDIN2 Slot 7	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	x
SDIN2 Slot 8	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x
SDIN2 Slot 9	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x
SDIN2 Slot 10	x	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x
SDIN2 Slot 11	x	x	x	x	x	x	x	x	x	x	0	x	x	x	x	x
SDIN2 Slot 12	x	x	x	x	x	x	x	x	x	x	x	0	x	x	x	x
SDIN2 Slot 13	x	x	x	x	x	x	x	x	x	x	x	x	0	x	x	x
SDIN2 Slot 14	x	x	x	x	x	x	x	x	x	x	x	x	x	0	x	x
SDIN2 Slot 15	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	x
SDIN2 Slot 16	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0

Table 7. Unmasking SDIN2 Data from DAC5 Path

Due to the flexibility of the DAC5 path, it is possible to errantly unmask several data slots simultaneously. If this occurs and DAC5 is not in Tracking Power Supply mode (see Section 4.6.5.1 Generating the Tracking Signal Inside the CS4234), only one data slot will be taken as the input into the DAC5 path. The selection of this data slot is based upon the priority level of each of the slots which have been unmasked. The priority structure is as follows:

1. Slot 1 of SDIN 1 receives 1st priority
2. Slot 2 of SDIN 1 receives 2nd priority
3. ...
4. Slot 16 of SDIN 1 receives 16th priority
5. Slot 1 of SDIN 2 receives 17th priority
6. ...
7. Slot 16 of SDIN 2 receives last priority.

4.6.2 ADC Path

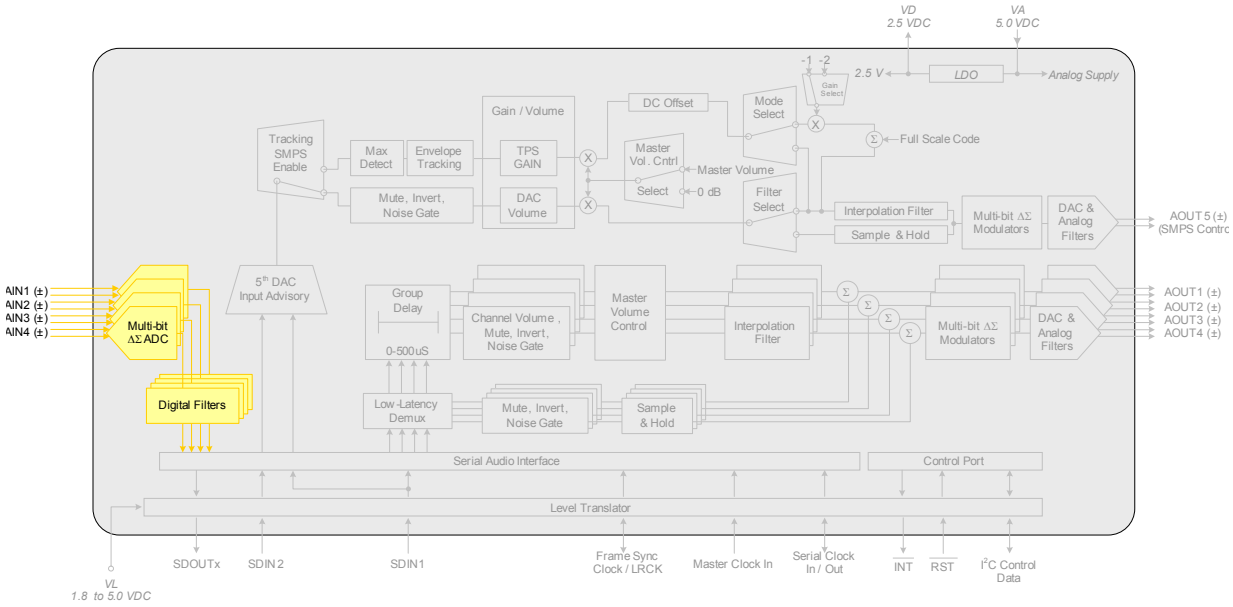


Figure 23. ADC Path

4.6.2.1 Analog Inputs

AINx+ and AINx- are line-level differential analog inputs. The analog input pins do not self-bias and must be externally biased to VA/2 to avoid clipping of the input signal. The full-scale analog input levels are scaled according to VA and can be found in the Analog Input Characteristics table.

The ADC output data is in two's complement binary format. For inputs above positive full scale or below negative full scale, the ADC will output 7FFFFFH or 800000H, respectively, and cause the ADC Overflow bit in the Interrupt Notification 1 register to be set to a '1'.

When used with the CS44417, whose current monitoring circuitry is single ended, the CS4234's AINx- nets should be joined together and connected to the VQ output from the CS44417. This connection will prevent any variances in the reference voltages of the CS4234 and the CS44417 from skewing the CS44417 output current measurements. Refer to Figure 2 for more details concerning these connections.

4.6.2.2 ADC HPF

The ADC path has an optional HPF which can be enabled or disabled for all four ADCs via the "ENABLE HPF" bit in the "ADC Control 1" register. The HPF should only be disabled when the DC component of the input signal needs to be preserved in the digital output data (i.e. current monitoring with the CS44417). The HPF characteristics are given in the ADC Digital Filter Characteristics table and plotted in Section 7. The Analog Input Characteristics table specifies the DC offset error when the HPF is enabled or disabled.

4.6.3 DAC1-4 Path

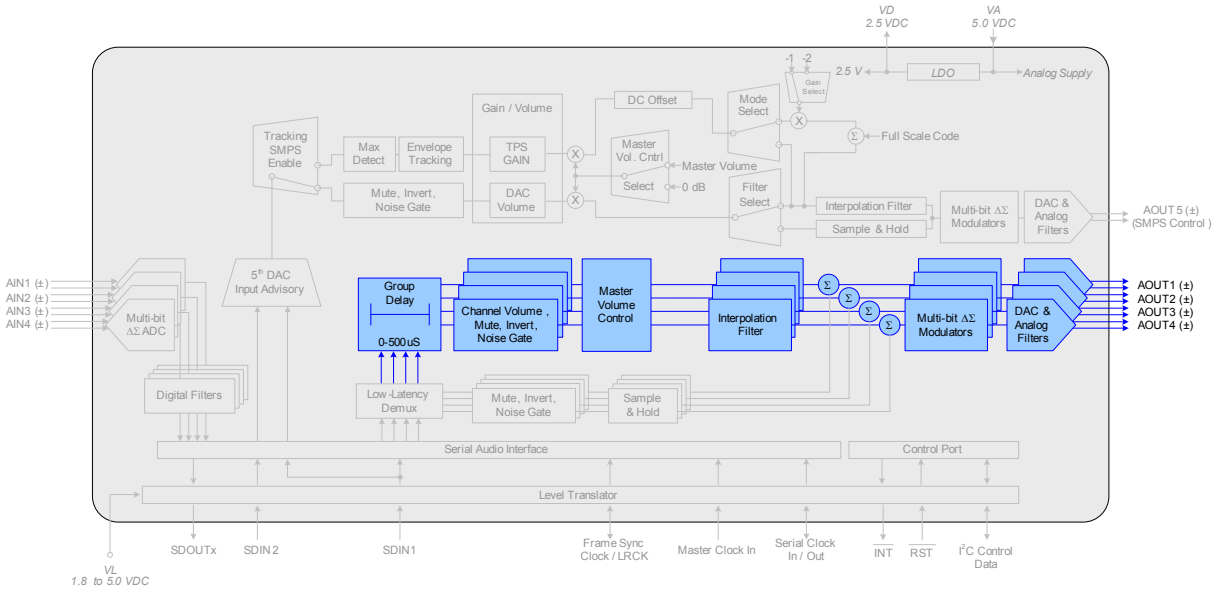


Figure 24. DAC1-4 Path

The AOUT1-4 signals are driven by the data placed into the DAC1-4 path. This data can be placed into the DAC1-4 path via the DAC1-4 Data Source settings in the control port. These settings allow the input source to be selected from any of the up to 32 slots of data on the incoming TDM streams on SDIN1 and SDIN2.

The DAC1-4 path includes a programmable group delay which delays the output audio signals to allow the DAC5 output to operate in feed-forward fashion, adjusting the voltage rails of the tracking power supply in anticipation of the coming audio signal. There is a connection between the group delay applied to the audio signal and the ability of the SMPS to respond to high amplitude transients. By having a shorter delay, the output voltage of the SMPS can track the audio signal more closely, increasing efficiency of the Class H system. However, providing too short of a delay may prevent the SMPS to react fast enough to high-amplitude transients, resulting in clipping of the output signal. For these reasons, the group delay of the CS4234 can be adjusted from 100 μs to 500 μs, based on the settings of Group Delay bits. The group delay should only be modified while all of the "Power Down ADCx" bits in the "ADC Control 2 (Address 10h)" register and the "Power Down DACx" bits in the "DAC Control 4 (Address 15h)" register are set to '1'b and the DAC outputs have entered the mute state (see Table 8 for mute ramp time when soft-ramp is enabled). Note that the "Base Rate Advisory" bits in the "Clock and SP Select (Address 06h)" register must be set to correctly calculate the selected group delay.

The DAC1-4 path also includes individual channel mutes. Separate volume controls are available for each channel, along with a master volume control that simultaneously attenuates all four channels. The master volume attenuation is added to any channel attenuation that is applied.

4.6.3.1 De-emphasis Filter

The CS4234 includes on-chip digital de-emphasis for 32, 44.1, and 48 kHz sample rates. It is not supported for 96 kHz or for any settings in Double-speed Mode. The filter response is adjusted to be appropriate for a particular base rate by the Base Rate Advisory bits. This filter response, shown in Figure 25, will vary if these bits are not set appropriately for the given base rate. The frequency response of the de-emphasis curve scales proportionally with changes in sample rate, F_S. Please see Section 6.15.2 DAC1-4 De-emphasis for de-emphasis control.

The de-emphasis feature is included to accommodate audio recordings that utilize 50/15 µs preemphasis equalization as a means of noise reduction.

De-emphasis is only available in Single-speed Mode.

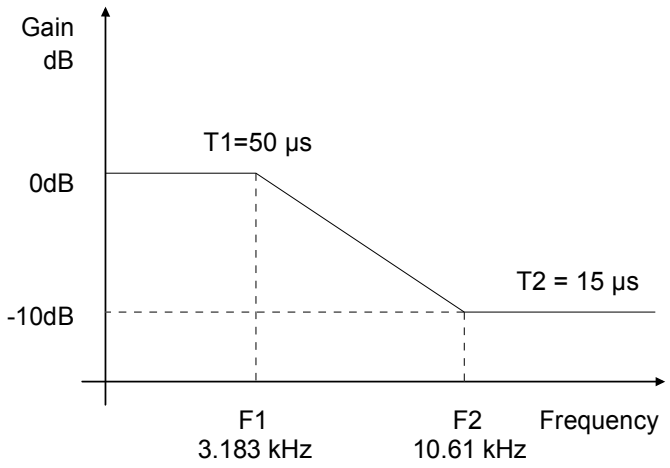


Figure 25. De-emphasis Curve

4.6.4 Low-Latency Path

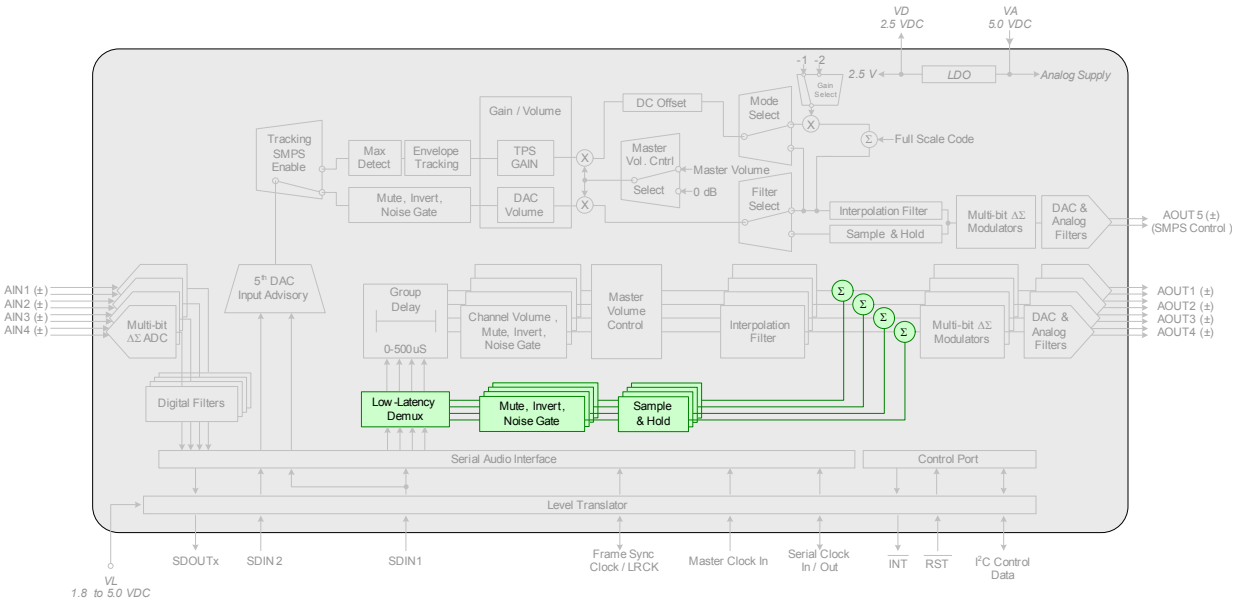


Figure 26. Low-latency Path

A low-latency path is provided to allow four user selectable data signals to be routed around the group delay block and interpolation filters of the DAC1-4 path. These four signals can be present in any of the 32 slots on the two TDM streams on SDIN1 and SDIN2.

The Low-Latency path also includes a global mute bit and individual channel invert bits. The signals from the low latency path are summed with the DAC1-4 path after the master volume control. Changes to the master volume control setting do not affect the low-latency-path signals. For details concerning the operation of the volume control, please see Section 4.6.6 Volume Control.

4.6.5 DAC5 Path

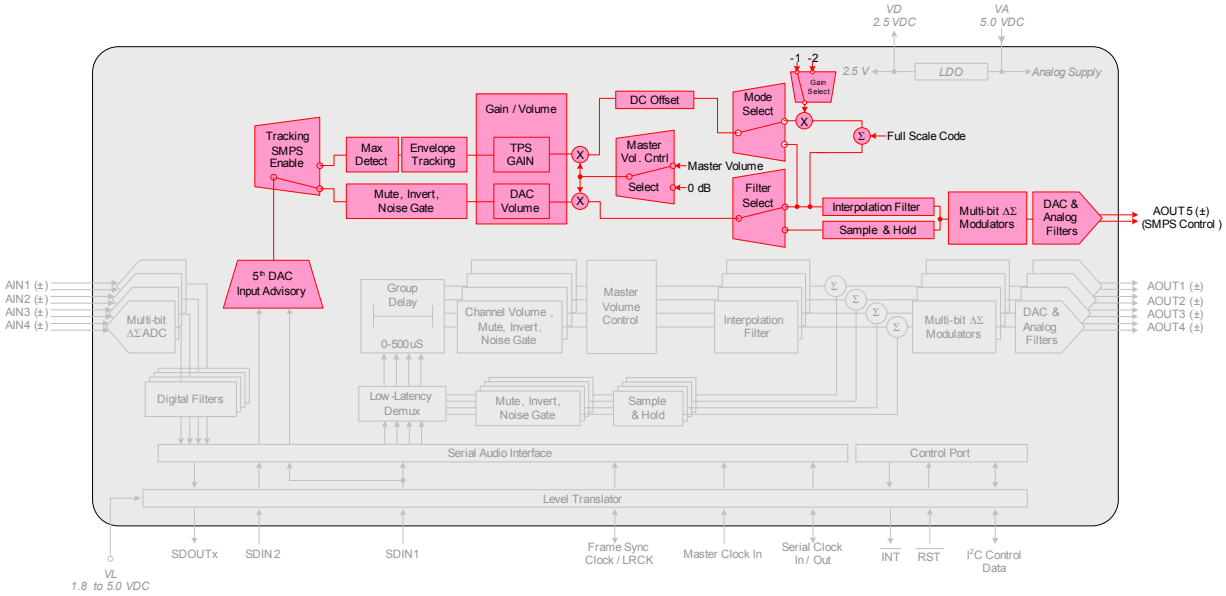


Figure 27. DAC5 Path

The 5th DAC in the CS4234 is a fully functional audio-grade DAC with performance specifications identical to that of the other four DACs. In addition to the standard feature set, such as independent channel volume and muting, the 5th DAC can also be used to create a reference signal for an off-chip tracking power supply. This functionality allows any Class AB amplifier to be operated as a Class H amplifier.

Within the DAC5 path, there are several routing options, primarily based upon which parts of the tracking signal (if any) will be generated within the CS4234 or in an external DSP.

4.6.5.1 Generating the Tracking Signal Inside the CS4234

To generate the tracking signal internally, up to 32 channels of data present in the two TDM streams on SDIN1 and SDIN2 can be considered. The max detect block determines the largest data sample on a sample by sample basis. It then holds that sample for a period of time equal to that set in the group delay block, effectively tracking the envelope of that calculated signal.

Set the “DAC5 CFG & FLTR[1:0]” bits in the "DAC Control 1" register to ‘10’ to select that the tracking signal is to be generated within the CS4234. To include a channel of data in the calculation, unmask its respective bit in the SDINx MASKx register. When the Tracking SMPS Enable bit is set, the signal can not be inverted using the INV DAC5 bit.

In order to compensate for the difference between the gain of the Class AB amplifier stage and the gain of the switch-mode power supply that generates the rails for the Class AB amplifier, the internal volume block in the DAC5 path can be adjusted by changing the "DAC5 Volume" register.

Voltage is customarily added to the rails of a Class H amplifier to prevent clipping events from occurring during high amplitude transients. This DC offset is accomplished within the CS4234 via the“TPS OFFSET[2:0]” bits in the "TPS Control" register.

See Appendix A: Internal Tracking Power Supply Signal for more detailed information about the internal tracking signal.

4.6.5.2 Generating the Tracking Signal Inside an External DSP

If the tracking signal is to be generated within an external DSP, the tracking signal generation blocks mentioned above can be bypassed by setting the "DAC5 CFG & FLTR[1:0]" bits in the "DAC Control 1" register to either the interpolation filter option ('00') or the sample and hold filter ('01'). Note that the DAC5 signal inversion caused by setting the "TPS MODE" bit in the "TPS Control" register is not bypassed and for most cases the bit should be cleared, see Figure 29. The "DAC5 SOURCE[2:0]" bits in the "SP Control" register advise the CS4234 where the tracking signal can be found among the incoming data. If the tracking signal has been coded into one of the 32 slots of the TDM stream, the signal can be routed into the DAC5 path by masking all of the other slots via the SDINx Maskx bits. As shown in the "DAC5 SOURCE[2:0]" bits in the "SP Control" register, the tracking signal can also be coded into the LSBs of the 16 slots of the SDIN1 stream.

4.6.5.3 Using DAC5 in a Traditional DAC Configuration (with no tracking signal)

As mentioned previously, DAC5 is identical in performance to the DACs in the DAC1-4 path. In this application, signal is routed into the DAC5 path in the same manner as in the previous section. If the data for DAC5 is in one of the 32 slots, simply unmask the appropriate slot by using the appropriate mask bits. If the data is coded into the LSBs of SDIN1, set the "DAC5 SOURCE[2:0]" bits in the "SP Control" register appropriately.

Please refer to Section 4.6.6 Volume Control regarding volume control within the DAC5 path. The operation is identical to the volume control in the DAC1-4 path.

One additional control that is present within the DAC5 path is the "DAC5 MVC" bit in the "DAC Control 1" register. When this bit is set, the CS4234 will apply any gain written to the master volume control register to the DAC5 path as well. If this bit is cleared, the DAC5 volume will operate independently of the setting of the master volume control register. This feature is provided to ensure that, when not desired, any changes made to the master volume control on the audio path will not affect the output amplitude of the tracking power supply signal, when DAC5 is used for that application.

4.6.5.4 De-emphasis Filter

The CS4234 includes on-chip digital de-emphasis for 32, 44.1, and 48 kHz sample rates. It is not supported for 96 kHz or for any settings in Double Speed Mode. The filter response is adjusted to be appropriate for a particular sample rate by the Base Rate Advisory bits. This filter response, shown in Figure 25, will vary if these bits are not set appropriately for the given sample rate. The frequency response of the de-emphasis curve scales proportionally with changes in sample rate, F_S. Please see Section 6.15.3 DAC5 De-emphasis for de-emphasis control.

The de-emphasis feature is included to accommodate audio recordings that utilize 50/15 μs preemphasis equalization as a means of noise reduction.

4.6.5.5 Filter Options

There are two internal filter options for the DAC5 path. A standard interpolation filter is provided for traditional applications as well as a "sample and hold" bypass option. To activate the bypass, set the "DAC5 CFG & FLTR[1:0]" bits in the "DAC Control 1" register to '01'.

4.6.6 Volume Control

The CS4234 includes a volume control for the DAC1-4 and DAC5 signal paths. While the general operation of the volume controls is identical between the two paths, the optional tracking power supply control present in the DAC5 path modifies the implementation slightly. The implementation details for the volume control and other associated peripheries for DAC1-4 is shown in Figure 28 below. The implementation de-

tails for the volume control and other associated peripheries for the DAC5 path is shown in Figure 29.

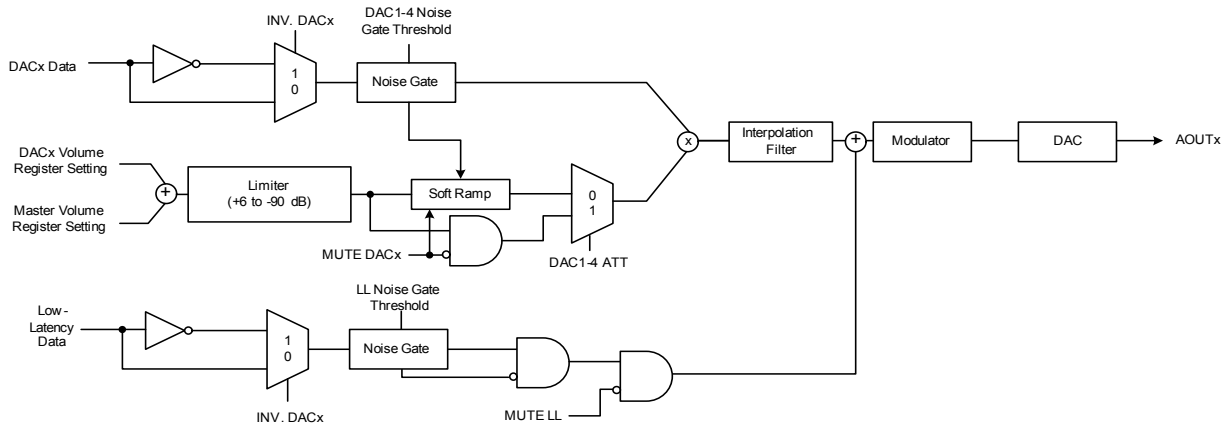


Figure 28. Volume Implementation for the DAC1-4 and Low-latency Path

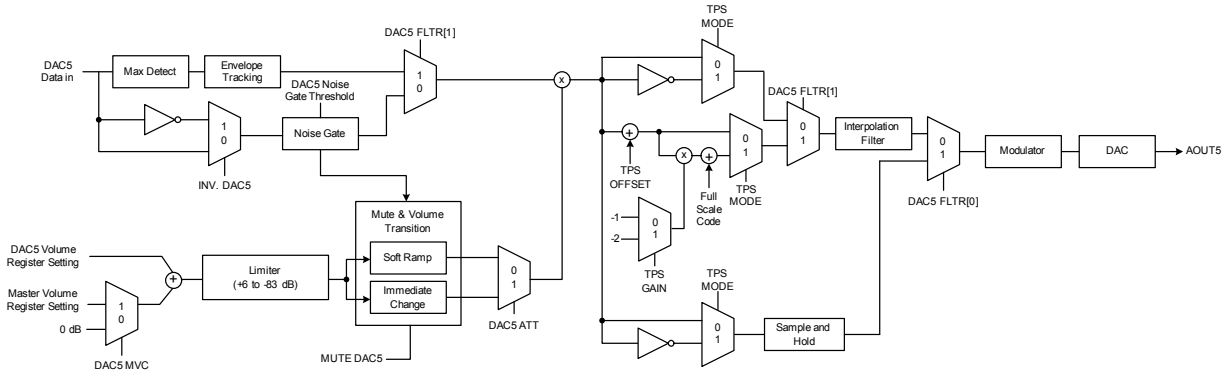


Figure 29. Volume Implementation for the DAC5 Path

4.6.6.1 Mute Behavior

Each DAC channel volume is controlled by the sum (in dB) of the individual channel volume and the master volume registers (except for DAC5 if the DAC5 MVC bit is cleared). The channel and master volume control registers have a range of +6 dB to -90 dB with a nominal resolution of $^{6.02}/_{16}$ dB per each bit, which is approximately 0.4 dB. For DAC1-4, the sum of the two volume settings is limited to a range of +6 dB to -90 dB. For DAC5, the sum of the two volume settings is limited to a range of +6 dB to -83 dB. Any volume setting below these ranges will result in infinite attenuation thus muting the channel.

A DAC channel or low latency path may alternatively be muted by using the mute register bits, power down bits, or the Noise Gate feature. For any case when the mute engages (volume is less than minimum limit, power down bit is set, mute bit is set, or Noise Gate is engaged), the CS4234 will mute the channel immediately or soft-ramp the volume down at a rate specified by the MUTE DELAY[1:0] bits depending on the settings of the DAC1-4 ATT. and DAC5 ATT. bits in the "DAC Control 3" register. This behavior also applies when unmuting a channel. The low latency paths are always muted or unmuted immediately.

4.6.6.2 Soft Ramp

The CS4234 soft ramp feature (enabled using the DAC1-4 ATT. and DAC5 ATT. bits) is activated on mute and unmute transitions as well as any normal volume register changes. To avoid any potential audible artifacts due to the soft ramping, the volume control algorithm implements the ramping function differently based upon how the user attempts to control the volume.

If the user changes the volume in distant discrete steps such as what would happen if a button were pressed on a user interface to temporarily add attenuation to or mute a channel, then the volume is ramped from the current setting to the new setting at a constant rate set by the MUTE DELAY[1:0] bits.

Alternatively, if the user controls the volume through a knob or slider interface, a volume envelope is sampled at a slow, not-necessarily uniform rate (typically 1-20 Hz) and sent to the CS4234. In this case the ramping algorithm detects a short succession of volume changes attempting to track the volume envelope and dynamically adjusts the soft-ramp rate.

If the CS4234 were to use a constant ramp rate between the volume changes it receives, its output volume envelope may either lag behind the user-generated envelope if the ramp rate is set too low (possibly not reaching the peaks and dulling the envelope) or the output volume envelope may cause a stair-case effect resulting in audible zipper noise if the ramp rate is set too high. By instead adapting the soft-ramp rate to fit the envelope given by the incoming volume samples, the envelope lag time is limited and the zipper noise is avoided. In this mode the soft ramp algorithm linearly interpolates the volume between the volume changes. There is a lag of one volume change sample since two samples are required to calculate the first ramp rate.

See Figure 30 for the soft ramp diagram. On the first volume sample received, the CS4234 only detects the possible beginning of a volume envelope sequence and resets an envelope counter. The volume starts ramping to the new volume setting at a constant rate controlled by the MUTE DELAY[1:0] setting. If the envelope counter times out before a new volume sample is received, the next received sample is treated in the same way as the previous sample and the ramp rate is kept constant. In this way, as long as the volume samples are distant from each other by more than the envelope counter time out, the rate is kept constant resulting in the soft-ramp behavior described in the button-press example.

However if the next volume sample is received before the envelope counter times out, then it is assumed to be part of a volume envelope sequence. The envelope counter is reset and as long as new samples are received in succession before a time out occurs, the sequence is continued. Starting at the second volume sample of an envelope sequence, the ramp rate is adjusted using the equation shown in Figure 30.

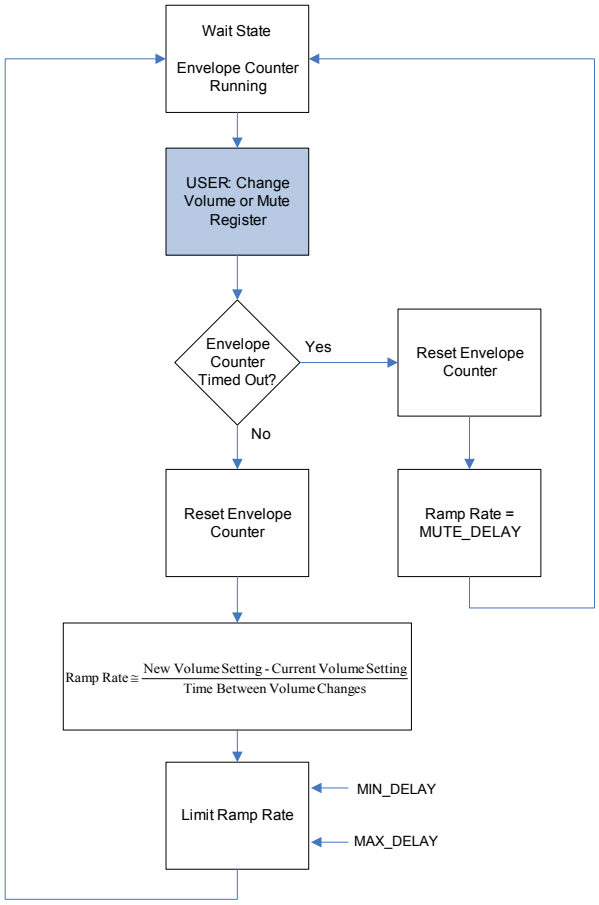


Figure 30. Soft Ramp Behavior

Two control parameters allow the user to limit the ramp-rate range to achieve optimum effect. The MIN DELAY[2:0] setting limits the maximum ramp rate; higher values will introduce more lag in the envelope tracking while providing a smoother ramp. The MAX DELAY[2:0] setting limits the minimum ramp rate; lower values will permit closer tracking of the envelope but may reintroduce zipper noise. The default values of these registers are recommended as a starting point. It is possible to disable the volume envelope tracking and always produce a constant ramp rate. To accomplish this, set the MIN DELAY[2:0] and MAX DELAY[2:0] values to match the MUTE DELAY[1:0] setting.

The envelope counter time out period which defines the boundary between the two soft-ramping behaviors depends on the base rate. It is equal to approximately 100,000/Fs.

The MUTE DELAY[1:0], MIN DELAY[2:0], and MAX DELAY[2:0] bits specify a delay equal to a multiple of the base period between volume steps of $^{6.02}/_{64}$ dB, which is approximately 0.1 dB. This is the internal resolution of the volume control engine. Consequently the soft-ramp rate can be expressed in ms/dB as shown in Table 8.

	Fs = 48 kHz or 96 kHz (Base = 48 kHz)			Fs = 32 kHz or 64 kHz (Base = 32 kHz)		
Ramp Rate	Time to Ramp to Full Scale (ms)	Time to Ramp 6 dB (ms)	ms/dB	Time to Ramp to Full Scale (ms)	Time to Ramp 6 dB (ms)	ms/dB
1 x Base	21.33	1.33	0.22	32	2	0.33
2 x Base	42.67	2.67	0.44	64	4	0.66
4 x Base	85.33	5.33	0.89	128	8	1.33
8 x Base	170.67	10.67	1.77	256	16	2.66
16 x Base	341.33	21.33	3.54	512	32	5.32
32 x Base	682.67	42.67	7.09	1024	64	10.63
64 x Base	1365.33	85.33	14.17	2048	128	21.26
128 x Base	2730.67	170.67	28.35	4096	256	42.52

Table 8. Soft Ramp Rates

Full-scale ramp is 96 dB (-90 dB to +6 dB)

4.6.6.3 Noise Gate

The CS4234 is equipped with a Noise Gate feature that mutes the output of a given path if the signal drops below a given bit depth for 8192 samples. This feature can be independently enabled for any of the three output paths. While the enabling or disabling of the Noise Gate feature is done by output path, each of the channels within the paths have separate monitoring circuitry that will trigger the Noise Gate function independently of the other channels. For instance, if the Noise Gate were enabled for a given path and one of the channels within that given path were to exhibit a pattern of more than 8192 samples of either all “1’s” or all “0’s”, the output for that particular channel would be muted (and subsequently unmuted), independently of the other channels within the same path. To enable the Noise Gate feature, set the xNG[2:0] bits to the desired bit depth. The available bit depth settings are shown in Table 9.

xNG[2:0] Setting	Channel is muted after “x” bits
000	Upper 13 Bits (-72 dB)
001	Upper 14 Bits (-78 dB)
010	Upper 15 Bits (-82 dB)
011	Upper 16 Bits (-90 dB)
100	Upper 17 Bits (-94 dB)
101	Upper 18 Bits (-102 dB)
110	Upper 24 Bits (-138 dB)
111	Noise Gate Disabled

Table 9. Noise Gate Bit Depth Settings

When the upper “x” bits, as dictated by the xNG[2:0] settings, are either all “1’s” or all “0’s” for 8192 consecutive samples, the Noise Gate will engage for that channel. Setting all of these bits to ‘111’ will disable the Noise Gate feature. If the Noise Gate feature engages for the Low-Latency path, the mute event will occur immediately. If the Noise Gate feature engages for the DAC1-4 or DAC5 path, it will transition into and out of mute as dictated by the DAC1-4 ATT. and DAC5 ATT. bits in the "DAC Control 3" register.

4.7 Reset Line

The reset line of the CS4234 is used to place the device into a reset condition. In this condition, all of the values of the CS4234 control port are set to their default values. This mode of operation is the lowest power mode of operation for the CS4234 and should be used whenever the device is not operating in order to save power. During the power up and power down sequence, it is often necessary for the CS4234 devices to be placed into (and taken out of) reset at a different moment in time than the amplifiers to which they are connected in order to minimize audible clicks and pops during the sequence. For this reason, it is advisable to run separate reset lines for each type of device, i.e. one reset line for the CS4234 devices and one for the CS44417 devices.

4.8 Error Reporting and Interrupt Behavior

The CS4234 is equipped with a suite of error reporting and protection. The types of errors that are detected, the notification method for these errors, and the steps needed to clear the errors are detailed in Table 10.

It is important to note that the interrupt notification bits for all of the errors are triggered on the edge of the occurrence of the event. They are not level-triggered and therefore do not indicate the presence of an error in real time. This means that, a “1” in the error’s respective field inside the Interrupt Notification register only indicates that the error occurred since the last time the register was cleared and not necessarily that the error is currently occurring.

Name of Error	Event(s) that caused the error	Outputs muted upon occurrence?	All PDNx bits must be set and then cleared to resume normal operation?
Disallowed Test Mode Entry (Note 36)	Device has entered test mode due to an errant I²C write.	No	No
Serial Port Error	FS/LRCK or SCLK has become invalid.	Yes	Yes
Clocking Error	The speed mode which the device is receiving is different than the speed mode set in the SPEED MODE[1:0] bits, or the PLL is unlocked from input signal.	Yes	Yes
ADCx Overflow	ADC inputs are larger than the permitted full scale signal.	No	No Normal operation continues but audible distortion occurs.
DACx Clip	DAC output level is larger than the available rail voltage.	No	No Normal operation continues but audible distortion occurs.

Table 10. Error Reporting and Interrupt Behavior Details

Note:

36. This error is provided to aid in troubleshooting during software development. Entry into the test mode of the device may cause permanent damage to the device and should not be done intentionally.

4.8.1 Interrupt Masking

An occurrence of any of the errors mentioned above will cause the interrupt line to engage in order to notify the system controller that an error occurred. If it is preferred that the error not cause the interrupt line to engage, this error can be masked in its respective mask register. It is important to note that, in the event of an error, the interrupt notification bit for the respective error will reflect the occurrence of the event, re-

gardless of the setting of the mask bit. Setting the mask bit only prevents the interrupt pin from being flagged upon the occurrence.

4.8.2 Interrupt Line Operation

As mentioned previously, the interrupt line of the CS4234 will be pulled low or high (depending on the settings of the “INT PIN[1:0]” bits in the "Interrupt Control" register) after an interrupt condition occurs, provided that the event is not masked in the mask register. If the CS4234’s interrupt line is to be connected onto a single bus with other devices, it is advisable to use it in the open drain mode of operation. If no other devices are connected to the interrupt line, it may be used in the CMOS mode of operation. When used in the open drain configuration, it is necessary to connect a pull-up resistor to this net, which will ensure a known state on the net when no error is present. Please refer to the typical connection diagram for the appropriate pull-up resistor value.

4.8.3 Error Reporting and Clearing

In the event of an error, the interrupt line will be engaged - provided the mask bit for that error is not set. When the interrupt notification registers are read to determine the source of the error, the mask bit for whichever error occurred will be set automatically by the CS4234. The system controller should begin to take corrective action to clear the error. Once the error has been cleared, the system controller should clear the mask bit in the appropriate mask register to ensure that a subsequent occurrence of the error will cause the interrupt line to engage appropriately. This behavior is detailed in Figure 31 on page 49.

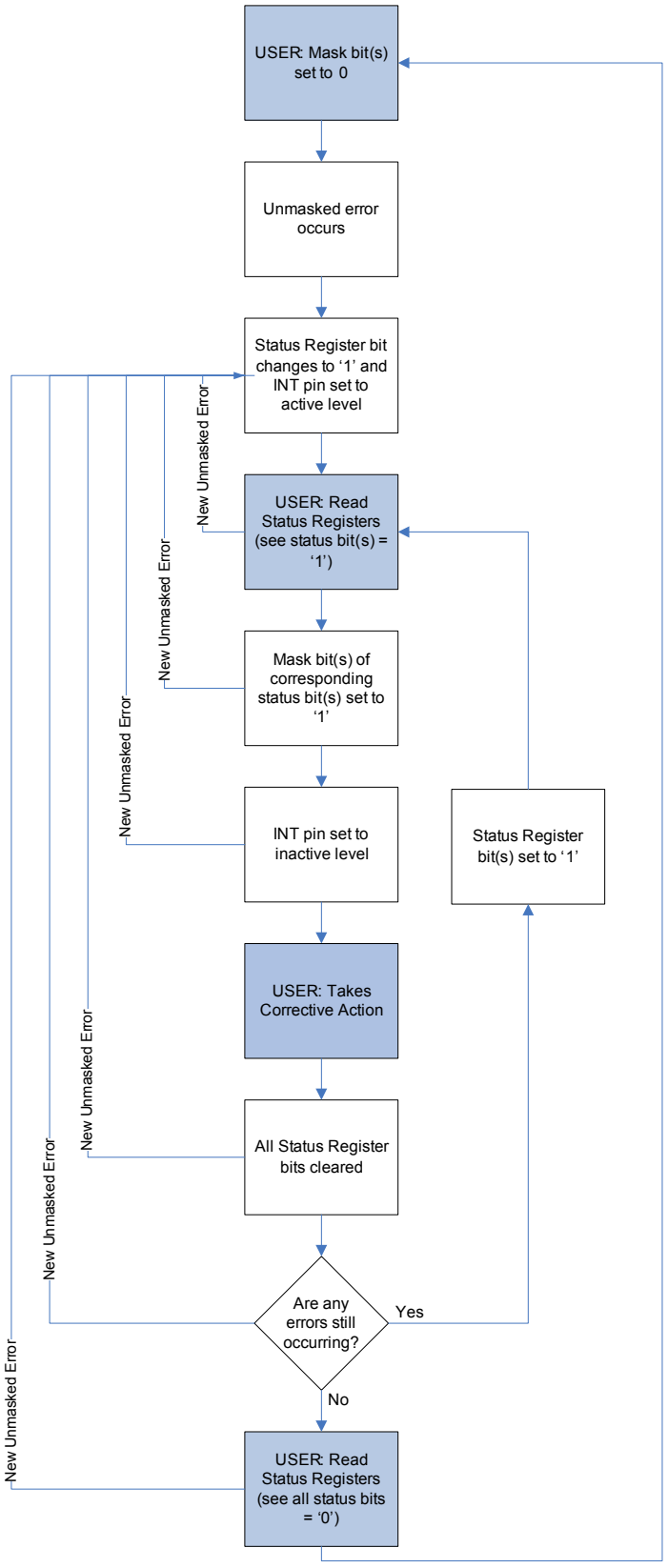


Figure 31. Interrupt Behavior and Example Interrupt Service Routine

5. REGISTER QUICK REFERENCE

Default values are shown below the bit names.

AD	Function	7	6	5	4	3	2	1	0
(Read Only Bits are shown in Italics)									
01h p 52	Device ID A and B	*DEV. ID A[3:0]* 0	1	0	0	*DEV. ID B[3:0]* 0	0	1	0
02h p 52	Device ID C and D	*DEV. ID C[3:0]* 0	0	1	1	*DEV. ID D[3:0]* 0	1	0	0
03h p 52	Device ID E and F	*DEV. ID E[3:0]* 0	0	0	0	*DEV. ID F[3:0]* 0	0	0	0
04h	Variant ID	Reserved [3:0] 0	0	0	0	Reserved [3:0] 0	0	0	0
05h p 52	Revision ID	*ALPHA REV. ID[3:0]* x	x	x	x	*NUMERIC REV. ID[3:0]* x	x	x	x
06h p 53	Clock and SP Sel.	BASE RATE[1:0] 0	0	SPEED MODE[1:0] 0	0	MCLK RATE[2:0] 0	1	0	Reserved 0
07h p 54	Sample Width Sel.	SDOUTx SW[1:0] 1	1	INPUT SW[1:0] 1	1	LOW LAT. SW[1:0] 1	1	DAC5 SW[1:0] 1	1
08h p 55	SP Control	INV SCLK 0	DAC5 SOURCE[2:0] 1	0	0	SP FORMAT[1:0] 1	0	SDO CHAIN 0	MASTER/ SLAVE 0
09h p 56	SP Data Sel.	Reserved 0	Reserved 0	DAC1-4 SOURCE[2:0] 0	0	0	LL SOURCE[2:0] 0	0	1
0Ah p 57	SDIN1 Mask 1	SDIN1 MASK 1[7:0] 1	1	1	1	1	1	1	1
0Bh p 57	SDIN1 Mask 2	SDIN1 MASK 2[7:0] 1	1	1	1	1	1	1	1
0Ch p 58	SDIN2 Mask 1	SDIN2 MASK 1[7:0] 1	1	1	1	1	1	1	1
0Dh p 58	SDIN2 Mask 2	SDIN2 MASK 2[7:0] 1	1	1	1	1	1	1	1
0Eh p 59	TPS Control	TPS MODE 0	TPS OFFSET[2:0] 0	0	0	GROUP DELAY[3:0] 0	0	0	0
0Fh p 60	ADC Control 1	Reserved 1	Reserved 1	VA_SEL 0	ENABLE HPF 0	INV. ADC4 0	INV. ADC3 0	INV. ADC2 0	INV. ADC1 0
10h p 61	ADC Control 2	MUTE ADC4 1	MUTE ADC3 1	MUTE ADC2 1	MUTE ADC1 1	PDN ADC4 1	PDN ADC3 1	PDN ADC2 1	PDN ADC1 1
11h p 61	Low Lat. Control 1	LL NG[2:0] 1	1	1	Reserved 0	INV. LL 4 0	INV. LL 3 0	INV. LL 2 0	INV. LL 1 0
12h p 62	DAC Control 1	DAC1-4 NG[2:0] 1	1	1	DAC1-4 DE 0	DAC5 DE 0	DAC5 MVC 0	DAC5 CFG & FLTR[1:0] 0	0
13h p 63	DAC Control 2	DAC5 NG[2:0] 1	1	1	INV. DAC5 0	INV. DAC4 0	INV. DAC3 0	INV. DAC2 0	INV. DAC1 0
14h p 63	DAC Control 3	DAC5 ATT. 1	DAC1-4 ATT. 0	MUTE LL 1	MUTE DAC5 1	MUTE DAC4 1	MUTE DAC3 1	MUTE DAC2 1	MUTE DAC1 1
15h p 64	DAC Control 4	VQ RAMP 0	TPS GAIN 0	Reserved 0	PDN DAC5 1	PDN DAC4 1	PDN DAC3 1	PDN DAC2 1	PDN DAC1 1

AD	Function	7	6	5	4	3	2	1	0
(Read Only Bits are shown in Italics)									
16h p 65	Volume Mode	MUTE DELAY[1:0] 1	 0	MIN DELAY[2:0] 0	 0	 0	MAX DELAY[2:0] 1	 1	 1
17h p 66	Master Volume	MASTER VOLUME[7:0] 0	 0	 0	 1	 0	 0	 0	 0
18h p 66	DAC1 Volume	DAC1 VOLUME[7:0] 0	 0	 0	 1	 0	 0	 0	 0
19h p 66	DAC2 Volume	DAC2 VOLUME[7:0] 0	 0	 0	 1	 0	 0	 0	 0
1Ah p 66	DAC3 Volume	DAC3 VOLUME[7:0] 0	 0	 0	 1	 0	 0	 0	 0
1Bh p 66	DAC4 Volume	DAC4 VOLUME[7:0] 0	 0	 0	 1	 0	 0	 0	 0
1Ch p 66	DAC5 Volume	DAC5 VOLUME[7:0] 0	 0	 0	 1	 0	 0	 0	 0
1Dh	Reserved	Reserved[3:0] 1	 0	 1	 1	Reserved[3:0] 1	 0	 1	 0
1Eh p 66	Interrupt Control	INT MODE 0	INT PIN[1:0] 1	 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
1Fh p 67	Interrupt Mask 1	MASK TST MODE ERR 0	MASK SP ERR 0	MASK CLK ERR 0	Reserved 1	MASK ADC4 OVFL 0	MASK ADC3 OVFL 0	MASK ADC2 OVFL 0	MASK ADC1 OVFL 0
20h p 68	Interrupt Mask 2	Reserved 0	Reserved 0	Reserved 1	MASK DAC5 CLIP 0	MASK DAC4 CLIP 0	MASK DAC3 CLIP 0	MASK DAC2 CLIP 0	MASK DAC1 CLIP 0
21h p 68	Interrupt Notification 1	*TST MODE* x	*SP ERR* x	*CLK MOD ERR* x	*Reserved* x	*ADC4 OVFL* x	*ADC3 OVFL* x	*ADC2 OVFL* x	*ADC1 OVFL* x
22h p 69	Interrupt Notification 2	*Reserved* x	*Reserved* x	*Reserved* x	*DAC5 CLIP* x	*DAC4 CLIP* x	*DAC3 CLIP* x	*DAC2 CLIP* x	*DAC1 CLIP* x

6. REGISTER DESCRIPTIONS

All registers are read/write unless otherwise stated. All “Reserved” bits must maintain their default state. Default values are shaded.

6.1 Device I.D. A and B (Address 01h) *(Read Only)*
Device I.D. C and D (Address 02h) *(Read Only)*
Device I.D. E and F (Address 03h) *(Read Only)*

7	6	5	4	3	2	1	0
DEV. ID A[3:0]				DEV. ID B[3:0]			
DEV. ID C[3:0]				DEV. ID D[3:0]			
DEV. ID E[3:0]				DEV. ID F[3:0]			

6.1.1 Device I.D. (Read Only)

Device I.D. code for the CS4234. Example:.

DEV. ID A[3:0]	DEV. ID B[3:0]	DEV. ID C[3:0]	DEV. ID D[3:0]	DEV. ID E[3:0]	DEV. ID F[3:0]	Part Number
4h	2h	3h	4h	0h	0h	CS4234

6.2 Revision I.D. (Address 05h) *(Read Only)*

7	6	5	4	3	2	1	0
AREVID3	AREVID2	AREVID1	AREVID0	NREVID3	NREVID2	NREVID1	NREVID0

6.2.1 Alpha Revision (Read Only)

CS4234 Alpha (silicon) revision level.

AREVID[3:0]	Alpha Revision Level
Ah	A
...	...

6.2.2 Numeric Revision (Read Only)

CS4234 Numeric (metal) revision level.

NREVID[3:0]	Numeric Revision Level
0h	0
...	...

Note: The Alpha and Numeric revision I.D. are used to form the complete device revision I.D. Example: A0, A1, B0, B1, B2, etc.

6.3 Clock and SP Select (Address 06h)

7	6	5	4	3	2	1	0
BASE RATE[1:0]		SPEED MODE[1:0]		MCLK RATE[2:0]			Reserved

6.3.1 Base Rate Advisory

Advises the CS4234 of the base rate of the incoming base rate. This allows for the de-emphasis filters to be adjusted appropriately and the group delay block for the DAC1-4 path to be calculated correctly. The CS4234 includes on-chip digital de-emphasis for 32, 44.1, and 48 kHz base rates. It is not supported for 96 kHz or for any settings in Double Speed Mode.

BASE RATE	Base Rate is:
00	48 kHz
01	44.1 kHz
10	32 kHz
11	Reserved

6.3.2 Speed Mode

Sets the speed mode in which the CS4234 will operate.

SPEED MODE	Speed Mode is:
00	Single Speed Mode
01	Double Speed Mode
10	Reserved
11	Auto Detect

6.3.3 Master Clock Rate

Sets the rate at which the master clock is entering the CS4234. Settings are given in “x” multiplied by the incoming sample rate, as MCLK must scale directly with incoming sample rate.

MCLK RATE	MCLK is:
000	$256xF_S$ in Single Speed Mode or $128xF_S$ in Double Speed Mode
001	$384xF_S$ in Single Speed Mode or $192xF_S$ in Double Speed Mode
010	$512xF_S$ in Single Speed Mode or $256xF_S$ in Double Speed Modex
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	Reserved

6.4 Sample Width Select (Address 07h)

7	6	5	4	3	2	1	0
SDOUTx SW[1:0]		INPUT SW[1:0]		LOW LAT. SW[1:0]		DAC5 SW[1:0]	

6.4.1 Output Sample Width

These bits set the width of the samples placed into the outgoing SDOUTx streams.

OUTPUT SW	Sample Width is:
00	16 bits
01	18 bits
10	20 bits
11	24 bits

Note: Bits which are wider than the Output Sample Width setting above will be set to zero within the SDOUTx data stream.

6.4.2 Input Sample Width

These bits set the width of the samples coming into the CS4234 through the SDINx TDM streams.

INPUT SW	Sample Width is:
00	16 bits
01	18 bits
10	20 bits
11	24 bits

6.4.3 Low-Latency Path Sample Width

These bits set the width of the samples which have been placed into the low latency path of the CS4234.

LOW LAT. SW	Sample Width is:
00	16 bits
01	18 bits
10	20 bits
11	24 bits

6.4.4 DAC5 Sample Width

These bits set the width of the samples which have been placed into the DAC5 path of the CS4234.

DAC5 SW	Sample Width is:
00	16 bits
01	18 bits
10	20 bits
11	24 bits

6.5 Serial Port Control (Address 08h)

7	6	5	4	3	2	1	0
INV SCLK	DAC5 SOURCE[2:0]			SP FORMAT[1:0]		SDO CHAIN	MASTER/SLAVE

6.5.1 Invert SCLK

When set, this bit inverts the polarity of the SCLK signal.

INV SCLK	SCLK is:
0	Not Inverted
1	Inverted

6.5.2 DAC5 Input Source

Sets which portion of data is to be routed to the DAC5 data path.

DAC5 SOURCE	Data is routed into the DAC5 path from:
000	LSB's of slots 1-3 of the TDM stream on SDIN1
001	LSB's of slots 5-7 of the TDM stream on SDIN1
010	LSB's of slots 9-11 of the TDM stream on SDIN1
011	LSB's of slots 13-15 of the TDM stream on SDIN1
100	Mask bits are used to determine the input signal in the DAC5 path. See Section 4.6.5 for details.
101	Reserved
110	Reserved
111	Reserved

6.5.3 Serial Port Format

Sets the format of both the incoming serial data signals and outgoing serial data signal.

SP FORMAT	Format is:
00	Left Justified
01	I^2S
10	TDM (Slave Mode Only)
11	Reserved

6.5.4 Serial Data Output Sidechain

Setting this bit enables the SDOUT1 side chain feature. In this mode, the samples from multiple devices can be coded into one TDM stream. See Section 4.6.2 ADC Path for more details.

SDO CHAIN	Sidechain is:
0	Disabled
1	Enabled

6.5.5 Master / Slave

Setting this bit places the CS4234 in master mode, clearing it places it in slave.

MASTER / SLAVE	CS4234 is in:
0	Slave Mode
1	Master Mode

I^2S and Left Justified are the only available serial port formats if the CS4234 is placed into Master Mode.

6.6 Serial Port Data Select (Address 09h)

7	6	5	4	3	2	1	0
Reserved	Reserved	DAC1-4 SOURCE[2:0]			LL SOURCE[2:0]		

6.6.1 DAC1-4 Data Source

Sets which portion of data is to be routed to the DAC1-4 data paths.

DAC1-4 SOURCE	Data is routed into the DAC1-4 path from:
000	Slots 1-4 of the TDM stream on SDIN1
001	Slots 5-8 of the TDM stream on SDIN1
010	Slots 9-12 of the TDM stream on SDIN1
011	Slots 13-16 of the TDM stream on SDIN1
100	Slots 1-4 of the TDM stream on SDIN2
101	Slots 5-8 of the TDM stream on SDIN2
110	Slots 9-12 of the TDM stream on SDIN2
111	Slots 13-16 of the TDM stream on SDIN2

6.6.2 Low-latency Path Source

Sets which portion of data is to be routed to the Low-Latency data path.

LL SOURCE	Data is routed into the Low Latency path from:
000	Slots 1-4 of the TDM stream on SDIN1
001	Slots 5-8 of the TDM stream on SDIN1
010	Slots 9-12 of the TDM stream on SDIN1
011	Slots 13-16 of the TDM stream on SDIN1
100	Slots 1-4 of the TDM stream on SDIN2
101	Slots 5-8 of the TDM stream on SDIN2
110	Slots 9-12 of the TDM stream on SDIN2
111	Slots 13-16 of the TDM stream on SDIN2

6.7 Serial Data Input 1 Mask 1 (Address 0Ah)

7	6	5	4	3	2	1	0
SDIN1 MASK 1[7:0]							

6.7.1 SDIN1 Mask 1

This field determines what data is masked from the max detect and envelope tracking blocks in the DAC5 data path.

SDIN1 MASK 1	Unmasked Data (in addition to any other data that is unmasked by its respective mask bits):
11111111	All Data is Masked.
0xxxxxxx	Slot 1 of SDIN1.
x0xxxxxx	Slot 2 of SDIN1.
xx0xxxxx	Slot 3 of SDIN1.
xxx0xxxx	Slot 4 of SDIN1.
xxxx0xxx	Slot 5 of SDIN1.
xxxxx0xx	Slot 6 of SDIN1.
xxxxxx0x	Slot 7 of SDIN1.
xxxxxxx0	Slot 8 of SDIN1.

6.8 Serial Data Input 1 Mask 2 (Address 0Bh)

7	6	5	4	3	2	1	0
SDIN1 MASK 2[7:0]							

6.8.1 SDIN1 Mask 2

This field determines what data is masked from the max detect and envelope tracking blocks in the DAC5 data path.

SDIN1 MASK 2	Unmasked Data (in addition to whatever other data is unmasked by its respective mask bits):
11111111	All Data is masked.
0xxxxxxx	Slot 9 of SDIN1.
x0xxxxxx	Slot 10 of SDIN1.
xx0xxxxx	Slot 11 of SDIN1.
xxx0xxxx	Slot 12 of SDIN1.
xxxx0xxx	Slot 13 of SDIN1.
xxxxx0xx	Slot 14 of SDIN1.
xxxxxx0x	Slot 15 of SDIN1.
xxxxxxx0	Slot 16 of SDIN1.

6.9 Serial Data Input 2 Mask 1 (Address 0Ch)

7	6	5	4	3	2	1	0
SDIN2 MASK 1[7:0]							

6.9.1 SDIN2 Mask 1

This field determines what data is masked from the max detect and envelope tracking blocks in the DAC5 data path.

SDIN2 MASK 1	Unmasked Data (in addition to any other data that is unmasked by its respective mask bits):
11111111	All Data is Masked.
0xxxxxxx	Slot 1 of SDIN2.
x0xxxxxx	Slot 2 of SDIN2.
xx0xxxxx	Slot 3 of SDIN2.
xxx0xxxx	Slot 4 of SDIN2.
xxxx0xxx	Slot 5 of SDIN2.
xxxxx0xx	Slot 6 of SDIN2.
xxxxxx0x	Slot 7 of SDIN2.
xxxxxxx0	Slot 8 of SDIN2.

6.10 Serial Data Input 2 Mask 2 (Address 0Dh)

7	6	5	4	3	2	1	0
SDIN2 MASK 2[7:0]							

6.10.1 SDIN2 Mask 2

This field determines what data is masked from the max detect and envelope tracking blocks in the DAC5 data path.

SDIN2 MASK 2	Unmasked Data (in addition to whatever other data is unmasked by its respective mask bits):
11111111	All Data is masked.
0xxxxxxx	Slot 9 of SDIN2.
x0xxxxxx	Slot 10 of SDIN2.
xx0xxxxx	Slot 11 of SDIN2.
xxx0xxxx	Slot 12 of SDIN2.
xxxx0xxx	Slot 13 of SDIN2.
xxxxx0xx	Slot 14 of SDIN2.
xxxxxx0x	Slot 15 of SDIN2.
xxxxxxx0	Slot 16 of SDIN2.

6.11 Tracking Power Supply Control (Address 0Eh)

7	6	5	4	3	2	1	0
TPS MODE	TPS OFFSET[2:0]			GROUP DELAY[3:0]			

6.11.1 Tracking Power Supply Mode

If DAC5 FLTR (Section 6.15.5) is set to Tracking Power Supply Mode, setting this bit changes the reference of the DAC5 output from 0 V to full-scale output voltage. This feature is used when the topology of the power supply decreases output signal as the reference signal is increased, and increases its output signal when the reference signal is decreased. If DAC5 FLTR is not set to Tracking Power Supply Mode, setting this bit inverts the DAC5 output.

TPS MODE	Output of DAC5 is referenced to:
0	0 VDREGC
1	Full Scale

6.11.2 Tracking Power Supply Offset

Determines the DC offset is added to the DAC5 output. The DC offset value changes proportionally to VA changes. Note when TPS Mode = 1 and TPS Gain = 1, the DC offset amount is double the values listed in the table.

TPS OFFSET	DC Offset on DAC5 output [% of Full Scale]:
000	0
001	3
010	6
011	9
100	12
101	15
110	18
111	21

6.11.3 Group Delay

Sets the group delay added to the DAC1-4 path. This delay is in addition to any inherent delay in the DAC. Modify these bits only while all of the ADCs and DACs are powered down and the DACs are in mute state.

GROUP DELAY [3:0]	Nominal Group Delay [µs]	Sample Rate		Sample Rate		Sample Rate		Sample Rate		Sample Rate		Sample Rate	
		32 kHz		44.1 kHz		48 kHz		64 kHz		88.2 kHz		96 kHz	
		# of Samples	Delay [µs]	# of Samples	Delay [µs]	# of Samples	Delay [µs]	# of Samples	Delay [µs]	# of Samples	Delay [µs]	# of Samples	Delay [µs]
0000	0	0	0	0	0	0	0	0	0	0	0	0	0
0001	100	3	94	4	91	5	104	6	94	9	102	10	104
0010	150	5	156	7	159	7	146	10	156	13	147	14	146
0011	200	6	188	9	204	10	208	13	203	18	204	19	198
0100	225	7	219	10	227	11	229	14	219	20	227	22	229
0101	250	8	250	11	249	12	250	16	250	22	249	24	250
0110	275	9	281	12	272	13	271	18	281	24	272	26	271
0111	300	10	312	13	295	14	292	19	297	27	306	29	302
1000	325	10	312	14	317	15	312	21	328	29	329	31	323
1001	350	11	344	15	340	17	354	22	344	31	351	34	354
1010	375	12	375	16	363	18	375	24	375	33	374	36	375
1011	400	13	406	17	386	19	396	26	406	36	408	38	396
1100	425	14	438	18	408	20	417	27	422	38	431	41	427
1101	450	15	469	20	454	21	438	29	453	40	454	43	448
1110	475	15	469	21	476	23	479	30	469	42	476	46	479
1111	500	16	500	22	499	24	500	32	500	44	499	48	500

6.12 ADC Control 1 (Address 0Fh)

7	6	5	4	3	2	1	0
Reserved	Reserved	VA_SEL	ENABLE HPF	INV. ADC4	INV. ADC3	INV. ADC2	INV. ADC1

6.12.1 VA Select

Scales internal operational voltages appropriately for VA level. This bit must be set appropriately for the VA voltage level used in the application to ensure proper operation and performance of the device.

VA_SEL	Must be set when VA is:
0	3.3 VDC
1	5 VDC

6.12.2 Enable High-Pass Filter

Enables high-pass filter for the ADC path.

ENABLE HPF	High Pass Filter is:
0	Disabled
1	Enabled

6.12.3 Invert ADCx

Inverts the polarity of the ADCx signal.

INV. ADCx	ADCx Polarity is:
0	Not Inverted
1	Inverted

6.13 ADC Control 2 (Address 10h)

7	6	5	4	3	2	1	0
MUTE ADC4	MUTE ADC3	MUTE_ADC2	MUTE ADC1	PDN ADC4	PDN ADC3	PDN ADC2	PDN ADC1

6.13.1 Mute ADCx

Mutes the ADCx signal

MUTE ADCx	ADC is:
0	Not Muted
1	Muted

6.13.2 Power Down ADCx

Powers down the ADCx path.

PDN ADCx	ADC is:
0	Powered Up
1	Powered Down

6.14 Low Latency Path Control (Address 11h)

7	6	5	4	3	2	1	0
LL NG[2:0]			Reserved	INV. LL4	INV. LL3	INV. LL2	INV. LL1

6.14.1 Low Latency Noise Gate

This sets the bit depth at which the Noise Gate feature should engage for the low-latency path.

LL NG[2:0]	Noise Gate is set at: [b]
000	Upper 13 Bits (72 dB)
001	Upper 14 Bits (78 dB)
010	Upper 15 Bits (84 dB)
011	Upper 16 Bits (90 dB)
100	Upper 17 Bits (96 dB)
101	Upper 18 Bits (102 dB)
110	Upper 24 Bits (138 dB)
111	Noise Gate Disabled

6.14.2 Invert Low Latency Channel x

Inverts the polarity of the data entering into the low-latency channel.

INV. LLx	Low Latency Data is:
0	Not Inverted
1	INverted

6.15 DAC Control 1 (Address 12h)

7	6	5	4	3	2	1	0
DAC1-4 NG			DAC1-4 DE	DAC5 DE	DAC5 MVC	DAC5 CFG & FLTR[1:0]	

6.15.1 DAC1-4 Noise Gate

This sets the bit depth at which the Noise Gate feature should engage for the DAC1-4 path.

DAC1-4 NG[2:0]	Noise Gate is set at: [b]
000	Upper 13 Bits (72 dB)
001	Upper 14 Bits (78 dB)
010	Upper 15 Bits (84 dB)
011	Upper 16 Bits (90 dB)
100	Upper 17 Bits (96 dB)
101	Upper 18 Bits (102 dB)
110	Upper 24 Bits (138 dB)
111	Noise Gate Disabled

6.15.2 DAC1-4 De-emphasis

Enables or disables de-emphasis for the DAC1-4 path. See Section 4.6.3.1 for details. The CS4234 includes on-chip digital de-emphasis for 32, 44.1, and 48 kHz base rates. It is not supported for 96 kHz or for any settings in Double-Speed Mode.

DAC1-4 DE	De-emphasis is:
0	Disabled
1	Enabled

6.15.3 DAC5 De-emphasis

Enables or disables de-emphasis for the DAC5 path. See Section 4.6.5.4 for details. The CS4234 includes on-chip digital de-emphasis for 32, 44.1, and 48 kHz sample rates. It is not supported for 96 kHz or for any settings in Double-speed Mode.

DAC5 DE	De-emphasis is:
0	Disabled
1	Enabled

6.15.4 DAC5 Master Volume Controlled

Selects whether the DAC5 data path is subject to or independent of the master volume control.

DAC5 MVC	DAC5 volume is:
0	Not subject to the master volume control
1	Subject to the master volume control.

6.15.5 DAC5 Configuration and Filter Selection

Selects the filtering applied to the DAC5 data or configures the DAC5 Path used to generate a tracking power supply reference. If placed into Tracking Power Supply mode, an interpolation filter is applied to the outgoing data; otherwise, either an interpolation or a sample-and-hold filter can be applied to the path.

DAC5 FLTR	Filter Selected is:
00	Interpolation Filter
01	Sample and Hold
10	Tracking Power Supply Mode (See Section 4.6.5.1 for details)
11	Reserved

6.16 DAC Control 2 (Address 13h)

7	6	5	4	3	2	1	0
DAC5 NG[2:0]			INV. DAC5	INV. DAC4	INV. DAC3	INV. DAC2	INV. DAC1

6.16.1 DAC5 Noise Gate

This sets the bit depth at which the Noise Gate feature should engage for the DAC5 path.

DAC5 NG	Noise Gate is set at: [b]
000	Upper 13 Bits (72 dB)
001	Upper 14 Bits (78 dB)
010	Upper 15 Bits (84 dB)
011	Upper 16 Bits (90 dB)
100	Upper 17 Bits (96 dB)
101	Upper 18 Bits (102 dB)
110	Upper 24 Bits (138 dB)
111	Noise Gate Disabled

6.16.2 Inv. DACx

Inverts the polarity of the DACx signal.

INV. DACx	DACx Polarity is:
0	Not Inverted
1	Inverted

When the DAC5 path is put into TPS mode, the invert bit for the DAC5 path will be inoperable.

6.17 DAC Control 3 (Address 14h)

7	6	5	4	3	2	1	0
DAC5 ATT	DAC1-4 ATT	MUTE LL	MUTE DAC5	MUTE DAC4	MUTE DAC3	MUTE DAC2	MUTE DAC1

6.17.1 DAC5 Attenuation

Sets the mode of attenuation used for the DAC5 path.

DAC5 ATT	Attenuation events happen:
0	On a soft ramp
1	Immediately

Note: See Section 4.6.6 Volume Control for details regarding the attenuation modes.

6.17.2 DAC1-4 Attenuation

Sets the mode of attenuation used for the DAC1-4 path.

DAC1-4 ATT	Attenuation events happen:
0	On a soft ramp
1	Immediately

Note: See Section 4.6.6 Volume Control for details regarding the attenuation modes.

6.17.3 Mute Low-latency Path

Mutes the low-latency path.

MUTE LL	Low latency path is:
0	Not Muted
1	Muted

6.17.4 Mute DACx

Mutes the DACx signal.

MUTE DACx	DACx is:
0	Not Muted
1	Muted

6.18 DAC Control 4 (Address 15h)

7	6	5	4	3	2	1	0
VQ RAMP	TPS GAIN	Reserved	PDN DAC5	PDN DAC4	PDN DAC3	PDN DAC2	PDN DAC1

6.18.1 VQ Ramp

Ramps common mode voltage “VQ” down to ground. This bit needs to be set before asserting reset pin.

VQ RAMP	Effect:
0	VQ is set at nominal level (VA/2)
1	VQ is ramped from nominal level to ground.

6.18.2 TPS Mode 1 Gain Select

When “TPS MODE” bit in the "TPS Control" register is set to 1, this bit sets the gain of the signal through the TPS path.

TPS GAIN	Effect:
0	Gain is 1
1	Gain is 2

6.18.3 Power Down DACx

Powers down the DACx path.

PDN DACx	DACx is:
0	Powered Up
1	Powered Down

6.19 Volume Mode (Address 16h)

7	6	5	4	3	2	1	0
MUTE DELAY[1:0]		MIN DELAY[2:0]			MAX DELAY[2:0]		

6.19.1 Mute Delay

Sets the delay between the volume steps during the muting and unmuting of a signal when the attenuation mode is set to soft ramp. Each step of the ramp is equal to $^{6.02}/_{64}$ dB ~= 0.094 dB. Settings are given as "x" times the base period.

MUTE DELAY	Delay is:
00	1x
01	4x
10	16x
11	64x

6.19.2 Minimum Delay

Sets the minimum delay before each volume transition. Settings are given in "x" times the base period. See Section 4.6.6 Volume Control for more details regarding the operation of the volume control.

MIN DELAY	Minimum Delay is:
000	1x
001	2x
010	4x
011	8x
100	16x
101	32x
110	64x
111	128x

6.19.3 Maximum Delay

Sets the maximum delay before the volume transition. Settings are given in "x" times the base period. See Section 4.6.6 Volume Control for more details regarding the operation of the volume control.

MAX DELAY	Maximum Delay is:
000	1x
001	2x
010	4x
011	8x
100	16x
101	32x
110	64x
111	128x

6.20 Master and DAC1-5 Volume Control (Address 17h, 18h, 19h, 1Ah, 1Bh, and 1Ch)

7	6	5	4	3	2	1	0
x VOLUME[7:0]							

6.20.1 x Volume Control

Sets the level of the x Volume Control. Each volume step equals $^{6.02}/_{16}$ dB ~= 0.38 dB. See Section 4.6.6.1 on page 43 for the muting behavior of these volume registers.

x VOLUME	x Volume is: [dB]
00000000	+6.02
00001111	+0.38
00010000	0
00010001	-0.38
00011000	-3.01
...	...
11101100	-82.78 (most total attenuation before mute for DAC5)
11101101	-83.15 (least total attenuation before unmute for DAC5)
...	...
11111110	-89.55 (most total attenuation before mute for DAC1-4)
11111111	-89.92 (least total attenuation before unmute for DAC1-4)

6.21 Interrupt Control (Address 1Eh)

7	6	5	4	3	2	1	0
INT MODE	INT POL [1:0]		Reserved	Reserved	Reserved	Reserved	Reserved

6.21.1 INT MODE

Sets the behavior mode of the interrupt registers of the device. In the default configuration, if the interrupt notification registers are read and any error is found to have occurred since the last clearing of that register, the device will automatically set the corresponding mask bit in the appropriate mask register. In the nondefault configuration, the mask bits will not be set automatically.

INT MODE	Upon the reading of an error out of the interrupt notification bits, the CS4234 will:
0	Automatically set the corresponding mask bit.
1	Not set the corresponding mask bit.

6.21.2 Interrupt Pin Polarity

Sets the output mode of the interrupt pin.

INT POL	Output mode of the interrupt pin is:
00	Active High
01	Active Low
10	Active Low/Open Drain
11	Reserved

6.22 Interrupt Mask 1 (Address 1Fh)

7	6	5	4	3	2	1	0
MASK TST MODE ERR	MASK SP ERR	MASK CLK ERR	Reserved	MASK ADC4 OVFL	MASK ADC3 OVFL	MASK ADC2 OVFL	MASK ADC1 OVFL

6.22.1 Test Mode Error Interrupt Mask

Allows or prevents a Test Mode Error event from flagging the interrupt pin. A test mode error occurs when an inadvertent I²C write places the device in test mode.

MASK TST MODE ERR	In the event of a Test Mode Error event, Interrupt Pin will:
0	Be Flagged
1	Not be flagged

6.22.2 Serial Port Error Interrupt Mask

Allows or prevents a Serial Port Error event from flagging the interrupt pin. A serial port error occurs when any of the following control port parameters are changed without first placing the device into power down (power down is defined as all Power Down ADCx and Power Down DACx bits are set to 1):

- Serial Port Format: SP FORMAT[1:0]
- Speed Mode: SPEED MODE[1:0] (If the MCLK/F_S ratio changes without the device being powered down, it will flag this error as well as the Clocking Error.)

MASK SP ERR	In the event of a Serial Port Error event, Interrupt Pin will:
0	Be Flagged
1	Not be flagged

6.22.3 Clocking Error Interrupt Mask

Allows or prevents a Clocking Error event from flagging the interrupt pin. See Section 4.8 for details.

MASK CLK ERR	In the event of a Clocking Error event, Interrupt Pin will:
0	Be Flagged
1	Not be flagged

6.22.4 ADCx Overflow Interrupt Mask

Allows or prevents an ADCx Overflow event from flagging the interrupt pin.

MASK ADCx OVFL	In the event of an ADCx Overflow event, Interrupt Pin will:
0	Be Flagged
1	Not be flagged

6.23 Interrupt Mask 2 (Address 20h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	MASK DAC5 CLIP	MASK DAC4 CLIP	MASK DAC3 CLIP	MASK DAC2 CLIP	MASK DAC1 CLIP

6.23.1 DACx Clip Interrupt Mask

Allows or prevents a DACx Clip event from flagging the interrupt pin.

MASK DACx CLIP	In the event of a DACx Clip event, Interrupt Pin will:
0	Be Flagged
1	Not be flagged

6.24 Interrupt Notification 1 (Address 21h) *(Read Only)*

7	6	5	4	3	2	1	0
TST MOD ERR	SP ERR	CLK ERR	Reserved	ADC4 OVFL	ADC3 OVFL	ADC2 OVFL	ADC1 OVFL

6.24.1 Test Mode Error

A Test Mode Error occurred since the last clearing of the Interrupt Notification register.

TST MOD ERR	Since the last clearing of the Interrupt Notification Register, a Test Mode Error:
0	Has Not Occurred
1	Has Occurred

6.24.2 Serial Port Error

A Serial Port Error occurred since the last clearing of the Interrupt Notification register.

SP ERR	Since the last clearing of the Interrupt Notification Register, a Serial Port Error:
0	Has Not Occurred
1	Has Occurred

6.24.3 Clocking Error

A Clocking Error occurred since the last clearing of the Interrupt Notification register.

CLK ERR	Since the last clearing of the Interrupt Notification Register, a Clocking Error:
0	Has Not Occurred
1	Has Occurred

6.24.4 ADCx Overflow

An ADCx Overflow occurred since the last clearing of the Interrupt Notification register.

ADCx OVFL	Since the last clearing of the Interrupt Notification Register, an ADCx Overflow Error:
0	Has Not Occurred
1	Has Occurred

6.25 Interrupt Notification 2 (Address 22h) *(Read Only)*

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	DAC5 CLIP	DAC4 CLIP	DAC3 CLIP	DAC2 CLIP	DAC1 CLIP

6.25.1 DACx Clip

A DACx Clip occurred since the last clearing of the Interrupt Notification register.

DACx CLIP	Since the last clearing of the Interrupt Notification Register, a DACx Clip Error:
0	Has Not Occurred
1	Has Occurred

7. ADC FILTER PLOTS

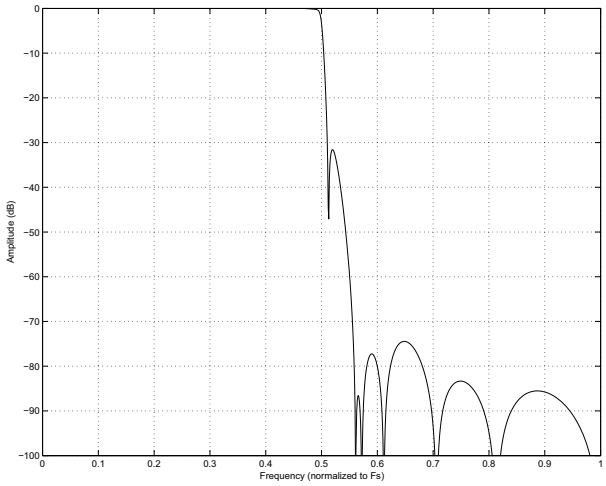


Figure 32. ADC Stopband Rejection

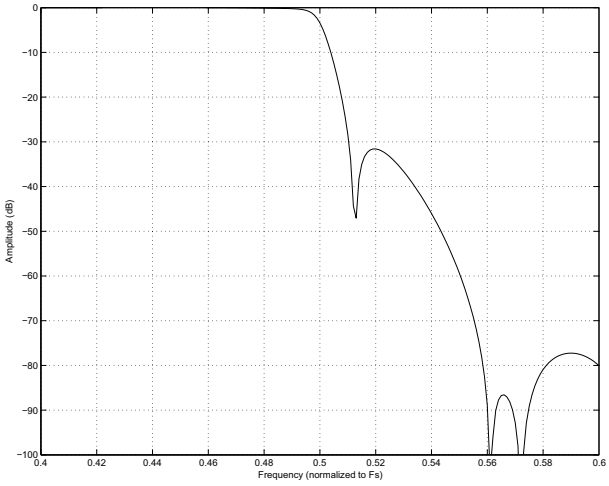


Figure 33. ADC Transition Band

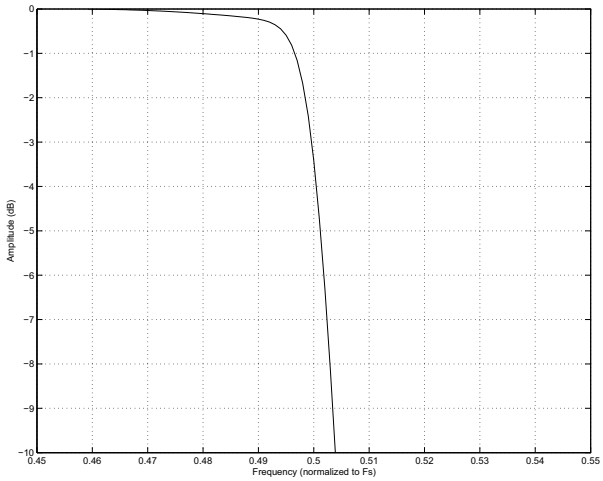


Figure 34. ADC Transition Band (Detail)

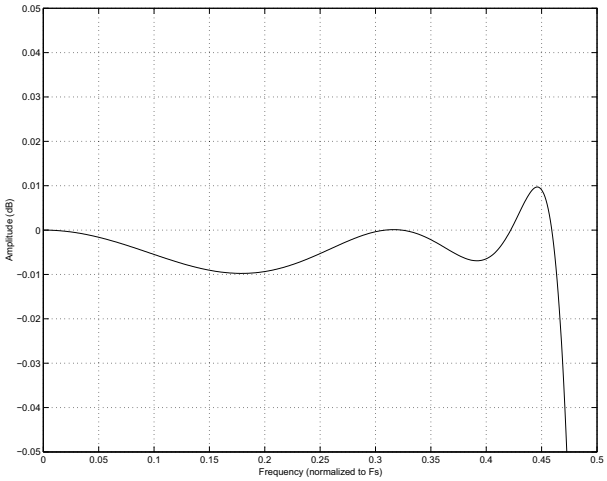


Figure 35. ADC Passband Ripple

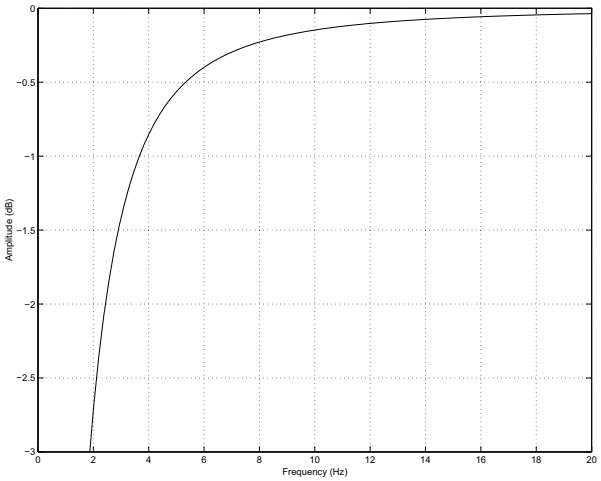


Figure 36. ADC HPF (48 kHz)

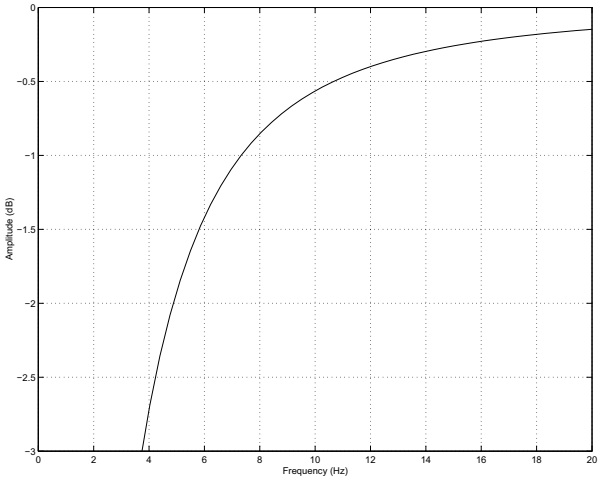


Figure 37. ADC HPF (96 kHz)

8. DAC FILTER PLOTS

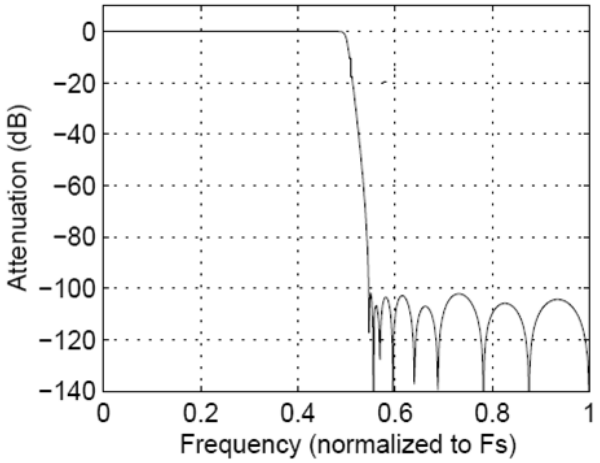


Figure 38. SSM DAC Stopband Rejection

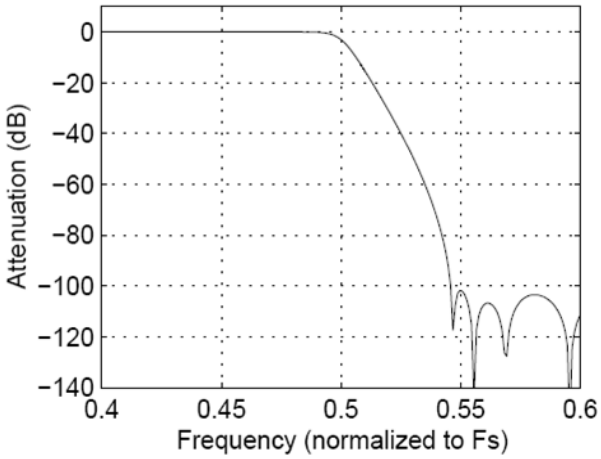


Figure 39. SSM DAC Transition Band

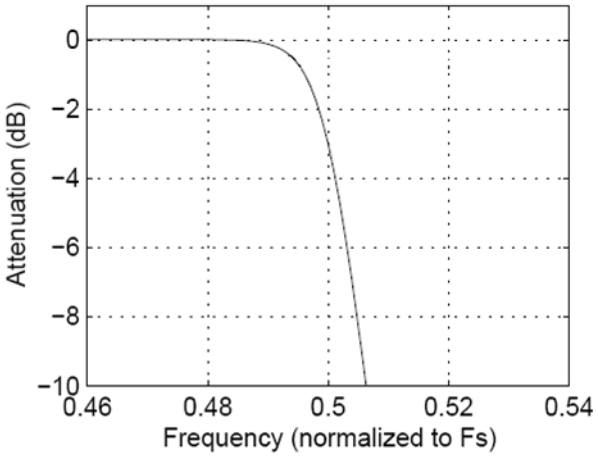


Figure 40. SSM DAC Transition Band (Detail)

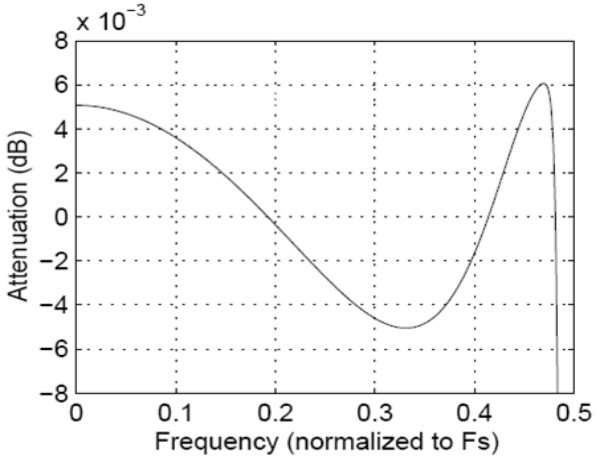


Figure 41. SSM DAC Passband Ripple

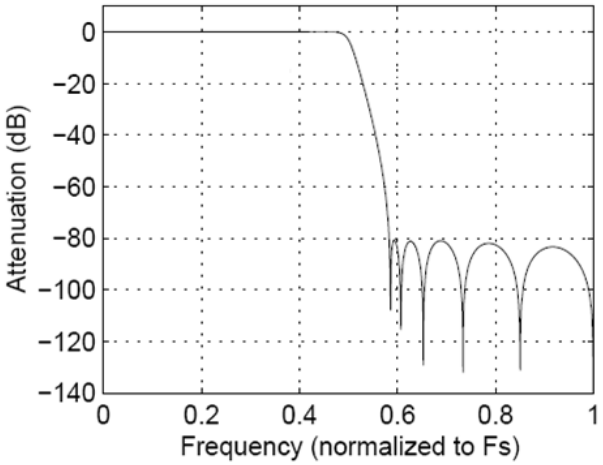


Figure 42. DSM DAC Stopband Rejection

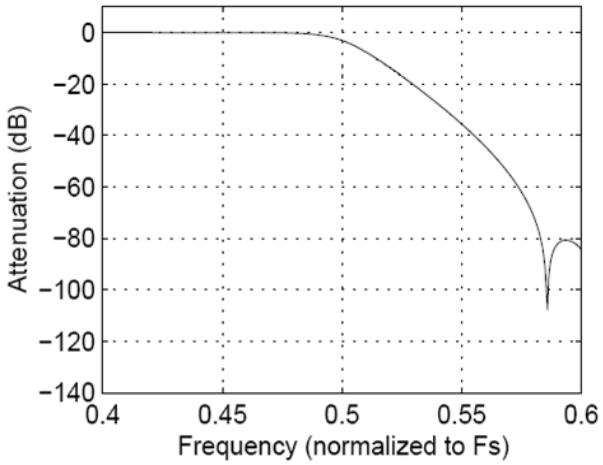


Figure 43. DSM DAC Transition Band

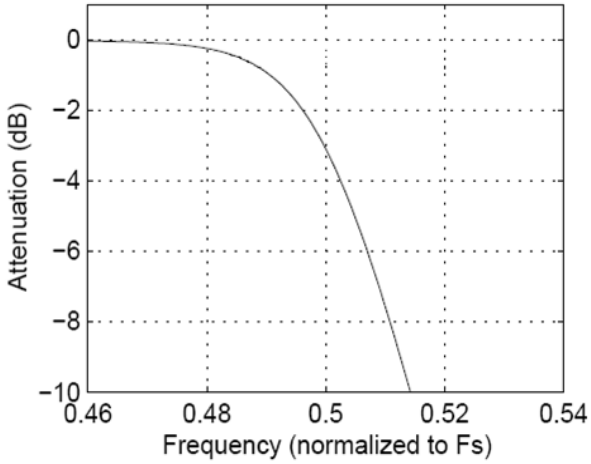


Figure 44. DSM DAC Transition Band (Detail)

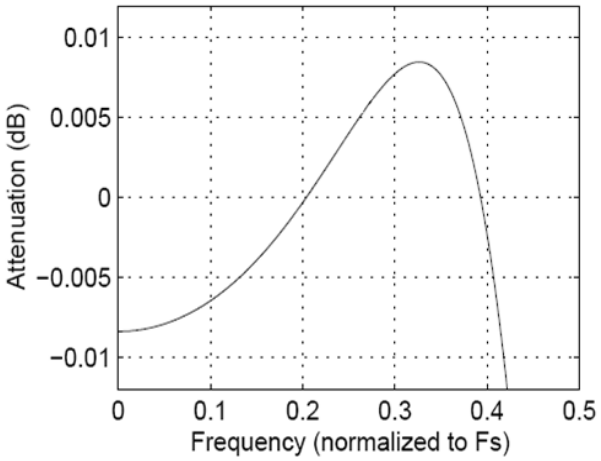


Figure 45. DSM DAC Passband Ripple

9. PACKAGE DIMENSIONS

40L QFN (6 × 6 MM BODY) PACKAGE DRAWING

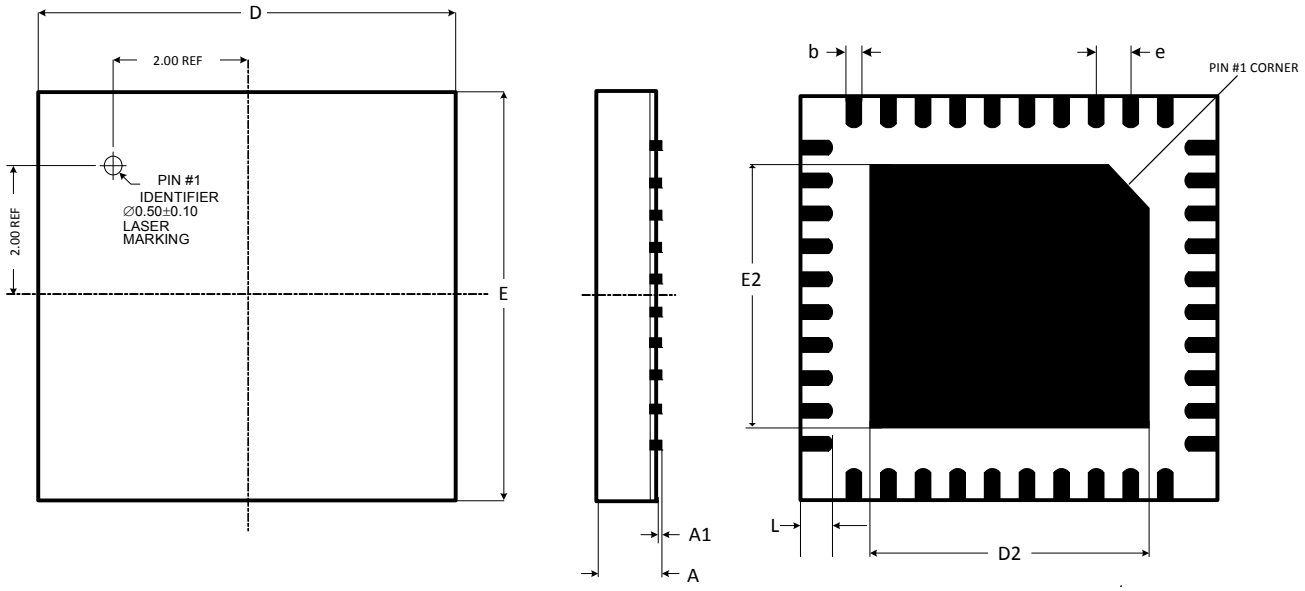


Figure 46. Package Drawing

	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	0.0315	0.0354	0.0354	0.8	0.85	0.9	1
A1	0	0.0014	0.002	0	0.035	0.05	1
b	0.0078	0.0098	0.011	0.2	0.25	0.3	1,2
D		0.2362 BSC			6 BSC		1
D2	0.1594	0.1614	0.1634	4	4.1	4.2	1
E		0.2362 BSC			6 BSC		1
E2	0.1594	0.1614	0.1634	4	4.1	4.2	1
e		0.0197 BSC			0.5 BSC		1
L	0.0118	0.0177	0.0197	0.3	0.45	0.5	1

JEDEC #: MO-220

Controlling Dimension is Millimeters.

Notes: 1. Dimensioning and tolerance per ASME Y4.5M - 1994.

2. Dimensioning lead width applies to the plated terminal and is measured between 0.20 mm and 0.25 mm from the terminal tip.

10.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order#
CS4234	4 In/5 Out CODEC with Programmable Group Delay	40-QFN	Yes	Automotive	-40° to +105°C	Rail	CS4234-ENZ
						Tape and Reel	CS4234-ENZR

11.APPENDIX A: INTERNAL TRACKING POWER SUPPLY SIGNAL

The tracking signal for a Class H amplifier tracks the envelope of the maximum of any arbitrary number of input signals (up to 32 channels for the CS4234). This tracking signal is used to modulate the output voltage of a switch mode power supply (SMPS), which serves as the rail voltages for an audio amplifier. The main goal in any tracking algorithm is to maximize the efficiency of the Class H amplifier by creating a signal that causes the rails of the SMPS, sometimes referred to as a tracking power supply or TPS, to track the amplified audio signal as closely as possible. However, the tracking algorithm must also ensure that the amplifier never clips due to the rail voltage being brought too low relative to the output voltage swing of the audio amplifier.

In order to track the output voltage swing of the amplifier without causing clipping, three controls are provided to ensure the tracking signal stays above (higher amplitude) and ahead of (occurs earlier in time) the output voltage swing of the amplifier. These controls and their respective effects on the tracking signal output on DAC5 are detailed in Figure 47 and listed in the following sections.

With the exception of the Gain Matching control, the appropriate levels for the tracking controls are usually determined experimentally, on an application by application basis. The reason is because the transitioning speed, or bandwidth, of the SMPS is heavily influenced by the capacitance connected to the output nets of the SMPS, the topology of the SMPS, the modulation technique, and the bandwidth of the error amplifier in the feedback loop.

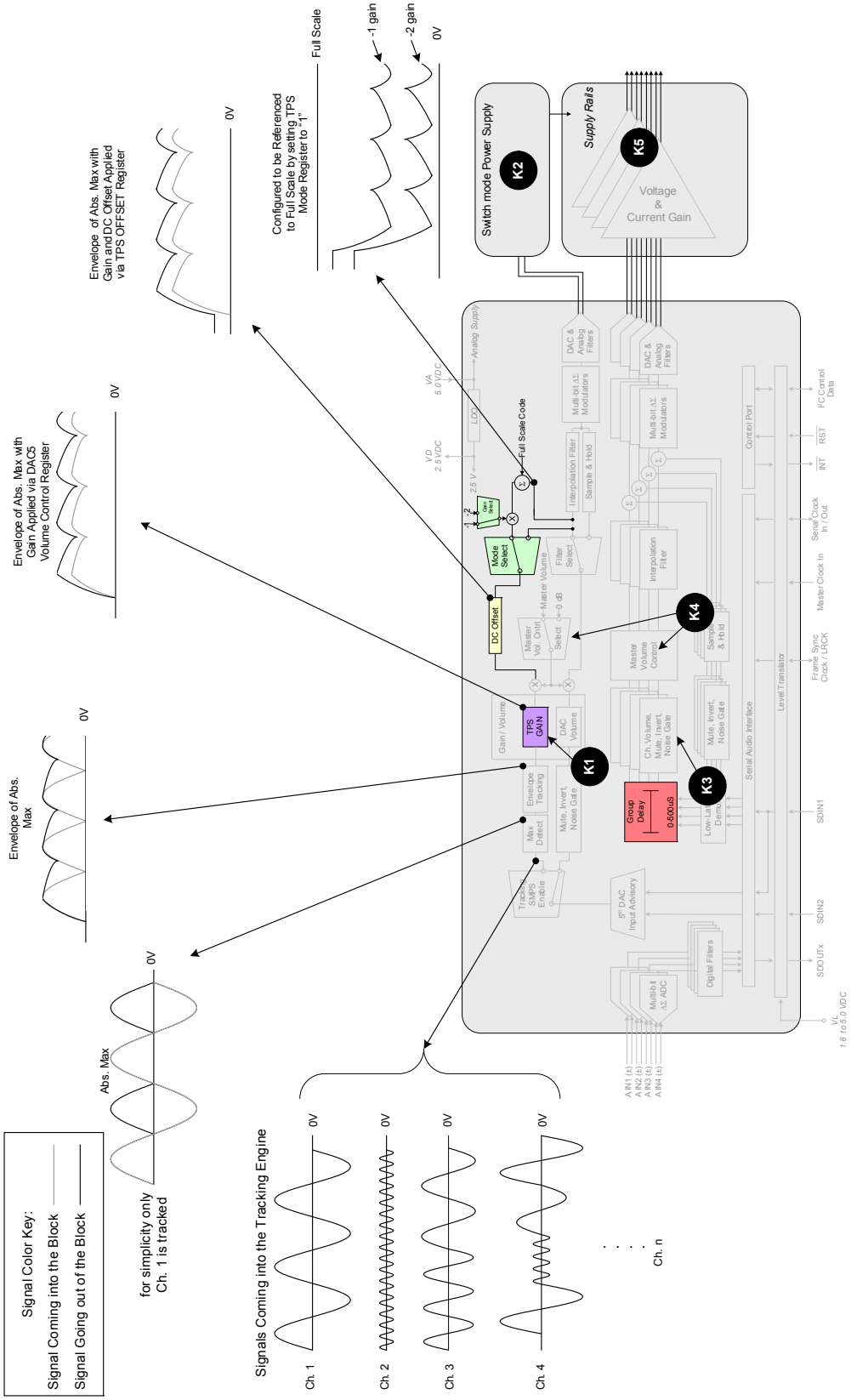


Figure 47. Progression of the Tracking Signal Through the DAC5 Path

11.1 Voltage Headroom

Headroom is another word for the static DC offset inserted into the tracking signal. This offset allows the rail voltages to track the audio amplifier outputs with a sufficient amount of voltage such that a sudden audio bandwidth transition (i.e. 20 kHz or less) across the full dynamic range of the audio amplifier (i.e from 0 V input to full scale input) will not cause the amplifier to clip. This control is contained within the DC Offset block highlighted in yellow in Figure 47.

Adjustment to the DC offset is done through the TPS OFFSET[2:0] bits in the "TPS Control" register. The offset is given in terms of %Full Scale, since the output voltage of the DACs are given relative to VA.

The DC offset applied to the tracking signal affects both the efficiency of the Class H amplifier and the ability of the SMPS to respond to high amplitude transients. By having a smaller DC Offset, the power that is wasted in the output stage of the audio amplifier is reduced. However, since the speed at which the SMPS rail voltages change depends heavily on the bulk capacitance attached to its outputs, providing too small of a DC offset may not provide enough head room for the SMPS to maintain an unclipped audio signal during the time that the rail voltage transitions are charging the bulk capacitance.

Also, unless the resting voltage of the SMPS is set by some other means within the SMPS, the lowest possible DC offset value is dictated by the minimum operating threshold of the audio amplifier attached to the rails of the SMPS. The DC offset, multiplied by the gain of the SMPS “K2”, cannot be less than the amplifier’s operating threshold. If this occurs, the undervoltage lockout protection of the audio amplifier (if equipped) engages prematurely when the rails collapse to a level lower than the allowable operating threshold.

11.2 Lead Time

Lead time is a static time interval that allows the SMPS rails to begin to transition before the amplified audio output signal begins to transition. This is accomplished by delaying the outgoing audio signal sufficiently to prevent the amplified output signal from transitioning faster than the rails can transition. This control is provided by the programmable Group Delay block highlighted in red in Figure 47.

As was the case with the DC offset, there is a connection between the group delay applied to the audio signal, the efficiency of the Class H amplifier, and the ability of the SMPS to respond to high amplitude transients. By having a shorter delay, the output voltage of the SMPS can track the audio signal more closely, increasing efficiency of the Class H system by reducing wasted power in the amplifier output devices. However, providing too short of a delay may not provide enough lead time for the SMPS to react to high frequency, high-amplitude transients, which will result in clipping of the output signal. For these reasons, the group delay of the CS4234 can be adjusted from 100 µs to 500 µs, based on the GROUP DELAY[3:0] setting.

11.3 Gain Matching

Gain matching is necessary to ensure that the gain of the path of the SMPS path is the same as the audio path. The SMPS path consists of the DAC5 path, the SMPS modulator, and the voltage conversion ratio of the SMPS and any components between DAC5 and the SMPS modulator. The audio path consists of DAC1-4 path and the audio amplifier and any components between them. The gains present in each of the blocks of interest are shown in Figure 47 as K1 through K5. The gain matching block “K1”, highlighted in violet, provides the means to ensure that the total gain of the SMPS path, which consists of K1*K4(if applicable)*K2, is as close as possible to the audio path gain, comprised of K3*K4*K5. If the “K3” channel gain is not equal for all channels, use the maximum channel’s gain during this matching calculation to prevent clipping on any channel.

As much as +6 dB of gain and as much as -83 dB of attenuation can be applied to the tracking signal in approximately 0.4 dB steps, although a much smaller range centered around 0 dB is likely. To match the gains between the SMPS and the amplifier, calculate the gain of the audio path and add gain or attenuation as necessary to the SMPS path to make the gains of both paths equal. The addition of gain or attenuation is accomplished via the DAC5 VOLUME[7:0] bits.

11.3.1 SMPS Voltage Conversion Gain (K2)

The gain of the SMPS voltage conversion, in units of V/V, can be determined by dividing the maximum voltage of the SMPS by the maximum voltage permitted by the SMPS modulator stage. Preferably, the maximum voltage permitted by the modulator will be equal to the full scale voltage of DAC5. If it is not, the gain (or attenuation) of any circuitry between the outputs of DAC5 and the modulator must be taken into account. For a differential SMPS, the maximum voltage is represented by VP+ - VP-. For single-ended supplies, the maximum voltage is simply the largest single ended voltage that the SMPS can create.

11.3.2 Amplifier Gain Path (K5)

The amplifier gain is simply the gain applied to the output audio signal by the power amplifier. It is important to note, however, that if different gain amplifiers are all connected to the SMPS, the highest gain setting should be used to set the gain of the SMPS path.

11.4 SMPS (TPS) Modes

The voltage output of a SMPS should be linear and will operate in one of two modes, depending on the topology and modulation of the SMPS. In Mode 0, the SMPS output voltage will be directly proportional to the control signal amplitude. In Mode 1, the SMPS output voltage will be inversely proportional to the control signal amplitude. The transfer function for each mode, which details this behavior, is shown in Figure 48.

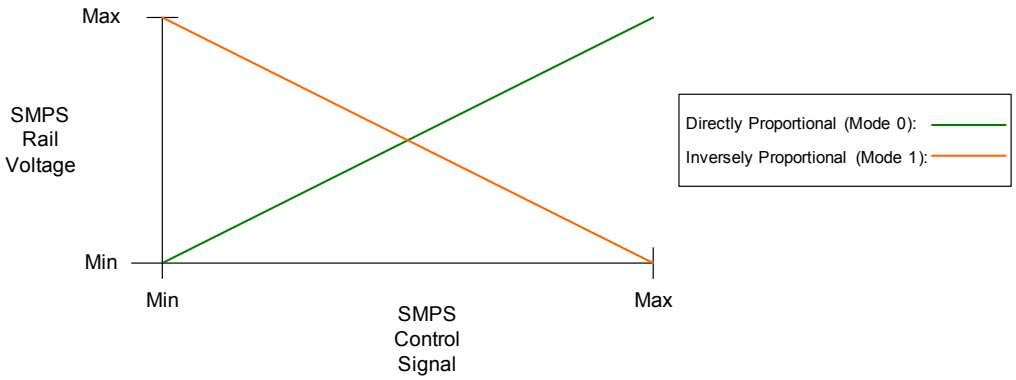


Figure 48. Directly Proportional vs. Indirectly Proportional Modes of Operation

Because of these different modes of operation for the SMPS, it is necessary that the control signal be referenced to 0 V when the SMPS is operated in Mode 0 and referenced to the full scale output voltage of the DAC when the SMPS is operated in Mode 1. To allow the control signal from DAC5 of the CS4234 to be configured for both modes of operation, the TPS MODE bit in the "TPS Control" register is provided. The TPS GAIN bit in the "DAC Control 4" register can be used to modify the control signal in mode 1. Figure 49 shows both the single-ended and differential output signals for each mode of operation. Figure 50 shows how modifying the TPS OFFSET[2:0] and DAC5 VOLUME[7:0] controls affect the transfer functions in each mode.

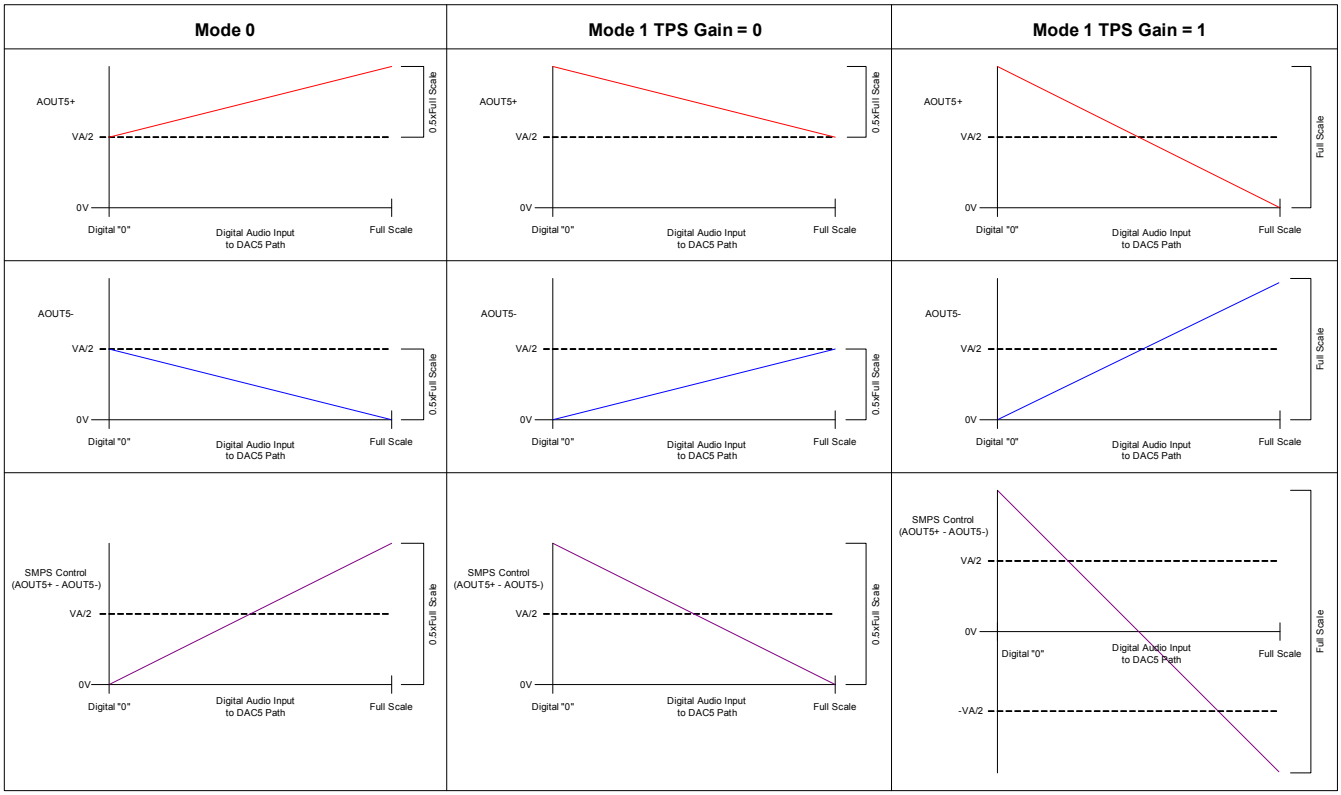


Figure 49. DAC5 TPS Modes of Operation

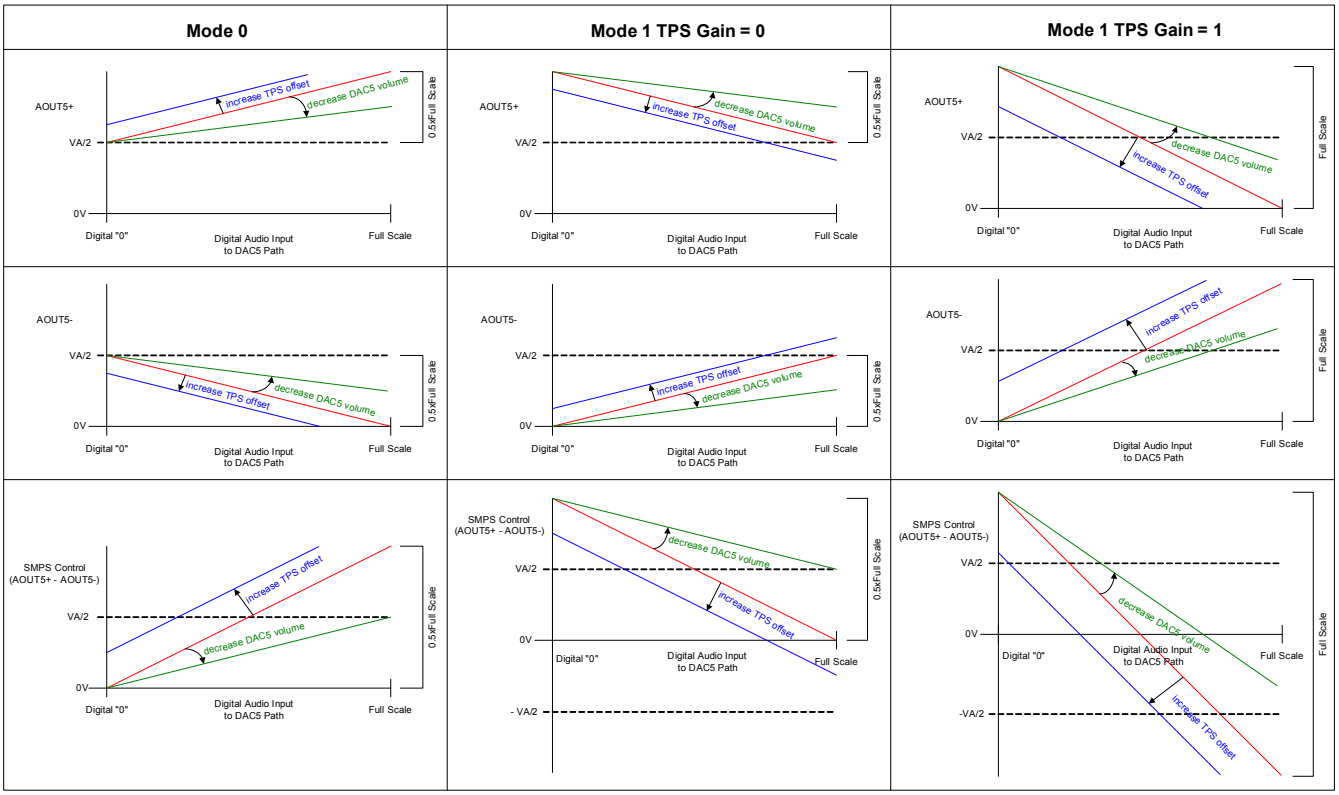


Figure 50. DAC5 Volume and TPS Offset Controls

12.REVISION HISTORY

Release	Changes
F1 MAR ‘12	– Added left justified and I^{2}S serial ports to system features on front page. – Renamed the FS pin to FS/LRCK throughout. – Renamed the SDOUT pin to SDOUT1 throughout and updated the SDOUT1 pin description in Section 1 to include in left justified and I²S modes. – Renamed the AD2 pin to AD2/SDOUT2 throughout and updated the pin description in Section 1 to reflect the combined functionality of the input/output pin, and updated figures throughout to show as bidirectional signal. – Changed SCLK from “Input” to “Input/Output” in pin description in Section 1. – Updated Section 1.1 to reflect the pin name changes. – Updated “Switching Characteristics - Serial Audio Interface” on page 18 to include slave and master modes. – Added Figure 6. TDM Serial Audio Interface Timing and Figure 7. PCM Serial Audio Interface Timing. – Updated Section 4.4 for master/slave mode and left justified/I²S mode functionality. – Added Section 4.5.2 Left Justified and I²S Modes. – Added left justified and I²S mode data routing description to Section 4.6.1.1 ADC Signal Routing and Section 4.6.1.2 DAC1-4, DAC5, and Low-latency Signal Routing. – Added I^{2}S and left-justified options SP_FORMAT field (reg 08h bits 3:2) in Section 6.5.3 Serial Port Format – Added MASTER/SLAVE bit (reg 08h bit 0) to Section 5. Register Quick Reference and Section 6.5 Serial Port Control (Address 08h) and added description, Section 6.5.5 Master / Slave. – Updated PSRR specification in the Analog Input Characteristics table. – Removed note about ADC CM bits in the Analog Input Characteristics table. – Added analog input pins must be externally biased in Section 4.6.2.1. – Changed ADC CM bits to reserved in Section 5 and Section 6.6. – Changed references to PA117 to CS44417 throughout.
F2 OCT ‘14	– Updated dimensions and figure in Section 9. Package Dimensions. (Data sheet change only; no change has been made to the physical device.)

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