STL10N65M2

N-channel 650 V, 0.85 Ω typ., 4.5 A MDmesh M2 Power MOSFET in a PowerFLAT™ 5x6 HV package

Datasheet - production data

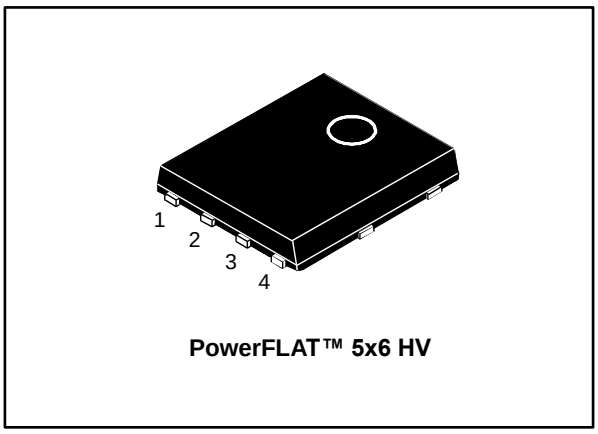
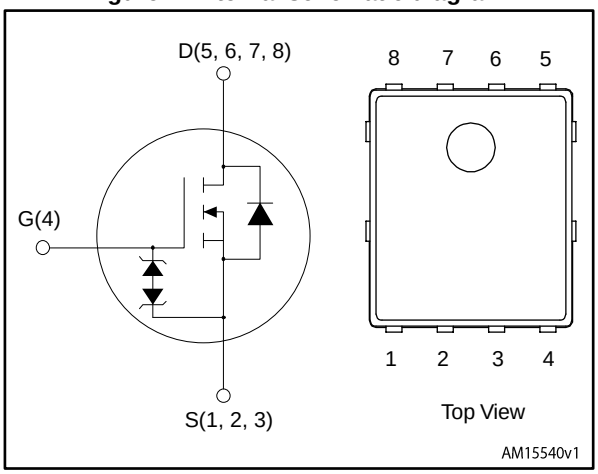


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL10N65M2	650 V	1.00 Ω	4.5 A

- Extremely low gate charge
- Lower $R_{DS(on)}$ x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STL10N65M2	10N65M2	PowerFLAT™ 5x6 HV	Tape and reel

Contents

1 Electrical ratings 3
2 Electrical characteristics 4
2.1 Electrical characteristics (curves) 6
3 Test circuits 8
4 Package information 9
4.1 PowerFLAT™ 5x6 HV package information 10
4.2 PowerFLAT™ 5x6 packing information 12
5 Revision history 14

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	4.5	A
	Drain current (continuous) at T_C = 100 °C	2.8	A
I_{DM} (2)	Drain current pulsed	18	A
P_{TOT}	Total dissipation at T_C = 25 °C	48	W
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_j max)	0.9	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	95	mJ
dv/dt (3)	Peak diode recovery voltage slope	15	V/ns
dv/dt (4)	MOSFET dv/dt ruggedness	50	
T_j	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

Notes:

(1)The value is limited by package.

(2)Pulse width is limited by safe operating area.

(3)I_{SD} ≤ 4.5 A, di/dt ≤ 400 A/µs, $V_{DS(peak)}$ ≤ $V_{(BR)DSS}$, V_{DD} = 80 % $V_{(BR)DSS}$

(4)V_{DS} ≤ 520 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.6	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	50	°C/W

Notes:

(1)When mounted on 1 inch² FR-4 board, 2 oz Cu

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 4: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V T_C = 125 °C(1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2.5 A		0.85	1.00	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	315	-	pF
C_{oss}	Output capacitance		-	18	-	pF
C_{rss}	Reverse transfer capacitance		-	0.86	-	pF
$C_{oss\ eq.}$ (1)	Equivalent capacitance energy related	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	109	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz open drain	-	6.6	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 5 A V_{GS} = 0 to 10 V (see *Figure 15: "Test circuit for gate charge behavior"*)	-	10.3	-	nC
Q_{gs}	Gate-source charge		-	2.4	-	nC
Q_{gd}	Gate-drain charge		-	4.8	-	nC

Notes:

(1)$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}.

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 2.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 14: "Test circuit for resistive load switching times"* and *Figure 19: "Switching time waveform"*)	-	7.5	-	ns
t_r	Rise time		-	6.6	-	ns
$t_{d(off)}$	Turn-off delay time		-	22.5	-	ns
t_f	Fall time		-	18	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4.5	A
I_{SDM}(1)	Source-drain current (pulsed)		-		18	A
V_{SD}(2)	Forward on voltage	I_{SD} = 4.5 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*)	-	276		ns
Q_{rr}	Reverse recovery charge		-	1.7		µC
I_{RRM}	Reverse recovery current		-	12.5		A
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*)	-	312		ns
Q_{rr}	Reverse recovery charge		-	1.9		µC
I_{RRM}	Reverse recovery current		-	12.4		A

Notes:

(1)Pulse width is limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

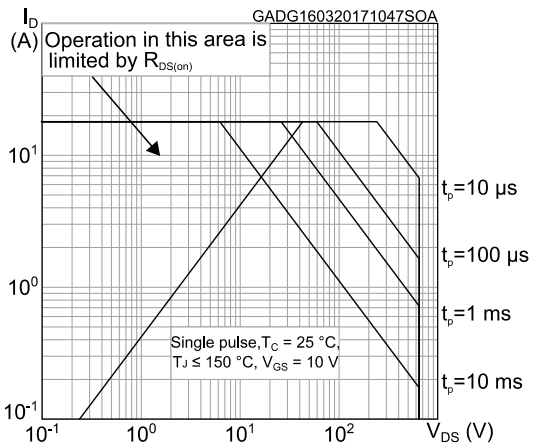


Figure 3: Thermal impedance

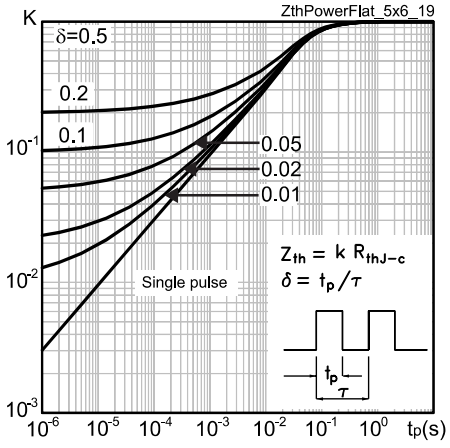


Figure 4: Output characteristics

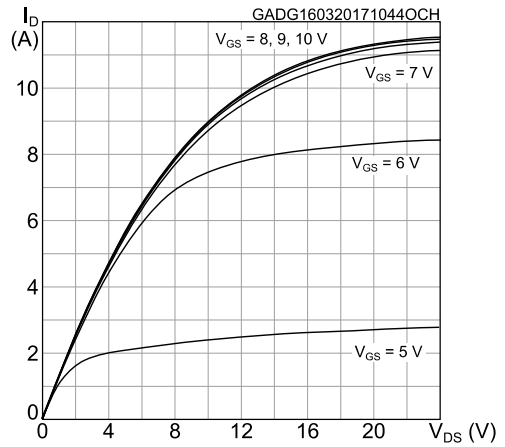


Figure 5: Transfer characteristics

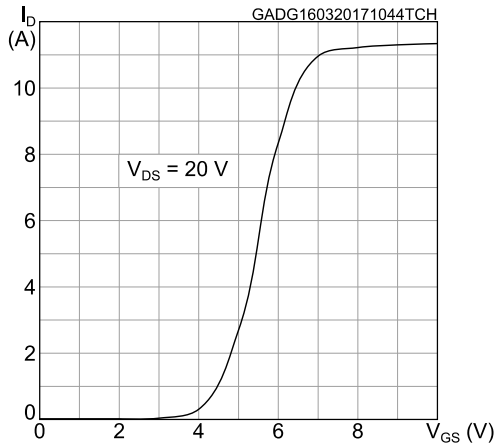


Figure 6: Gate charge vs gate-source voltage

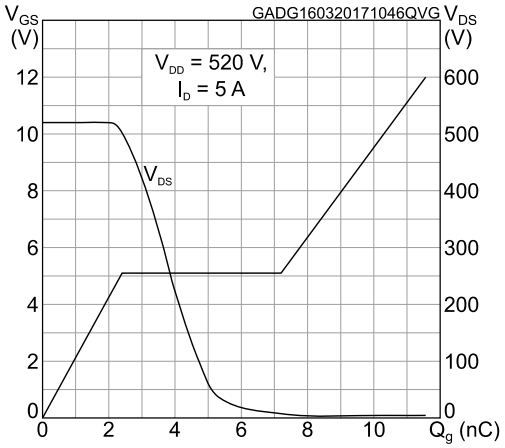


Figure 7: Static drain-source on-resistance

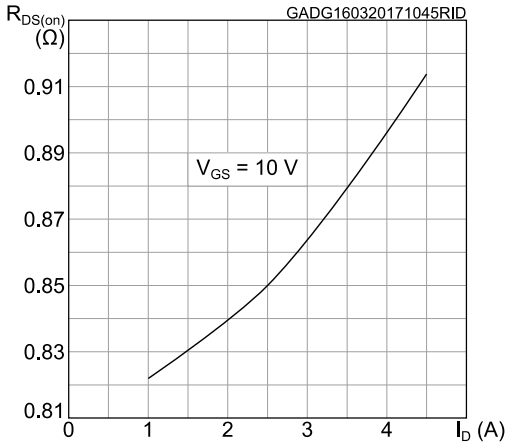


Figure 8: Capacitance variations

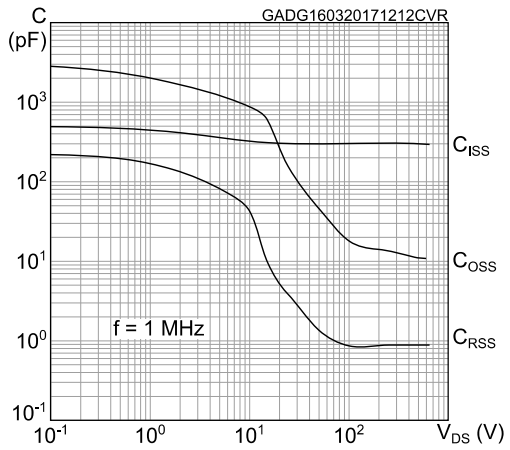


Figure 9: Output capacitance stored energy

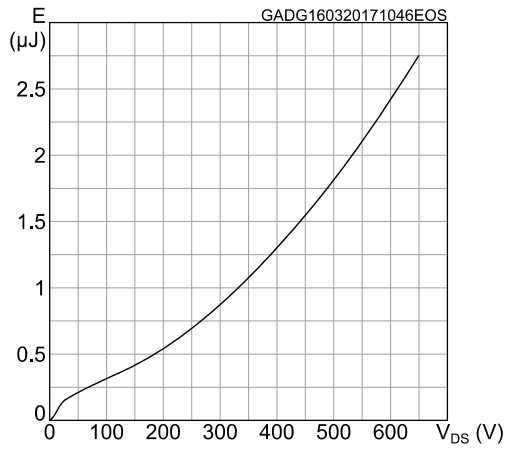


Figure 10: Normalized gate threshold voltage vs temperature

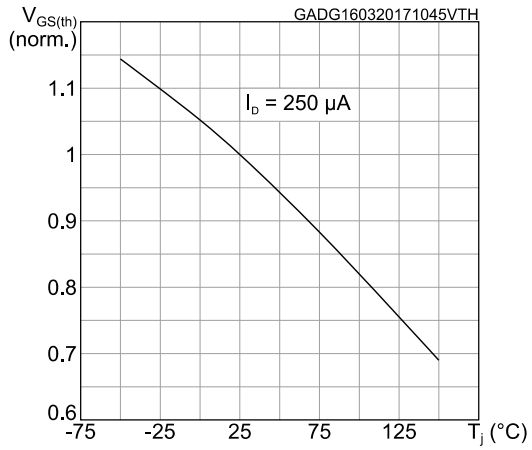


Figure 11: Normalized on-resistance vs temperature

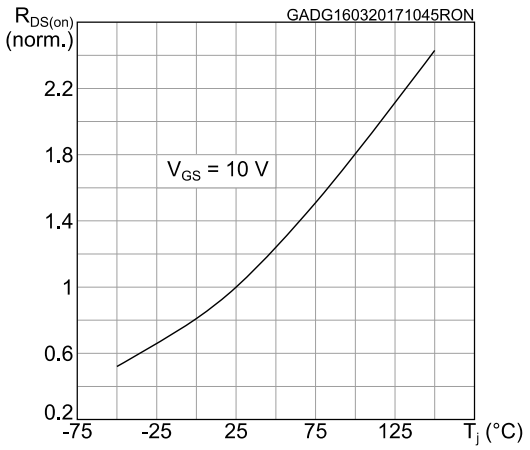


Figure 12: Normalized $V_{(BR)DSS}$ vs temperature

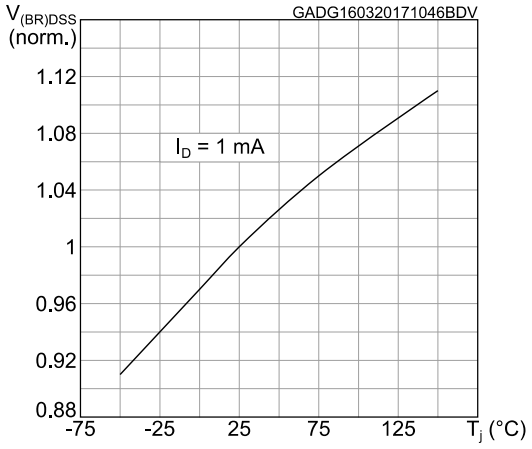
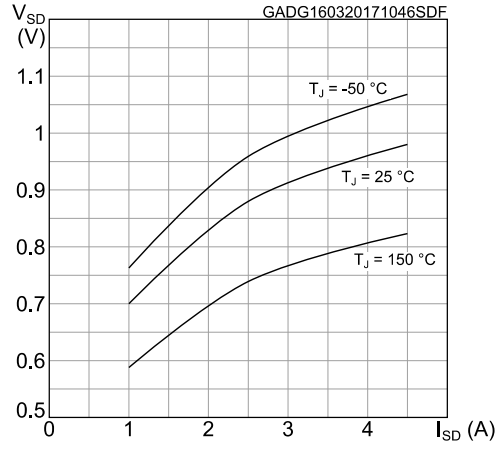


Figure 13: Source-drain diode forward characteristics



3 Test circuits

Figure 14: Test circuit for resistive load switching times

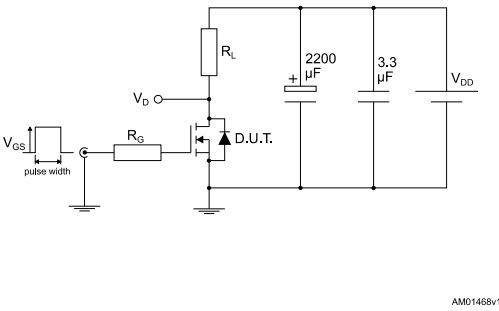


Figure 15: Test circuit for gate charge behavior

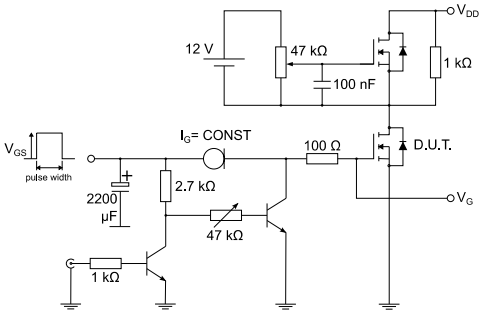


Figure 16: Test circuit for inductive load switching and diode recovery times

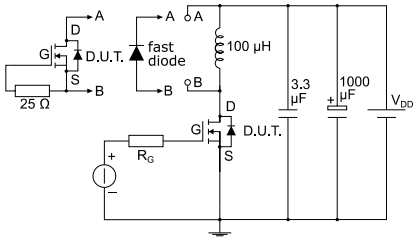


Figure 17: Unclamped inductive load test circuit

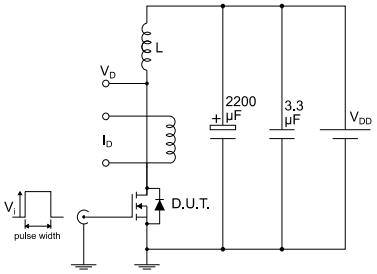


Figure 18: Unclamped inductive waveform

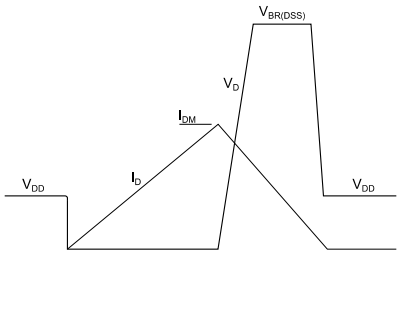
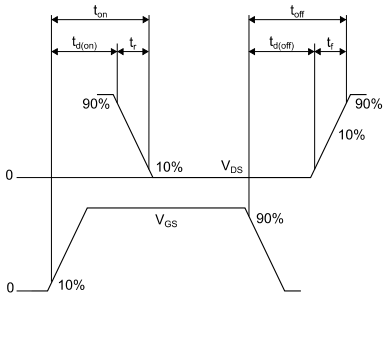


Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 HV package information

Figure 20: PowerFLAT™ 5x6 HV package outline

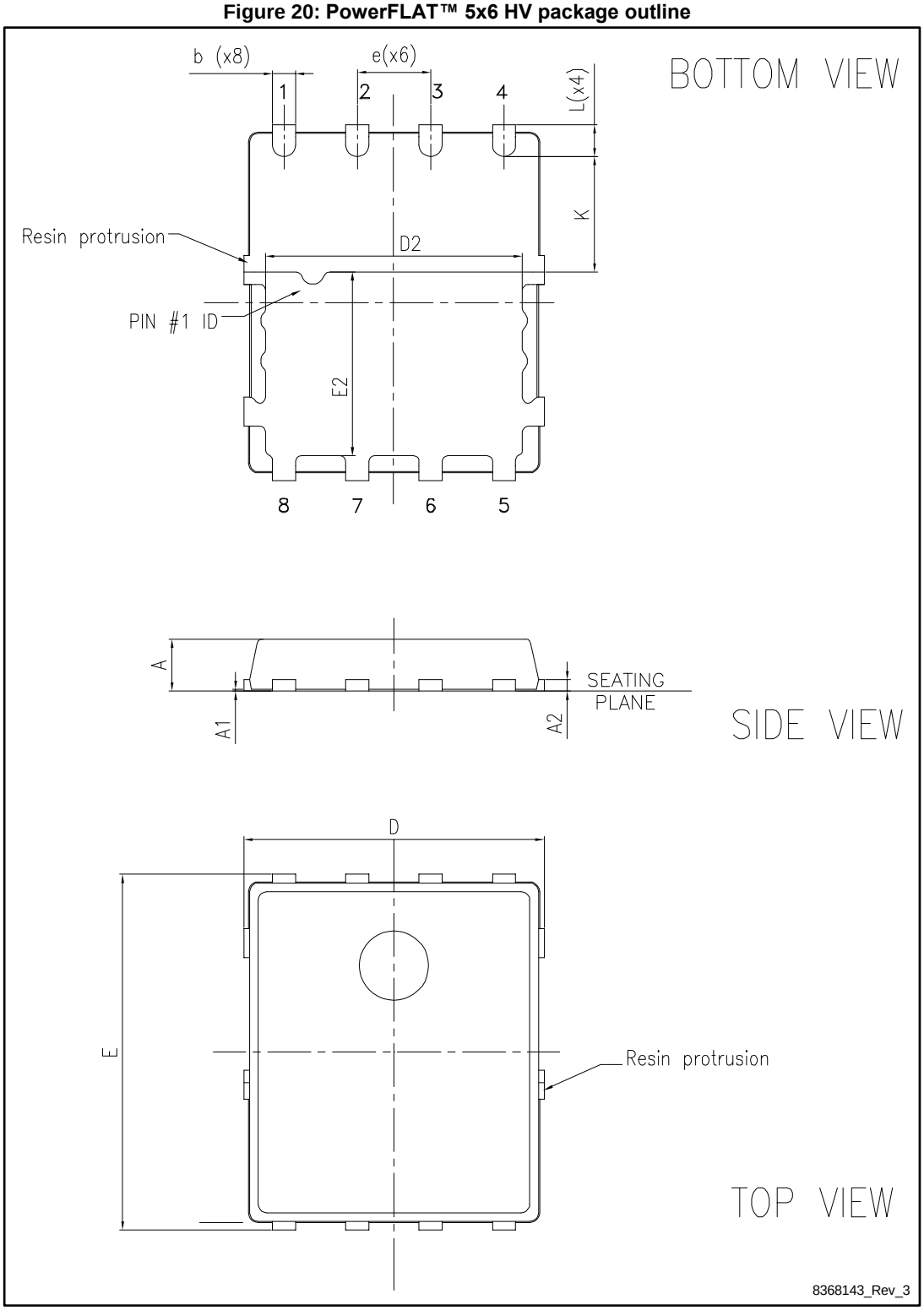
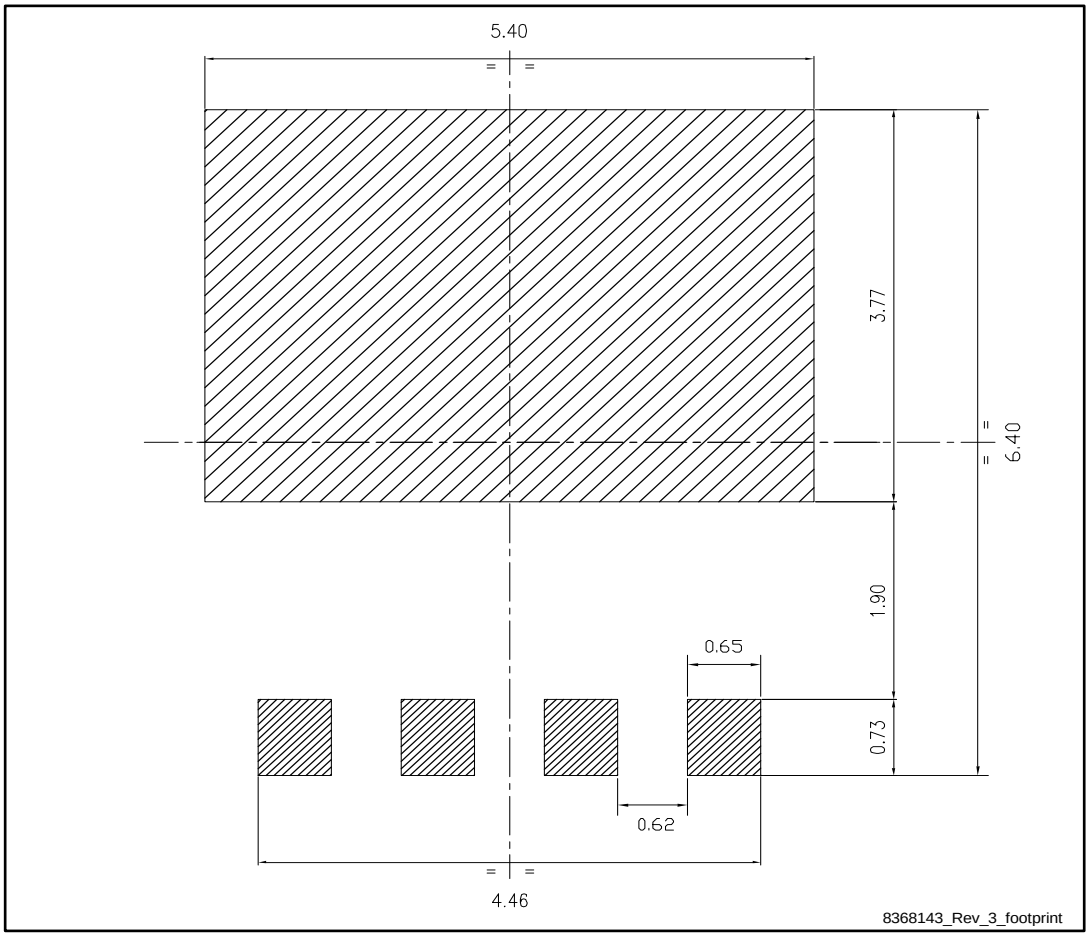


Table 8: PowerFLAT™ 5x6 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.10	5.20	5.30
E	6.05	6.15	6.25
E2	3.10	3.20	3.30
D2	4.30	4.40	4.50
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

Figure 21: PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 packing information

Figure 22: PowerFLAT™ 5x6 tape (dimensions are in mm)

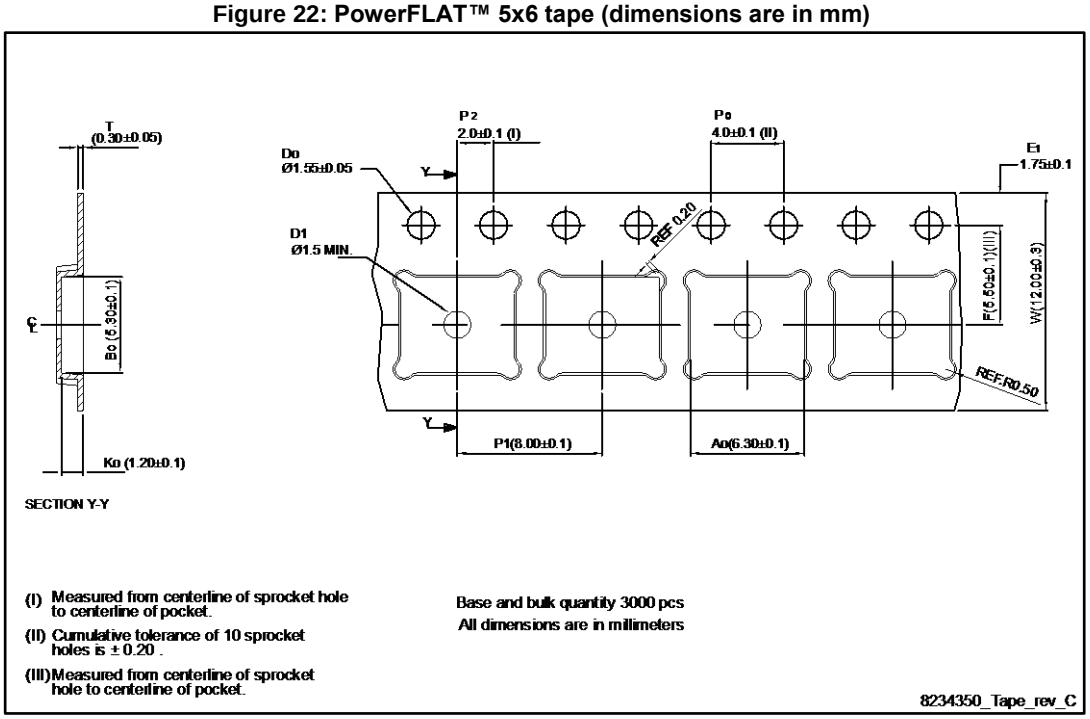


Figure 23: PowerFLAT™ 5x6 package orientation in carrier tape

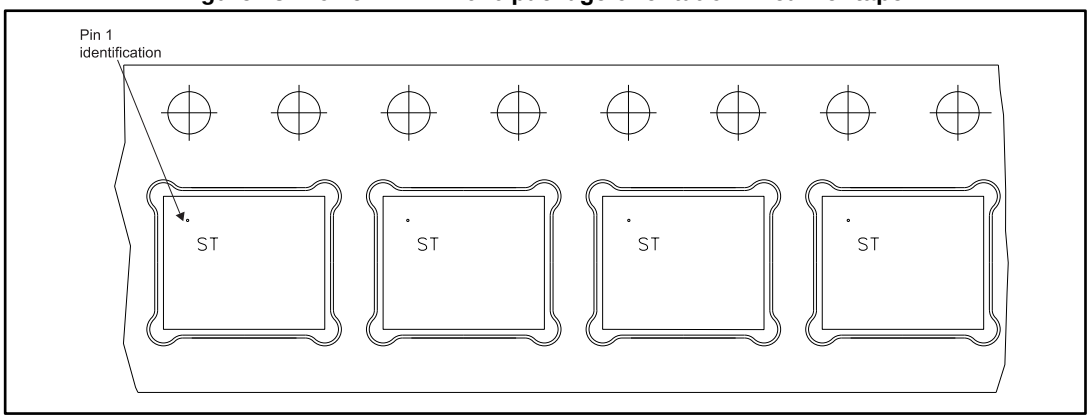
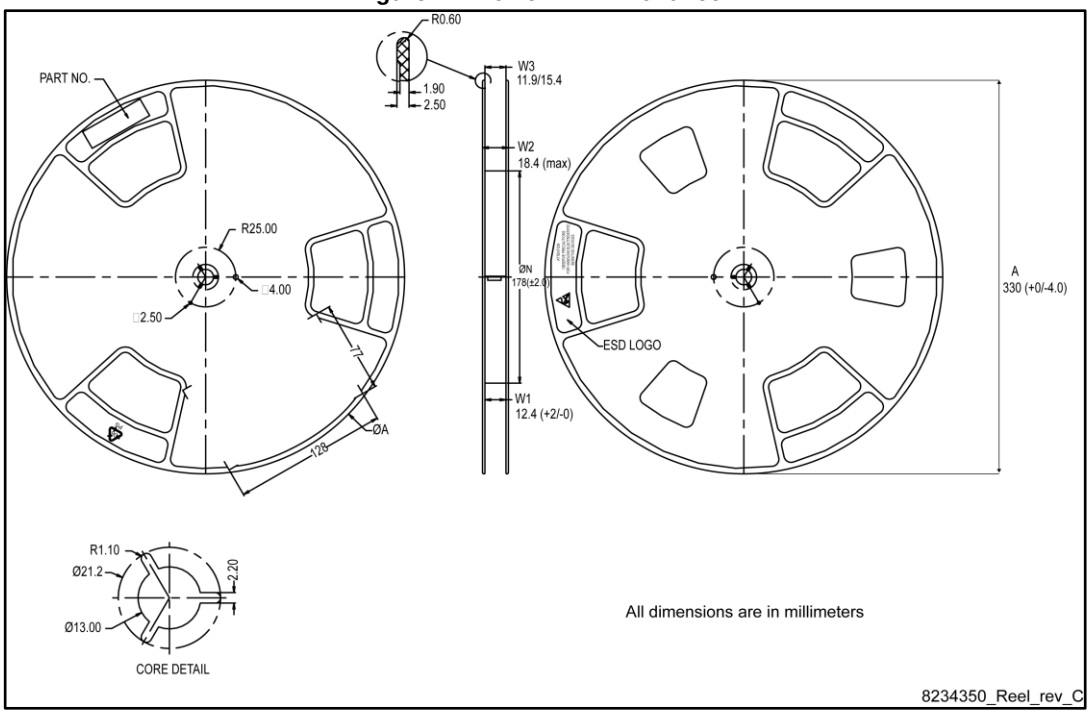


Figure 24: PowerFLAT™ 5x6 reel



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
16-Mar-2017	1	First release

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург, Промышленная ул, дом № 19, литера Н, помещение 100-Н Офис 331