

SN54ABT16501, SN74ABT16501 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS086C – FEBRUARY 1991 – REVISED JANUARY 1997

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- *UBT™* (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

description

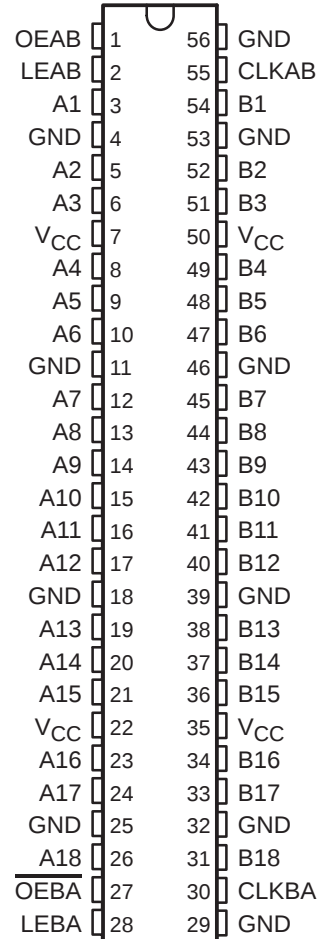
These 18-bit universal bus transceivers consist of storage elements that can operate either as D-type latches or D-type flip-flops to allow data flow in transparent or clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor and $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sourcing/current-sinking capability of the driver.

SN54ABT16501 . . . WD PACKAGE
SN74ABT16501 . . . DGG OR DL PACKAGE
(TOP VIEW)



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**TEXAS
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SN54ABT16501, SN74ABT16501

18-BIT UNIVERSAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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description (continued)

The SN54ABT16501 is characterized for operation over the full military temperature range of -55°C to 125°C .
The SN74ABT16501 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE[†]

INPUTS				OUTPUT B
OEAB	LEAB	CLKAB	A	
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B ₀ [‡]
H	L	L	X	B ₀ [§]

[†] A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{CLKBA}}$.

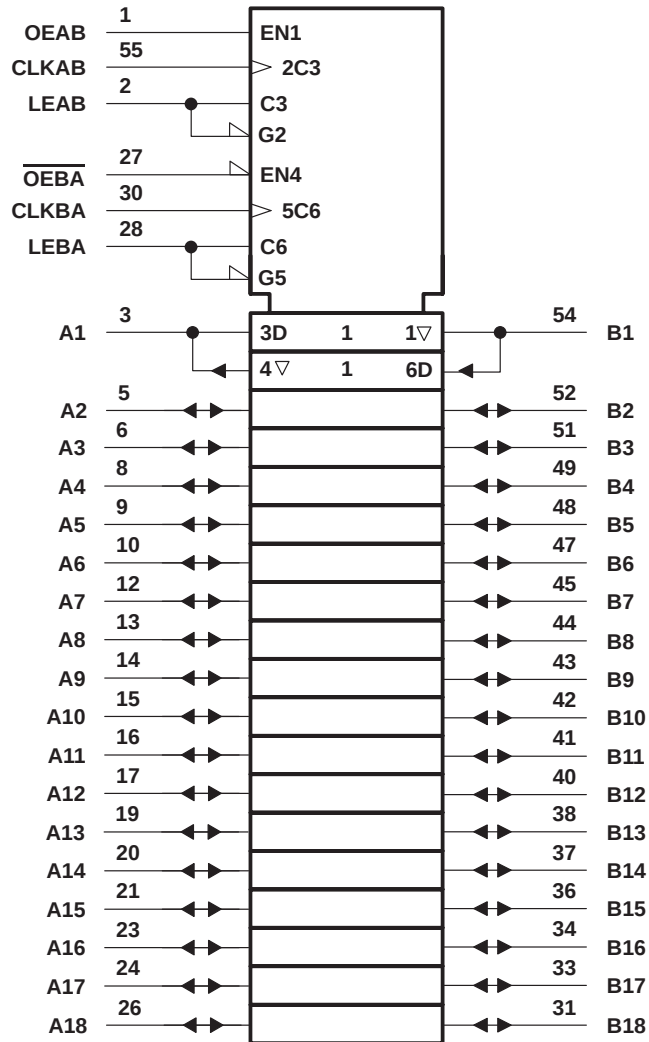
[‡] Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

[§] Output level before the indicated steady-state input conditions were established

SN54ABT16501, SN74ABT16501
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

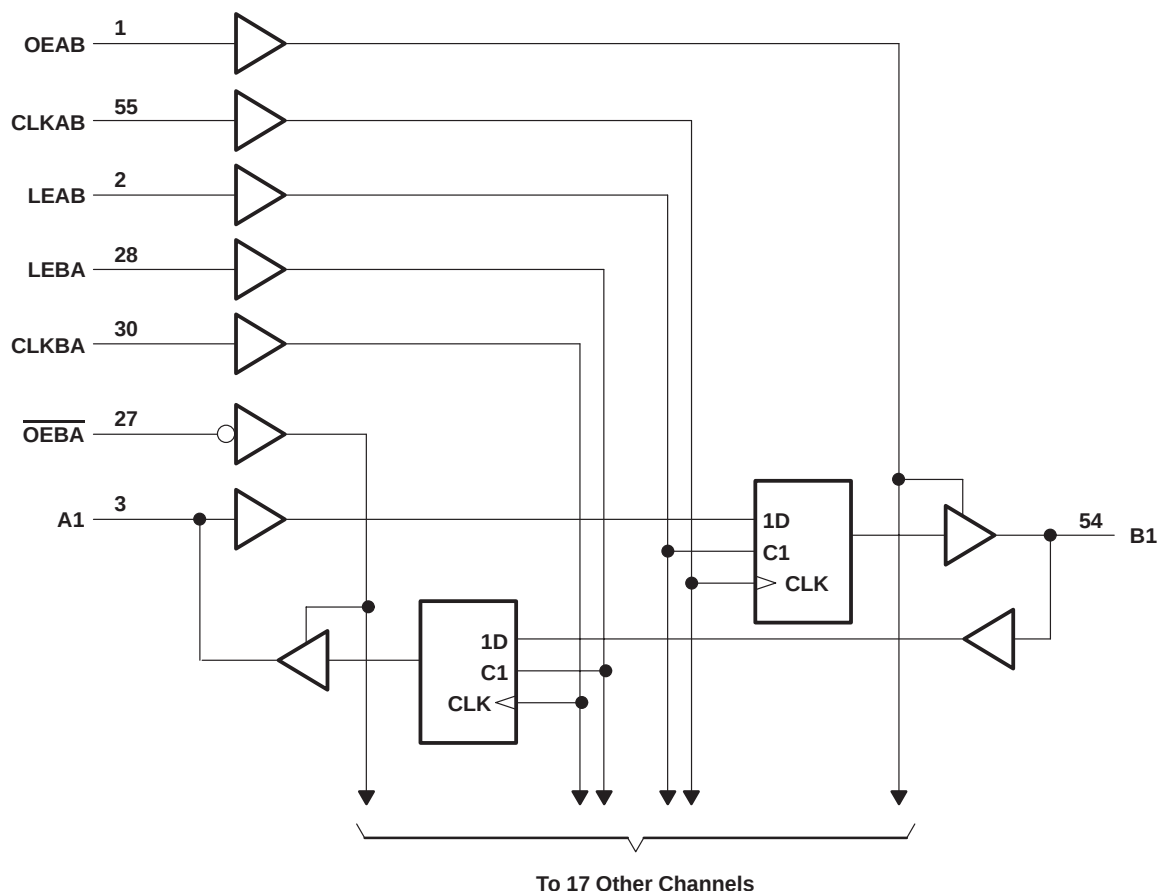
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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16501	96 mA
SN74ABT16501	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

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recommended operating conditions (see Note 3)

			SN54ABT16501		SN74ABT16501		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A = 25°C			SN54ABT16501		SN74ABT16501		UNIT		
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX			
V _{IK}		V _{CC} = 4.5 V, I _I = –18 mA		–1.2			–1.2		–1.2		V		
V _{OH}		V _{CC} = 4.5 V, I _{OH} = –3 mA		2.5			2.5		2.5		V		
		V _{CC} = 5 V, I _{OH} = –3 mA		3			3		3				
		V _{CC} = 4.5 V		I _{OH} = –24 mA			2						
				I _{OH} = –32 mA			2*			2			
V _{OL}		V _{CC} = 4.5 V		I _{OL} = 48 mA		0.55			0.55		V		
				I _{OL} = 64 mA		0.55*			0.55				
V _{hys}				100							mV		
I _I	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND		±1			±1		±1		μA		
	A or B ports			±100			±100		±100				
I _{OZH} ‡		V _{CC} = 5.5 V, V _O = 2.7 V		50			50		50		μA		
I _{OZL} ‡		V _{CC} = 5.5 V, V _O = 0.5 V		–50			–50		–50		μA		
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V		±100					±100		μA		
I _{CEX}		V _{CC} = 5.5 V, V _O = 5.5 V		Outputs high		50			50		μA		
I _O §		V _{CC} = 5.5 V, V _O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA		
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND		Outputs high			3			5		mA	
				Outputs low			76			76			
				Outputs disabled			3.3			5.3			3.3
ΔI _{CC} ¶	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			5			6			5		mA
	A or B ports				1.5			1.5			1.5		
C _i	Control inputs	V _I = 2.5 V or 0.5 V			4						pF		
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V			8						pF		

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				SN54ABT16501		SN74ABT16501		UNIT
				MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency, CLKAB or CLKBA			0	105	0	105	MHz
t _w #	Pulse duration		LEAB or LEBA high	3.3		3.3		ns
			CLKAB or CLKBA high or low	4.7		4.7		
t _{su}	Setup time		A before CLKAB↑ or B before CLKBA↑	4		3.5		ns
			A before LEAB↓ or B before LEBA↓	4		4		
				1.5		1.5		
			CLK low					
t _h	Hold time		A after CLKAB↑ or B after CLKBA↑	1		1		ns
			A after LEAB↓ or B after LEBA↓	2.5		2.5		

This parameter is specified by design, but not production tested.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABT16501		SN74ABT16501		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$	CLKAB or CLKBA		105	160		105		105		MHz
t_{PLH}	A or B	B or A	1	2.6	3.4	1	3.9	1	3.7	ns
t_{PHL}			1	2.6	3.4	1	4.1	1	4	
t_{PLH}	LEAB or LEBA	B or A	1.3	3.3	4.3	1.3	5.4	1.3	5.1	ns
t_{PHL}			1.4	3.1	4.1	1.4	4.6	1.4	4.4	
t_{PLH}	CLKAB or CLKBA	B or A	1.5	3.5	4.5	1.5	5.3	1.5	5	ns
t_{PHL}			1.3	3.1	4.1	1.3	4.6	1.3	4.4	
t_{PZH}	OEAB or $\overline{\text{OEBA}}$	B or A	1	3	4	1	4.8	1	4.7	ns
t_{PZL}			2.6	4.9	5.9	2.6	6.6	2.6	6.5	
t_{PHZ}	OEAB or $\overline{\text{OEBA}}$	B or A	1.6	3.9	4.9	1.6	5.9	1.6	5.8	ns
t_{PLZ}			1.1	3.4	4.4	1.1	5.1	1.1	4.9	

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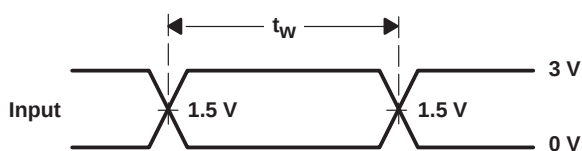
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PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



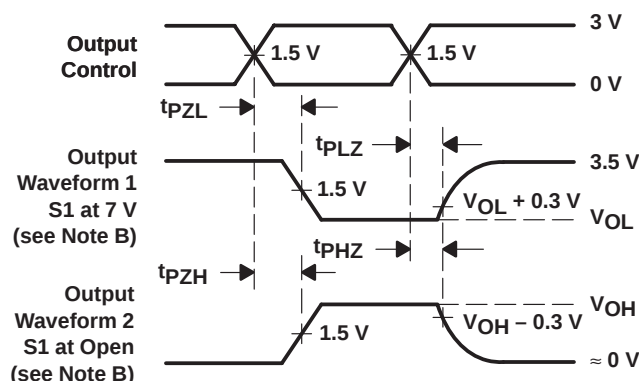
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ABT16501DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ABT16501DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16501DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16501DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16501DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16501DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16501DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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*All dimensions are nominal

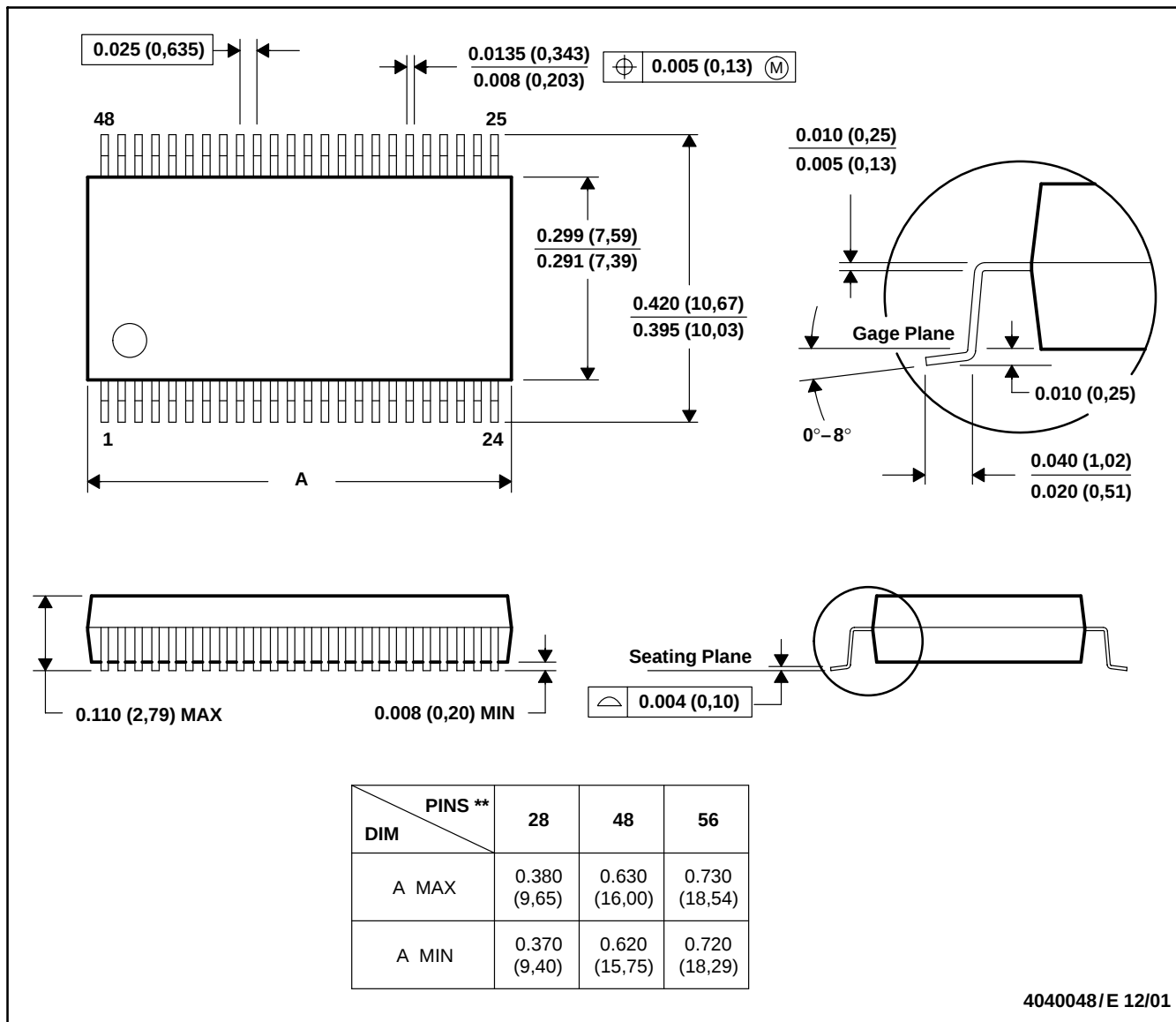
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16501DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ABT16501DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16501DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74ABT16501DLR	SSOP	DL	56	1000	346.0	346.0	49.0

DL (R-PDSO-G)**
PLASTIC SMALL-OUTLINE PACKAGE
48 PINS SHOWN


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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