

GENERAL DESCRIPTION

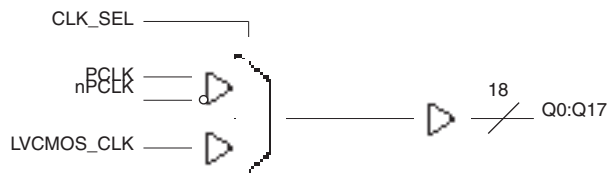
The ICS83940-01 is a low skew, 1-to-18 LVPECL-to-LVCMOS/LVTTTL Fanout Buffer. The ICS83940-01 has two selectable clock inputs. The PCLK, nPCLK pair can accept LVPECL, CML or SSTL input levels. The single ended clock input accepts LVCMOS or LVTTTL input levels. The low impedance LVCMOS/LVTTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 18 to 36 by utilizing the ability of the outputs to drive two series terminated lines.

The ICS83940-01 is characterized at full 3.3V, full 2.5V and mixed 3.3V input and 2.5V output operating supply modes. Guaranteed output and part-to-part skew characteristics make the ICS83940-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

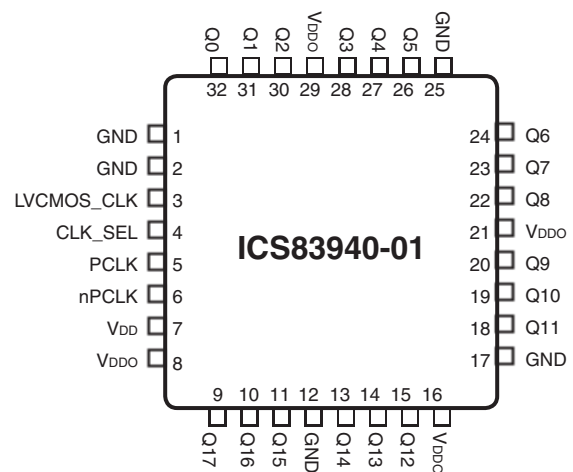
FEATURES

- Eighteen LVCMOS/LVTTTL outputs, 23Ω typical output impedance
- Selectable LVCMOS_CLK or LVPECL clock inputs
- LVCMOS_CLK supports the following input types: LVCMOS or LVTTTL
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- Maximum output frequency: 250MHz
- Output skew: 85ps (maximum)
- Part-to-part skew: 750ps (maximum)
- Full 3.3V, 2.5V or mixed 3.3V, 2.5V supply modes
- 0°C to 70°C ambient operating temperature
- Available in lead-free RoHS compliant package

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP Y Package

7mm x 7mm x 1.4mm package body
Top View

TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|---|--|--------|----------|---|
| 1, 2, 12, 17, 25 | GND | Power | | Power supply ground. |
| 3 | LVC MOS_CLK | Input | Pulldown | Clock input. LVC MOS / LV TTL interface levels. |
| 4 | CLK_SEL | Input | Pulldown | Clock select input. Selects LVC MOS / LV TTL clock input when HIGH. Selects PCLK, nPCLK inputs when LOW. LVC MOS / LV TTL interface levels. |
| 5 | PCLK | Input | Pulldown | Non-inverting differential LVPECL clock input. |
| 6 | nPCLK | Input | | Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating. |
| 7 | V_{DD} | Power | | Power supply pin. |
| 8, 16, 21, 29 | V_{DDO} | Power | | Output supply pins. |
| 9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32 | Q17, Q16, Q15, Q14, Q13, Q12, Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0 | Output | | Clock outputs. LVC MOS / LV TTL interface levels. |

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------|--|-----------------|---------|---------|---------|------------|
| C_{IN} | Input Capacitance | | | 4 | | pF |
| C_{PD} | Power Dissipation Capacitance (per output) | | | 6 | | pF |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | k Ω |
| R_{OUT} | Output Impedance | | 18 | | 28 | Ω |

TABLE 3A. CLOCK SELECT FUNCTION TABLE

| Control Input | Clock | |
|---------------|-------------|-------------|
| CLK_SEL | PCLK, nPCLK | LVC MOS_CLK |
| 0 | Selected | De-selected |
| 1 | De-selected | Selected |

TABLE 3B. CLOCK INPUT FUNCTION TABLE

| Inputs | | | | Outputs | Input to Output Mode | Polarity |
|---------|-------------|----------------|----------------|---------|------------------------------|---------------|
| CLK_SEL | LVC MOS_CLK | PCLK | nPCLK | Q0:Q17 | | |
| 0 | — | 0 | 1 | LOW | Differential to Single Ended | Non Inverting |
| 0 | — | 1 | 0 | HIGH | Differential to Single Ended | Non Inverting |
| 0 | — | 0 | Biased; NOTE 1 | LOW | Single Ended to Single Ended | Non Inverting |
| 0 | — | 1 | Biased; NOTE 1 | HIGH | Single Ended to Single Ended | Non Inverting |
| 0 | — | Biased; NOTE 1 | 0 | HIGH | Single Ended to Single Ended | Inverting |
| 0 | — | Biased; NOTE 1 | 1 | LOW | Single Ended to Single Ended | Inverting |
| 1 | 0 | — | — | LOW | Single Ended to Single Ended | Non Inverting |
| 1 | 1 | — | — | HIGH | Single Ended to Single Ended | Non Inverting |

NOTE 1: Please refer to the Application Information section, "Wiring the Differential Input to Accept Single Ended Levels".

ABSOLUTE MAXIMUM RATINGS

| | |
|--------------------------------|---------------------------|
| Supply Voltage, V_{DD} | 3.6V |
| Inputs, V_I | -0.3V to $V_{DD} + 0.3V$ |
| Outputs, V_O | -0.3V to $V_{DDO} + 0.3V$ |
| Input Current, I_{IN} | $\pm 20mA$ |
| Storage Temperature, T_{STG} | -40°C to 125°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ$ TO 70°

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|---|------------------|----------------|---------|----------------|---------|
| V_{IH} | Input High Voltage | LVCNOS_CLK | 2.4 | | V_{DD} | V |
| V_{IL} | Input Low Voltage | LVCNOS_CLK | | | 0.8 | V |
| V_{PP} | Peak-to-Peak Input Voltage | PCLK, nPCLK | 500 | | 1000 | mV |
| V_{CMR} | Input Common Mode Voltage; NOTE 1, 2 | PCLK, nPCLK | $V_{DD} - 1.4$ | | $V_{DD} - 0.6$ | V |
| I_{IN} | Input Current | | | | ± 200 | μA |
| V_{OH} | Output High Voltage | $I_{OH} = -20mA$ | 2.4 | | | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 20mA$ | | | 0.5 | V |
| I_{DD} | Power Supply Current | | | | 25 | mA |

NOTE 1: For single ended applications, the maximum input voltage for PCLK, nPCLK is $V_{DD} + 0.3V$.

NOTE 2: Common mode voltage is defined as V_{IH} .

TABLE 4B. DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ$ TO 70°

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|---|------------------|----------------|---------|----------------|---------|
| V_{IH} | Input High Voltage | LVCNOS_CLK | 2.4 | | V_{DD} | V |
| V_{IL} | Input Low Voltage | LVCNOS_CLK | | | 0.8 | V |
| V_{PP} | Peak-to-Peak Input Voltage | PCLK, nPCLK | 300 | | 1000 | mV |
| V_{CMR} | Input Common Mode Voltage; NOTE 1, 2 | PCLK, nPCLK | $V_{DD} - 1.4$ | | $V_{DD} - 0.6$ | V |
| I_{IN} | Input Current | | | | ± 200 | μA |
| V_{OH} | Output High Voltage | $I_{OH} = -20mA$ | 1.8 | | | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 20mA$ | | | 0.5 | V |
| I_{DD} | Power Supply Current | | | | 25 | mA |

NOTE 1: For single ended applications, the maximum input voltage for PCLK, nPCLK is $V_{DD} + 0.3V$.

NOTE 2: Common mode voltage is defined as V_{IH} .

TABLE 4C. DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ$ TO 70°

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|---|------------------|----------------|---------|----------------|---------|
| V_{IH} | Input High Voltage | LVC MOS_CLK | 2 | | V_{DD} | V |
| V_{IL} | Input Low Voltage | LVC MOS_CLK | | | 0.8 | V |
| V_{PP} | Peak-to-Peak Input Voltage | PCLK, nPCLK | 300 | | 1000 | mV |
| V_{CMR} | Input Common Mode Voltage; NOTE 1, 2 | PCLK, nPCLK | $V_{DD} - 1.4$ | | $V_{DD} - 0.6$ | V |
| I_{IN} | Input Current | | | | ± 200 | μA |
| V_{OH} | Output High Voltage | $I_{OH} = -12mA$ | 1.8 | | | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 12mA$ | | | 0.5 | V |
| I_{DD} | Power Supply Current | | | | 25 | mA |

NOTE 1: For single ended applications, the maximum input voltage for PCLK, nPCLK is $V_{DD} + 0.3V$.NOTE 2: Common mode voltage is defined as V_{IH} .**TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ$ TO 70°**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------|---------------------------------|---------------------------|--|---------|---------|-------|
| f_{MAX} | Output Frequency | | | | 250 | MHz |
| t_{PLH} | Propagation Delay | PCLK, nPCLK; NOTE 1, 5 | f 150MHz | 1.6 | 3.0 | ns |
| | | LVC MOS_CLK; NOTE 2, 5 | f 150MHz | 1.8 | 3.0 | ns |
| t_{PLH} | Propagation Delay | PCLK, nPCLK; NOTE 1, 5 | f > 150MHz | 1.6 | 3.3 | ns |
| | | LVC MOS_CLK; NOTE 2, 5 | f > 150MHz | 1.8 | 3.2 | ns |
| tsk(o) | Output Skew; NOTE 3, 5 | PCLK, nPCLK | Measured on rising edge @ $V_{DDO}/2$ | | 85 | ps |
| | | LVC MOS_CLK | | | 85 | ps |
| tsk(pp) | Part-to-Part Skew; NOTE 6 | PCLK, nPCLK | f 150MHz | | 1.4 | ns |
| | | LVC MOS_CLK | f 150MHz | | 1.2 | ns |
| tsk(pp) | Part-to-Part Skew; NOTE 6 | PCLK, nPCLK | f > 150MHz | | 1.7 | ns |
| | | LVC MOS_CLK | f > 150MHz | | 1.4 | ns |
| tsk(pp) | Part-to-Part Skew; NOTE 4, 5 | PCLK, nPCLK | Measured on rising edge @ $V_{DDO}/2$ | | 850 | ps |
| | | LVC MOS_CLK | | | 750 | ps |
| t_R, t_F | Output Rise/Fall Time | 20% to 80% | 400 | | 800 | ps |
| odc | Output Duty Cycle | f 150MHz | 45 | | 55 | % |
| | | 150MHz < f 250MHz | 40 | | 60 | % |

All parameters measured at 200MHz unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output $V_{DDO}/2$.NOTE 2: Measured from $V_{DD}/2$ to $V_{DDO}/2$.NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages, same temperature, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6: Defined as skew between outputs on different devices, across temperature and voltage ranges, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ$ TO 70°

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------|---------------------------------|----------------------------|--|---------|---------|-------|
| f_{MAX} | Output Frequency | | | | 250 | MHz |
| t_{pLH} | Propagation Delay | PCLK, nPCLK; NOTE 1, 5 | f 150MHz | 1.7 | 3.2 | ns |
| | | LVCOSMOS_CLK; NOTE 2, 5 | f 150MHz | 1.7 | 3.0 | ns |
| t_{pLH} | Propagation Delay | PCLK, nPCLK; NOTE 1, 5 | f > 150MHz | 1.6 | 3.4 | ns |
| | | LVCOSMOS_CLK; NOTE 2, 5 | f > 150MHz | 1.8 | 3.3 | ns |
| tsk(o) | Output Skew; NOTE 3, 5 | PCLK, nPCLK | Measured on rising edge @ $V_{DDO}/2$ | | 150 | ps |
| | | LVCOSMOS_CLK | | | 150 | ps |
| tsk(pp) | Part-to-Part Skew; NOTE 6 | PCLK, nPCLK | f 150MHz | | 1.5 | ns |
| | | LVCOSMOS_CLK | f 150MHz | | 1.3 | ns |
| tsk(pp) | Part-to-Part Skew; NOTE 6 | PCLK, nPCLK | f > 150MHz | | 1.8 | ns |
| | | LVCOSMOS_CLK | f > 150MHz | | 1.5 | ns |
| tsk(pp) | Part-to-Part Skew; NOTE 4, 5 | PCLK, nPCLK | Measured on rising edge @ $V_{DDO}/2$ | | 850 | ps |
| | | LVCOSMOS_CLK | | | 750 | ps |
| t_R, t_F | Output Rise/Fall Time | 20% to 80% | 400 | | 800 | ps |
| odc | Output Duty Cycle | | f < 134MHz | 45 | 55 | % |
| | | | 134MHz f < 250MHz | 40 | 60 | % |

All parameters measured at 200MHz unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output $V_{DDO}/2$.

NOTE 2: Measured from $V_{DD}/2$ to $V_{DDO}/2$.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages, same temperature, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6: Defined as skew between outputs on different devices, across temperature and voltage ranges, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

TABLE 5C. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ$ TO 70°

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------|---------------------------------|----------------------------|--|---------|---------|-------|
| f_{MAX} | Output Frequency | | | | 200 | MHz |
| t_{pLH} | Propagation Delay; | PCLK, nPCLK; NOTE 1, 5 | f 150MHz | 1.2 | 3.8 | ns |
| | | LVCOSMOS_CLK; NOTE 2, 5 | f 150MHz | 1.5 | 3.2 | ns |
| t_{pLH} | Propagation Delay; | PCLK, nPCLK; NOTE 1, 5 | f > 150MHz | 1.5 | 3.7 | ns |
| | | LVCOSMOS_CLK; NOTE 2, 5 | f > 150MHz | 2 | 3.6 | ns |
| tsk(o) | Output Skew; NOTE 3, 5 | PCLK, nPCLK | Measured on rising edge @ $V_{DDO}/2$ | | 150 | ps |
| | | LVCOSMOS_CLK | | | 150 | ps |
| tsk(pp) | Part-to-Part Skew; NOTE 6 | PCLK, nPCLK | f 150MHz | | 2.6 | ns |
| | | LVCOSMOS_CLK | f 150MHz | | 1.7 | ns |
| tsk(pp) | Part-to-Part Skew; NOTE 6 | PCLK, nPCLK | f > 150MHz | | 2.2 | ns |
| | | LVCOSMOS_CLK | f > 150MHz | | 1.7 | ns |
| tsk(pp) | Part-to-Part Skew; NOTE 4, 5 | PCLK, nPCLK | Measured on rising edge @ $V_{DDO}/2$ | | 1.2 | ns |
| | | LVCOSMOS_CLK | | | 1.0 | ns |
| t_R, t_F | Output Rise/Fall Time | 20% to 80% | 400 | | 800 | ps |
| odc | Output Duty Cycle | f < 134MHz | 45 | | 55 | % |
| | | 134MHz f 200MHz | 40 | | 60 | % |

All parameters measured at 200MHz unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output $V_{DDO}/2$.

NOTE 2: Measured from $V_{DD}/2$ to $V_{DDO}/2$.

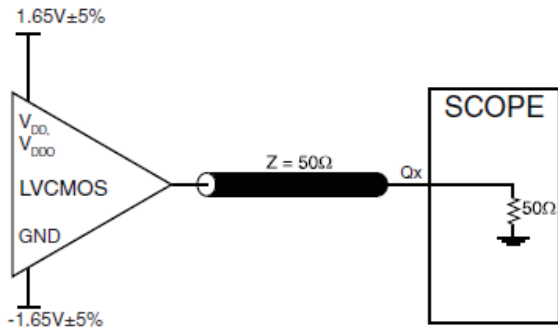
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages, same temperature, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

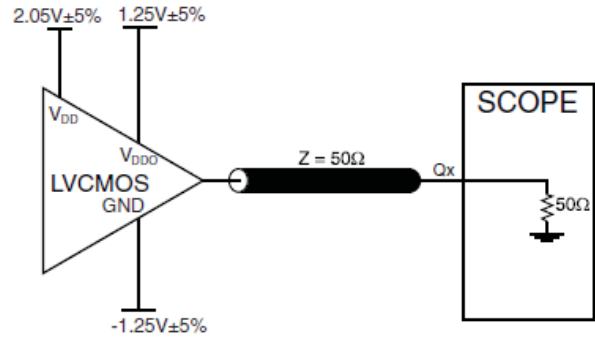
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6: Defined as skew between outputs on different devices, across temperature and voltage ranges, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

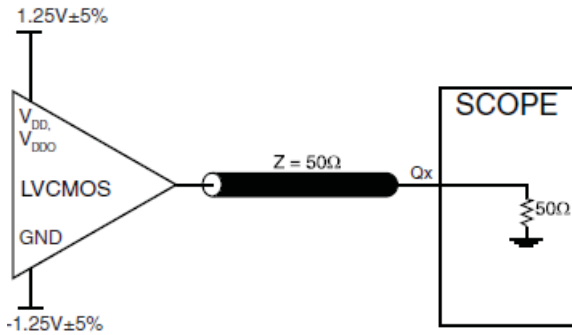
PARAMETER MEASUREMENT INFORMATION



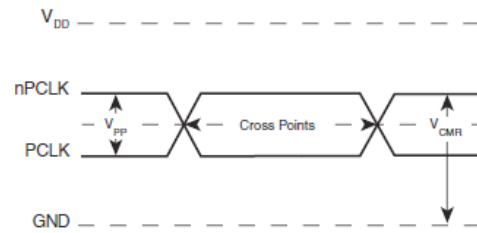
3.3V OUTPUT LOAD AC TEST CIRCUIT



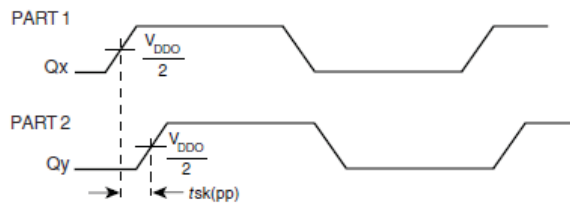
3.3V/2.5V OUTPUT LOAD AC TEST CIRCUIT



2.5V OUTPUT LOAD AC TEST CIRCUIT



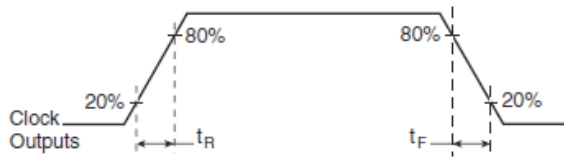
DIFFERENTIAL INPUT LEVEL



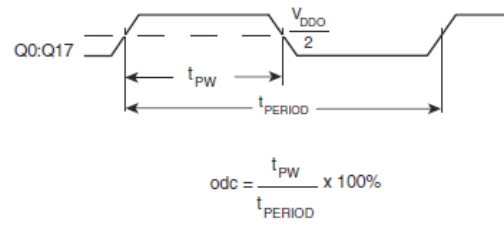
PART-TO-PART SKEW



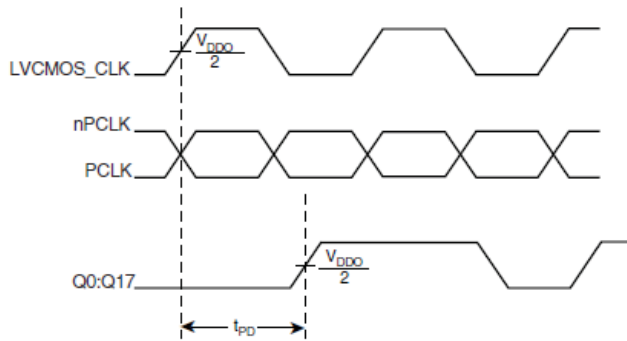
OUTPUT SKEW



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



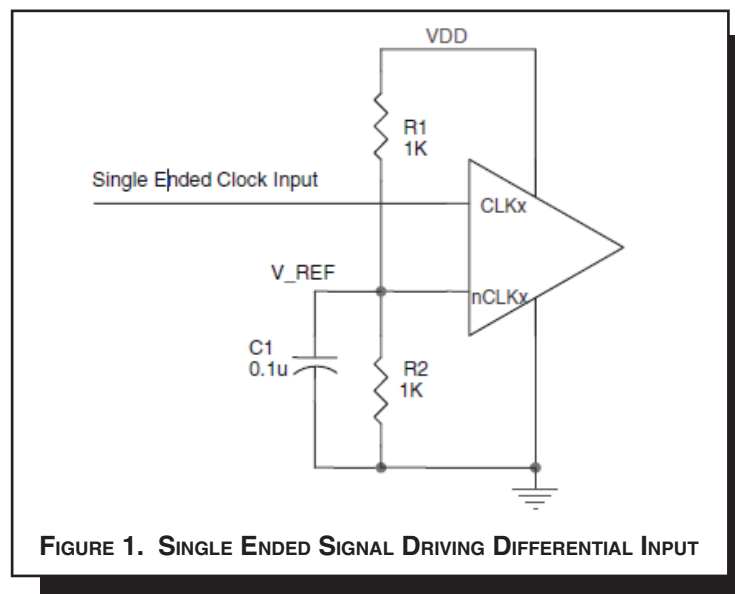
PROPAGATION DELAY

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_{REF}

in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.



RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK INPUT:

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from the CLK input to ground.

PCLK/nPCLK INPUT:

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from PCLK to ground.

LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

OUTPUTS:

LVC MOS OUTPUT:

All unused LVC MOS output can be left floating. We recommend that there is no trace attached.

LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The input interfaces

suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

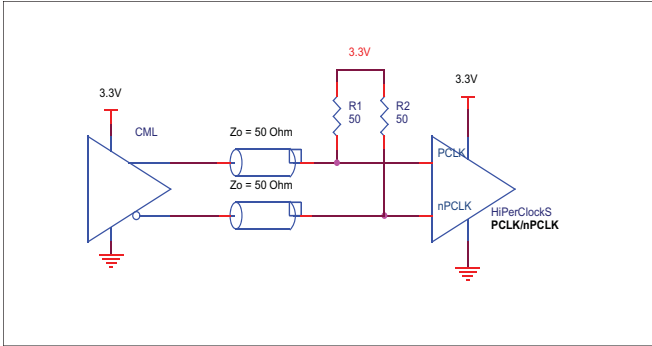


FIGURE 2A. PCLK/nPCLK INPUT DRIVEN BY AN OPEN COLLECTOR CML DRIVER

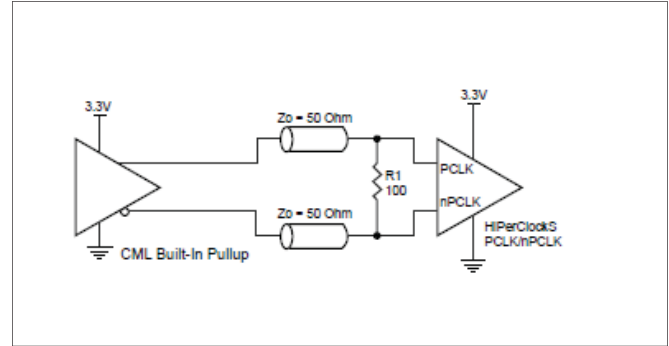


FIGURE 2B. PCLK/nPCLK INPUT DRIVEN BY A BUILT-IN PULLUP CML DRIVER

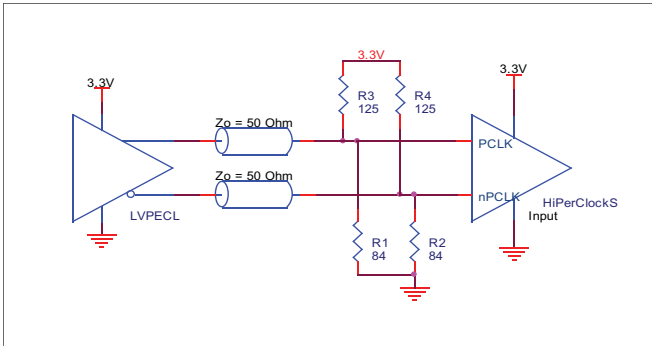


FIGURE 2C. PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

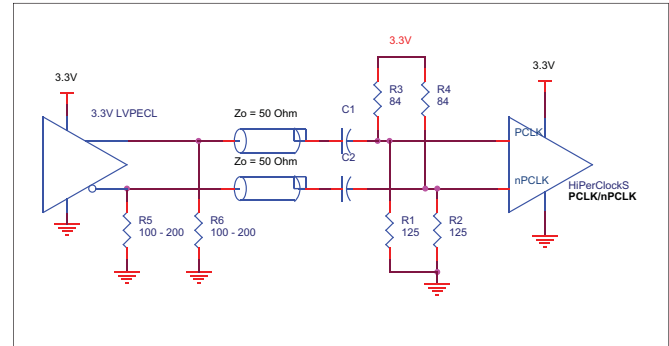


FIGURE 2D. PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE

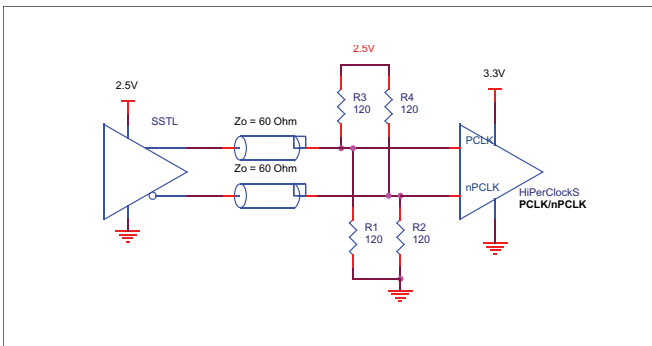


FIGURE 2E. PCLK/nPCLK INPUT DRIVEN BY AN SSTL DRIVER

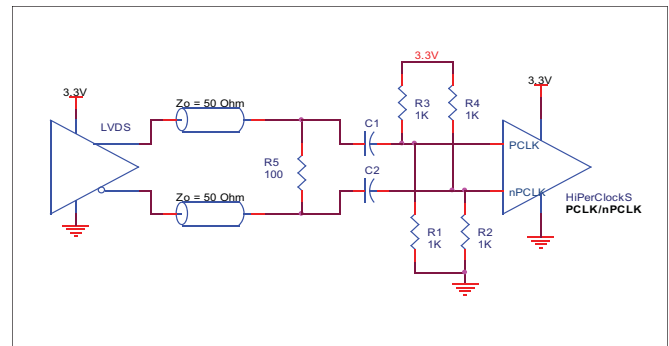


FIGURE 2F. PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD LQFP

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|----------|----------|----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 47.9°C/W | 42.1°C/W | 39.4°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS83940-01 is: 819

PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP

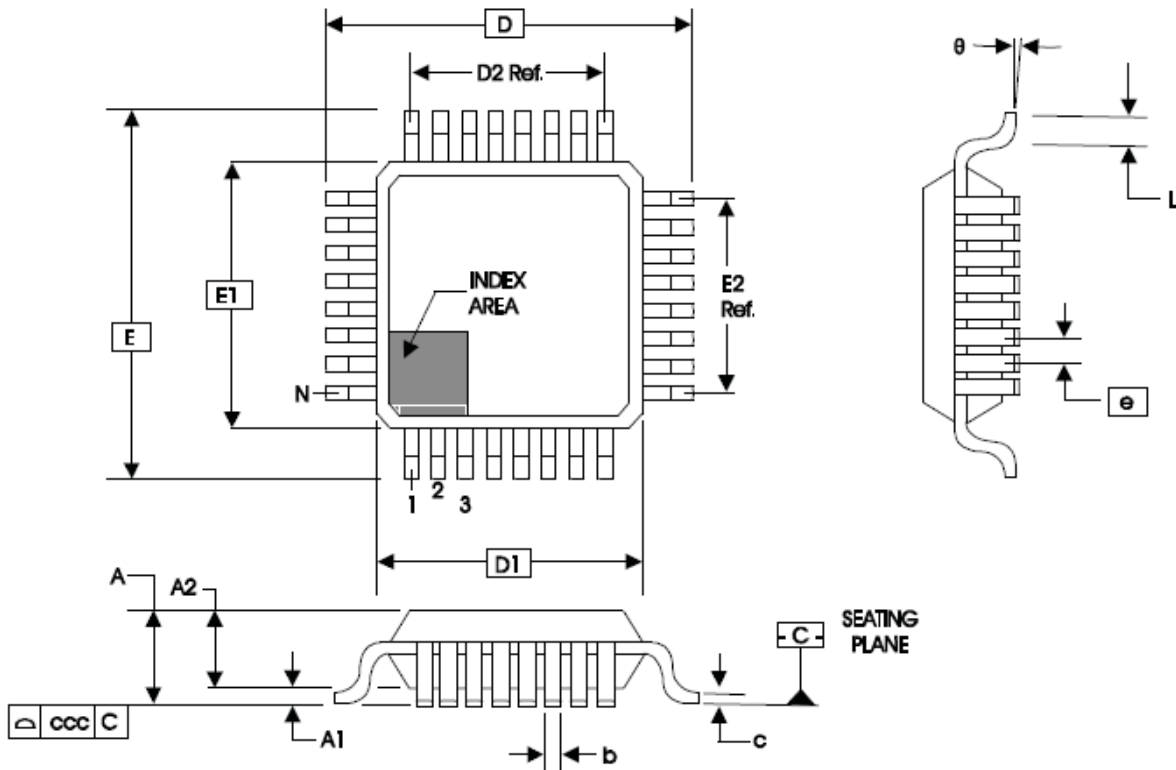


TABLE 7. PACKAGE DIMENSIONS

| JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS | | | |
|--|------------|---------|---------|
| SYMBOL | BBA | | |
| | MINIMUM | NOMINAL | MAXIMUM |
| N | 32 | | |
| A | -- | -- | 1.60 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.30 | 0.37 | 0.45 |
| c | 0.09 | -- | 0.20 |
| D | 9.00 BASIC | | |
| D1 | 7.00 BASIC | | |
| D2 | 5.60 Ref. | | |
| E | 9.00 BASIC | | |
| E1 | 7.00 BASIC | | |
| E2 | 5.60 Ref. | | |
| e | 0.80 BASIC | | |
| L | 0.45 | 0.60 | 0.75 |
| theta | 0° | -- | 7° |
| ccc | -- | -- | 0.10 |

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|--------------|--------------------------|--------------------|-------------|
| 83940DY-01LF | ICS83940D01L | 32 Lead "Lead-Free" LQFP | tray | 0°C to 70°C |
| 83940DY-01LFT | ICS83940D01L | 32 Lead "Lead-Free" LQFP | reel | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

| REVISION HISTORY SHEET | | | | |
|------------------------|-------|------|--|----------|
| Rev | Table | Page | Description of Change | Date |
| A | T8 | 1 | Added Lead-Free bullet. | 11/18/05 |
| | | 9 | Added <i>Recommendations for Unused Input and Output Pins</i> . | |
| | | 10 | Updated <i>LVPECL Clock Input Interface</i> section. | |
| | | 13 | Added Lead-Free part number, marking and note. | |
| A | T8 | 13 | Updated datasheet's header/footer with IDT from ICS. | 8/4/10 |
| | | 15 | Removed ICS prefix from Part/Order Number column. Added Contact Page. | |
| A | T | 13 | Removed Leaded devices Updated Datasheet format | 11/4/14 |
| | | | | |

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