SHARC® Processor

ADSP-21371

SUMMARY

High performance 32-bit/40-bit floating point processor optimized for high performance audio processing

Single-instruction, multiple-data (SIMD) computational architecture

On-chip memory—1M bit of on-chip SRAM and a dedicated 4M bit of on-chip mask-programmable ROM

Code compatible with all other members of the SHARC family

The ADSP-21371 is available with a 266 MHz core instruction rate with unique audiocentric peripherals such as the digital applications interface, serial ports, precision clock generators, and more. For complete ordering information, see Ordering Guide on Page 48.

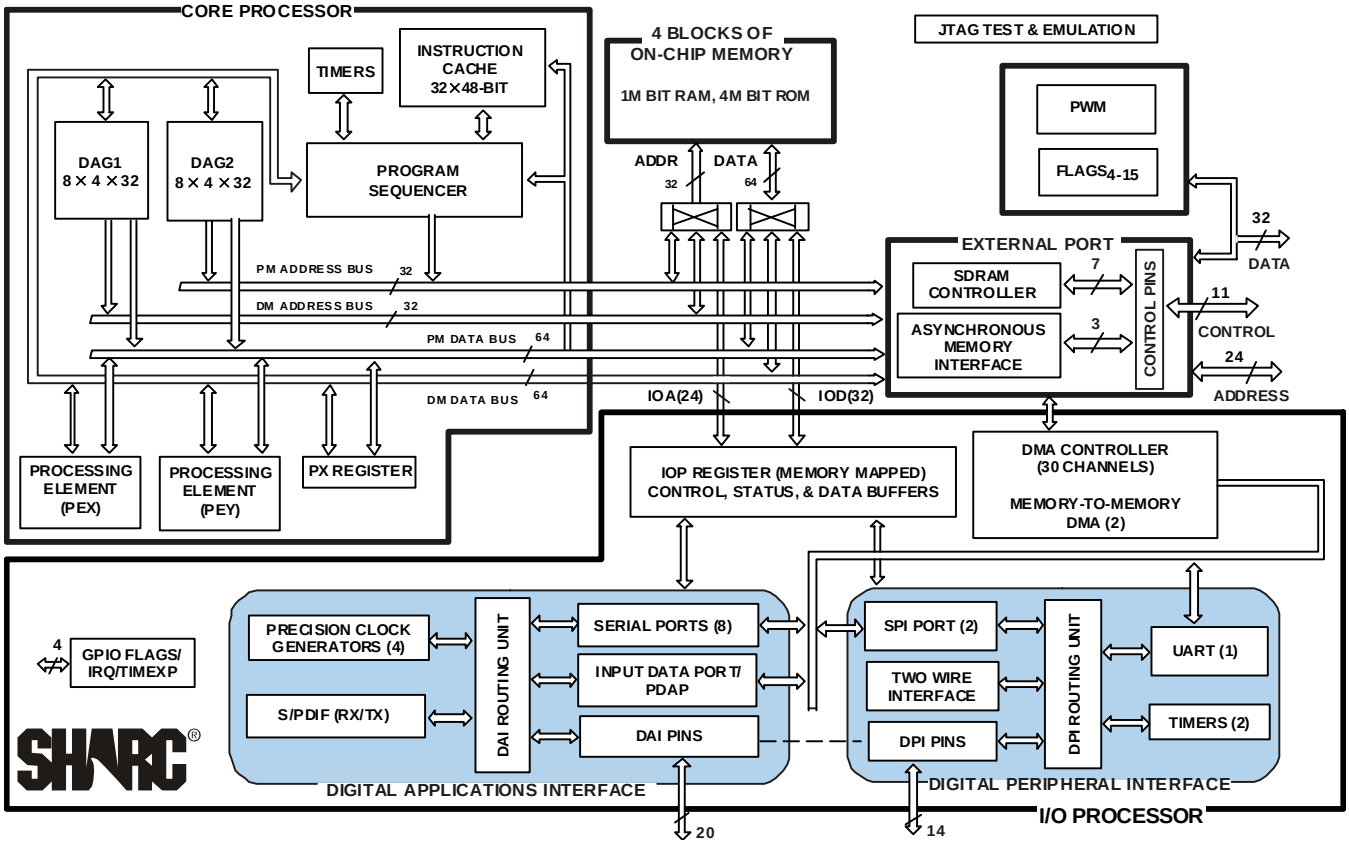


Figure 1. Functional Block Diagram

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Rev. 0

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KEY FEATURES—PROCESSOR CORE

- At 266 MHz (3.75 ns) core instruction rate, the ADSP-21371 performs 1.596 GFLOPs/533 MMACs
- 1M bit on-chip, SRAM for simultaneous access by the core processor and DMA
- 4M bit on-chip, mask-programmable ROM
- Dual data address generators (DAGs) with modulo and bit-reverse addressing
- Zero-overhead looping with single-cycle loop setup, providing efficient program sequencing
- Single instruction multiple data (SIMD) architecture provides:
  - Two computational processing elements
  - Concurrent execution
  - Code compatibility with other SHARC family members at the assembly level
  - Parallelism in buses and computational units allows:
    - Single cycle executions (with or without SIMD) of a multiply operation, an ALU operation, a dual memory read or write, and an instruction fetch
- Transfers between memory and core at a sustained 4.25G bytes/second bandwidth at 266 MHz core instruction rate

INPUT/OUTPUT FEATURES

- DMA controller supports:
  - 32 DMA channels for transfers between ADSP-21371 internal memory and a variety of peripherals
  - 32-bit DMA transfers at peripheral clock speed, in parallel with full-speed processor execution
- 32-bit wide external port provides glueless connection to both synchronous (SDRAM) and asynchronous memory devices
  - Programmable wait state options: 2 to 31 SDCLK cycles
  - Delay-line DMA engine maintains circular buffers in external memory with tap/offset based reads
  - SDRAM accesses at 133 MHz and asynchronous accesses at 44.4 MHz
  - 4 memory select lines allows multiple external memory devices
- Digital audio interface (DAI) includes eight serial ports, four precision clock generators, an input data port, an S/PDIF transceiver, and a signal routing unit
- Digital peripheral interface (DPI) includes, two timers, one UART, and two SPI ports, and a 2-wire interface port
  - Outputs of PCG's A and B can be routed through DAI pins
  - Outputs of PCG's C and D can be driven on to DAI as well as DPI pins
- Eight dual data line serial ports that operate at up to 50 Mbps on each data line — each has a clock, frame sync, and two data lines that can be configured as either a receiver or transmitter pair
- TDM support for telecommunications interfaces including 128 TDM channel support for newer telephony interfaces such as H.100/H.110
- Up to 16 TDM stream support, each with 128 channels per frame
- Companding selection on a per channel basis in TDM mode
- Input data port, configurable as eight channels of serial data or seven channels of serial data and up to a 20-bit wide parallel data channel
- Signal routing unit provides configurable and flexible connections between the various peripherals and the DAI/DPI components
- 2 muxed flag/$\overline{\text{IRQ}}$ lines
- 1 muxed flag/$\overline{\text{IRQ}}$ /$\overline{\text{MS}}$ pin
- 1 muxed flag/Timer expired line /$\overline{\text{MS}}$ pin
- S/PDIF-compatible digital audio receiver/transmitter supports EIAJ CP-340 (CP-1201), IEC-958, AES/EBU standards
  - Left-justified, I^2S or right-justified serial data input with 16-, 18-, 20- or 24-bit word widths (transmitter)
- Pulse-width modulation provides:
  - 16 PWM outputs configured as four groups of four outputs supports center-aligned or edge-aligned PWM waveforms
- ROM based security features include:
  - JTAG access to memory permitted with a 64-bit key
  - Protected memory regions that can be assigned to limit access under program control to sensitive code
- PLL has a wide variety of software and hardware multiplier/divider ratios
- Newly introduced "Running Reset" feature that allows a reset of the processor core and peripherals, but without resetting the PLL and SDRAM controller, or performing a boot
  - Dual voltage: 3.3 V I/O, 1.2 V core
- Available in 208-lead MQFP package (see Ordering Guide on Page 48)

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REVISION HISTORY

6/07—Revision PrA to Rev. 0

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GENERAL DESCRIPTION

The ADSP-21371 SHARC processor is a member of the SIMD SHARC family of DSPs that feature Analog Devices' Super Harvard Architecture. The ADSP-21371 is source code compatible with the ADSP-2126x, ADSP-2136x, and ADSP-2116x DSPs as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. The ADSP-21371 is a 32-bit/40-bit floating point processors optimized for high performance automotive audio applications with its large on-chip SRAM and mask-programmable ROM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital applications interface (DAI).

As shown in the functional block diagram on Page 1, the ADSP-21371 uses two computational units to deliver a significant performance increase over the previous SHARC processors on a range of DSP algorithms. Fabricated in a state-of-the-art, high speed, CMOS process, the ADSP-21371 processor achieves an instruction cycle time of 3.75 ns at 266 MHz. With its SIMD computational hardware, the ADSP-21371 can perform 1.596 GFLOPS running at 266 MHz.

Table 1 shows performance benchmarks for the ADSP-21371.

Table 1. ADSP-21371 Benchmarks (at 266 MHz)

Benchmark Algorithm	Speed (at 266 MHz)
1024 Point Complex FFT (Radix 4, With Reversal)	34.5 µs
FIR Filter (per Tap)[1]	1.88 ns
IIR Filter (per Biquad)[1]	7.5 ns
Matrix Multiply (Pipelined)	
[3 × 3] × [3 × 1]	16.91 ns
[4 × 4] × [4 × 1]	30.07 ns
Divide (y/x)	13.1 ns
Inverse Square Root	20.4 ns

[1] Assumes two files in multichannel SIMD mode

The ADSP-21371 continues SHARC's industry-leading standards of integration for DSPs, combining a high performance 32-bit DSP core with integrated, on-chip system features.

The block diagram of the ADSP-21371 on Page 1 illustrates the following architectural features:

- Two processing elements, each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core at every core processor cycle
- Two programmable interval timers with external event counter capabilities
- On-chip SRAM (1M bit)
- On-chip mask-programmable ROM (4M bit)
- JTAG test access port

The block diagram of the ADSP-21371 on Page 1 also illustrates the following architectural features:

- DMA controller
- Digital applications interface that includes four precision clock generators (PCG), an S/PDIF-compatible digital audio receiver/transmitter, an input data port (IDP), eight serial ports, eight serial interfaces, a 20-bit parallel input port (PDAP), and a flexible signal routing unit (DAI SRU).
- Digital peripheral interface that includes two timers, one UART, two serial peripheral interfaces (SPI), a 2-wire interface (TWI), and a flexible signal routing unit (DPI SRU).

ADSP-21371 FAMILY CORE ARCHITECTURE

The ADSP-21371 is code compatible at the assembly level with the ADSP-21375, ADSP-2136x, ADSP-2126x, ADSP-21160, and ADSP-21161, and with the first generation ADSP-2106x SHARC processors. The ADSP-21371 shares architectural features with the ADSP-2126x, ADSP-2136x, and ADSP-2116x SIMD SHARC processors, as detailed in the following sections.

SIMD Computational Engine

The ADSP-21371 contains two computational processing elements that operate as a single-instruction, multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing ele-

ments. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

Data Register File

A general-purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the ADSP-2136x enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0-R15 and in PEY as S0-S15.

Single-Cycle Fetch of Instruction and Four Operands

The ADSP-21371 features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 1 on page 1). With the ADSP-21371's separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-21371 includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators With Zero-Overhead Hardware Circular Buffer Support

The ADSP-21371's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the ADSP-21371 contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21371 can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

ADSP-21371 MEMORY

The ADSP-21371 adds the following architectural features to the SIMD SHARC family core.

On-Chip Memory

The ADSP-21371 contains 1 megabit of internal RAM and four megabits of internal mask-programmable ROM. Each block can be configured for different combinations of code and data storage (see Table 2 on Page 6). Each memory block supports single-cycle, independent accesses by the core processor and I/O processor. The ADSP-21371 memory architecture, in combination with its separate on-chip buses, allow two data transfers from the core and one from the I/O processor, in a single cycle.

The ADSP-21371's SRAM can be configured as a maximum of 32k words of 32-bit data, 64k words of 16-bit data, 21.3k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 1 megabit. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

EXTERNAL MEMORY

The external port on the ADSP-21371 SHARC provides a high performance, glueless interface to a wide variety of industry-standard memory devices. The 32-bit wide bus may be used to interface to synchronous and/or asynchronous memory devices through the use of its separate internal memory controllers: the first is an SDRAM controller for connection of industry-standard synchronous DRAM devices and DIMMs (dual inline memory module), while the second is an asynchronous memory controller intended to interface to a variety of memory devices. Four memory select pins enable up to four separate devices to coexist, supporting any desired combination of synchronous and asynchronous device types. Non SDRAM external memory address space is shown in Table 3.

External Memory Execution

In the ADSP-21371, the program sequencer can execute code directly from external memory bank 0 (SRAM, SDRAM). This allows a reduction in internal memory size, thereby reducing the die area. With external execution, programs run at slower speeds since 48-bit instructions are fetched in parts from a 32-bit external bus coupled with the inherent latency of fetching instructions from SDRAM. Fetching instructions from external memory generally takes 1.5 peripheral clock cycles per instruction.

Table 2. ADSP-21371 Internal Memory Space

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 bits)	**Extended Precision Normal or Instruction Word (48 bits)**	**Normal Word (32 bits)**	**Short Word (16 bits)**
BLOCK 0 ROM 0x0004 0000–0x0004 7FFF	BLOCK 0 ROM 0x0008 0000–0x0008 AAA9	BLOCK 0 ROM 0x0008 0000–0x0008 FFFF	BLOCK 0 ROM 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 BFFF	Reserved 0x0008 AAAA–0x0008 FFFF	Reserved 0x0009 0000–0x0009 7FFF	Reserved 0x0012 0000–0x0012 FFFF
BLOCK 0 RAM 0x0004 C000–0x0004 CFFF	BLOCK 0 RAM 0x0009 0000–0x0009 1554	BLOCK 0 RAM 0x0009 8000–0x0009 9FFF	BLOCK 0 RAM 0x0013 0000–0x0013 3FFF
Reserved 0x0004 D000–0x0004 FFFF	Reserved 0x0009 1555–0x0009 FFFF	Reserved 0x0009 A000–0x0009 FFFF	Reserved 0x0013 4000–0x0013 FFFF
BLOCK 1 ROM 0x0005 0000–0x0005 7FFF	BLOCK 1 ROM 0x000A 0000–0x000A AAA9	BLOCK 1 ROM 0x000A 0000–0x000A FFFF	BLOCK 1 ROM 0x0014 0000–0x0015 FFFF
Reserved 0x0005 8000–0x0005 BFFF	Reserved 0x000A AAAA–0x000A FFFF	Reserved 0x000B 0000–0x000B 7FFF	Reserved 0x0016 0000–0x0016 FFFF
BLOCK 1 RAM 0x0005 C000–0x0005 CFFF	BLOCK 1 RAM 0x000B 0000–0x000B 1554	BLOCK 1 RAM 0x000B 8000–0x000B 9FFF	BLOCK 1 RAM 0x0017 0000–0x0017 3FFF
Reserved 0x0005 D000–0x0005 FFFF	Reserved 0x000B 1555–0X000B FFFF	Reserved 0x000B A000–0x000B FFFF	Reserved 0x0017 4000–0x0017 FFFF
BLOCK 2 RAM 0x0006 0000–0x0006 0FFF	BLOCK 2 RAM 0x000C 0000–0x000C 1554	BLOCK 2 RAM 0X000C 0000–0X000C 1FFF	BLOCK 2 RAM 0x0018 0000–0x001B 3FFF
Reserved 0x0006 1000–0x0006 FFFF	Reserved 0x000C 1555–0x000D FFFF	Reserved 0x000C 2000–0x000D FFFF	Reserved 0x0018 4000–0x001B FFFF
BLOCK 3 RAM 0x0007 0000–0x0007 0FFF	BLOCK 3 RAM 0x000E 0000–0x000E 1554	BLOCK 3 RAM 0x000E 0000–0x000E 1FFF	BLOCK 3 RAM 0x001C 0000–0x001C 3FFF
Reserved 0x0007 1000–0x0007 FFFF	Reserved 0x000E 1555–0x000F FFFF	Reserved 0x000E 2000–0x000F FFFF	Reserved 0x001C 4000–0x001F FFFF

SDRAM Controller

The SDRAM controller provides an interface to up to four separate banks of industry-standard SDRAM devices or DIMMs. Fully compliant with the SDRAM standard, each bank can has its own memory select line ($\overline{MS0}$–$\overline{MS3}$), and can be configured to contain between 16M bytes and 128M bytes of memory. SDRAM external memory address space is shown in Table 4.

The controller maintains all of the banks as a contiguous address space so that the processor sees this as a single address space, even if different size devices are used in the different banks.

A set of programmable timing parameters is available to configure the SDRAM banks to support slower memory devices. The memory banks can be configured as 16 bits wide or as 32 bits wide.

The SDRAM controller address, data, clock, and command pins can drive loads up to 30 pF. For larger memory systems, the SDRAM controller external buffer timing should be selected and external buffering should be provided so that the load on the SDRAM controller pins does not exceed 30 pF.

Table 3. External Memory for Non SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	14M	0x0020 0000 – 0x00FF FFFF
Bank 1	16M	0x0400 0000 – 0x04FF FFFF
Bank 2	16M	0x0800 0000 – 0x08FF FFFF
Bank 3	16M	0x0C00 0000 – 0x0CFF FFFF

Table 4. External Memory for SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	62M	0x0020 0000 – 0x03FF FFFF
Bank 1	64M	0x0400 0000 – 0x07FF FFFF
Bank 2	64M	0x0800 0000 – 0x0BFF FFFF
Bank 3	64M	0x0C00 0000 – 0x0FFF FFFF

Note that the external memory bank addresses shown are for normal word accesses. If 48-bit instructions are placed in any such bank (with two instructions packed into three 32-bit locations), then care must be taken to map data buffers in the same bank. For example, if 2k instructions are placed starting at the bank 0 base address (0x0020 0000), then the data buffers can be placed starting at an address that is offset by 3k words (0x0020 0C00).

Asynchronous Controller

The asynchronous memory controller provides a configurable interface for up to four separate banks of memory or I/O devices. Each bank can be independently programmed with different timing parameters, enabling connection to a wide variety of memory devices including SRAM, ROM, flash, and EPROM, as well as I/O devices that interface with standard memory control lines. Bank 0 occupies a 14.7M word window and banks 1, 2, and 3 occupy a 16M word window in the processor's address space but, if not fully populated, these windows are not made contiguous by the memory controller logic. The banks can also be configured as 8-bit or 16-bit wide buses for ease of interfacing to a range of memories and I/O devices tailored either to high performance or to low cost and power.

The asynchronous memory controller is capable of a maximum throughput of 176 Mbps using a 44 MHz external bus speed. Other features include 8 to 32-bit and 16 to 32-bit packing and unpacking, booting from bank select 1, and support for delay line DMA.

ADSP-21371 INPUT/OUTPUT FEATURES

The ADSP-21371 I/O processor provides 32 channels of DMA, as well as an extensive set of peripherals. These include a 20 lead digital applications interface, which controls:

- Eight serial ports
- S/PDIF receiver/transmitter
- Four precision clock generators
- Input data port/parallel data acquisition port

The ADSP-21371 processor also contains a 14 lead digital peripheral interface, which controls:

- Two general-purpose timers
- Two serial peripheral interfaces
- One universal asynchronous receiver/transmitter (UART)
- An $I^2C^®$-compatible 2-wire interface

DMA Controller

The ADSP-21371's on-chip DMA controller allows data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the ADSP-21371's internal memory and its serial ports, the SPI-compatible (serial peripheral interface) ports, the IDP (input data port), the parallel data acquisition port (PDAP) or the UART. Thirty-two channels of DMA are available on the ADSP-21371, 16 via the serial ports, eight via the input data port, two for the UART, two for the SPI interface, two for the external port, and two for memory-to-memory transfers. Programs can be downloaded to the ADSP-21371 using DMA transfers. Other DMA features include interrupt generation upon completion of DMA transfers, and DMA chaining for automatic linked DMA transfers.

Delay Line DMA

The ADSP-21371 processor provides delay line DMA functionality. This allows processor reads and writes to external delay line buffers (and hence to external memory) with limited core interaction.

Digital Applications Interface (DAI)

The digital applications interface (DAI) provides the ability to connect various peripherals to any of the DSP DAI pins (DAI_P20–1).

Programs make these connections using the signal routing unit (SRU), shown in Figure 1.

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI also includes eight serial ports, four precision clock generators (PCG), and an input data port (IDP). The IDP provides an additional input path to the ADSP-21371 core, configurable as either eight channels of I²S serial data, or a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the ADSP-21371's serial ports.

Serial Ports

The ADSP-21371 features eight synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports are enabled via eight programmable pins and simultaneous receive or transmit pins that support up to 16 transmit or 16 receive channels of audio data when all four SPORTs are enabled, or four full duplex TDM streams of 128 channels per frame.

The serial ports operate at a maximum data rate of 50 Mbps. Serial port data can be automatically transferred to and from on-chip memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard DSP serial mode
- Multichannel (TDM) mode with support for packed I²S mode
- I²S mode
- Packed I²S mode
- Left-justified sample pair mode

Left-justified sample pair mode is a mode where in each frame sync cycle two samples of data are transmitted/received—one sample on the high segment of the frame sync, the other on the low segment of the frame sync. Programs have control over various attributes of this mode.

Each of the serial ports supports the left-justified sample pair and I²S protocols (I²S is an industry-standard interface commonly used by audio codecs, ADCs, and DACs such as the Analog Devices AD183x family), with two data pins, allowing four left-justified sample pair or I²S channels (using two stereo devices) per serial port, with a maximum of up to 32 I²S channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For the left-justified sample pair and I²S modes, data-word lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding selection on a per channel basis. Serial port clocks and frame syncs can be internally or externally generated.

The serial ports also contain frame sync error detection logic where the serial ports detect frame syncs that arrive early (for example frame syncs that arrive while the transmission/reception of the previous word is occurring). All the serial ports also share one dedicated error interrupt.

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the receiver/transmitter can be formatted as left justified, I²S or right justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources such as the SPORTs, external pins, the precision clock generators (PCGs), and are controlled by the SRU control registers.

Digital Peripheral Interface (DPI)

The digital peripheral interface provides connections to two serial peripheral interface ports (SPI), one universal asynchronous receiver-transmitter (UART), 12 flags, a 2-wire interface (TWI), and two general-purpose timers.

Serial Peripheral (Compatible) Interface

The ADSP-21371 SHARC processor contains two serial peripheral interface ports (SPIs). The SPI is an industry-standard synchronous serial link, enabling the ADSP-21371 SPI-compatible port to communicate with other SPI compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The ADSP-21371 SPI-compatible peripheral implementation also features programmable baud rate and clock phase and polarities. The ADSP-21371 SPI-compatible port uses open drain drivers to support a multimaster configuration and to avoid data contention.

UART Port

The ADSP-21371 processor provides a full-duplex Universal Asynchronous Receiver/Transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART also has multiprocessor communication capability using 9-bit address detection. This allows it to be used in multidrop networks through the RS-485 data interface standard. The UART port also includes support for 5 to 8 data bits, 1 or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{PCLK}/ 1,048,576) to (f_{PCLK}/16) bits per second.
- Supporting data formats from 7 to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

In conjunction with the general-purpose timer functions, autobaud detection is supported.

Timers

The ADSP-21371 has a total of three timers: a core timer that can generate periodic software interrupts and two general purpose timers that can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watchdog mode

The core timer can be configured to use FLAG3 as a timer expired signal, and each general-purpose timer has one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables both general-purpose timers independently.

2-Wire Interface Port (TWI)

The TWI is a bidirectional 2-wire, serial bus used to move 8-bit data while maintaining compliance with the I^2C bus protocol. The TWI master incorporates the following features:

- 7-bit addressing
- Simultaneous master and slave operation on multiple device systems with support for multi master data arbitration
- Digital filtering and timed event processing
- 100 kbps and 400 kbps data rates
- Low interrupt rate

Pulse-Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs each. Therefore, this module generates 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single update mode or double update mode. In single update mode the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the mid-point of the PWM period. In double update mode, a second updating of the PWM registers is implemented at the mid-point of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in three-phase PWM inverters.

ROM Based Security

The ADSP-21371 has a ROM security feature that provides hardware support for securing user software code by preventing unauthorized reading from the internal code when enabled. When using this feature, the processor does not boot-load any external code, executing exclusively from internal SRAM/ROM. Additionally, the processor is not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through the JTAG or Test Access Port will be assigned to each customer. The device will ignore a wrong key. Emulation features and external boot modes are only available after the correct key is scanned.

SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

Program Booting

The internal memory of the ADSP-21371 boots at system power-up from an 8-bit EPROM via the external port, an SPI master, or an SPI slave. Booting is determined by the boot configuration (BOOTCFG1–0) pins (see Table 7 on Page 14). Selection of the boot source is controlled via the SPI as either a master or slave device, or it can immediately begin executing from ROM.

The newly introduced "Running Reset" feature allows a user to perform a reset of the processor core and peripherals, but without resetting the PLL and SDRAM controller, or performing a Boot. The functionality of the CLKOUT/$\overline{\text{RESETOUT}}$/$\overline{\text{RUNRSTIN}}$ pin has now been extended to also act as the input for initiating a Running Reset. For more information, see the *ADSP-2136x SHARC Processor Hardware Reference* for the ADSP-21367/8/9 Processors.

Power Supplies

The ADSP-21371 has separate power supply connections for the internal (V_{DDINT}), and external (V_{DDEXT}) power supplies. The internal supplies must meet the 1.2 V requirement. The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same power supply.

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-21371 processor to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate "Emulator Hardware User's Guide".

DEVELOPMENT TOOLS

The ADSP-21371 is supported with a complete set of CROSSCORE® software and hardware development tools, including Analog Devices emulators and VisualDSP++® development environment. The same emulator hardware that supports other SHARC processors also fully emulates the ADSP-21371.

The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy to use assembler (which is based on an algebraic syntax), an archiver (librarian/library builder), a linker, a loader, a cycle-accurate instruction-level simulator, a C/C++ compiler, and a C/C++ runtime library that includes DSP and mathematical functions. A key point for these tools is C/C++ code efficiency. The compiler has been developed for efficient translation of C/C++ code to DSP assembly. The SHARC has architectural features that improve the efficiency of compiled C/C++ code.

The VisualDSP++ debugger has a number of important features. Data visualization is enhanced by a plotting package that offers a significant level of flexibility. This graphical representation of user data enables the programmer to quickly determine the performance of an algorithm. As algorithms grow in complexity, this capability can have increasing significance on the designer's development schedule, increasing productivity. Statistical profiling enables the programmer to nonintrusively poll the processor as it is running the program. This feature, unique to VisualDSP++, enables the software developer to passively gather important code execution metrics without interrupting the real-time characteristics of the program. Essentially, the developer can identify bottlenecks in software quickly and efficiently. By using the profiler, the programmer can focus on those areas in the program that impact performance and take corrective action.

Debugging both C/C++ and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C/C++ and assembly code (interleaved source and object information)
- Insert breakpoints
- Set conditional breakpoints on registers, memory, and stacks
- Perform linear or statistical profiling of program execution
- Fill, dump, and graphically plot the contents of memory
- Perform source level debugging
- Create custom debugger windows

The VisualDSP++ IDDE lets programmers define and manage DSP software development. Its dialog boxes and property pages let programmers configure and manage all of the SHARC development tools, including the color syntax highlighting in the VisualDSP++ editor. This capability permits programmers to:

- Control how the development tools process inputs and generate outputs
- Maintain a one-to-one correspondence with the tool's command line switches

The VisualDSP++ Kernel (VDK) incorporates scheduling and resource management tailored specifically to address the memory and timing constraints of DSP programming. These capabilities enable engineers to develop code more effectively, eliminating the need to start from the very beginning, when developing new application code. The VDK features include threads, critical and unscheduled regions, semaphores, events, and device flags. The VDK also supports priority-based, preemptive, cooperative, and time-sliced scheduling approaches. In addition, the VDK was designed to be scalable. If the application does not use a specific feature, the support code for that feature is excluded from the target system.

Because the VDK is a library, a developer can decide whether to use it or not. The VDK is integrated into the VisualDSP++ development environment, but can also be used via standard command line tools. When the VDK is used, the development environment assists the developer with many error-prone tasks and assists in managing system resources, automating the generation of various VDK based objects, and visualizing the system state, when debugging an application that uses the VDK.

VisualDSP++ Component Software Engineering (VCSE) is Analog Devices' technology for creating, using, and reusing software components (independent modules of substantial functionality) to quickly and reliably assemble software applications. Download components from the Web and drop them into the application. Publish component archives from within VisualDSP++. VCSE supports component implementation in C/C++ or assembly language.

Use the Expert Linker to visually manipulate the placement of code and data on the embedded system. View memory utilization in a color-coded graphical form, easily move code and data to different areas of the processor or external memory with the drag of the mouse, examine run time stack and heap usage. The Expert Linker is fully compatible with the existing Linker Definition File (LDF), allowing the developer to move between the graphical and textual environments.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the SHARC processor family. Hardware tools include SHARC processor PC plug-in cards. Third party software tools include DSP libraries, real-time operating systems, and block diagram design tools.

Designing an Emulator-Compatible DSP Board (Target)

The Analog Devices family of emulators are tools that every DSP developer needs to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG Test Access Port (TAP) on each JTAG DSP. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing. The emulator uses the TAP to access the internal features of the processor, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The processor must be halted to send data and commands, but once an operation has been completed by the emulator, the DSP system is set running at full speed with no impact on system timing.

To use these emulators, the target board must include a header that connects the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

Evaluation Kit

Analog Devices offers a range of EZ-KIT Lite® evaluation platforms to use as a cost effective method to learn more about developing or prototyping applications with Analog Devices processors, platforms, and software tools. Each EZ-KIT Lite includes an evaluation board along with an evaluation suite of the VisualDSP++® development and debugging environment with the C/C++ compiler, assembler, and linker. Also included are sample application programs, power supply, and a USB cable. All evaluation versions of the software tools are limited for use only with the EZ-KIT Lite product.

The USB controller on the EZ-KIT Lite board connects the board to the USB port of the user's PC, enabling the VisualDSP++ evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also allows in-circuit programming of the on-board Flash device to store user-specific boot code, enabling the board to run as a standalone unit without being connected to the PC.

With a full version of VisualDSP++ installed (sold separately), engineers can develop software for the EZ-KIT Lite or any custom defined system. Connecting one of Analog Devices JTAG emulators to the EZ-KIT Lite board enables high speed, nonintrusive emulation.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21371 architecture and functionality. For detailed information on the ADSP-2137x family core architecture and instruction set, refer to the *ADSP-2136x SHARC Processor Programming Reference*.

PIN FUNCTION DESCRIPTIONS

The following symbols appear in the Type column of Table 5:
A = asynchronous, I = input, O = output, S = synchronous,
(A/D) = active drive, (O/D) = open drain, and T = three-state,
(pd) = pull-down resistor, (pu) = pull-up resistor.

Table 5. Pin List

Name	Type	State During and After Reset	Description
$ADDR_{23-0}$	O/T (pu)	Pulled high/ driven low	**External Address.** The ADSP-21371 outputs addresses for external memory and peripherals on these pins.
$DATA_{31-0}$	I/O (pu)	Pulled high/ pulled high	**External Data.** The data pins can be multiplexed to support the external memory interface data (I/O), the PDAP (I), FLAGS (I/O) and PWM (O). After reset, all DATA pins are in EMIF mode and FLAG(0-3) pins will be in FLAGS mode (default). When configured in the IDP_PDAP_CTL register, IDP channel 0 scans the $DATA_{31-8}$ pins for parallel input data.
DAI _P_{20-1}	I/O with programmable pu[1]	Pulled high/ pulled high	**Digital Applications Interface Pins**. These pins provide the physical interface to the DAI SRU. The DAI SRU configuration registers define the combination of on-chip audiocentric peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DAI SRU may be routed to any of these pins. The DAI SRU provides the connection from the serial ports, the S/PDIF module, input data ports (2), and the precision clock generators (4), to the DAI_P20–1 pins. Pullups can be disabled via the DAI_PIN_PULLUP register.
DPI _P_{14-1}	I/O with programmable pu[1]	Pulled high/ pulled high	**Digital Peripheral Interface.** These pins provide the physical interface to the DPI SRU. The DPI SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DPI SRU may be routed to any of these pins. The DPI SRU provides the connection from the timers (2), SPIs (2), UART (1), flags (12), and general-purpose I/O (9) to the DPI_P14–1 pins. Pull-ups can be disabled via the DPI_PIN_PULLUP register.
ACK	I (pu)		**Memory Acknowledge.** External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{RD}$	O/T (pu)	Pulled high/ driven high	**External Port Read Enable.** $\overline{RD}$ is asserted whenever the ADSP-21371 reads a word from external memory. $\overline{RD}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{WR}$	O/T (pu)	Pulled high/ driven high	**External Port Write Enable.** $\overline{WR}$ is asserted when the ADSP-21371 writes a word to external memory. $\overline{WR}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{SDRAS}$	O/T (pu)	Pulled high/ driven high	**SDRAM Row Address Strobe.** Connect to SDRAM's RAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{SDCAS}$	O/T (pu)	Pulled high/ driven high	**SDRAM Column Address Select.** Connect to SDRAM's CAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{SDWE}$	O/T (pu)	Pulled high/ driven high	**SDRAM Write Enable.** Connect to SDRAM's WE or W buffer pin.
SDCKE	O/T (pu)	Pulled high/ driven high	**SDRAM Clock Enable.** Connect to SDRAM's CKE pin. Enables and disables the CLK signal. For details, see the data sheet supplied with the SDRAM device.
SDA10	O/T (pu)	Pulled high/ driven low	**SDRAM A10 Pin.** Enables applications to refresh an SDRAM in parallel with a non-SDRAM accesses. This pin replaces the DSP's A10 pin only during SDRAM accesses.
SDCLK	O/T	High-Z/driving	**SDRAM Clock.**
$\overline{MS}_{0-1}$	O/T (pu)	Pulled high/ driven high	**Memory Select Lines 0–1.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. The $\overline{MS}_{3-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{MS}_{3-0}$ lines are inactive; they are active however when a conditional memory access instruction is executed, whether or not the condition is true. The $\overline{MS1}$ pin can be used in EPORT/FLASH boot mode. For more information, see the *ADSP-2136x SHARC Processor Hardware Reference for the ADSP-21367/8/9 Processors.*

Table 5. Pin List (Continued)

Name	Type	State During and After Reset	Description
FLAG[0]/IRQ0	I/O	High-Z/high-Z	**FLAG0/Interrupt Request0.**
FLAG[1]/IRQ1	I/O	High-Z/high-Z	**FLAG1/Interrupt Request1.**
FLAG[2]/IRQ2/ MS2	I/O with programmable pu (for MS mode)	High-Z/high-Z	**FLAG2/Interrupt Request/Memory Select2.**
FLAG[3]/TIMEXP/MS3	I/O with programmable pu (for MS mode)	High-Z/high-Z	**FLAG3/Timer Expired/Memory Select3.**
TDI	I (pu)		**Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a 22.5 kΩ internal pull-up resistor.
TDO	O /T		**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
TMS	I (pu)		**Test Mode Select (JTAG).** Used to control the test state machine. TMS has a 22.5 kΩ internal pull-up resistor.
TCK	I		**Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21371.
TRST	I (pu)		**Test Reset (JTAG).** Resets the test state machine. TRST must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21371. TRST has a 22.5 kΩ internal pull-up resistor.
EMU	O/T (pu)		**Emulation Status.** Must be connected to the ADSP-21371 Analog Devices DSP Tools product line of JTAG emulators target board connector only. EMU has a 22.5 kΩ internal pull-up resistor.
CLK_CFG_{1-0}	I		**Core to CLKIN Ratio Control.** These pins set the start up clock frequency. See Table 8 for a description of the clock configuration modes. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset.
$BOOT_CFG_{1-0}$	I		**Boot Configuration Select.** These pins select the boot mode for the processor. The BOOTCFG pins must be valid before reset is asserted. See Table 7 for a description of the boot modes.
RESET	I		**Processor Reset.** Resets the ADSP-21371 to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The RESET input must be asserted (low) at power-up.
XTAL	O		**Crystal Oscillator Terminal.** Used in conjunction with CLKIN to drive an external crystal.
CLKIN	I		**Local Clock In.** Used in conjunction with XTAL. CLKIN is the ADSP-21371 clock input. It configures the ADSP-21371 to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the ADSP-21371 to use the external clock source such as an external clock oscillator. CLKIN may not be halted, changed, or operated below the specified frequency.
CLKOUT/ RESETOUT/ RUNRSTIN	I/O (pu)		**Clock Out/Reset Out/Running Reset In.** The functionality can be switched between the PLL output clock and reset out by setting Bit 12 of the PMCTREG register. The default is reset out. This pin also has a third function as RUNRSTIN. The functionality of which is enabled by setting bit 0 of the RUNRSTCTL register. For more information, see the *ADSP-2136x SHARC Processor Hardware Reference for the ADSP-21367/8/9 Processors.*

[1] Pull-up can be enabled/disabled, value of pull-up cannot be programmed.

DATA MODES

The upper 32 data pins of the external memory interface are muxed (using bits in the SYSCTL register) to support the external memory interface data (input/output), the PDAP (input only), and the FLAGS (input/output). Table 6 provides the pin settings.

Table 6. Function of Data Pins

DATA PIN MODE	DATA31–16	DATA15–8	DATA7–0
000	EPDATA32–0		
001	FLAGS/PWM15–0[1]	EPDATA15–0	
010	FLAGS/PWM15–0[1]	FLAGS15–8	EPDATA7–0
011	FLAGS/PWM15–0[1]	FLAGS15–0	
100	PDAP (DATA + CTRL)		EPDATA7–0
101	PDAP (DATA + CTRL)		FLAGS7–0
110	Reserved		
111	Three-state all pins		

[1] These signals can be FLAGS or PWM or a mix of both. However, they can be selected only in groups of four. Their function is determined by the control signals FLAGS/PWM_SEL. For more information, see the *ADSP-2136x SHARC Processor Hardware Reference for the ADSP-21367/8/9 Processors*.

BOOT MODES

Table 7. Boot Mode Selection

BOOTCFG1–0	Booting Mode
00	SPI Slave Boot
01	SPI Master Boot
10	EPROM/FLASH Boot

CORE INSTRUCTION RATE TO CLKIN RATIO MODES

For details on processor timing, see Timing Specifications and Figure 3 on Page 17.

Table 8. Core Instruction Rate/ CLKIN Ratio Selection

CLKCFG1–0	Core to CLKIN Ratio
00	6:1
01	32:1
10	16:1

ADSP-21371 SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	Min	Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	1.14	1.26	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	V
V_{IH}[2]	High Level Input Voltage @ V_{DDEXT} = max	2.0	V_{DDEXT} + 0.5	V
V_{IL}[2]	Low Level Input Voltage @ V_{DDEXT} = min	–0.5	+0.8	V
V_{IH_CLKIN}[3]	High Level Input Voltage @ V_{DDEXT} = max	1.74	V_{DDEXT} + 0.5	V
V_{IL_CLKIN}[3]	Low Level Input Voltage @ V_{DDEXT} = min	–0.5	+1.10	V
$T_{JUNCTION}$	Junction Temperature 208-Lead MQFP @ $T_{AMBIENT}$ 0°C to +70°C	0	115	C

[1] Specifications subject to change without notice.
[2] Applies to input and bidirectional pins: AD23–0, DATA31–0, FLAG3–0, DAI_Px, DPI_Px, $\overline{SPIDS}$, BOOTCFGx, CLKCFGx, CLKOUT ($\overline{RUNRSTIN}$), $\overline{RESET}$, TCK, TMS, TDI, $\overline{TRST}$.
[3] Applies to input pin CLKIN.

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	Min	Typical	Max	Unit
V_{OH}[2]	High Level Output Voltage	@ V_{DDEXT} = min, I_{OH} = –1.0 mA[3]	2.4			V
V_{OL}[2]	Low Level Output Voltage	@ V_{DDEXT} = min, I_{OL} = 1.0 mA[3]			0.4	V
I_{IH}[4, 5]	High Level Input Current	@ V_{DDEXT} = max, V_{IN} = V_{DDEXT} max			10	µA
I_{IL}[4]	Low Level Input Current	@ V_{DDEXT} = max, V_{IN} = 0 V			10	µA
I_{ILPU}[5]	Low Level Input Current Pull-up	@ V_{DDEXT} = max, V_{IN} = 0 V			200	µA
I_{OZH}[6, 7]	Three-State Leakage Current	@ V_{DDEXT} = max, V_{IN} = V_{DDEXT} max			10	µA
I_{OZL}[6]	Three-State Leakage Current	@ V_{DDEXT} = max, V_{IN} = 0 V			10	µA
I_{OZLPU}[7]	Three-State Leakage Current Pull-up	@ V_{DDEXT} = max, V_{IN} = 0 V			200	µA
$I_{DD-INTYP}$[8, 9]	Supply Current (Internal)	t_{CCLK} = 3.75 ns, V_{DDINT} = 1.2 V, 25°C		600		mA
C_{IN}[10, 11]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 1.2 V			4.7	pF

[1] Specifications subject to change without notice.
[2] Applies to output and bidirectional pins: ADDR23-0, DATA31-0, $\overline{RD}$, $\overline{WR}$, FLAG3–0, DAI_Px, DPI_Px, $\overline{EMU}$, TDO, CLKOUT, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCKE, SDA10, and SDCLK0.
[3] See Output Drive Currents on Page 44 for typical drive current capabilities.
[4] Applies to input pins: BOOTCFGx, CLKCFGx, TCK, $\overline{RESET}$, CLKIN.
[5] Applies to input pins with 22.5 kΩ internal pull-ups: $\overline{TRST}$, TMS, TDI.
[6] Applies to three-statable pins: FLAG3–0.
[7] Applies to three-statable pins with 22.5 kΩ pull-ups: DAI_Px, DPI_Px, $\overline{EMU}$.
[8] Typical internal current data reflects nominal operating conditions.
[9] See Engineer-to-Engineer Note “Estimating Power Dissipation for ADSP-2137x SHARC Processors” (EE-319) for further information.
[10] Applies to all signal pins.
[11] Guaranteed, but not tested.

PACKAGE INFORMATION

The information presented in Figure 2 provides details about the package branding for the ADSP-21371 processor. For a complete listing of product availability, see Ordering Guide on Page 48.



Figure 2. Typical Package Brand

Table 9. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Part
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

ESD SENSITIVITY



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be take to avoid performance degradation or loss of functionality.

MAXIMUM POWER DISSIPATION

See Engineer-to-Engineer Note "Estimating Power Dissipation for ADSP-2137x SHARC Processors" (EE-319) for detailed thermal and power information regarding maximum power dissipation. For information on package thermal specifications, see Thermal Characteristics on Page 45.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 10 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 10. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.5 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage –0.5 V to V_{DDEXT}	+0.5 V
Output Voltage Swing –0.5 V to V_{DDEXT}	+0.5 V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C
Junction Temperature under Bias	125°C

TIMING SPECIFICATIONS

The ADSP-21371's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, and serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLKCFG1–0 pins (see Table 8 on Page 14). To determine switching frequencies for the serial ports, divide down the internal clock, using the programmable divider control of each port (DIVx for the serial ports).

Figure 3 shows core to CLKIN ratios of 6:1, 16:1, and 32:1 with external oscillator or crystal. Note that more ratios are possible and can be set through software using the power management control register (PMCTL). For more information, see the *ADSP-2136x SHARC Processor Programming Reference*.

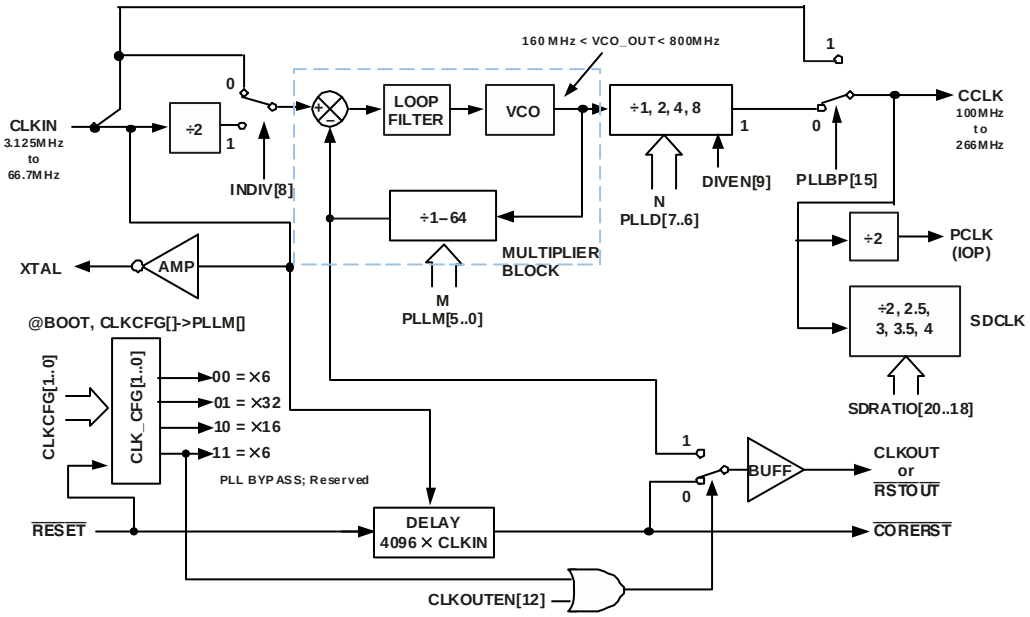


Figure 3. Core Clock and System Clock Relationship to CLKIN

The ADSP-21371's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

Core clock frequency can be calculated as:

$$CCLK = 1 \times t_{CCLK} = f_{INPUT} \times (PLLM/PLLD)$$

Note that in the user application, the PLL multiplier value should be selected in such a way that the VCO frequency falls in between 160 MHz and 800 MHz. The VCO frequency is calculated as follows:

where:

f_{VCO} = VCO frequency.

$PLLM$ = multiplier value programmed.

$PLLD$ = divider value programmed.

f_{INPUT} = input frequency to the PLL.

f_{INPUT} = CLKIN when the input divider is disabled.

f_{INPUT} = CLKIN/2 when the input divider is enabled.

Note the definitions of various clock periods shown in Table 12 which are a function of CLKIN and the appropriate ratio control shown in Table 11.

Table 11. ADSP-21371 CLKOUT and CCLK Clock Generation Operation

Timing Requirements	Description	Calculation
CLKIN	Input Clock	$1/t_{CK}$
CCLK	Core Clock	$1/t_{CCLK}$

Table 12. Clock Periods

Timing Requirements	Description[1]
t_{CK}	CLKIN Clock Period
t_{CCLK}	(Processor) Core Clock Period
t_{PCLK}	(Peripheral) Clock Period = $2 \times t_{CCLK}$
t_{SCLK}	Serial Port Clock Period = $(t_{PCLK}) \times SR$
t_{SDCLK}	SDRAM Clock Period = $(t_{CCLK}) \times SDR$
t_{SPICLK}	SPI Clock Period = $(t_{PCLLK}) \times SPIR$

[1] where:
SR = serial port-to-core clock ratio (wide range, determined by SPORT CLKDIV bits in DIVx register)
SPIR = SPI-to-Core Clock Ratio (wide range, determined by SPIBAUD register setting)
SDR=SDRAM-to-Core Clock Ratio (Values determined by bits 20-18 of the PMCTL register)

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. See Figure 36 on Page 44 under Test Conditions for voltage reference levels.

Switching Characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Power-Up Sequencing

The timing requirements for processor startup are given in Table 13.

Table 13. Power Up Sequencing Timing Requirements (Processor Startup)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DDINT}/V_{DDEXT} On	0		ns
$t_{IVDDEVDD}$	V_{DDINT} on Before V_{DDEXT}	–50	200	ms
t_{CLKVDD}[1]	CLKIN Valid After V_{DDINT}/V_{DDEXT} Valid	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10[2]		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20[3]		µs
Switching Characteristic				
$t_{CORERST}$	Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096 \times t_{CK} + 2 \times t_{CCLK}$[4, 5]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their 1.2 and 3.3 volt rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case startup timing of crystal oscillators. Refer to your crystal oscillator manufacturer's datasheet for startup time. Assume a 25 ms maximum oscillator startup time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Based on CLKIN cycles.

[4] Applies after the power-up sequence is complete. Subsequent resets require a minimum of four CLKIN cycles for $\overline{\text{RESET}}$ to be held low in order to properly initialize and propagate default states at all I/O pins.

[5] The 4096 cycle count depends on t_{SRST} specification in Table 15. If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

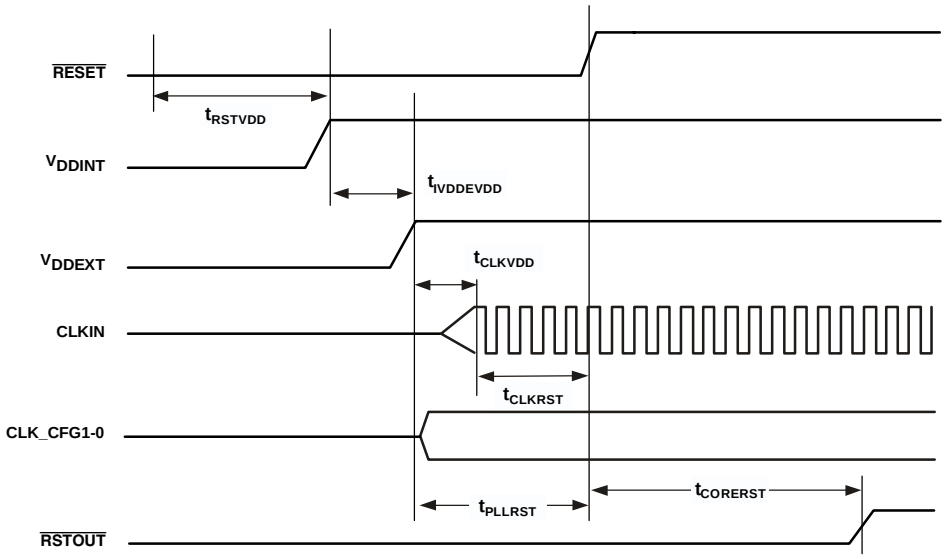


Figure 4. Power-Up Sequencing

Clock Input

Table 14. Clock Input

Parameter		266 MHz Min	266 MHz Max	Unit
Timing Requirements				
t_{CK}	CLKIN Period	22.5[1]	320[2]	ns
t_{CKL}	CLKIN Width Low	10[1]	180[2]	ns
t_{CKH}	CLKIN Width High	10[1]	180[2]	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		6	ns
t_{CCLK}[3]	CCLK Period	3.75[1]	10	ns

[1] Applies only for CLKCFG1–0 = 00 and default values for PLL control bits in PMCTL.
[2] Applies only for CLKCFG1–0 = 01 and default values for PLL control bits in PMCTL.
[3] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.

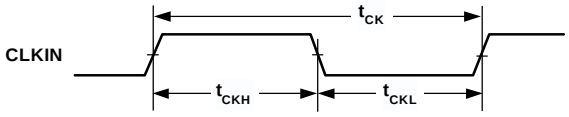


Figure 5. Clock Input

Clock Signals

The ADSP-21371 can use an external clock or a crystal. See the CLKIN pin description in Table 5. The programmer can configure the ADSP-21371 to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 6 shows the component connections used for a crystal operating in fundamental mode. Note that the clock rate is achieved using a 16.67 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN achieves a clock speed of 266 MHz). To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register.

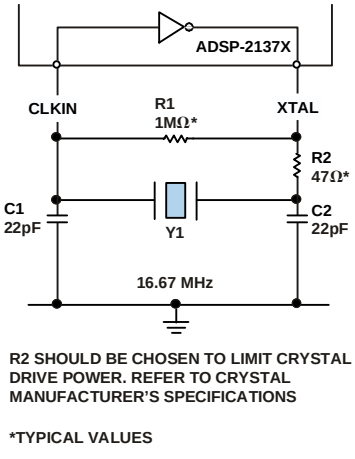


Figure 6. 266 MHz Operation (Fundamental Mode Crystal)

Reset

Table 15. Reset

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}[1]	$\overline{\text{RESET}}$ Pulse Width Low	4 × t_{CK}		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN Low	8		ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 ms while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

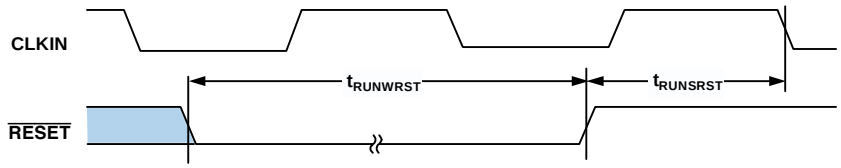


Figure 7. Reset

Running Reset

The following timing specification applies to CLKOUT/$\overline{\text{RESETOUT}}$/$\overline{\text{RUNRSTIN}}$ pin when it is configured as $\overline{\text{RUNRSTIN}}$.

Table 16. Running Reset

Parameter		Min	Max	Unit
Timing Requirements				
$t_{WRUNRST}$	Running $\overline{\text{RESET}}$ Pulse Width Low	4 × t_{CK}		ns
$t_{SRUNRST}$	Running $\overline{\text{RESET}}$ Setup Before CLKIN High	8		ns

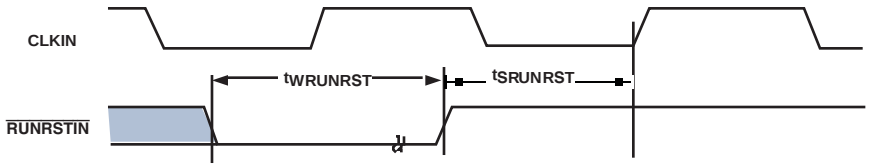


Figure 8. Running Reset

Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts as well as the DAI_P20-1 and DPI_P14-1 pins when they are configured as interrupts.

Table 17. Interrupts

Parameter		Min	Max	Unit
Timing Requirement				
t_{IPW}	$\overline{\text{IRQx}}$ Pulse Width	$2 \times t_{PCLK} + 2$		ns

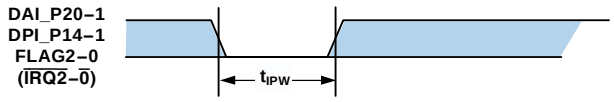


Figure 9. Interrupts

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (CTIMER).

Table 18. Core Timer

Parameter		Min	Max	Unit
Switching Characteristic				
t_{WCTIM}	CTIMER Pulse Width	$4 \times t_{PCLK} - 1$		ns

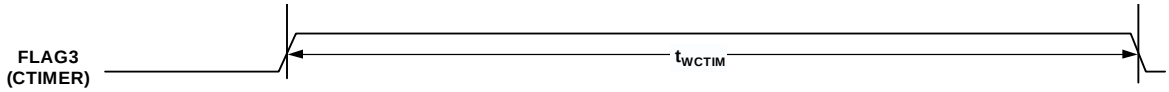


Figure 10. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to Timer0 and Timer1 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 19. Timer PWM_OUT Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{PWMO}	Timer Pulse Width Output	$2 \times t_{PCLK} - 2$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

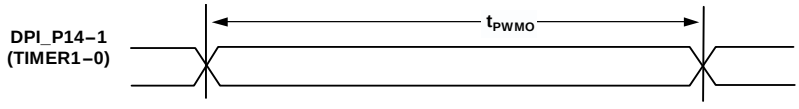


Figure 11. Timer PWM_OUT Timing

Timer WDTH_CAP Timing

The following timing specification applies to timer0, and timer1, and in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DPI_P14–1 pins through the SRU. Therefore, the timing specification provided below is valid at the DPI_P14–1 pins.

Table 20. Timer Width Capture Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{PWI}	Timer Pulse Width	$2 \times t_{PCLK}$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

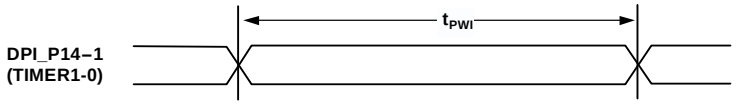


Figure 12. Timer Width Capture Timing

Pin to Pin Direct Routing (DAI and DPI)

For direct pin connections only (for example DAI_PB01_I to DAI_PB02_O).

Table 21. DAI Pin to Pin Routing

Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI/DPI Pin Input Valid to DAI Output Valid	1.5	10	ns

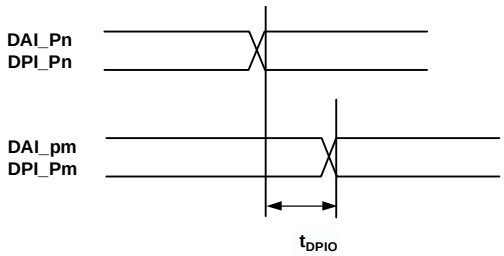


Figure 13. DAI Pin to Pin Direct Routing

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers) there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01 – DAI_P20).

Table 22. Precision Clock Generator (Direct Pin Routing)

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCGIW}	Input Clock Period	24		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3		ns
Switching Characteristics				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	10	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + ((2.5) \times t_{PCGIW})$	$10 + ((2.5) \times t_{PCGIW})$	ns
$t_{DTRIGFS}$	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIW})$	$10 + ((2.5 + D - PH) \times t_{PCGIW})$	ns
t_{PCGOW}[1]	Output Clock Period	$2 \times t_{PCGIW} - 1$		ns

D = FSxDIV, PH = FSxPHASE. For more information, see the ADSP-2136x SHARC Processor Hardware Reference for the ADSP-21368 Processor, "Precision Clock Generators" chapter.

[1] Normal mode of operation.

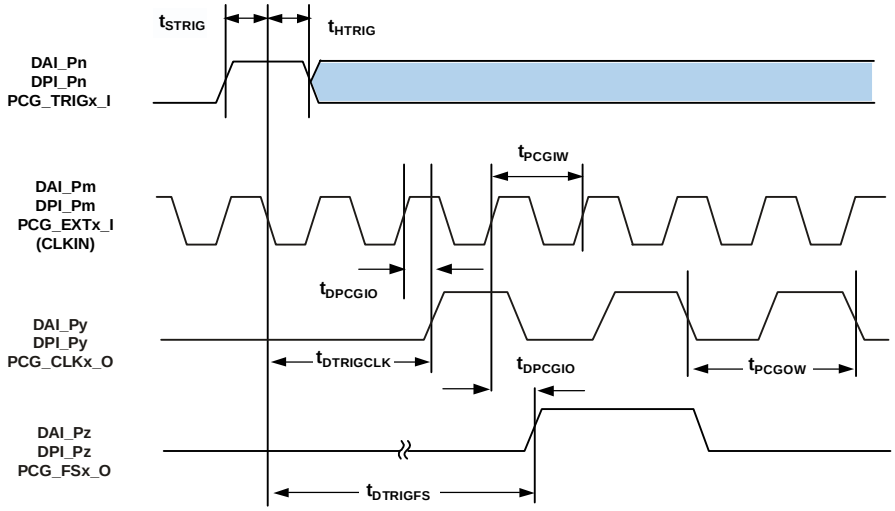


Figure 14. Precision Clock Generator (Direct Pin Routing)

Flags

The timing specifications provided below apply to the FLAG3–0 and DPI_P14–1 pins, and the DATA31-0 pins. See Table 5 on page 12 for more information on flag use.

Table 23. Flags

Parameter		Min	Max	Unit
Timing Requirement				
t_{FIPW}	DPI_P14-1, DATA31-0, FLAG3–0 IN Pulse Width	$2 \times t_{PCLK} + 3$		ns
Switching Characteristic				
t_{FOPW}	DPI_P14-1, DATA31-0, FLAG3–0 OUT Pulse Width	$2 \times t_{PCLK} - 2$		ns

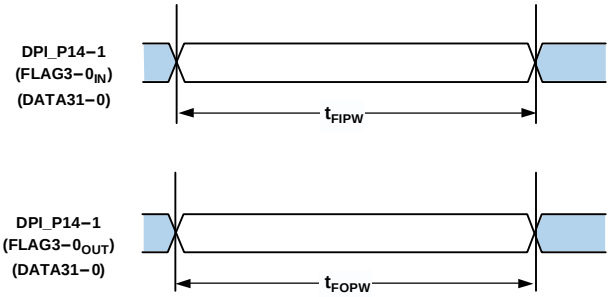


Figure 15. Flags

SDRAM Interface Timing (133 MHz SDCLK)

Table 24. SDRAM Interface Timing[1]

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSDAT}	DATA Setup Before SDCLK	0.58		ns
t_{HSDAT}	DATA Hold After SDCLK	2.2		ns
Switching Characteristics				
t_{SDCLK}	SDCLK Period	7.5		ns
t_{SDCLKH}	SDCLK Width High	3		ns
t_{SCCLKL}	SDCLK Width Low	3		ns
t_{DCAD}	Command, ADDR, Data Delay After SDCLK[2]		5.3	ns
t_{HCAD}	Command, ADDR, Data Hold After SDCLK[2]	1.3		ns
t_{DSDAT}	Data Disable After SDCLK		5.3	ns
t_{ENSDAT}	Data Enable After SDCLK	1.6		ns

[1] For F_{CCLK} = 133 MHz (SDCLK ratio = 1:2).
[2] Command pins include: $\overline{SDCAS}$, $\overline{SDRAS}$, $\overline{SDWE}$, $\overline{MSx}$, SDA10, and SDCKE.

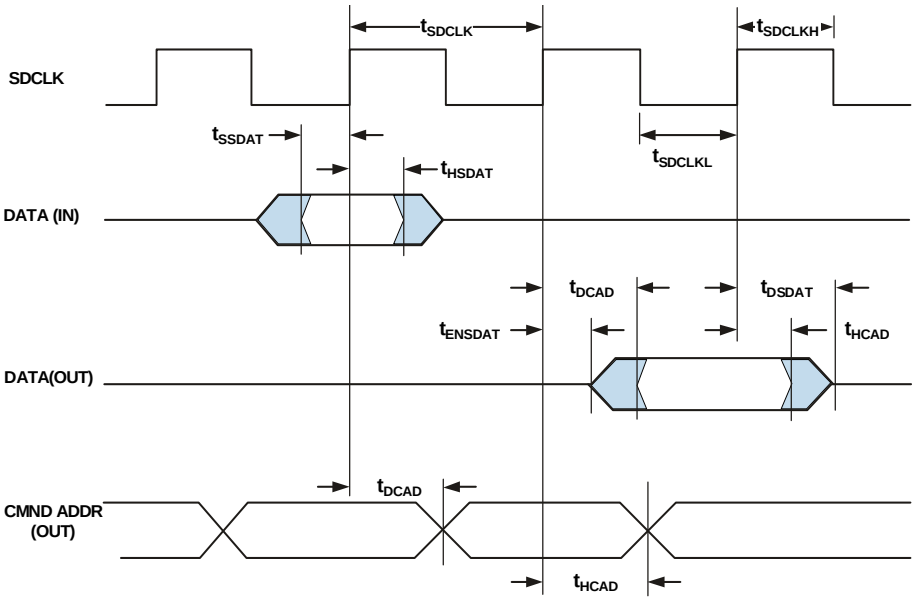


Figure 16. SDRAM Interface Timing for 133 MHz SDCLK

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only apply to asynchronous access mode.

Table 25. Memory Read—Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAD}	Address, Selects Delay to Data Valid[1, 2]		W+t_{SDCLK} –5.12	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1]		W – 3	ns
t_{SDS}	Data Setup to $\overline{RD}$ High	2.2		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[3, 4]	0		ns
t_{DAAK}	ACK Delay from Address, Selects[2, 5]		t_{SDCLK}–10.1+ W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[4]		W – 7.0	ns
Switching Characteristics				
t_{DRHA}	Address Selects Hold After $\overline{RD}$ High	RHC + 0.38		ns
t_{DARL}	Address Selects to $\overline{RD}$ Low[2]	t_{SDCLK}–3.3		ns
t_{RW}	$\overline{RD}$ Pulse Width	W – 1.4		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$, Low	HI + t_{SDCLK}–0.8		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}.
HI = RHC + IC (RHC = (number of Read Hold Cycles specified in AMICTLx register) x t_{SDCLK}
IC = (number of idle cycles specified in AMICTLx register) x t_{SDCLK}).
H = (number of hold cycles specified in AMICTLx register) x t_{SDCLK}.

[1] Data delay/setup: System must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
[2] The falling edge of $\overline{MS}$x, is referenced.
[3] Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only apply to asynchronous access mode.
[4] Data hold: User must meet t_{HDRH} in asynchronous access mode. See Test Conditions on Page 44 for the calculation of hold times given capacitive and dc loads.
[5] ACK delay/setup: User must meet t_{DAAK}, or t_{DSAK}, for deassertion of ACK (low). For asynchronous assertion of ACK (high) user must meet t_{DAAK} or t_{DSAK}.

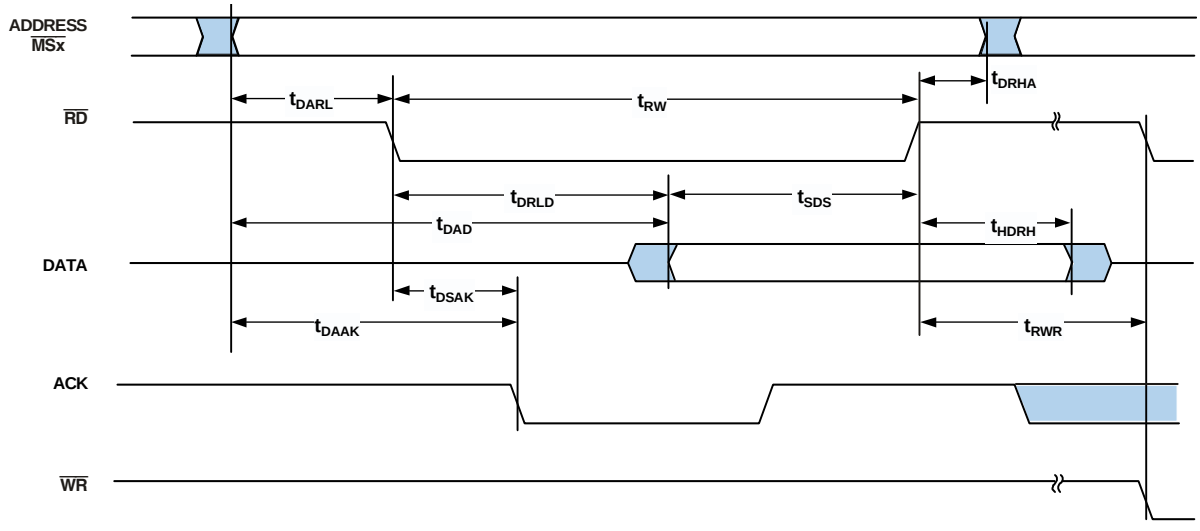


Figure 17. Memory Read—Bus Master

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only apply to asynchronous access mode.

Table 26. Memory Write—Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		t_{SDCLK} – 10.1 + W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low [1, 3]		W – 7.1	ns
Switching Characteristics				
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	t_{SDCLK} – 3.6+ W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	t_{SDCLK} – 2.7		ns
t_{WW}	$\overline{WR}$ Pulse Width	W – 1.3		ns
t_{DDWH}	Data Setup Before $\overline{WR}$ High	t_{SDCLK} – 3.0+ W		ns
t_{DWHA}	Address Hold After $\overline{WR}$ Deasserted	H + 0.15		ns
t_{DWHD}	Data Hold After $\overline{WR}$ Deasserted	H + 0.02		ns
t_{DATRWH}	Data Disable After $\overline{WR}$ Deasserted[4]	t_{SDCLK} – 1.37+ H	t_{SDCLK} + 4.9+ H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$ Low	t_{SDCLK} – 1.5+ H		ns
t_{DDWR}	Data Disable Before $\overline{RD}$ Low	2t_{SDCLK} – 5.1		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	t_{SDCLK} – 4.1		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}
H = (number of hold cycles specified in AMICTLx register) x t_{SDCLK}

[1] ACK delay/setup: System must meet t_{DAAK}, or t_{DSAK}, for deassertion of ACK (low). For asynchronous assertion of ACK (high) user must meet t_{DAAK} or t_{DSAK}.
[2] The falling edge of $\overline{MSx}$ is referenced.
[3] Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only applies to asynchronous access mode.
[4] See Test Conditions on Page 44 for calculation of hold times given capacitive and dc loads.

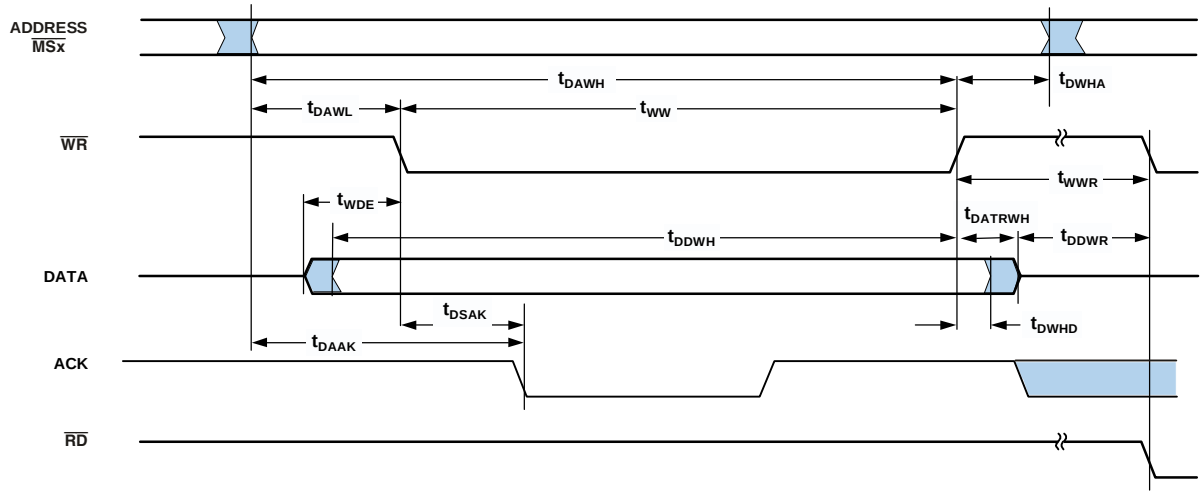


Figure 18. Memory Write—Bus Master

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Serial port signals (SCLK, FS, Data Channel A, Data Channel B) are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 27. Serial Ports—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}[1]	FS Setup Before SCLK (Externally Generated FS in either Transmit or Receive Mode)	2.5		ns
t_{HFSE}[1]	FS Hold After SCLK (Externally Generated FS in either Transmit or Receive Mode)	2.5		ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	2.5		ns
t_{HDRE}[1]	Receive Data Hold After SCLK	2.5		ns
t_{SCLKW}	SCLK Width	10		ns
t_{SCLK}	SCLK Period	20		ns
Switching Characteristics				
t_{DFSE}[2]	FS Delay After SCLK (Internally Generated FS in either Transmit or Receive Mode)		10.5	ns
t_{HOFSE}[2]	FS Hold After SCLK (Internally Generated FS in either Transmit or Receive Mode)	2		ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		11	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 28. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}[1]	FS Setup Before SCLK (Externally Generated FS in either Transmit or Receive Mode)	7		ns
t_{HFSI}[1]	FS Hold After SCLK (Externally Generated FS in either Transmit or Receive Mode)	2.5		ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	7		ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5		ns
Switching Characteristics				
t_{DFSI}[2]	FS Delay After SCLK (Internally Generated FS in Transmit Mode)		4	ns
t_{HOFSI}[2]	FS Hold After SCLK (Internally Generated FS in Transmit Mode)	–1.0		ns
t_{DFSIR}[2]	FS Delay After SCLK (Internally Generated FS in Receive Mode)		10.7	ns
t_{HOFSIR}[2]	FS Hold After SCLK (Internally Generated FS in Receive Mode)	–1.0		ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		3.6	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–1.0		ns
t_{SCKLIW}	Transmit or Receive SCLK Width	$0.5t_{SCLK} - 2$	$0.5t_{SCLK} + 2$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

Table 29. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}[1]	Data Enable from External Transmit SCLK	2		ns
t_{DDTTE}[1]	Data Disable from External Transmit SCLK		10	ns
t_{DDTIN}[1]	Data Enable from Internal Transmit SCLK	–1		ns

[1] Referenced to drive edge.

Table 30. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$[1]	Data Delay from Late External Transmit FS or External Receive FS with MCE = 1, MFD = 0		10	ns
$t_{DDTENFS}$[1]	Data Enable for MCE = 1, MFD = 0	0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified sample pair as well as DSP serial mode, and MCE = 1, MFD = 0.

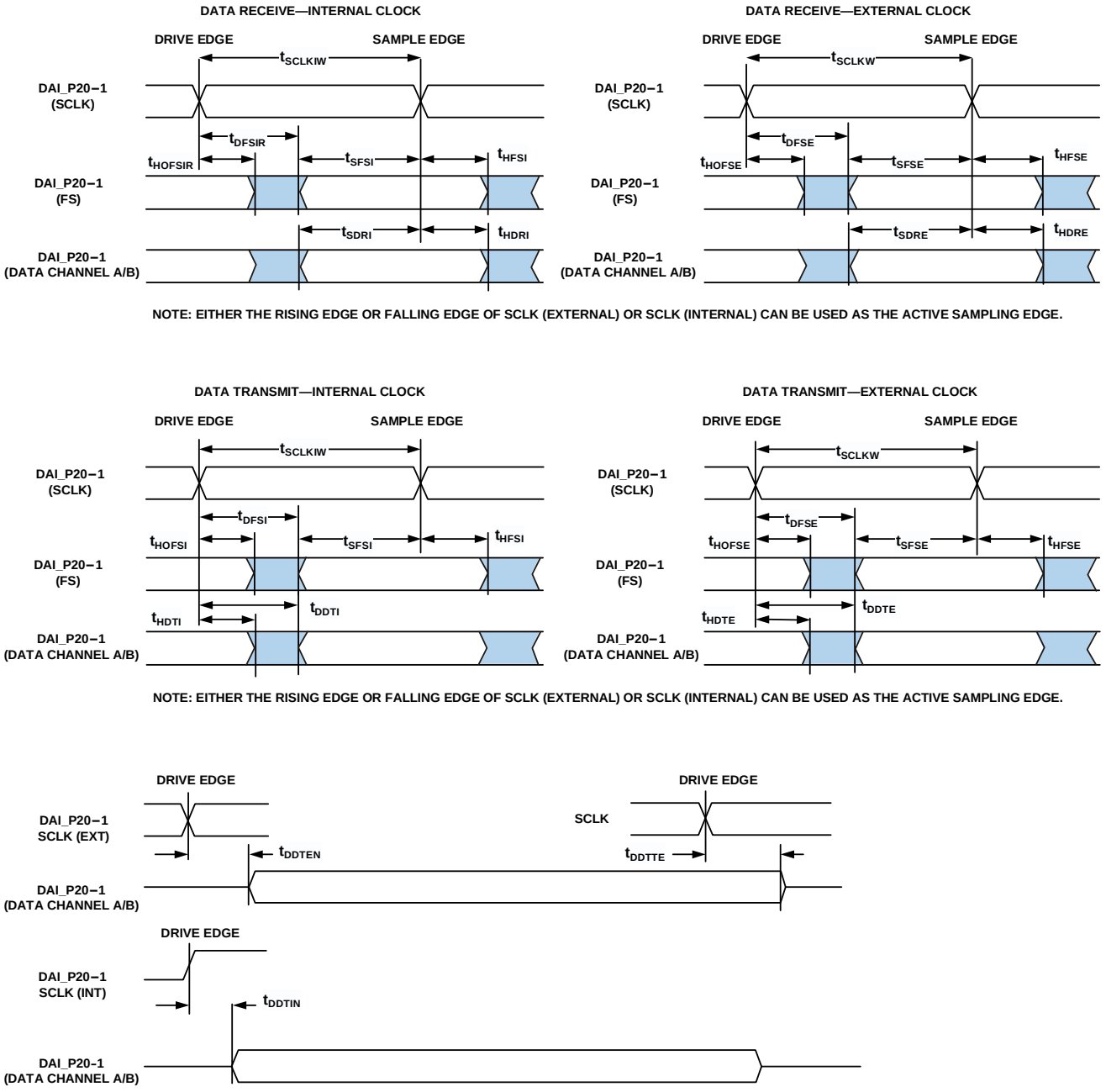


Figure 19. Serial Ports

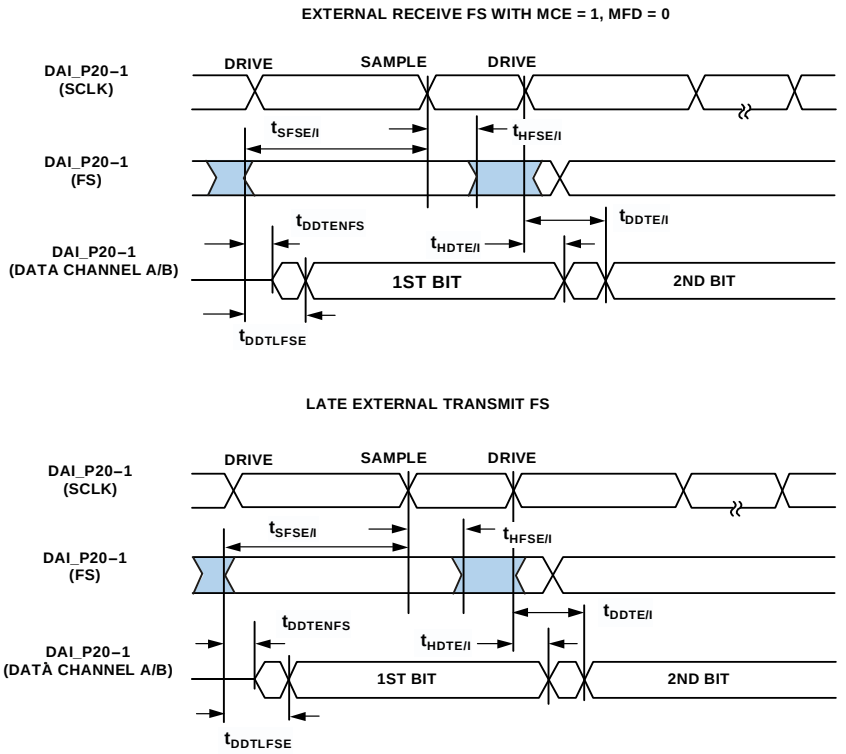


Figure 20. External Late Frame Sync[1]

[1] This figure reflects changes made to support left-justified sample pair mode.

Input Data Port (IDP)

The timing requirements for the IDP are given in Table 31. IDP signals (SCLK, FS, and SDATA) are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 31. Input Data Port (IDP)

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	FS Setup Before SCLK Rising Edge	3.8		ns
t_{SIHFS}[1]	FS Hold After SCLK Rising Edge	2.5		ns
t_{SISD}[1]	SData Setup Before SCLK Rising Edge	2.5		ns
t_{SIHD}[1]	SData Hold After SCLK Rising Edge	2.5		ns
$t_{IDPCLKW}$	Clock Width	9		ns
t_{IDPCLK}	Clock Period	24		ns

[1] DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

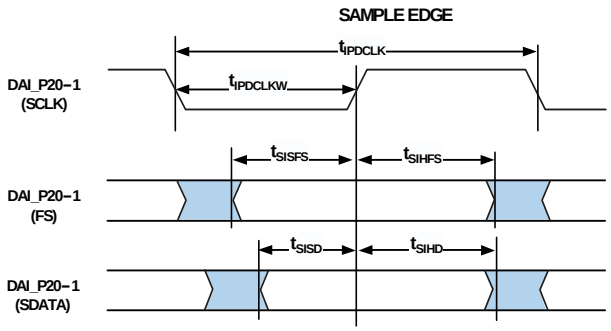


Figure 21. IDP Master Timing

Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in Table 32. PDAP is the parallel mode operation of Channel 0 of the IDP. For details on the operation of the PDAP, see the PDAP chapter of the *ADSP-21368 SHARC Processor Hardware Reference*. Note that the most significant 16 bits of external PDAP data can be provided through the DATA31–16 pins. The remaining four bits can only be sourced through DAI_P4–1. The timing below is valid at the DATA31–16 pins.

Table 32. Parallel Data Acquisition Port (PDAP)

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SPCLKEN}$[1]	PDAP_CLKEN Setup Before PDAP_CLK Sample Edge	2.5		ns
$t_{HPCLKEN}$[1]	PDAP_CLKEN Hold After PDAP_CLK Sample Edge	2.5		ns
t_{PDSD}[1]	PDAP_DAT Setup Before SCLK PDAP_CLK Sample Edge	3.85		ns
t_{PDHD}[1]	PDAP_DAT Hold After SCLK PDAP_CLK Sample Edge	2.5		ns
t_{PDCLKW}	Clock Width	7		ns
t_{PDCLK}	Clock Period	24		ns
Switching Characteristics				
t_{PDHLDD}	Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word	$2 \times t_{PCLK} + 3$		ns
t_{PDSTRB}	PDAP Strobe Pulse Width	$2 \times t_{PCLK} - 1$		ns

[1] Source pins of DATA are DATA31–12 or DAI pins. Source pins for SCLK and FS are: 1) DAI pins, 2) CLKIN through PCG, or 3) DAI pins through PCG.

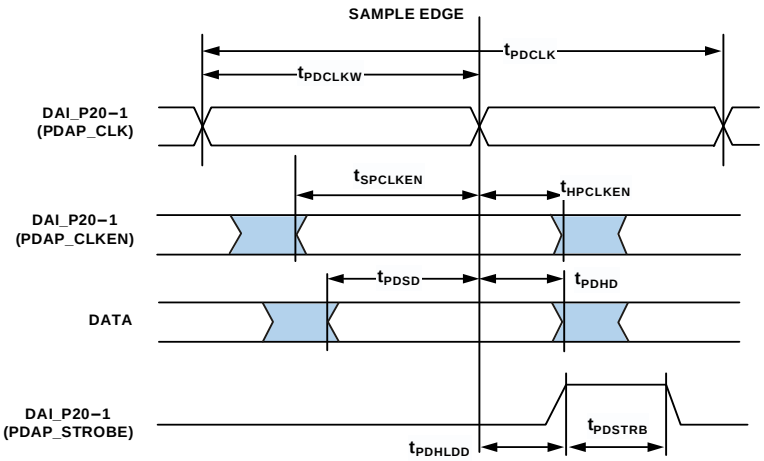


Figure 22. PDAP Timing

Pulse-Width Modulation Generators (PWM)

The following timing specifications apply when the DATA31-16 pins are configured as PWM.

Table 33. Pulse-Width Modulation (PWM) Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{PWMW}	PWM Output Pulse Width	$t_{PCLK} - 2.5$	$(2^{16} - 2) \times t_{PCLK} - 2.5$	ns
t_{PWMP}	PWM Output Period	$2 \times t_{PCLK} - 2.5$	$(2^{16} - 1) \times t_{PCLK} - 2.5$	ns

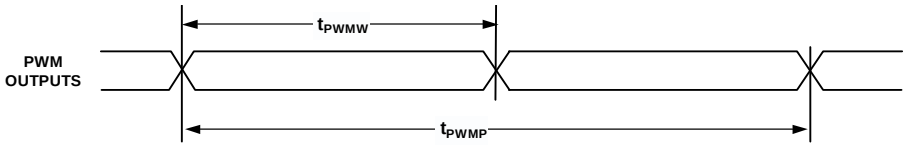


Figure 23. PWM Timing

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left justified, I²S, or right justified with word widths of 16-, 18-, 20-, or 24-bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter-Serial Input Waveforms

Figure 24 shows the right-justified mode. LRCLK is high for the left channel and low for the right channel. Data is valid on the rising edge of SCLK. The MSB is delayed 12-bit clock periods (in 20-bit output mode) or 16-bit clock periods (in 16-bit output mode) from an LRCLK transition, so that when there are 64 SCLK periods per LRCLK period, the LSB of the data will be right-justified to the next LRCLK transition.

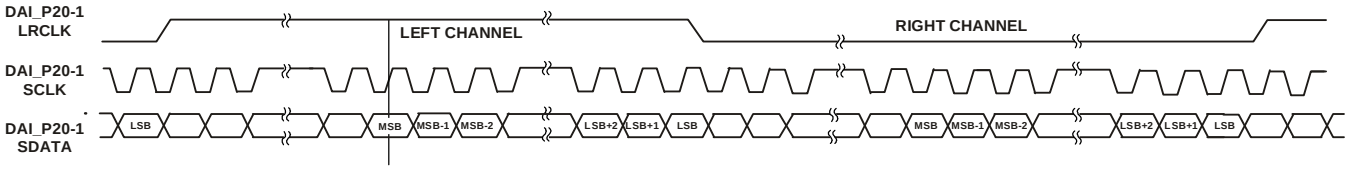


Figure 24. Right-Justified Mode

Figure 25 shows the default I²S-justified mode. LRCLK is low for the left channel and HI for the right channel. Data is valid on the rising edge of SCLK. The MSB is left-justified to an LRCLK transition but with a single SCLK period delay.

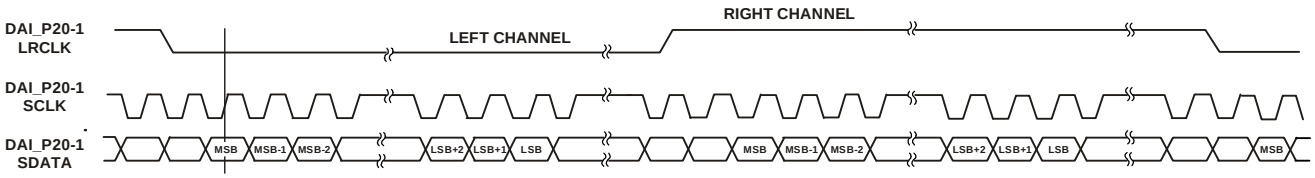


Figure 25. I²S-Justified Mode

Figure 26 shows the left-justified mode. LRCLK is high for the left channel and LO for the right channel. Data is valid on the rising edge of SCLK. The MSB is left-justified to an LRCLK transition with no MSB delay.

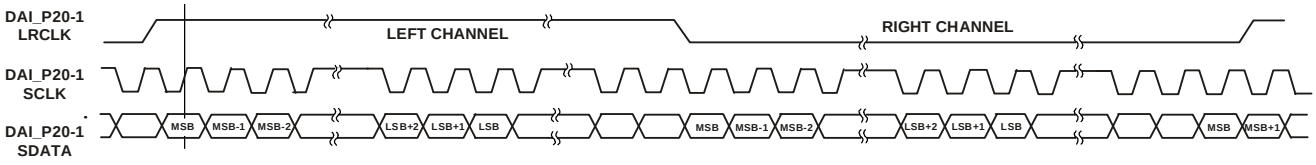


Figure 26. Left-Justified Mode

S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 34. Input signals (SCLK, FS, SDATA) are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 34. S/PDIF Transmitter Input Data Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	FS Setup Before SCLK Rising Edge	3		ns
t_{SIHFS}[1]	FS Hold After SCLK Rising Edge	3		ns
t_{SISD}[1]	SData Setup Before SCLK Rising Edge	3		ns
t_{SIHD}[1]	SData Hold After SCLK Rising Edge	3		ns
$t_{SITXCLKW}$	Transmit Clock Width	9		ns
$t_{SITXCLK}$	Transmit Clock Period	20		ns
$t_{SISCLKW}$	Clock Width	36		ns
t_{SISCLK}	Clock Period	80		ns

[1] DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

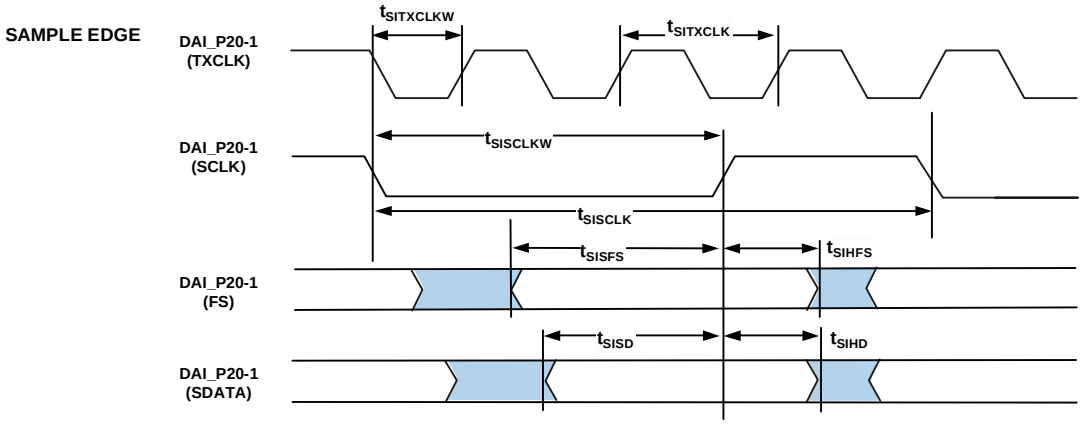


Figure 27. S/PDIF Transmitter Input Timing

Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter has an oversampling clock. This TxCLK input is divided down to generate the biphase clock.

Table 35. Over Sampling Clock (TxCLK) Switching Characteristics

Parameter	Min	Max	Unit
TxCLK Frequency for TxCLK = 384 × FS		73.8	MHz
TxCLK Frequency for TxCLK = 256 × FS		49.2	MHz
Frame Rate		192.0	kHz

S/PDIF Receiver

The following section describes timing as it relates to the S/PDIF receiver.

Internal Digital PLL Mode

In the internal digital phase-locked loop mode the internal PLL (digital PLL) generates the 512 × FS clock.

Table 36. S/PDIF Receiver Internal Digital PLL Mode Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	LRCLK Delay After SCLK		5	ns
t_{HOFSI}	LRCLK Hold After SCLK	–2		ns
t_{DDTI}	Transmit Data Delay After SCLK		5	ns
t_{HDTI}	Transmit Data Hold After SCLK	–2		ns
t_{SCLKIW}[1]	Transmit SCLK Width	38.5		ns

[1] SCLK frequency is 64 × FS where FS = the frequency of LRCLK.

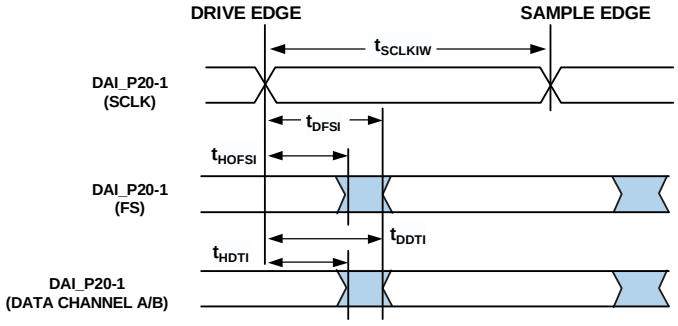


Figure 28. S/PDIF Receiver Internal Digital PLL Mode Timing

SPI Interface—Master

The ADSP-21371 contains two SPI ports. Both primary and secondary are available through DPI only. The timing provided in Table 37 and Table 38 applies to both.

Table 37. SPI Interface Protocol—Master Switching and Timing Specifications

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid To SPICLK Edge (Data Input Setup Time)	8.2		ns
t_{HSPIDM}	SPICLK Last Sampling Edge To Data Input Not Valid	2		ns
Switching Characteristics				
$t_{SPICLKM}$	Serial Clock Cycle	$8 \times t_{PCLK} - 2$		ns
t_{SPICHM}	Serial Clock High Period	$4 \times t_{PCLK} - 2$		ns
t_{SPICLM}	Serial Clock Low Period	$4 \times t_{PCLK} - 2$		ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		2.5	
$t_{HDSPIDM}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	2		ns
t_{SDSCIM}	FLAG3–0IN (SPI device select) Low to First SPICLK Edge	$4 \times t_{PCLK} - 2$		ns
t_{HDSM}	Last SPICLK Edge to FLAG3–0IN High	$4 \times t_{PCLK} - 2$		ns
t_{SPITDM}	Sequential Transfer Delay	$4 \times t_{PCLK} - 1$		ns

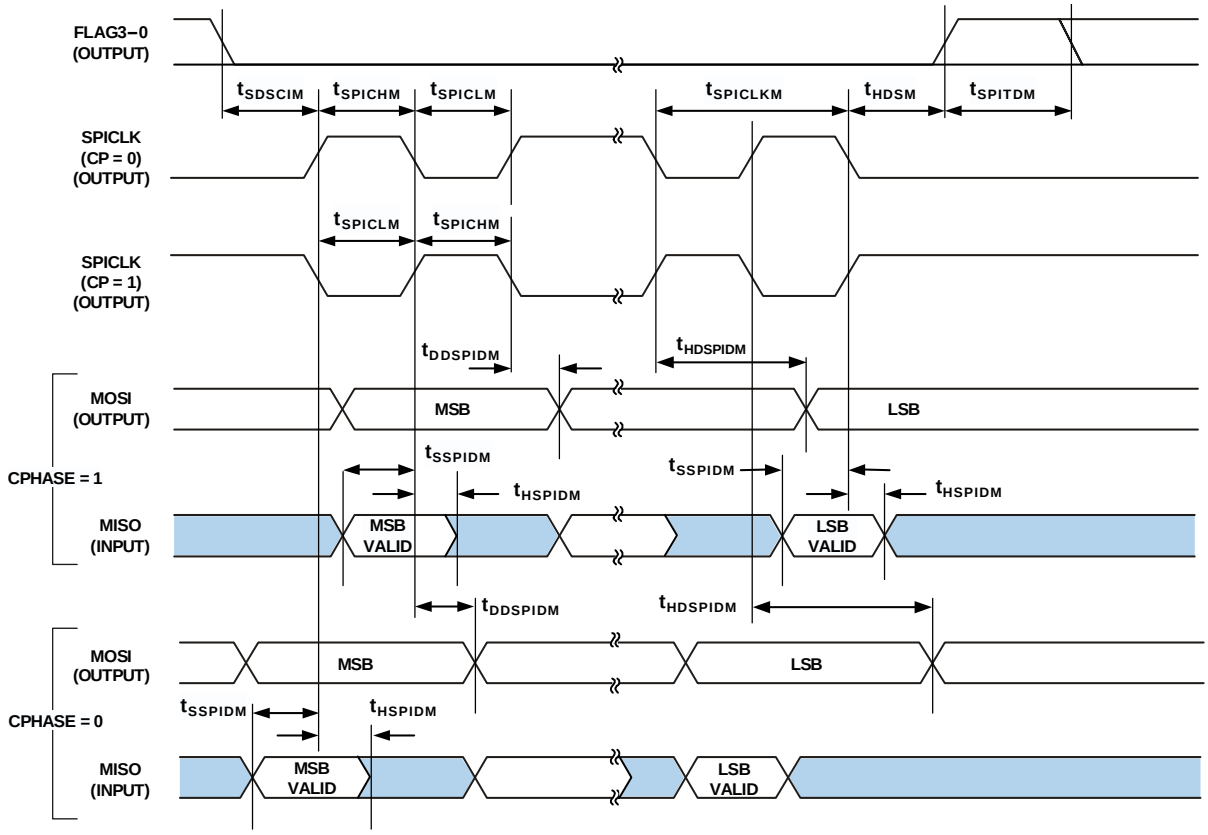


Figure 29. SPI Master Timing

SPI Interface—Slave

Table 38. SPI Interface Protocol—Slave Switching and Timing Specifications

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SPICLKS}$	Serial Clock Cycle	$4 \times t_{PCLK} - 2$		ns
t_{SPICHS}	Serial Clock High Period	$2 \times t_{PCLK} - 2$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{PCLK} - 2$		ns
t_{SDSCO}	$\overline{SPIDS}$ Assertion to First SPICLK Edge			ns
	CPHASE = 0	$2 \times t_{PCLK}$		
	CPHASE = 1	$2 \times t_{PCLK}$		
t_{HDS}	Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted, CPHASE = 0	$2 \times t_{PCLK}$		ns
t_{SSPIDS}	Data Input Valid to SPICLK edge (Data Input Set-up Time)	2		ns
t_{HSPIDS}	SPICLK Last Sampling Edge to Data Input Not Valid	2		ns
t_{SDPPW}	$\overline{SPIDS}$ Deassertion Pulse Width (CPHASE=0)	$2 \times t_{PCLK}$		ns
Switching Characteristics				
t_{DSOE}	$\overline{SPIDS}$ Assertion to Data Out Active	0	6.8	ns
t_{DSDHI}	$\overline{SPIDS}$ Deassertion to Data High Impedance	0	6.8	ns
$t_{DDSPIDS}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		9.5	ns
$t_{HDSPIDS}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$2 \times t_{PCLK}$		ns
t_{DSOV}	$\overline{SPIDS}$ Assertion to Data Out Valid (CPHAS E = 0)		$5 \times t_{PCLK}$	ns

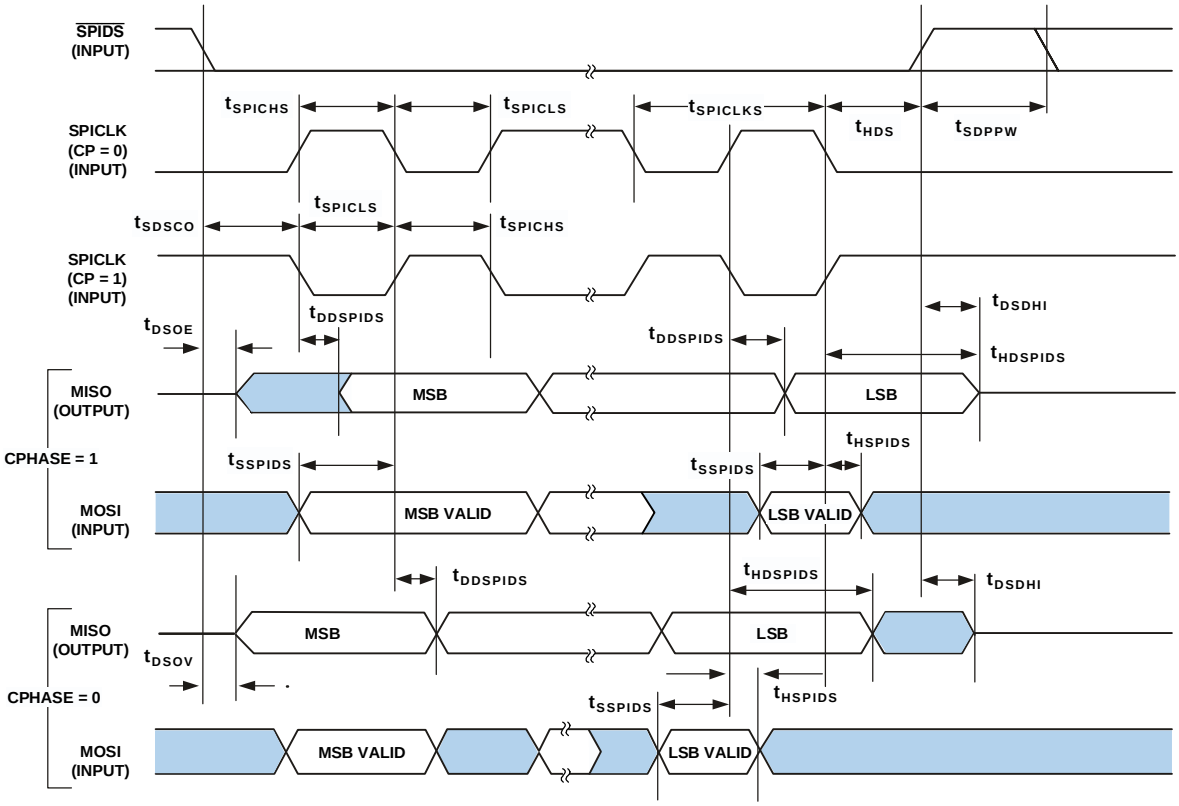


Figure 30. SPI Slave Timing

Universal Asynchronous Receiver-Transmitter (UART) Port—Receive and Transmit Timing

Figure 31 describes UART port receive and transmit operations. The maximum baud rate is PCLK/16 where PCLK = $1/t_{PCLK}$. As shown in Figure 31 there is some latency between the generation of internal UART interrupts and the external data operations. These latencies are negligible at the data transmission rates for the UART.

Table 39. UART Port

Parameter		Min	Max	Unit
Timing Requirement				
t_{RXD}[1]	Incoming Data Pulse Width	≥95		ns
Switching Characteristic				
t_{RXD}[1]	Incoming Data Pulse Width	≥95		ns

[1] UART signals RXD and TXD are routed through DPI P14-1 pins using the SRU.

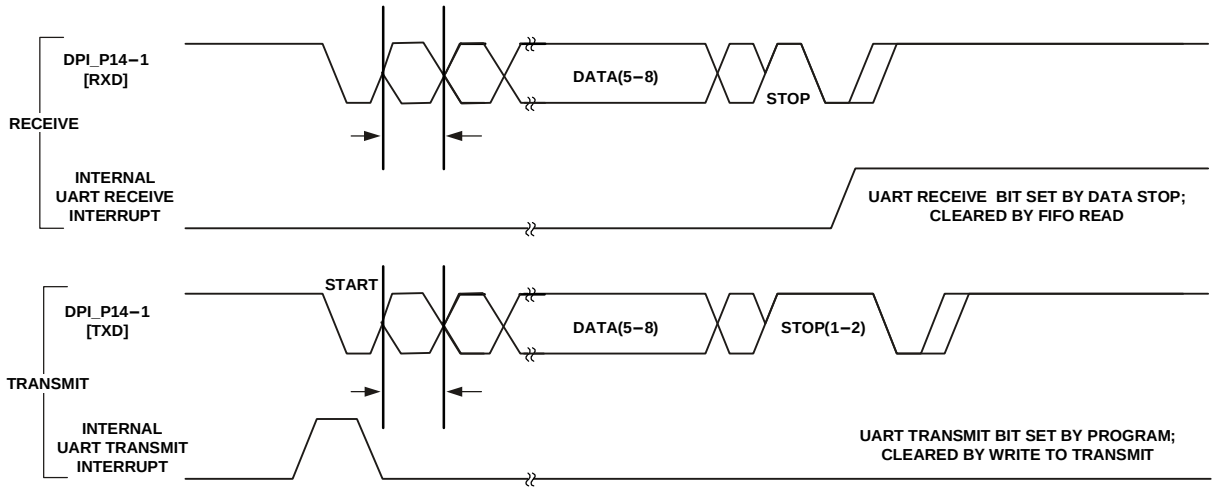


Figure 31. UART Port—Receive and Transmit Timing

TWI Controller Timing

Table 40 and Figure 32 provide timing information for the TWI interface. Input Signals (SCL, SDA) are routed to the DPI_P14–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 40. Characteristics of the SDA and SCL Bus Lines for F/S-Mode TWI Bus Devices[1]

Parameter		Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency	0	100	0	400	kHz
t_{HDSTA}	Hold Time (repeated) Start Condition. After This Period, the First Clock Pulse is Generated.	4.0		0.6		µs
t_{LOW}	Low Period of the SCL Clock	4.7		1.3		µs
t_{HIGH}	High Period of the SCL Clock	4.0		0.6		µs
t_{SUSTA}	Setup Time for a Repeated Start Condition	4.7		0.6		µs
t_{HDDAT}	Data Hold Time for TWI-bus Devices	0		0		µs
t_{SUDAT}	Data Setup Time	250		100		ns
t_{SUSTO}	Setup Time for Stop Condition	4.0		0.6		µs
t_{BUF}	Bus Free Time Between a Stop and Start Condition	4.7		1.3		µs
t_{SP}	Pulse Width of Spikes Suppressed By the Input Filter	n/a	n/a	0	50	ns

[1] All values referred to V_{IHmin} and V_{ILmax} levels. For more information, see Electrical Characteristics on page 15.

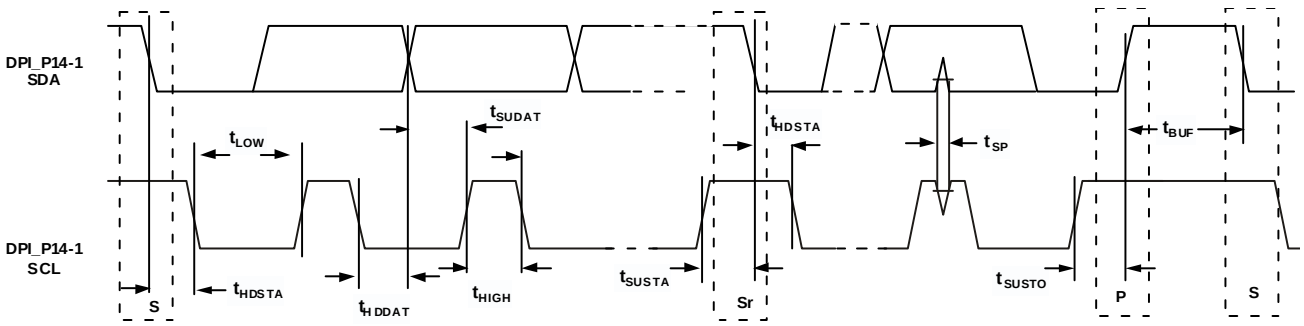


Figure 32. Fast and Standard Mode Timing on the TWI Bus

JTAG Test Access Port and Emulation

Table 41. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4 \times t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		7	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} / 2 + 7$	ns

[1] System Inputs = AD15–0, CLKCFG1–0, $\overline{\text{RESET}}$, BOOTCFG1–0, DAI_Px, and FLAG3–0.
[2] System Outputs = DAI_Px, AD15–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, FLAG3–0, CLKOUT, $\overline{\text{EMU}}$, and ALE.

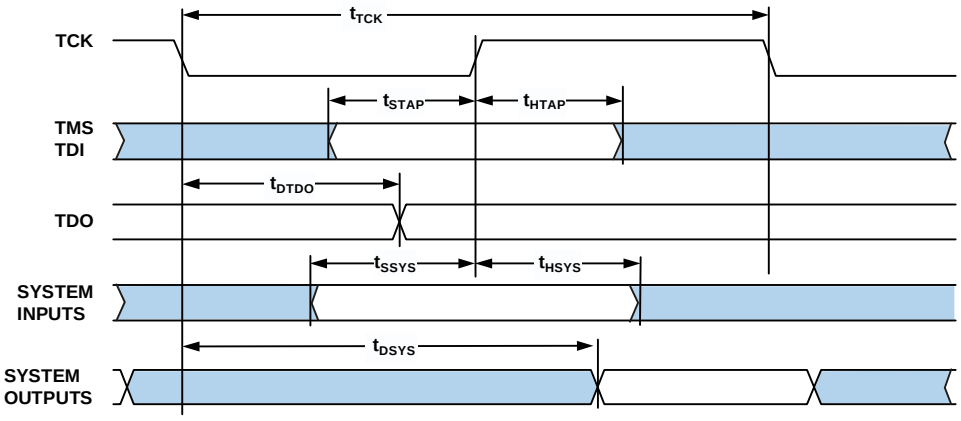


Figure 33. IEEE 1149.1 JTAG Test Access Port

OUTPUT DRIVE CURRENTS

Figure 34 shows typical I-V characteristics for the output drivers of the ADSP-21371. The curves represent the current drive capability of the output drivers as a function of output voltage.

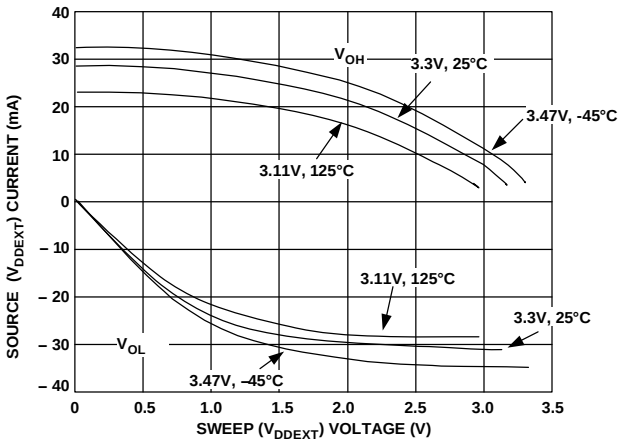


Figure 34. ADSP-21371 Typical Drive at Junction Temperature

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 15 on Page 21 through Table 41 on Page 43. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 35.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 36. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

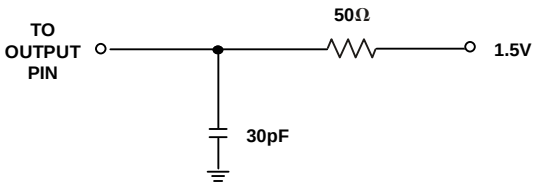


Figure 35. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

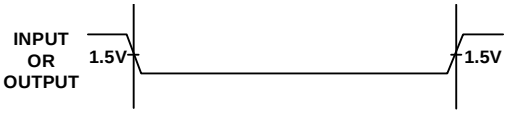


Figure 36. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 35). Figure 39 shows graphically how output delays and holds vary with load capacitance. The graphs of Figure 37, Figure 38, and Figure 39 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.

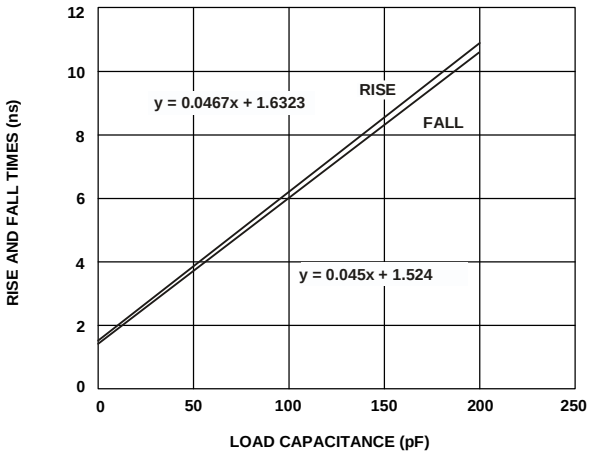


Figure 37. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Max)

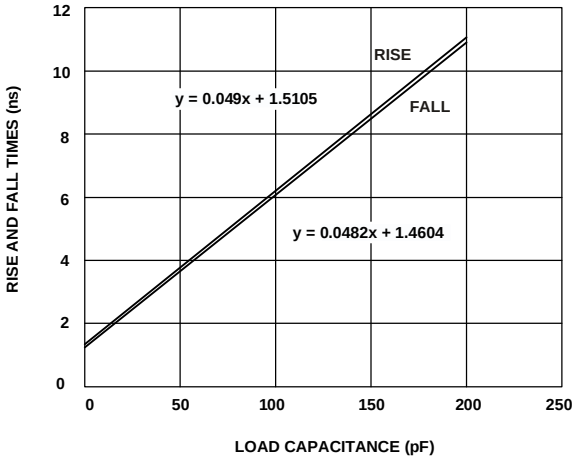


Figure 38. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Min)

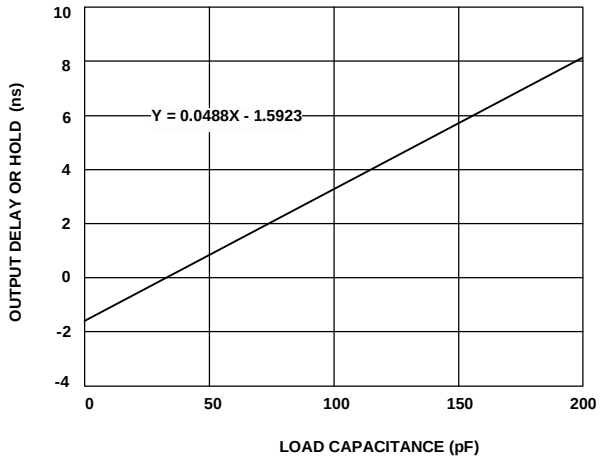


Figure 39. Typical Output Delay or Hold vs. Load Capacitance (at Ambient Temperature)

THERMAL CHARACTERISTICS

The ADSP-21371 processor is rated for performance over the temperature range specified in Operating Conditions on Page 15.

Table 42 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standards JESD51-7 (MQFP). The junction-to-case measurement complies with MIL- STD-883. All measurements use a 2S2P JEDEC test board.

To determine the junction temperature of the device while on the application PCB, use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature °C

T_{CASE} = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the Typical value from Table 42.

P_D = power dissipation

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature °C

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heatsink is required.

Values of θ_{JB} are provided for package comparison and PCB design considerations. Note that the thermal characteristics values provided in Table 42 are modeled values.

Table 42. Thermal Characteristics for 208-Lead MQFP

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	30.82	°C/W
θ_{JMA}	Airflow = 1 m/s	27.53	°C/W
θ_{JMA}	Airflow = 2 m/s	26.22	°C/W
θ_{JC}		14.04	°C/W
Ψ_{JT}	Airflow = 0 m/s	2.0	°C/W
Ψ_{JMT}	Airflow = 1 m/s	2.65	°C/W
Ψ_{JMT}	Airflow = 2 m/s	3.12	°C/W

208-LEAD MQFP PINOUT

Table 43. 208-Lead MQFP Pin Assignment (Numerically by Lead Number)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	V_{DDINT}	53	V_{DD}	105	V_{DD}	157	V_{DD}
2	DATA28	54	GND	106	GND	158	V_{DD}
3	DATA27	55	V_{DDEXT}	107	V_{DDEXT}	159	GND
4	GND	56	ADDR0	108	$\overline{SDCAS}$	160	V_{DD}
5	V_{DDEXT}	57	ADDR2	109	$\overline{SDRAS}$	161	V_{DD}
6	DATA26	58	ADDR1	110	SDCKE	162	V_{DD}
7	DATA25	59	ADDR4	111	$\overline{SDWE}$	163	TDI
8	DATA24	60	ADDR3	112	$\overline{WR}$	164	$\overline{TRST}$
9	DATA23	61	ADDR5	113	SDA10	165	TCK
10	GND	62	GND	114	GND	166	GND
11	V_{DDINT}	63	V_{DD}	115	V_{DDEXT}	167	V_{DD}
12	DATA22	64	GND	116	SDCLK	168	TMS
13	DATA21	65	V_{DDEXT}	117	GND	169	CLK_CFG0
14	DATA20	66	ADDR6	118	V_{DD}	170	BOOTCFG0
15	V_{DDEXT}	67	ADDR7	119	$\overline{RD}$	171	CLK_CFG1
16	GND	68	ADDR8	120	ACK	172	$\overline{EMU}$
17	DATA19	69	ADDR9	121	FLAG3	173	BOOTCFG1
18	DATA18	70	ADDR10	122	FLAG2	174	TDO
19	V_{DDINT}	71	GND	123	FLAG1	175	DAI4
20	GND	72	V_{DD}	124	FLAG0	176	DAI2
21	DATA17	73	GND	125	DAI20	177	DAI3
22	V_{DDINT}	74	V_{DDEXT}	126	GND	178	DAI1
23	GND	75	ADDR11	127	V_{DD}	179	V_{DDEXT}
24	V_{DDINT}	76	ADDR12	128	GND	180	GND
25	GND	77	ADDR13	129	V_{DDEXT}	181	V_{DD}
26	DATA16	78	GND	130	DAI19	182	GND
27	DATA15	79	V_{DD}	131	DAI18	183	DPI14
28	DATA14	80	NC	132	DAI17	184	DPI13
29	DATA13	81	NC	133	DAI16	185	DPI12
30	DATA12	82	GND	134	DAI15	186	DPI11
31	V_{DDEXT}	83	CLKIN	135	DAI14	187	DPI10
32	GND	84	XTAL	136	DAI13	188	DPI9
33	V_{DDINT}	85	V_{DDEXT}	137	DAI12	189	DPI8
34	GND	86	GND	138	V_{DD}	190	DPI7
35	DATA11	87	V_{DD}	139	V_{DDEXT}	191	V_{DDEXT}
36	DATA10	88	ADDR14	140	GND	192	GND
37	DATA9	89	GND	141	V_{DD}	193	V_{DD}
38	DATA8	90	V_{DDEXT}	142	GND	194	GND
39	DATA7	91	ADDR15	143	DAI11	195	DPI6
40	DATA6	92	ADDR16	144	DAI10	196	DPI5
41	V_{DDEXT}	93	ADDR17	145	DAI8	197	DPI4
42	GND	94	ADDR18	146	DAI9	198	DPI3
43	V_{DDINT}	95	GND	147	DAI6	199	DPI1
44	DATA4	96	V_{DDEXT}	148	DAI7	200	DPI2

Table 43. 208-Lead MQFP Pin Assignment (Numerically by Lead Number) (Continued)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
45	DATA5	97	ADDR19	149	DAI5	201	CLKOUT/ ~RESETOUT/ ~RUNRSTIN
46	DATA2	98	ADDR20	150	V_{DDEXT}	202	$\overline{RESET}$
47	DATA3	99	ADDR21	151	GND	203	V_{DDEXT}
48	DATA0	100	ADDR23	152	V_{DD}	204	GND
49	DATA1	101	ADDR22	153	GND	205	DATA30
50	V_{DDEXT}	102	$\overline{MS1}$	154	V_{DD}	206	DATA31
51	GND	103	$\overline{MS0}$	155	GND	207	DATA29
52	V_{DDINT}	104	V_{DD}	156	V_{DD}	208	V_{DD}

OUTLINE DIMENSIONS

The ADSP-21371 is available in a 208-lead Pb-free MQFP package.

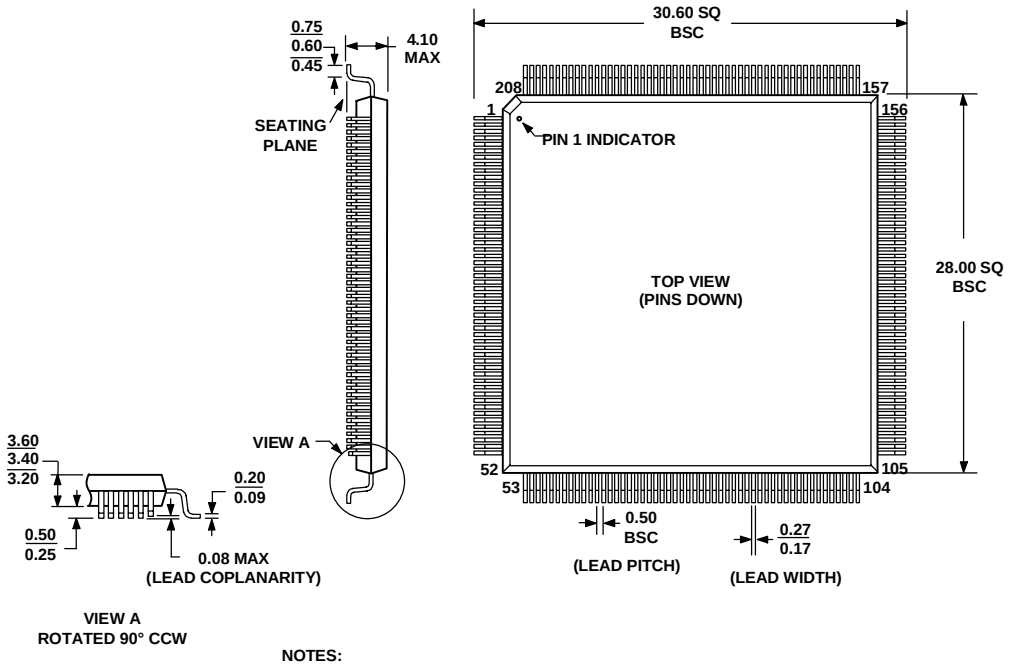


Figure 40. 208-Lead MQFP (S-208-2)

ORDERING GUIDE

Model	Temperature Range[1]	On-Chip SRAM	ROM	Operating Voltage	Package Description	Package Option
ADSP-21371KSZ-2B[2]	0°C to +70°C	1M bit	4M bit	1.2 INT V/3.3 EXT V	208-Lead MQFP	S-208-2
ADSP-21371KSZ-2A[2,3]	0°C to +70°C	1M bit	4M bit	1.2 INT V/3.3 EXT V	208-Lead MQFP	S-208-2

[1] Referenced temperature is ambient temperature.

[2] Z = RoHS Compliant Part

[3] Available with a wide variety of audio algorithm combinations sold as part of a chipset and bundled with necessary software. For a complete list, visit our website at www.analog.com/SHARC

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