

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT377

Octal D-type flip-flop with data enable; positive-edge trigger

Product specification
File under Integrated Circuits, IC06

December 1990

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74HC/HCT377

FEATURES

- Ideal for addressable register applications
- Data enable for address and data synchronization applications
- Eight positive-edge triggered D-type flip-flops
- See “273” for master reset version
- See “373” for transparent latch version
- See “374” for 3-state version
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT377 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT377 have eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. A common clock (CP) input loads all flip-flops simultaneously when the data enable (\bar{E}) is LOW. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop.

The \bar{E} input must be stable only one set-up time prior to the LOW-to-HIGH transition for predictable operation.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^\circ\text{C}$; $t_r = t_f = 6\text{ ns}$

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------|---|--|---------|-----|------|
| | | | HC | HCT | |
| t_{PHL}/t_{PLH} | propagation delay CP to Q_n | $C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$ | 13 | 14 | ns |
| f_{max} | maximum clock frequency | | 77 | 53 | MHz |
| C_I | input capacitance | | 3.5 | 3.5 | pF |
| C_{PD} | power dissipation capacitance per flip-flop | notes 1 and 2 | 20 | 20 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = \text{GND to } V_{CC}$
For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

ORDERING INFORMATION

See “74HC/HCT/HCU/HCMOS Logic Package Information”.

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PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|----------------------------|----------------|---|
| 1 | \bar{E} | data enable input (active LOW) |
| 2, 5, 6, 9, 12, 15, 16, 19 | Q_0 to Q_7 | flip-flop outputs |
| 3, 4, 7, 8, 13, 14, 17, 18 | D_0 to D_7 | data inputs |
| 10 | GND | ground (0 V) |
| 11 | CP | clock input (LOW-to-HIGH, edge-triggered) |
| 20 | V_{CC} | positive supply voltage |

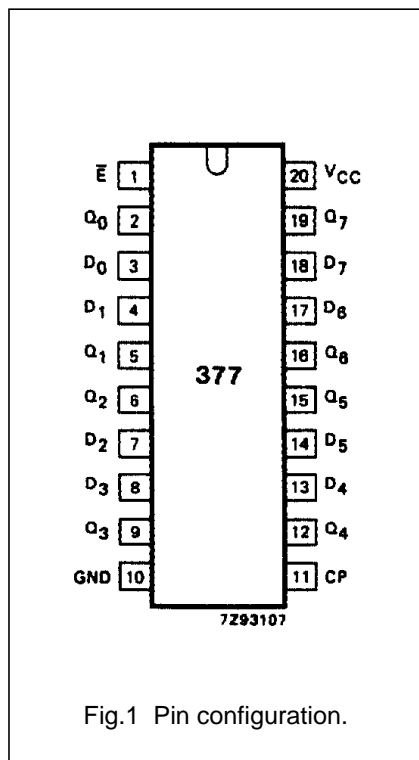


Fig.1 Pin configuration.

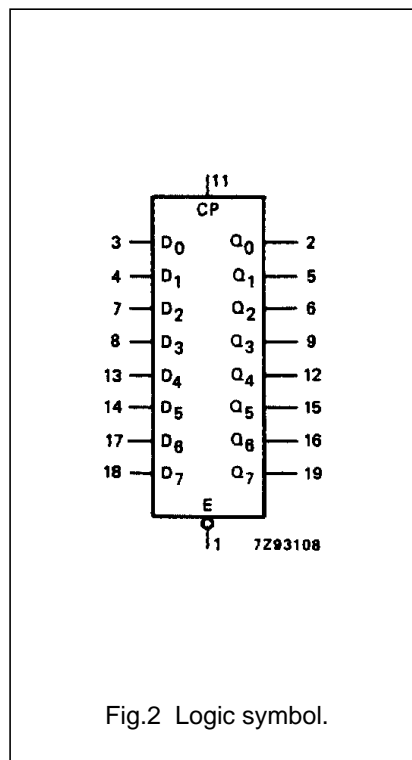


Fig.2 Logic symbol.

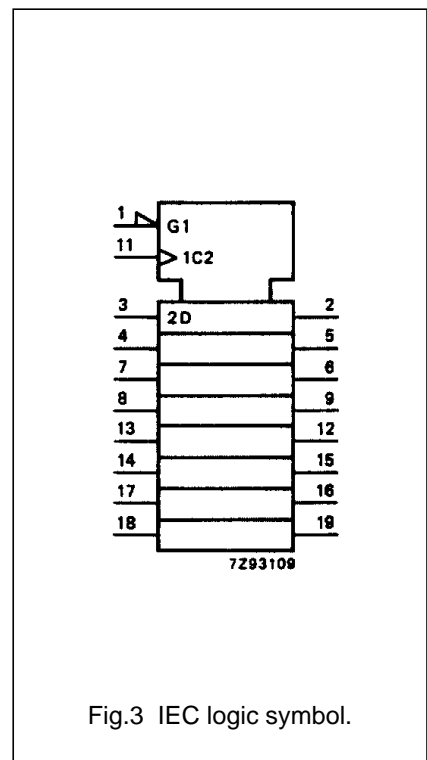


Fig.3 IEC logic symbol.

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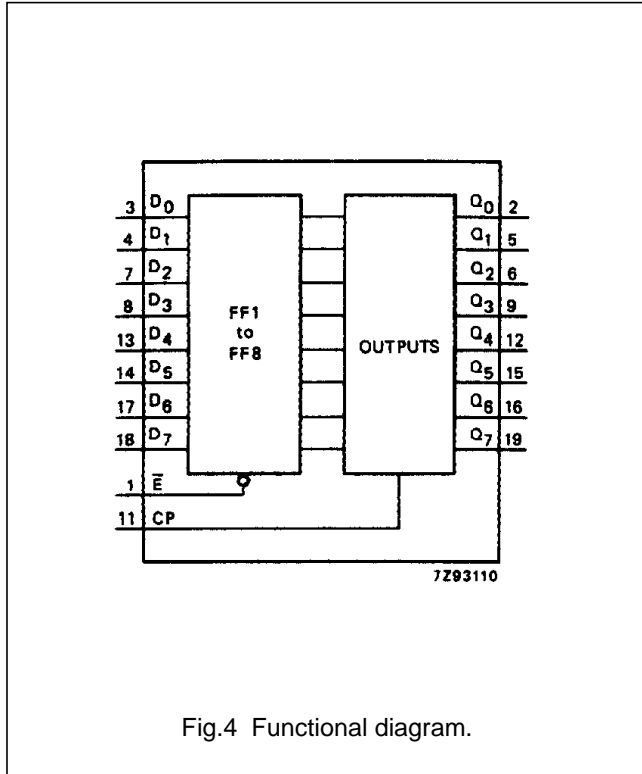


Fig.4 Functional diagram.

FUNCTION TABLE

| OPERATING MODES | INPUTS | | | OUTPUTS |
|-------------------|--------|-----------|-------|-----------|
| | CP | \bar{E} | D_n | Q_n |
| load "1" | ↑ | l | h | H |
| load "0" | ↑ | l | l | L |
| hold (do nothing) | ↑ | h | X | no change |
| | X | H | X | no change |

Notes

- H = HIGH voltage level
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
 L = LOW voltage level
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
 ↑ = LOW-to-HIGH CP transition
 X = don't care

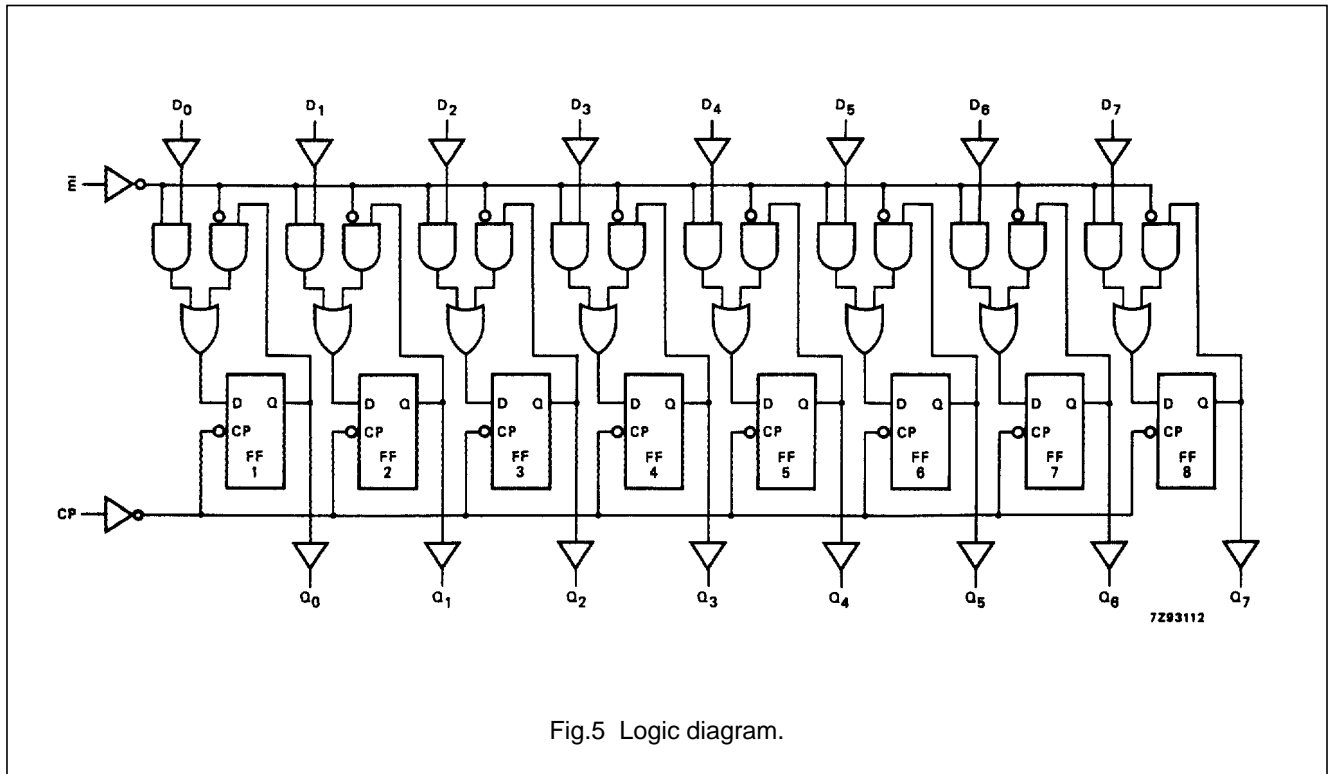


Fig.5 Logic diagram.

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | |
|-------------------------------------|---|-----------------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------------|-------------------|-------|
| | | 74HC | | | | | | | V _{CC} (V) | WAVEFORMS | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | | | | max. |
| t _{PHL} / t _{PLH} | propagation delay CP to Q _n | | 44 16 13 | 160 32 27 | | 200 40 34 | | 240 48 41 | ns | 2.0 4.5 6.0 | Fig.6 |
| t _{THL} / t _{TLH} | output transition time | | 19 7 6 | 75 15 13 | | 95 19 16 | | 110 22 19 | ns | 2.0 4.5 6.0 | Fig.6 |
| t _W | clock pulse width HIGH or LOW | 80 16 14 | 14 5 4 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.6 |
| t _{su} | set-up time D _n to CP | 60 12 10 | 14 5 4 | | 75 15 13 | | 90 18 15 | | ns | 2.0 4.5 6.0 | Fig.7 |
| t _{su} | set-up time \bar{E} to CP | 60 12 10 | 6 2 2 | | 75 15 13 | | 90 18 15 | | ns | 2.0 4.5 6.0 | Fig.7 |
| t _h | hold time D _n to CP | 3 3 3 | -8 -3 -2 | | 3 3 3 | | 3 3 3 | | ns | 2.0 4.5 6.0 | Fig.7 |
| t _h | hold time \bar{E} to CP | 4 4 4 | -3 -1 -1 | | 4 4 4 | | 4 4 4 | | ns | 2.0 4.5 6.0 | Fig.7 |
| f _{max} | maximum clock pulse frequency | 6 30 35 | 23 70 83 | | 5 24 28 | | 4 20 24 | | MHz | 2.0 4.5 6.0 | Fig.6 |

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|----------------|-----------------------|
| \bar{E} | 1.50 |
| CP | 0.50 |
| D _n | 0.20 |

AC CHARACTERISTICS FOR 74HCT

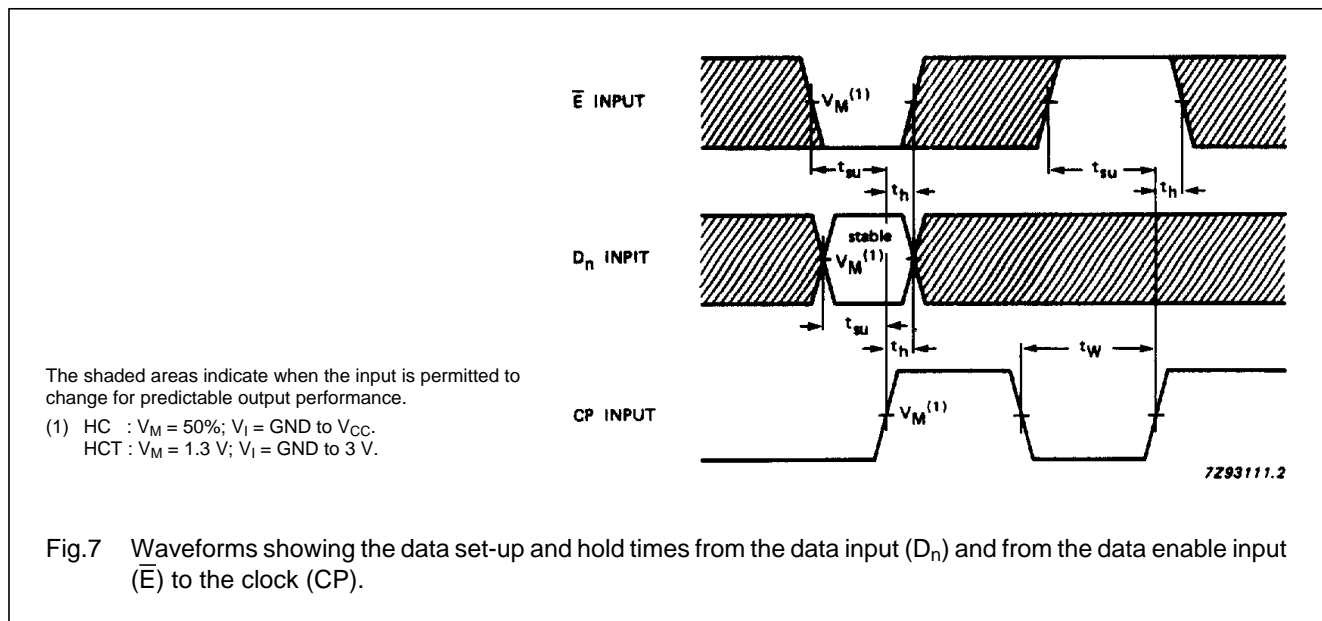
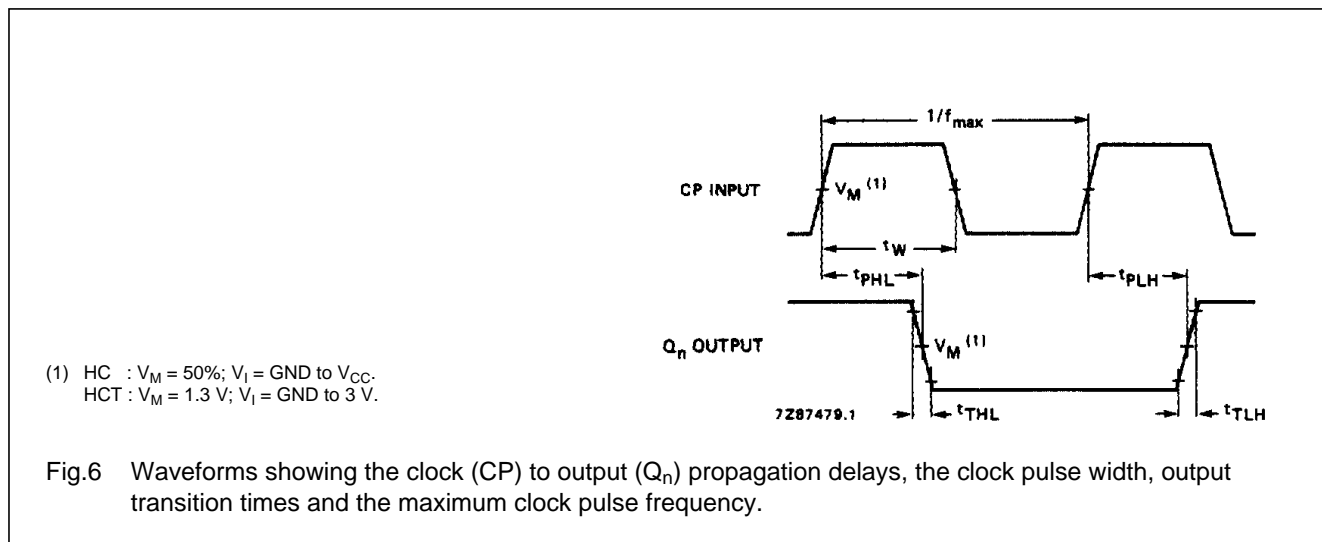
GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | | UNIT | TEST CONDITIONS | |
|-------------------------------------|---|-----------------------|------|------|------------|------|-------------|------|-----|------|------------------------|-----------|
| | | 74HCT | | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | |
| t _{PHL} / t _{PLH} | propagation delay CP to Q _n | | 17 | 32 | | 40 | | 48 | ns | 4.5 | Fig.6 | |
| t _{THL} / t _{TLH} | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | Fig.6 | |
| t _W | clock pulse width HIGH or LOW | 20 | 8 | | 25 | | 30 | | ns | 4.5 | Fig.6 | |
| t _{su} | set-up time D _n to CP | 12 | 4 | | 15 | | 18 | | ns | 4.5 | Fig.7 | |
| t _{su} | set-up time \bar{E} to CP | 22 | 12 | | 28 | | 33 | | ns | 4.5 | Fig.7 | |
| t _h | hold time D _n to CP | 2 | -4 | | 2 | | 2 | | ns | 4.5 | Fig.7 | |
| t _h | hold time \bar{E} to CP | 3 | -2 | | 3 | | 3 | | ns | 4.5 | Fig.7 | |
| f _{max} | maximum clock pulse frequency | 27 | 48 | | 22 | | 18 | | MHz | 4.5 | Fig.6 | |

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".



Стандарт Электрон Связь

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