

## Automotive fully integrated H-bridge motor driver

Datasheet - production data



- Output protected against short to ground and short to  $V_{CC}$
- Standby mode
- Half bridge operation
- Package: ECOPACK®

### Features

| Type      | $R_{DS(on)}$        | $I_{out}$ | $V_{CCmax}$ |
|-----------|---------------------|-----------|-------------|
| VNH7070AY | 72 mΩ typ (per leg) | 20 A      | 38 V        |

- AEC-Q100 qualified
- Output current: 20 A
- 3 V CMOS compatible inputs
- Undervoltage shutdown
- Overvoltage clamp
- Thermal shutdown
- Cross-conduction protection
- Current and power limitation
- Very low standby power consumption
- Protection against loss of ground and loss of  $V_{CC}$
- PWM operation up to 20 KHz
- Multisense monitoring functions
  - Analog motor current feedback
  - Chip temperature monitoring
  - Battery voltage monitoring
- Multisense diagnostic functions
  - Output short to ground detection
  - Thermal shutdown indication
  - OFF-state open-load detection
  - High-side power limitation indication
  - Low-side overcurrent shutdown indication
  - Output short to  $V_{CC}$  detection



### Description

The device is a full bridge motor driver intended for a wide range of automotive applications. The device incorporates a dual monolithic high-side driver and two low-side switches. All switches are designed using STMicroelectronics® well known and proven proprietary VIPower® M0 technology that allows to efficiently integrate on the same die a true Power MOSFET with an intelligent signal/protection circuitry. The three dice are assembled in a PowerSSO-36 package equipped with three exposed islands for optimized dissipation performances. This package is specifically designed for the harsh automotive environment and offers improved thermal performance thanks to exposed die pads. A Multisense\_EN pin is available to enable the MultiSense diagnostic. The input signals  $IN_A$  and  $IN_B$  can directly interface the microcontroller to select the motor direction and the brake condition. Two selection pins (SEL0 and SEL1) are available to address to the microcontroller the information available on the Multisense. The Multisense pin allows to monitor the motor current by delivering a current proportional to the motor current value and provides also the diagnostic feedback according to the implemented truth table. When MultiSense\_EN pin is driven low, MultiSense pin is in high impedance condition. The PWM, up to 20 KHz, allows to control the speed of the motor in all possible conditions. In all cases, a low level state on the PWM pin turns off both the  $LS_A$  and  $LS_B$  switches.

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# 1 Block diagram and pin description

Figure 1. Block diagram

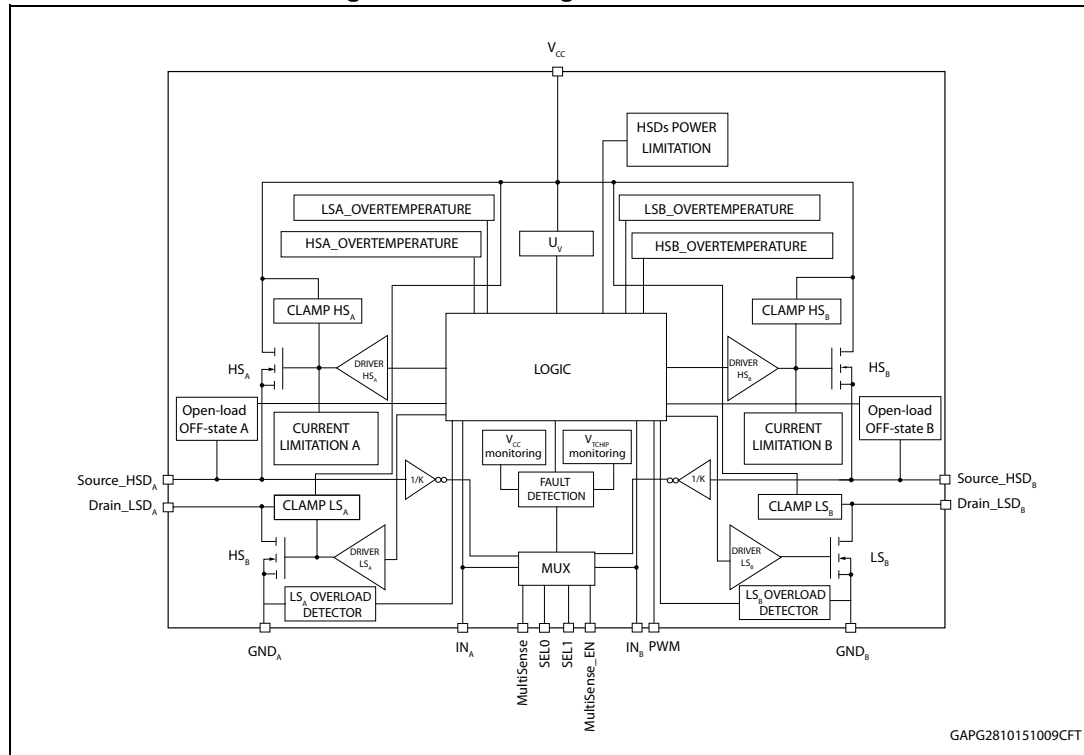


Table 1. Block description

| Name                                              | Description                                                                                                                                               |
|---------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| Logic control                                     | Allows the turn-on and the turn-off of the high-side and the low-side switches according to the truth table.                                              |
| Undervoltage                                      | Shuts down the device for battery voltage below (4 V).                                                                                                    |
| High-side and low-side clamp voltage              | Protect the high-side and the low-side switches from high voltage on the battery line.                                                                    |
| High-side and low-side driver                     | Drive the gate of the concerned switch to allow a proper $R_{DS(on)}$ for the leg of the bridge.                                                          |
| Current limitation                                | Limits the motor current in case of short circuit.                                                                                                        |
| High-side and low-side overtemperature protection | In case of short-circuit with the increase of the junction temperature, it shuts down the concerned driver to prevent degradation and to protect the die. |
| Low-side overcurrent detector                     | Detects when low-side current exceeds shutdown current and latches off the concerned low-side.                                                            |
| Fault detection                                   | Signalizes an abnormal condition of the switch (output shorted to ground or output shorted to battery) by a feedback on the MultiSense                    |
| Power limitation                                  | Limits the power dissipation of the high-side driver inside safe range in case of short to ground condition.                                              |

Table 1. Block description (continued)

| Name                         | Description                                                                      |
|------------------------------|----------------------------------------------------------------------------------|
| Open-load in OFF-state       | Signalize an open-load when the switches are off by a feedback on the MultiSense |
| T <sub>chip</sub> monitoring | Provides a signal linked to the Chip temperature by a feedback on the MultiSense |
| V <sub>CC</sub> monitoring   | Provides a signal linked to the Chip temperature by a feedback on the MultiSense |

Table 2. Suggested connections for unused and not connected pins

| Connection / pin | MultiSense            | N.C. | SOURCE_HSx  | DRAIN_LSx | INPUTx, PWM<br>SELx<br>MultiSense_EN |
|------------------|-----------------------|------|-------------|-----------|--------------------------------------|
| Floating         | Not allowed           | X    | X           | X         | X                                    |
| To ground        | Through 1 kΩ resistor | X    | Not allowed | X         | Through 15 kΩ resistor               |

Figure 2. Configuration diagram (top view)

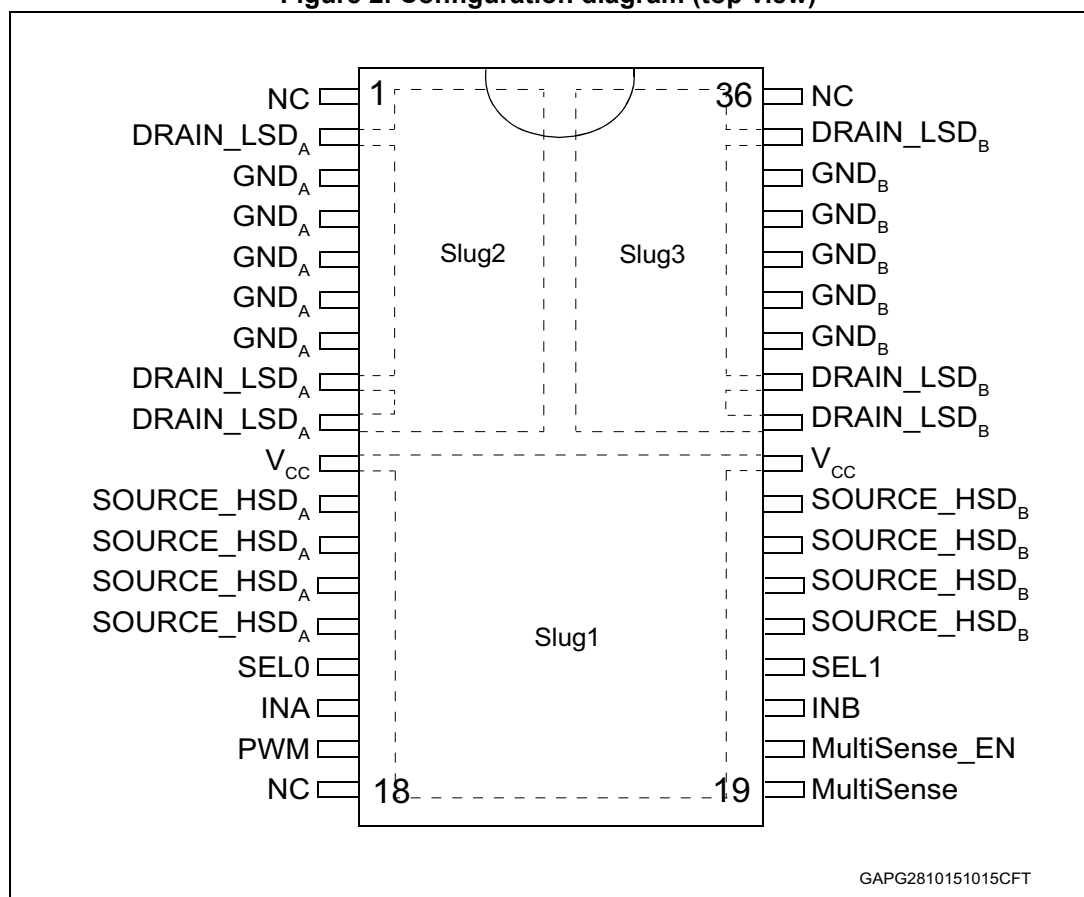


Table 3. Pin definitions and functions

| Pin N°             | Symbol                                 | Function                                              |
|--------------------|----------------------------------------|-------------------------------------------------------|
| 1, 18, 36          | NC                                     | Not connected.                                        |
| 10, 27             | V <sub>CC</sub> , Heat slug1           | Drain of high-side switches and power supply voltage. |
| 16                 | IN <sub>A</sub>                        | Clockwise input.                                      |
| 17                 | PWM                                    | PWM input.                                            |
| 19                 | MultiSense                             | Output of current sense and diagnostic feedback       |
| 20                 | MultiSense_EN                          | Enables the MultiSense diagnostic pin                 |
| 15                 | SEL0                                   | Address the MultiSense multiplexer                    |
| 22                 | SEL1                                   | Address the MultiSense multiplexer                    |
| 21                 | IN <sub>B</sub>                        | Counter clockwise input.                              |
| 28, 29, 35         | Drain_LSD <sub>B</sub> ,<br>Heat Slug3 | Drain of low-side switch B.                           |
| 23, 24, 25, 26     | Source_HSD <sub>B</sub>                | Source of high-side switch B                          |
| 30, 31, 32, 33, 34 | GND <sub>B</sub>                       | Source of low-side switch B.                          |
| 2, 8, 9            | Drain_LSD <sub>A</sub> ,<br>Heat Slug2 | Drain of low-side switch A.                           |
| 11, 12, 13, 14     | Source_HSD <sub>A</sub>                | Source of high-side switch A                          |
| 3, 4, 5, 6, 7      | GND <sub>A</sub>                       | Source of low-side switch A.                          |

Table 4. Pin functions description

| Name                                                                | Description                                                                                                                                                                                                                                                                                                           |
|---------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V <sub>CC</sub>                                                     | Battery connection.                                                                                                                                                                                                                                                                                                   |
| GND                                                                 | Power ground.                                                                                                                                                                                                                                                                                                         |
| Source_LSD <sub>A</sub> ,<br>Source_LSD <sub>B</sub> <sup>(1)</sup> | Power connections to the motor or the bridge configuration: Source HSD <sub>A</sub> and Drain LSD <sub>A</sub> must be externally connected; Source HSD <sub>B</sub> and Drain LSD <sub>B</sub> must be externally connected.                                                                                         |
| IN <sub>A</sub><br>IN <sub>B</sub>                                  | Voltage controlled input pins with hysteresis, CMOS compatible. These two pins control the state of the bridge in normal operation according to the truth table (brake to V <sub>CC</sub> , Brake to GND, clockwise and counterclockwise).                                                                            |
| PWM                                                                 | Voltage controlled input pin with hysteresis, CMOS compatible. This pin turns ON the low-side driver according to the IN <sub>A</sub> and IN <sub>B</sub> settings (see <a href="#">Table 13</a> ). Gates of low-side FETS get modulated by the PWM signal during their on phase allowing speed control of the motor. |
| SEL <sub>0</sub><br>SEL <sub>1</sub>                                | Active high compatible with 3 V and 5 V CMOS output pin; they addresses the Multisense multiplexer                                                                                                                                                                                                                    |

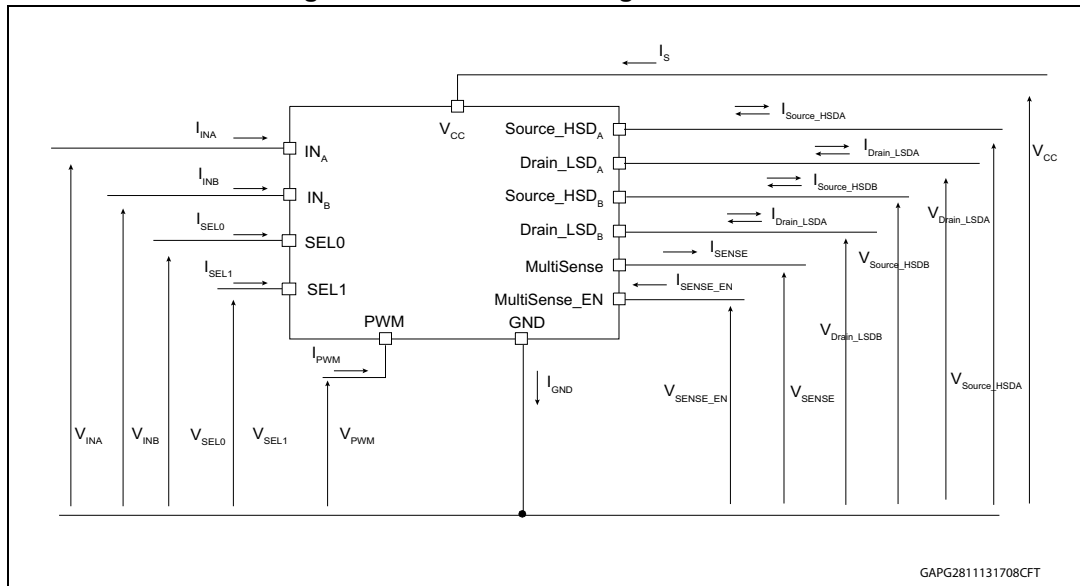
Table 4. Pin functions description (continued)

| Name          | Description                                                                                                                                                                                                                                                                                                                                                                            |
|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MultiSense    | Multiplexed Analog Signal. It delivers a current proportional to the load or a voltage proportional to the $V_{CC}$ voltage or a voltage proportional to the chip temperature whenever the MultiSense_EN is set to high. The desired signal is chosen via SEL0 and SEL1 levels. The MultiSense pin supplies as well a Fault Flag when a fault is detected on the selected path A or B. |
| MultiSense_EN | Active high compatible with 3 V and 5 V CMOS output pin. It enables the MultiSense diagnostic pin.                                                                                                                                                                                                                                                                                     |

1. If the device is used in Bridge configuration we indicate: Source\_HSD<sub>A</sub> = Drain\_LSD<sub>A</sub> = OUT<sub>A</sub>; Source HSD<sub>B</sub> = Drain LSD<sub>B</sub> = OUT<sub>B</sub>; OUT<sub>A</sub> and OUT<sub>B</sub> are the power connections to the motor.

## 2 Electrical specifications

Figure 3. Current and voltage conventions



### 2.1 Absolute maximum ratings

Table 5. Absolute maximum ratings

| Symbol          | Parameter                                                                                     | Value              | Unit |
|-----------------|-----------------------------------------------------------------------------------------------|--------------------|------|
| $V_{CC}$        | Supply voltage                                                                                | 38                 | V    |
| $-V_{CC}$       | Reverse $V_{CC}$ supply voltage                                                               | 0.3                | V    |
| $I_{max}$       | DC output current (continuous)                                                                | Internally limited | A    |
| $I_R$           | Reverse output current (continuous) <sup>(1)</sup>                                            | -16                | A    |
| $V_{CCPK}$      | Maximum transient supply voltage (ISO 16750-2 2010 Test B clamped to 40 V; $R_L = 4 \Omega$ ) | 40                 | V    |
| $V_{CCJS}$      | Maximum jump start voltage for single pulse short circuit protection                          | 28                 | V    |
| $I_{IN}$        | Input current ( $IN_A$ and $IN_B$ pins)                                                       | -1 to 10           | mA   |
| $I_{SEL}$       | $SEL_{0,1}$ DC input current                                                                  |                    |      |
| $I_{PWM}$       | PWM Input current                                                                             |                    |      |
| $I_{SENSE\_EN}$ | MultiSense_EN DC input current                                                                | -1 to 1.5          | mA   |
| $I_{SENSE}$     | CS pin DC output current ( $V_{GND} = V_{CC}$ and $V_{SENSE} < 0$ V)                          | 10                 | mA   |
|                 | CS pin DC output current in reverse ( $V_{CC} < 0$ V)                                         | -20                |      |

Table 5. Absolute maximum ratings (continued)

| Symbol    | Parameter                                                                                   | Value      | Unit |
|-----------|---------------------------------------------------------------------------------------------|------------|------|
| $V_{ESD}$ | Electrostatic discharge (Human body model: $R = 1.5\text{ k}\Omega$ ; $C = 100\text{ pF}$ ) |            |      |
|           | – $IN_A, IN_B$ , PWM                                                                        | 2          | kV   |
|           | – MultiSense, SEL0, SEL1, MultiSense_EN                                                     | 2          |      |
|           | – $V_{CC}$                                                                                  | 4          |      |
|           | – Output                                                                                    | 4          |      |
| $T_c$     | Junction operating temperature                                                              | -40 to 150 | °C   |
| $T_{STG}$ | Storage temperature                                                                         | -55 to 150 | °C   |

1. Based on the internal wires capability.

## 2.2 Thermal data

Table 6. Thermal data

| Symbol         | Parameter                                                       |     | Max. value                        | Unit |
|----------------|-----------------------------------------------------------------|-----|-----------------------------------|------|
| $R_{thj-case}$ | Thermal resistance junction-case (per leg)<br>(JEDEC JESD 51-8) | HSD | 4                                 | °C/W |
|                |                                                                 | LSD | 4.3                               | °C/W |
| $R_{thj-amb}$  | Thermal resistance junction-ambient                             |     | See <a href="#">Section 9.1.1</a> | °C/W |

## 2.3 Electrical characteristics

$V_{CC} = 7\text{ V}$  up to  $28\text{ V}$ ;  $-40\text{ °C} < T_j < 150\text{ °C}$ , unless otherwise specified.

**Table 7. Power section**

| Symbol              | Parameter                                             | Test conditions                                                                                                                                              | Min. | Typ. | Max. | Unit          |
|---------------------|-------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $V_{CC}$            | Operating supply voltage                              |                                                                                                                                                              | 4    |      | 28   | V             |
| $I_S$               | Supply current                                        | Off-state standby $IN_A = IN_B = PWM = 0$ ;<br>$SEL_{0,1} = 0$ ; $T_j = 25\text{ °C}$ ; $V_{CC} = 13\text{ V}$ ;<br>$MultiSense\_EN = 0$                     |      |      | 1    | $\mu\text{A}$ |
|                     |                                                       | Off-state standby <sup>(1)</sup> ;<br>$IN_A = IN_B = PWM = 0$ ; $SEL_{0,1} = 0$ ;<br>$V_{CC} = 13\text{ V}$ ; $T_j = 85\text{ °C}$ ;<br>$MultiSense\_EN = 0$ |      |      | 1    | $\mu\text{A}$ |
|                     |                                                       | Off-state standby; $IN_A = IN_B = PWM = 0$ ;<br>$SEL_{0,1} = 0$ ; $V_{CC} = 13\text{ V}$ ; $T_j = 125\text{ °C}$ ;<br>$MultiSense\_EN = 0$                   |      |      | 3    | $\mu\text{A}$ |
|                     |                                                       | Off-state (no standby)<br>$IN_A = IN_B = PWM = 0$ ; $SEL_{0,1} = 1$ ;<br>$MultiSense\_EN = 0$                                                                |      | 2    | 4    | mA            |
|                     |                                                       | On-state: $IN_A$ or $IN_B = 5\text{ V}$ ; $PWM = 1$ ;<br>$SEL_{0,1} = 0$ ; $MultiSense\_EN = 0$ ; No Load                                                    |      | 3.5  | 6    | mA            |
| $t_{D\_STBY}^{(2)}$ | Standby mode blanking time                            | $V_{CC} = 13\text{ V}$ ;<br>$IN_A = IN_B = MultiSense\_EN = 0\text{ V}$ ;<br>$PWM = SEL_1 = 0\text{ V}$ ;<br>$V_{SEL0}$ from $5\text{ V}$ to $0\text{ V}$ .  | 60   | 300  | 550  | $\mu\text{s}$ |
| $R_{ONHS}$          | Static high-side resistance                           | $I_{OUTx} = 3.5\text{ A}$ ; $T_j = 25\text{ °C}$                                                                                                             |      | 42   |      | m $\Omega$    |
|                     |                                                       | $I_{OUTx} = 3.5\text{ A}$ ;<br>$T_j = -40\text{ °C}$ to $150\text{ °C}$                                                                                      |      |      | 85   | m $\Omega$    |
|                     |                                                       | $V_{CC} = 4\text{ V}$ ; $I_{OUT} = 3.5\text{ A}$ ; $T_j = 25\text{ °C}$                                                                                      |      | 42   |      | m $\Omega$    |
| $R_{ONLS}$          | Static low-side resistance                            | $I_{OUTx} = 3.5\text{ A}$ ; $T_j = 25\text{ °C}$                                                                                                             |      | 30   |      | m $\Omega$    |
|                     |                                                       | $I_{OUTx} = 3.5\text{ A}$ ;<br>$T_j = -40\text{ °C}$ to $150\text{ °C}$                                                                                      |      |      | 60   | m $\Omega$    |
|                     |                                                       | $V_{CC} = 4\text{ V}$ ; $I_{OUT} = 3.5\text{ A}$ ; $T_j = 25\text{ °C}$                                                                                      |      | 30   |      | m $\Omega$    |
| $V_f$               | High-side free-wheeling diode forward voltage         | $I_{OUTx} = -5\text{ A}$ ; $T_j = 150\text{ °C}$                                                                                                             |      | 0.7  | 0.9  | V             |
| $I_{L(off)}$        | Off-State Output current of one leg                   | $T_j = 25\text{ °C}$ ; $V_{CC} = 13\text{ V}$ ; $V_{OUTA} = 0$ or<br>$V_{OUTB} = 0$ ; $IN_A = IN_B = PWM = 0$                                                | 0    |      | 1    | $\mu\text{A}$ |
|                     |                                                       | $T_j = 125\text{ °C}$ ; $V_{CC} = 13\text{ V}$ ; $V_{OUTA} = 0$ or<br>$V_{OUTB} = 0$ ; $IN_A = IN_B = PWM = 0$                                               | 0    |      | 3    | $\mu\text{A}$ |
| $I_{L(off)h}$       | Off-state output current of one leg with other HSD on | $IN_A = PWM = 0$ ; $IN_B = 5\text{ V}$ ; $V_{CC} = 13\text{ V}$ ;<br>$V_{OUTA} = 0$                                                                          | 20   |      | 60   | $\mu\text{A}$ |

- Parameter guaranteed by design and characterization; not subject to production test.
- To power on the device from standby, it is recommended to: toggle  $IN_A$  or  $IN_B$  or  $SEL_0$  or  $SEL_1$  or  $MultiSense\_EN$  from 0 to 1 first to come out from STBY mode; toggle  $PWM$  from 0 to 1 with a delay of  $20\text{ }\mu\text{s}$  this avoids any overstress on the device in case of existing short-to-battery.

Table 8. Logic inputs ( $V_{CC}=7\text{ V}$  up to  $28\text{ V}$ ;  $-40\text{ }^{\circ}\text{C} < T_J < 150\text{ }^{\circ}\text{C}$ )

| Symbol                                                                                                   | Parameter                | Test conditions          | Min. | Typ. | Max. | Unit |
|----------------------------------------------------------------------------------------------------------|--------------------------|--------------------------|------|------|------|------|
| V <sub>IL</sub>                                                                                          | Input low level voltage  |                          |      |      | 0.9  | V    |
| V <sub>IH</sub>                                                                                          | Input high level voltage |                          | 2.1  |      |      | V    |
| V <sub>IHYST</sub>                                                                                       | Input hysteresis voltage |                          | 0.2  |      |      | V    |
| V <sub>ICL</sub>                                                                                         | Input clamp voltage      | I <sub>IN</sub> = 1 mA   | 5.3  |      | 7.2  | V    |
|                                                                                                          |                          | I <sub>IN</sub> = -1 mA  |      | -0.7 |      | V    |
| I <sub>INL</sub>                                                                                         | Input current            | V <sub>IN</sub> = 0.9 V  | 1    |      |      | μA   |
| I <sub>INH</sub>                                                                                         | Input current            | V <sub>IN</sub> = 2.1 V  |      |      | 10   | μA   |
| SEL <sub>0</sub> , SEL <sub>1</sub> (V <sub>CC</sub> = 7 V up to 18 V; -40 °C < T <sub>j</sub> < 150 °C) |                          |                          |      |      |      |      |
| V <sub>SELL</sub>                                                                                        | Input low level voltage  |                          |      |      | 0.9  | V    |
| I <sub>SELL</sub>                                                                                        | Low level input current  | V <sub>SEL</sub> = 0.9 V | 1    |      |      | μA   |
| V <sub>SELH</sub>                                                                                        | Input high level voltage |                          | 2.1  |      |      | V    |
| I <sub>SELH</sub>                                                                                        | High level input current | V <sub>SEL</sub> = 2.1 V |      |      | 10   | μA   |
| V <sub>SEL(hyst)</sub>                                                                                   | Input hysteresis voltage |                          | 0.2  |      |      | V    |
| V <sub>SELCL</sub>                                                                                       | Input clamp voltage      | I <sub>SEL</sub> = 1 mA  | 5.3  |      | 7.2  | V    |
|                                                                                                          |                          | I <sub>SEL</sub> = -1 mA |      | -0.7 |      | V    |
| PWM (V <sub>CC</sub> = 7 V up to 28 V; -40 °C < T <sub>j</sub> < 150 °C)                                 |                          |                          |      |      |      |      |
| V <sub>PWM</sub>                                                                                         | Input low level voltage  |                          |      |      | 0.9  | V    |
| I <sub>PWM</sub>                                                                                         | Low level input current  | V <sub>PWM</sub> = 0.9 V | 1    |      |      | μA   |
| V <sub>PWM</sub>                                                                                         | Input high level voltage |                          | 2.1  |      |      | V    |
| I <sub>PWMH</sub>                                                                                        | High level input current | V <sub>PWM</sub> = 2.1 V |      |      | 10   | μA   |
| V <sub>PWM(hyst)</sub>                                                                                   | Input hysteresis voltage |                          | 0.2  |      |      | V    |
| V <sub>PMWCL</sub>                                                                                       | Input clamp voltage      | I <sub>PWM</sub> = 1 mA  | 5.3  |      | 7.2  | V    |
|                                                                                                          |                          | I <sub>PWM</sub> = -1 mA |      | -0.7 |      | V    |
| SENSE_EN (V <sub>CC</sub> = 7 V up to 18 V; -40 °C < T <sub>j</sub> < 150 °C)                            |                          |                          |      |      |      |      |
| V <sub>SEnL</sub>                                                                                        | Input low level voltage  |                          |      |      | 0.9  | V    |
| I <sub>SEnL</sub>                                                                                        | Low level input current  | V <sub>SEn</sub> = 0.9 V | 1    |      |      | μA   |
| V <sub>SEnH</sub>                                                                                        | Input high level voltage |                          | 2.1  |      |      | V    |
| I <sub>SEnH</sub>                                                                                        | High level input current | V <sub>SEn</sub> = 2.1 V |      |      | 10   | μA   |
| V <sub>SEn(hyst)</sub>                                                                                   | Input hysteresis voltage |                          | 0.2  |      |      | V    |
| V <sub>SEnCL</sub>                                                                                       | Input clump voltage      | I <sub>SEn</sub> = 1 mA  | 5.3  |      | 7.5  | V    |
|                                                                                                          |                          | I <sub>SEn</sub> = -1 mA |      | -0.7 |      | V    |

Table 9. Switching ( $V_{CC} = 13\text{ V}$ ;  $R_{LOAD} = 2.6\ \Omega$ )

| Symbol       | Parameter                   | Test conditions                                                                                                             | Min. | Typ. | Max. | Unit          |
|--------------|-----------------------------|-----------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $f^{(1)}$    | PWM frequency               |                                                                                                                             | 0    |      | 20   | kHz           |
| $t_{d(on)}$  | Turn-on delay time          | Input rise time $< 1\ \mu\text{s}$ ;<br>MultiSense_EN = 5 V (no standby); SEL <sub>0,1</sub> = 0; PWM = 0<br>(see Figure 6) |      | 25   |      | $\mu\text{s}$ |
| $t_{d(off)}$ | Turn-off delay time         | Input rise time $< 1\ \mu\text{s}$ ;<br>MultiSense_EN = 5 V (no standby); SEL <sub>0,1</sub> = 0; PWM = 0<br>(see Figure 6) |      | 15   |      | $\mu\text{s}$ |
| $t_r$        | Rise time                   | See Figure 5                                                                                                                |      | 0.7  | 1.5  | $\mu\text{s}$ |
| $t_f$        | Fall time                   | See Figure 5                                                                                                                |      | 0.2  | 0.5  | $\mu\text{s}$ |
| $t_{cross}$  | Low-side turn-on delay time | See Figure 7                                                                                                                | 40   | 160  | 300  | $\mu\text{s}$ |

1. Parameter guaranteed by design and characterization; not subject to production test.

Table 10. Protections and diagnostics ( $7\text{ V} < V_{CC} < 18\text{ V}$ ;  $-40\text{ }^\circ\text{C} < T_j < 150\text{ }^\circ\text{C}$ )

| Symbol          | Parameter                                                                                  | Test conditions                                                                      | Min. | Typ. | Max. | Unit             |
|-----------------|--------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|------|------|------|------------------|
| $V_{USD}$       | Undervoltage shutdown                                                                      | $V_{CC}$ falling                                                                     |      |      | 4    | V                |
| $V_{USDreset}$  | Undervoltage shutdown reset                                                                | $V_{CC}$ rising                                                                      |      |      | 5    | V                |
| $V_{USDhyst}$   | Undervoltage shutdown hysteresis                                                           |                                                                                      |      | 0.3  |      | V                |
| $I_{LIM\_HSD}$  | High-side current limitation                                                               | $V_{CC} = 13\text{ V}$                                                               | 20   | 29   | 40   | A                |
|                 |                                                                                            | $4\text{ V} < V_{CC} < 18\text{ V}$                                                  |      |      | 40   | A                |
| $I_{SD\_LSD}$   | Shutdown LS current                                                                        |                                                                                      | 25   | 38   | 54   | A                |
| $t_{SD\_LSD}$   | Time to shutdown for the low-side                                                          | IN <sub>A</sub> = IN <sub>B</sub> = 0; PWM = 5 V (see Figure 8)                      |      | 5    |      | $\mu\text{s}$    |
| $V_{CL\_HSD}$   | High-side clamp voltage ( $V_{CC}$ to OUT <sub>A</sub> = 0 or OUT <sub>B</sub> = 0)        | I <sub>OUT</sub> = 100 mA; t <sub>clamp</sub> = 1 ms;<br>I <sub>clamp</sub> = 100 mA | 38   | 46   |      | V                |
| $V_{CL\_LSD}$   | Low-side clamp voltage (OUT <sub>A</sub> = $V_{CC}$ or OUT <sub>B</sub> = $V_{CC}$ to GND) | I <sub>OUT</sub> = 100 mA; t <sub>clamp</sub> = 1 ms;<br>I <sub>clamp</sub> = 100 mA | 38   | 46   |      | V                |
| $T_{TSD\_HSD}$  | High-side thermal shutdown temperature                                                     | IN <sub>x</sub> = 2.1 V                                                              | 150  | 175  | 200  | $^\circ\text{C}$ |
| $T_{TR\_HSD}$   | High-side thermal reset temperature                                                        |                                                                                      | 135  |      |      | $^\circ\text{C}$ |
| $T_{HYST\_HSD}$ | High-side thermal hysteresis ( $T_{TSD\_HSD} - T_{TR\_HSD}$ )                              |                                                                                      |      | 7    |      | $^\circ\text{C}$ |
| $T_{TSD\_LSD}$  | Low-side thermal shutdown temperature                                                      | IN <sub>x</sub> = 0 V, PWM = 5 V                                                     | 150  | 175  | 200  | $^\circ\text{C}$ |

Table 10. Protections and diagnostics (7 V < V<sub>CC</sub> < 18 V; -40 °C < T<sub>j</sub> < 150 °C) (continued)

| Symbol                                   | Parameter                                                                                  | Test conditions                                                                                                                                                                                                                                                  | Min. | Typ. | Max. | Unit |
|------------------------------------------|--------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| V <sub>CL</sub>                          | Total clamp voltage (V <sub>CC</sub> to GND)                                               | I <sub>OUT</sub> = 100 mA; t <sub>clamp</sub> = 1 ms;<br>I <sub>clamp</sub> = 100 mA                                                                                                                                                                             | 38   | 46   | 52   | V    |
| V <sub>OL</sub>                          | OFF-state open-load voltage detection threshold                                            | IN <sub>A</sub> = IN <sub>B</sub> = 0; PWM = 0;<br>MultiSense_EN = 5 V;<br>V <sub>SEL0</sub> = 5 V;<br>V <sub>SEL1</sub> = 0 V for CHA;<br>V <sub>SEL0</sub> = 0 V;<br>V <sub>SEL1</sub> = 0 V for CHB                                                           | 2    | 3    | 4    | V    |
| I <sub>L(off2)</sub>                     | OFF-state output sink current                                                              | IN <sub>A</sub> = IN <sub>B</sub> = 0; V <sub>OUTx</sub> = V <sub>OL</sub> ;<br>PWM = 0; MultiSense_EN = 5 V;<br>SEL <sub>0</sub> = 1; SEL <sub>1</sub> = 0 for CHA;<br>SEL <sub>0</sub> = 0; SEL <sub>1</sub> = 0 for CHB                                       | -100 |      | -15  | μA   |
| ΔT <sub>LSD</sub> <sup>(1)</sup>         | Dynamic temperature                                                                        |                                                                                                                                                                                                                                                                  |      | 60   |      | °C   |
| t <sub>DSTKON</sub>                      | OFF-state diagnostic delay time from falling edge of INPUT (see <a href="#">Figure 4</a> ) | V <sub>INA</sub> = 5 V to 0 V; IN <sub>B</sub> = 0;<br>PWM = 0; V <sub>SEL0</sub> = 5 V;<br>V <sub>SEL1</sub> = 0 V; SENSE_EN = 1;<br>I <sub>OUTA</sub> = 0 A; V <sub>OUTA</sub> = 4 V                                                                           | 40   | 160  | 300  | μs   |
| t <sub>D_VOL</sub>                       | OFF-state diagnostic delay time from rising edge of V <sub>OUT</sub>                       | IN <sub>A</sub> = IN <sub>B</sub> = 0; PWM = 0;<br>V <sub>SENSE_EN</sub> = 5 V; V <sub>OUTx</sub> = 0 V to 4 V;<br>SEL <sub>0</sub> = 1; SEL <sub>1</sub> = 0 for CHA;<br>SEL <sub>0</sub> = 0; SEL <sub>1</sub> = 0 for CHB<br>(see <a href="#">Figure 11</a> ) |      | 5    | 30   | μs   |
| t <sub>Latch_RST_HD</sub> <sup>(1)</sup> | Input reset time for high-side fault unlatch                                               | V <sub>INx</sub> = 5 V to 0 V; H <sub>SDx</sub> faulting<br>(see <a href="#">Figure 9</a> )                                                                                                                                                                      | 3    | 10   | 20   | μs   |
| t <sub>Latch_RST_LS</sub> <sup>(1)</sup> | Input reset time for low-side fault unlatch                                                | V <sub>INx</sub> = 0 V to 5 V; L <sub>SDx</sub> faulting<br>(see <a href="#">Figure 10</a> )                                                                                                                                                                     | 3    | 10   | 20   | μs   |

1. Parameter guaranteed by design and characterization; not subject to production test.

Table 11. MultiSense (7 V < V<sub>CC</sub> < 18 V; -40 °C < T<sub>j</sub> < 150 °C)

| Symbol                                           | Parameter                            | Test conditions                                                                                                                                                                                                                                                                                                                                           | Min. | Typ. | Max. | Unit |
|--------------------------------------------------|--------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| V <sub>SENSE_CL</sub>                            | MultiSense clamp voltage             | V <sub>SEN</sub> = 0 V; I <sub>SENSE</sub> = -1 mA                                                                                                                                                                                                                                                                                                        |      | 7    |      | V    |
|                                                  |                                      | V <sub>SEN</sub> = 0 V; I <sub>SENSE</sub> = 1 mA                                                                                                                                                                                                                                                                                                         | -17  |      | -12  | V    |
| K <sub>OL</sub>                                  | I <sub>OUT</sub> /I <sub>SENSE</sub> | I <sub>OUTx</sub> = 0.05 A; V <sub>SENSE</sub> = 0.5 V;<br>V <sub>SENSE_EN</sub> = 5 V;<br>T <sub>j</sub> = -40 °C to 150 °C                                                                                                                                                                                                                              | 665  | 1900 |      |      |
| K <sub>0</sub>                                   | I <sub>OUT</sub> /I <sub>SENSE</sub> | I <sub>OUTx</sub> = 0.2 A; V <sub>SENSE</sub> = 0.5 V;<br>V <sub>SENSE_EN</sub> = 5 V;<br>T <sub>j</sub> = -40 °C to 150 °C                                                                                                                                                                                                                               | 1083 | 1900 | 2716 |      |
| K <sub>1</sub>                                   | I <sub>OUT</sub> /I <sub>SENSE</sub> | I <sub>OUTx</sub> = 3.5 A; V <sub>SENSE</sub> = 4 V;<br>V <sub>SENSE_EN</sub> = 5 V;<br>T <sub>j</sub> = -40 °C to 150 °C                                                                                                                                                                                                                                 | 1420 | 1680 | 1940 |      |
| K <sub>2</sub>                                   | I <sub>OUT</sub> /I <sub>SENSE</sub> | I <sub>OUTx</sub> = 5.5 A; V <sub>SENSE</sub> = 4 V;<br>V <sub>SENSE_EN</sub> = 5 V;<br>T <sub>j</sub> = -40 °C to 150 °C                                                                                                                                                                                                                                 | 1480 | 1690 | 1900 |      |
| dK <sub>OL</sub> /K <sub>OL</sub> <sup>(1)</sup> | Analog sense current drift           | I <sub>OUTx</sub> = 0.05 A; V <sub>SENSE</sub> = 0.5 V;<br>V <sub>SENSE_EN</sub> = 5 V;<br>T <sub>j</sub> = -40 °C to 150 °C                                                                                                                                                                                                                              | -25  |      | 25   | %    |
| dK <sub>0</sub> /K <sub>0</sub> <sup>(1)</sup>   | Analog sense current drift           | I <sub>OUTx</sub> = 0.2 A; V <sub>SENSE</sub> = 0.5 V;<br>V <sub>SENSE_EN</sub> = 5 V;<br>T <sub>j</sub> = -40 °C to 150 °C                                                                                                                                                                                                                               | -21  |      | 21   | %    |
| dK <sub>1</sub> /K <sub>1</sub> <sup>(1)</sup>   | Analog sense current drift           | I <sub>OUTx</sub> = 3.5 A; V <sub>SENSE</sub> = 4 V;<br>V <sub>SENSE_EN</sub> = 5 V;<br>T <sub>j</sub> = -40 °C to 150 °C                                                                                                                                                                                                                                 | -5   |      | 5    | %    |
| dK <sub>2</sub> /K <sub>2</sub> <sup>(1)</sup>   | Analog sense current drift           | I <sub>OUTx</sub> = 5.5 A; V <sub>SENSE</sub> = 4 V;<br>V <sub>SENSE_EN</sub> = 5 V;<br>T <sub>j</sub> = -40 °C to 150 °C                                                                                                                                                                                                                                 | -4   |      | 4    | %    |
| I <sub>SENSE0</sub>                              | MultiSense leakage current           | IN <sub>A</sub> = IN <sub>B</sub> = PWM = 0 V;<br>SEL <sub>0</sub> = SEL <sub>0</sub> = SEN = 0 V; T <sub>j</sub> = -40 °C to 150 °C (standby)                                                                                                                                                                                                            | 0    |      | 0.5  | μA   |
|                                                  |                                      | SEN = 5 V; IN <sub>A</sub> = IN <sub>B</sub> = 5 V;<br>PWM = 0 V; legX diagnostic selected; I <sub>OUTx</sub> = 0 A<br>E.g.<br>– LegA: SEL <sub>0</sub> = 5 V; SEL <sub>1</sub> = 0 V;<br>I <sub>OUTA</sub> = 0 A; I <sub>OUTB</sub> = 5 A<br>– LegB: SEL <sub>0</sub> = 0 V; SEL <sub>1</sub> = 0 V;<br>I <sub>OUTA</sub> = 5 A; I <sub>OUTB</sub> = 0 V | 0    |      | 5    | μA   |
|                                                  |                                      | SEN = 5 V; PWM = 0 V; legX diagnostic selected; HSx OFF<br>E.g.:<br>– LegA: SEL <sub>0</sub> = 5 V; SEL <sub>1</sub> = 0 V;<br>IN <sub>A</sub> = 0 V; IN <sub>B</sub> = 5 V; I <sub>OUTB</sub> = 5 A<br>– LegB: SEL <sub>0</sub> = 0 V; SEL <sub>1</sub> = 0 V;<br>IN <sub>A</sub> = 5 V; IN <sub>B</sub> = 0 V; I <sub>OUTA</sub> = 5 A                  | 0    |      | 5    | μA   |

Table 11. MultiSense (7 V < V<sub>CC</sub> < 18 V; -40 °C < T<sub>j</sub> < 150 °C) (continued)

| Symbol                                         | Parameter                                                                | Test conditions                                                                                                                                                                                                                                           | Min.  | Typ.  | Max.  | Unit |
|------------------------------------------------|--------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|-------|------|
| V <sub>SENSEH</sub>                            | MultiSense output voltage in fault condition                             | V <sub>CC</sub> = 13 V; R <sub>SENSE</sub> = 1 kΩ;<br>V <sub>SEn</sub> = 5 V<br>– E.g: OUT <sub>A</sub> in open-load;<br>V <sub>INA</sub> = 0 V; V <sub>SEL0</sub> = 5 V;<br>V <sub>SEL1</sub> = 0 V; I <sub>OUTA</sub> = 0 A;<br>V <sub>OUTA</sub> = 4 V | 5     |       | 7     | V    |
| V <sub>OUT_MSD</sub> <sup>(1)</sup>            | Output Voltage for MultiSense shutdown                                   | V <sub>INA</sub> = 5 V; V <sub>INB</sub> = 0 V; V <sub>SEn</sub> = 5 V;<br>V <sub>SEL0</sub> = 5 V; V <sub>SEL1</sub> = 0 V;<br>R <sub>SENSE</sub> = 2.7 kΩ I <sub>OUTx</sub> = 5 A                                                                       |       | 5     |       | V    |
| V <sub>SENSE_SAT</sub>                         | MultiSense saturation voltage                                            | V <sub>CC</sub> = 7 V; V <sub>SEn</sub> = 5 V;<br>R <sub>SENSE</sub> = 10 kΩ; V <sub>INA</sub> = 5 V;<br>V <sub>INB</sub> = 0 V; I <sub>OUTA</sub> = 5.5 A;<br>V <sub>SEL0</sub> = 5 V; V <sub>SEL1</sub> = 0 V;<br>T <sub>j</sub> = 150 °C               | 5     |       |       | V    |
| I <sub>SENSE_SAT</sub> <sup>(1)</sup>          | MultiSense saturation current                                            | V <sub>CC</sub> = 13 V; V <sub>SENSE</sub> = 4 V;<br>V <sub>SEn</sub> = 5 V; V <sub>INA</sub> = 5 V; V <sub>INB</sub> = 0 V;<br>V <sub>SEL0</sub> = 5 V; V <sub>SEL1</sub> = 0 V;<br>T <sub>j</sub> = 150 °C                                              | 4.6   |       |       | mA   |
| I <sub>OUT_SAT</sub> <sup>(1)</sup>            | Output saturation current                                                | V <sub>CC</sub> = 13 V; V <sub>SENSE</sub> = 4 V;<br>V <sub>SEn</sub> = 5 V; V <sub>INA</sub> = 5 V; V <sub>INB</sub> = 0 V;<br>V <sub>SEL0</sub> = 5 V; V <sub>SEL1</sub> = 0 V;<br>T <sub>j</sub> = 150 °C                                              | 8.7   |       |       | A    |
| I <sub>SENSEH</sub>                            | MultiSense current in fault condition                                    | 9 V < V <sub>CC</sub> < 18 V; V <sub>SENSE</sub> = 5 V;<br>MultiSense in fault condition                                                                                                                                                                  | 10    | 20    | 30    | mA   |
| Chip temperature analog feedback               |                                                                          |                                                                                                                                                                                                                                                           |       |       |       |      |
| V <sub>SENSE_TC</sub>                          | MultiSense output voltage proportional to chip temperature               | V <sub>SENSE_EN</sub> = 5 V; V <sub>SEL0</sub> = 0 V;<br>V <sub>SEL1</sub> = 5 V; V <sub>INA</sub> = V <sub>INB</sub> = 0 V;<br>R <sub>SENSE</sub> = 1 kΩ; T <sub>j</sub> = -40 °C                                                                        | 2.277 | 2.371 | 2.465 | V    |
|                                                |                                                                          | V <sub>SENSE_EN</sub> = 5 V; V <sub>SEL0</sub> = 0 V;<br>V <sub>SEL1</sub> = 5 V; V <sub>INA</sub> = V <sub>INB</sub> = 0 V;<br>R <sub>SENSE</sub> = 1 kΩ; T <sub>j</sub> = 25 °C                                                                         | 1.948 | 2.033 | 2.119 | V    |
|                                                |                                                                          | V <sub>SENSE_EN</sub> = 5 V; V <sub>SEL0</sub> = 0 V;<br>V <sub>SEL1</sub> = 5 V; V <sub>INA</sub> = V <sub>INB</sub> = 0 V;<br>R <sub>SENSE</sub> = 1 kΩ; T <sub>j</sub> = 125 °C                                                                        | 1.401 | 1.486 | 1.572 | V    |
| dV <sub>SENSE_TC</sub> /dT <sub>(1)</sub>      | Temperature coefficient                                                  | T <sub>j</sub> = -40 °C to 150 °C                                                                                                                                                                                                                         |       | -5.5  |       | mV/K |
| Transfer function                              |                                                                          | V <sub>SENSE_TC</sub> (T) = V <sub>SENSE_TC</sub> (T <sub>0</sub> ) + dV <sub>SENSE_TC</sub> /dT * (T - T <sub>0</sub> )                                                                                                                                  |       |       |       |      |
| V <sub>CC</sub> supply voltage analog feedback |                                                                          |                                                                                                                                                                                                                                                           |       |       |       |      |
| V <sub>SENSE_VCC</sub>                         | MultiSense output voltage proportional to V <sub>CC</sub> supply voltage | V <sub>CC</sub> = 13 V; V <sub>SENSE_EN</sub> = 5 V;<br>V <sub>SEL0</sub> = V <sub>SEL1</sub> = 5 V;<br>R <sub>SENSE</sub> = 1 kΩ                                                                                                                         | 3.16  | 3.23  | 3.3   | V    |
| Transfer function                              |                                                                          | V <sub>SENSE_VCC</sub> = V <sub>CC</sub> /4                                                                                                                                                                                                               |       |       |       |      |

Table 11. MultiSense (7 V < V<sub>CC</sub> < 18 V; -40 °C < T<sub>j</sub> < 150 °C) (continued)

| Symbol                                                                 | Parameter                                                                      | Test conditions                                                                                                                                                                                                                            | Min. | Typ. | Max. | Unit |
|------------------------------------------------------------------------|--------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| <b>MultiSense timings (Multiplexer transition times)<sup>(2)</sup></b> |                                                                                |                                                                                                                                                                                                                                            |      |      |      |      |
| t <sub>D_AtoB</sub>                                                    | Multisense transition delay from legA to legB                                  | V <sub>INA</sub> = 5 V to 0 V,<br>V <sub>INB</sub> = 5 V<br>V <sub>sense_EN</sub> = 5 V<br>V <sub>sel0</sub> = 5 V to 0 V<br>V <sub>sel1</sub> = 0 V<br>R <sub>sense</sub> = 1 kΩ<br>I <sub>OUTA</sub> = 150 mA<br>I <sub>OUTB</sub> = 6 A |      |      | 20   | μs   |
| t <sub>D_BtoA</sub>                                                    | Multisense transition delay from legB to legA                                  | V <sub>INB</sub> = 5 V to 0 V,<br>V <sub>INA</sub> = 5 V<br>V <sub>sense_EN</sub> = 5 V<br>V <sub>sel0</sub> = 0 V to 5 V<br>V <sub>sel1</sub> = 0 V<br>R <sub>sense</sub> = 1 kΩ<br>I <sub>OUTB</sub> = 150 mA<br>I <sub>OUTA</sub> = 6 A |      |      | 20   | μs   |
| t <sub>D_CStoTC</sub>                                                  | MultiSense transition delay from current sense to T <sub>C</sub> sense         | V <sub>INA</sub> = 5 V; V <sub>SENSE_EN</sub> = 5 V;<br>V <sub>SEL0</sub> = 5 V to 0 V;<br>V <sub>SEL1</sub> = 0 V to 5 V; I <sub>OUTA</sub> = 2.5 A;<br>R <sub>SENSE</sub> = 1 kΩ;                                                        |      |      | 60   | μs   |
| t <sub>D_TCtoCS</sub>                                                  | MultiSense transition delay from T <sub>C</sub> sense to current sense         | V <sub>INA</sub> = 5 V; V <sub>SENSE_EN</sub> = 5 V;<br>V <sub>SEL0</sub> = 0 V to 5 V;<br>V <sub>SEL1</sub> = 5 V to 0 V; I <sub>OUTA</sub> = 2.5 A;<br>R <sub>SENSE</sub> = 1 kΩ;                                                        |      |      | 20   | μs   |
| t <sub>D_CStoVCC</sub>                                                 | MultiSense transition delay from current sense to V <sub>CC</sub> sense        | V <sub>INA</sub> = 5 V; V <sub>SENSE_EN</sub> = 5 V;<br>V <sub>SEL0</sub> = 5 V; V <sub>SEL1</sub> = 0 V to 5 V;<br>I <sub>OUTA</sub> = 2.5 A; R <sub>SENSE</sub> = 1 kΩ;                                                                  |      |      | 60   | μs   |
| t <sub>D_VCCtoCS</sub>                                                 | MultiSense transition delay from V <sub>CC</sub> sense to current sense        | V <sub>INA</sub> = 5 V; V <sub>SENSE_EN</sub> = 5 V;<br>V <sub>SEL0</sub> = 5 V; V <sub>SEL1</sub> = 5 V to 0 V;<br>I <sub>OUTA</sub> = 2.5 A; R <sub>SENSE</sub> = 1 kΩ;                                                                  |      |      | 20   | μs   |
| t <sub>D_TCtoVCC</sub>                                                 | MultiSense transition delay from T <sub>C</sub> sense to V <sub>CC</sub> sense | V <sub>CC</sub> = 13 V; T <sub>j</sub> = 125 °C;<br>V <sub>SENSE_EN</sub> = 5 V;<br>V <sub>SEL0</sub> = 0 V to 5 V;<br>V <sub>SEL1</sub> = 5 V; R <sub>SENSE</sub> = 1 kΩ;                                                                 |      |      | 20   | μs   |
| t <sub>D_VCCtoTC</sub>                                                 | MultiSense transition delay from V <sub>CC</sub> sense to T <sub>C</sub> sense | V <sub>CC</sub> = 13 V; T <sub>j</sub> = 125 °C;<br>V <sub>SENSE_EN</sub> = 5 V;<br>V <sub>SEL0</sub> = 5 V to 0 V;<br>V <sub>SEL1</sub> = 5 V; R <sub>SENSE</sub> = 1 kΩ;                                                                 |      |      | 20   | μs   |
| <b>MultiSense timings (CurrentSense mode)</b>                          |                                                                                |                                                                                                                                                                                                                                            |      |      |      |      |
| t <sub>DSense1H</sub>                                                  | Current sense settling time from rising edge of V <sub>SENSE_EN</sub>          | V <sub>INA</sub> = 5 V; V <sub>INB</sub> = 0 V;<br>V <sub>SENSE_EN</sub> = 0 V to 5 V;<br>R <sub>SENSE</sub> = 1 kΩ; R <sub>L</sub> = 2.6 Ω;<br>V <sub>PWM</sub> = 5 V; V <sub>SEL0</sub> = 5 V;<br>V <sub>SEL1</sub> = 0 V                |      |      | 60   | μs   |

Table 11. MultiSense (7 V < V<sub>CC</sub> < 18 V; -40 °C < T<sub>j</sub> < 150 °C) (continued)

| Symbol                                                       | Parameter                                                                      | Test conditions                                                                                                                                                                                                             | Min. | Typ. | Max. | Unit |
|--------------------------------------------------------------|--------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| t <sub>DSENSE1L</sub>                                        | Current sense disable delay time from falling edge of V <sub>SENSE_EN</sub>    | V <sub>INA</sub> = 5 V; V <sub>INB</sub> = 0 V;<br>V <sub>SENSE_EN</sub> = 5 V to 0 V;<br>R <sub>SENSE</sub> = 1 kΩ; R <sub>L</sub> = 2.6 Ω;<br>V <sub>PWM</sub> = 5 V; V <sub>SEL0</sub> = 5 V;<br>V <sub>SEL1</sub> = 0 V |      |      | 20   | μs   |
| <b>MultiSense timings (chip temperature sense mode)</b>      |                                                                                |                                                                                                                                                                                                                             |      |      |      |      |
| t <sub>DSENSE2H</sub>                                        | V <sub>SENSE_TC</sub> setting time from rising edge of V <sub>SENSE_EN</sub>   | V <sub>SENSE_EN</sub> = 0 V to 5 V;<br>V <sub>SEL0</sub> = 0 V; V <sub>SEL1</sub> = 5 V;<br>R <sub>SENSE</sub> = 1 kΩ                                                                                                       |      |      | 60   | μs   |
| t <sub>DSENSE2L</sub>                                        | V <sub>SENSE_TC</sub> setting time from falling edge of V <sub>SENSE_EN</sub>  | V <sub>SENSE_EN</sub> = 5 V to 0 V;<br>V <sub>SEL0</sub> = 0 V; V <sub>SEL1</sub> = 5 V;<br>R <sub>SENSE</sub> = 1 kΩ                                                                                                       |      |      | 20   | μs   |
| <b>MultiSense timing (V<sub>CC</sub> voltage sense mode)</b> |                                                                                |                                                                                                                                                                                                                             |      |      |      |      |
| t <sub>DSENSE3H</sub>                                        | V <sub>SENSE_VCC</sub> setting time from rising edge of V <sub>SENSE_EN</sub>  | V <sub>SENSE_EN</sub> = 0 V to 5 V;<br>V <sub>SEL0</sub> = 5 V; V <sub>SEL1</sub> = 5 V;<br>R <sub>SENSE</sub> = 1 kΩ                                                                                                       |      |      | 60   | μs   |
| t <sub>DSENSE3L</sub>                                        | V <sub>SENSE_VCC</sub> setting time from falling edge of V <sub>SENSE_EN</sub> | V <sub>SENSE_EN</sub> = 5 V to 0 V;<br>V <sub>SEL0</sub> = 5 V; V <sub>SEL1</sub> = 5 V;<br>R <sub>SENSE</sub> = 1 kΩ                                                                                                       |      |      | 20   | μs   |

1. Parameter guaranteed by design and characterization; not subject to production test.
2. Transition delay are measured up to +/- 10% of final conditions.

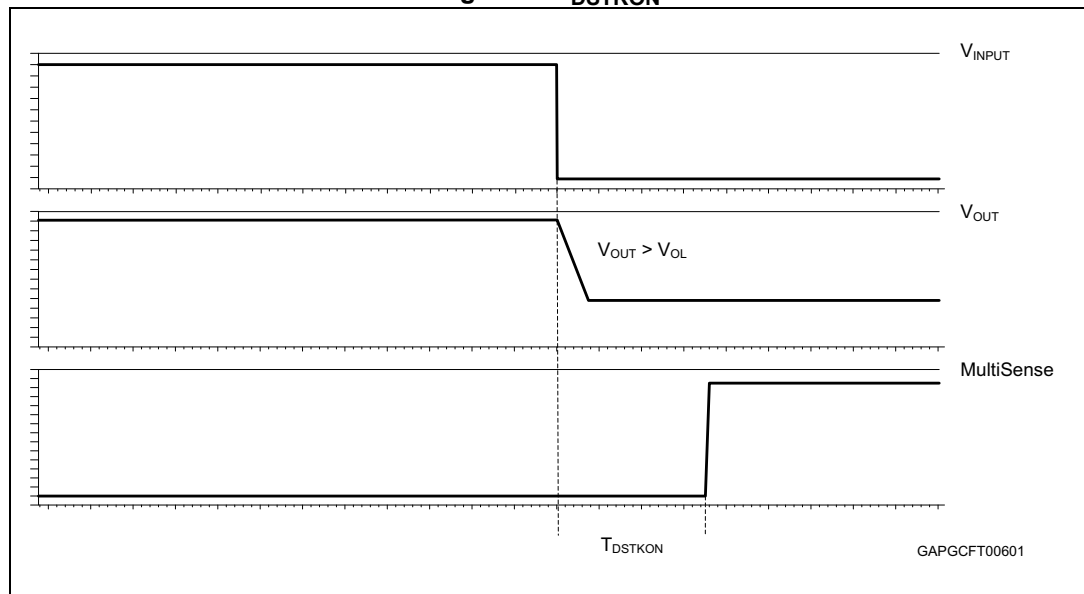
Figure 4. T<sub>DSTKON</sub>

Figure 5. Definition of the low-side switching times

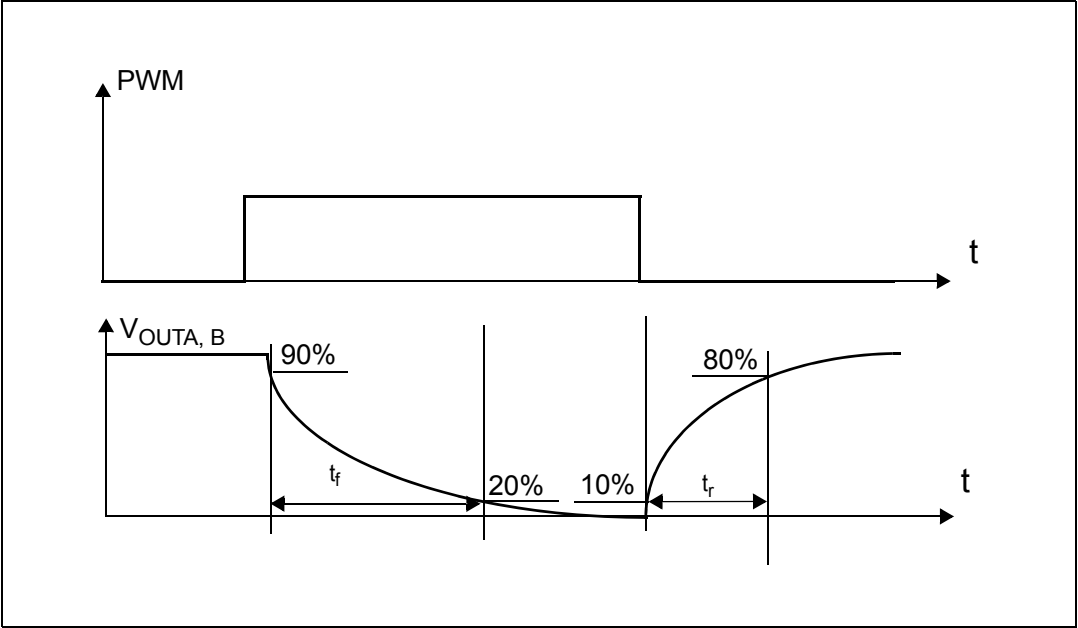


Figure 6. Definition of the high-side switching times

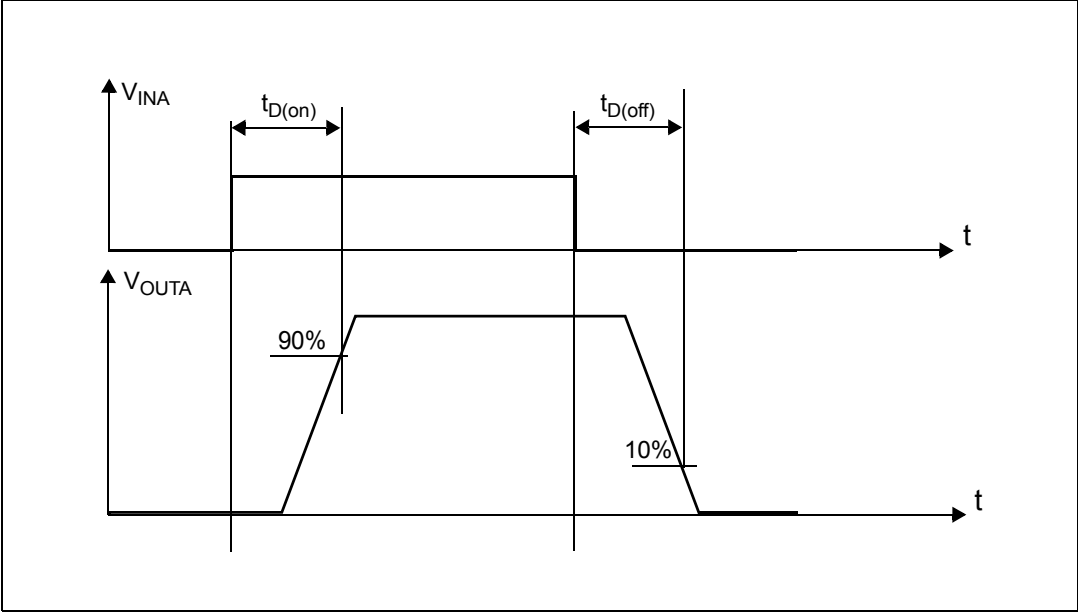


Figure 7. Low-side turn-on delay time

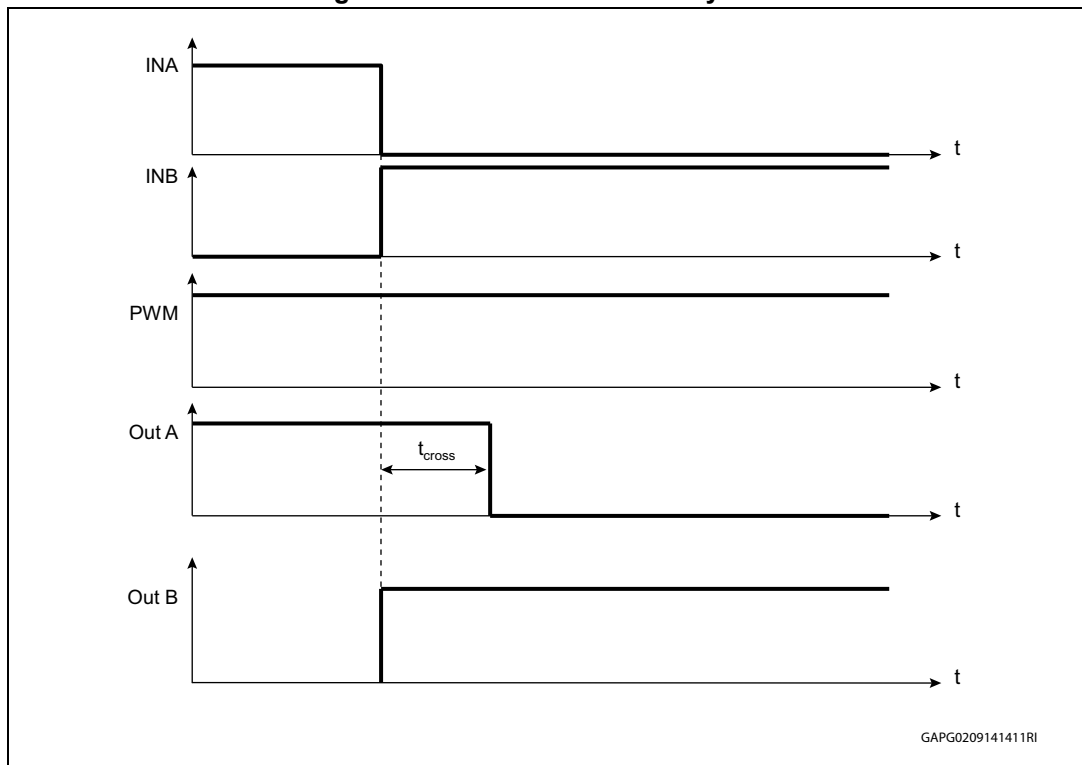
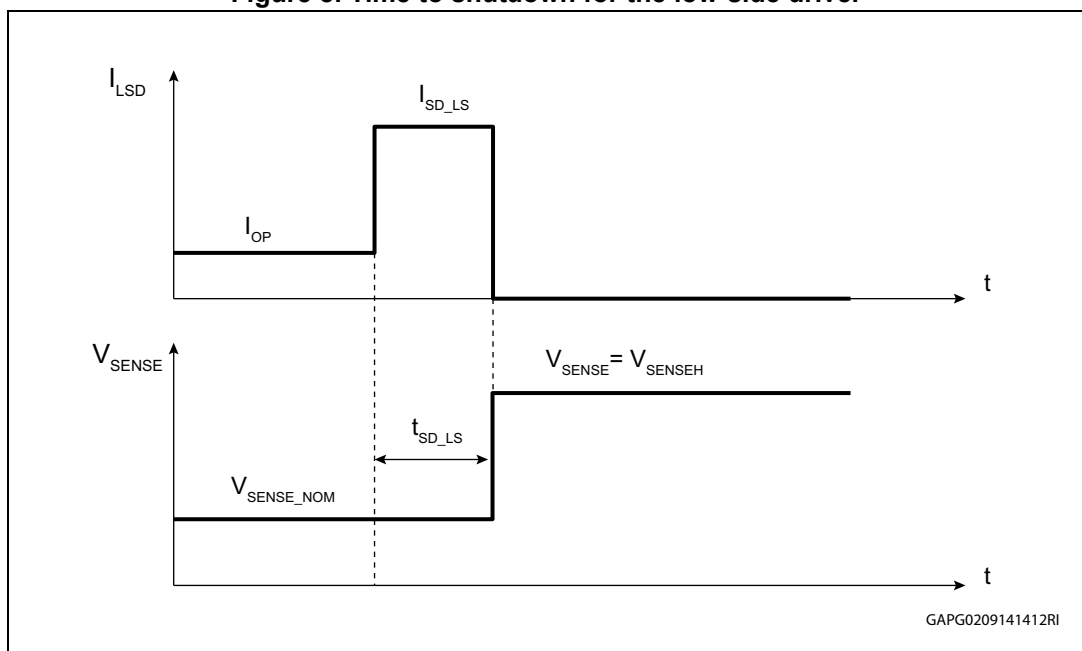
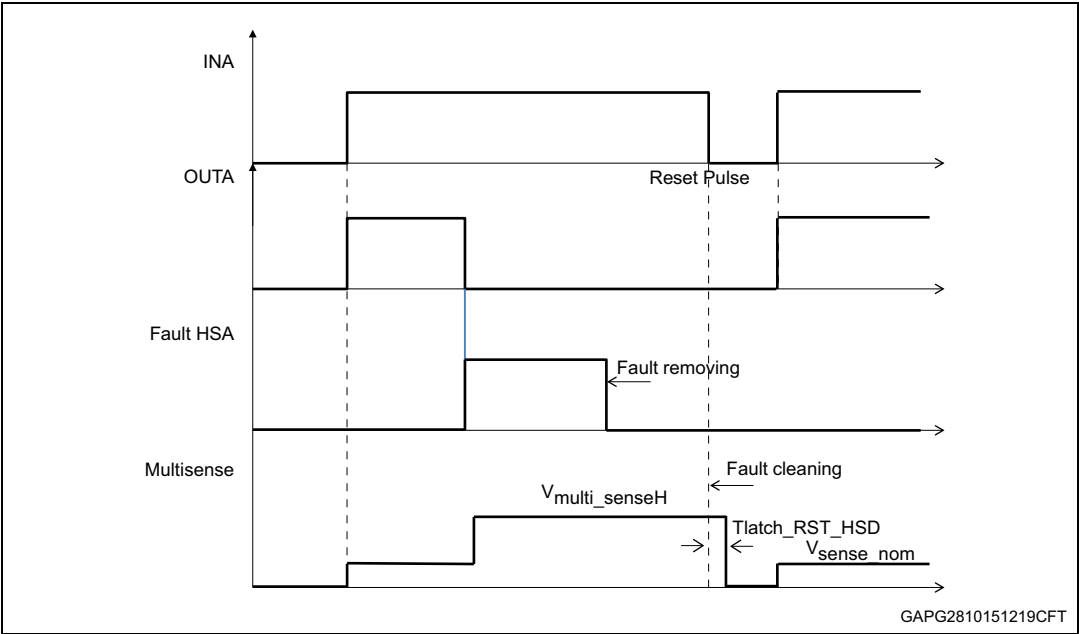


Figure 8. Time to shutdown for the low-side driver



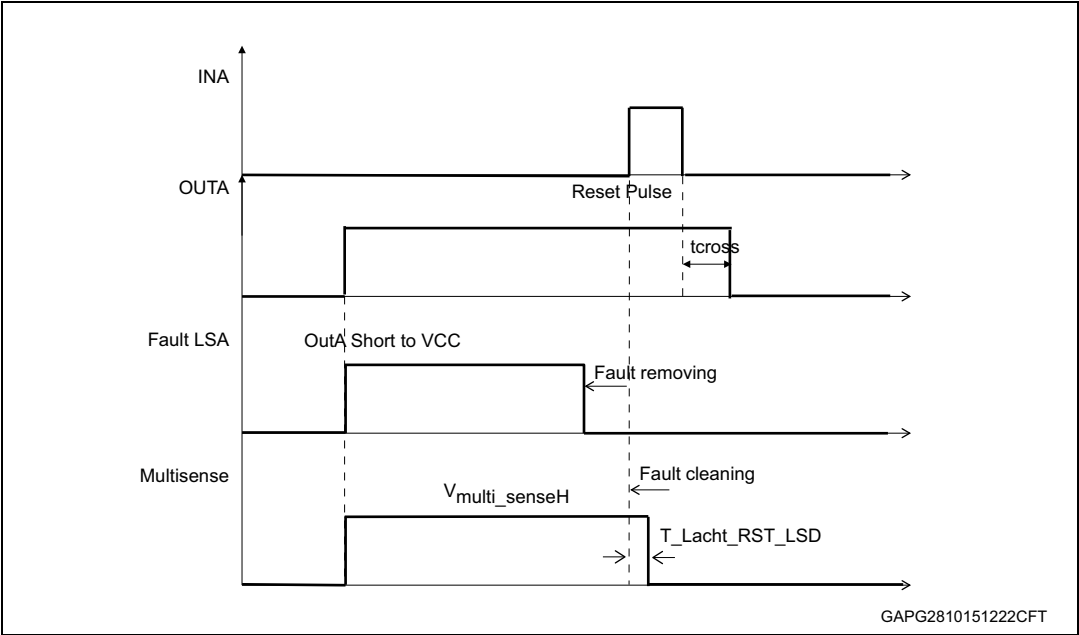
Note:  $MultiSense\_EN=1$

Figure 9. Input reset time for HSD-fault unlatch



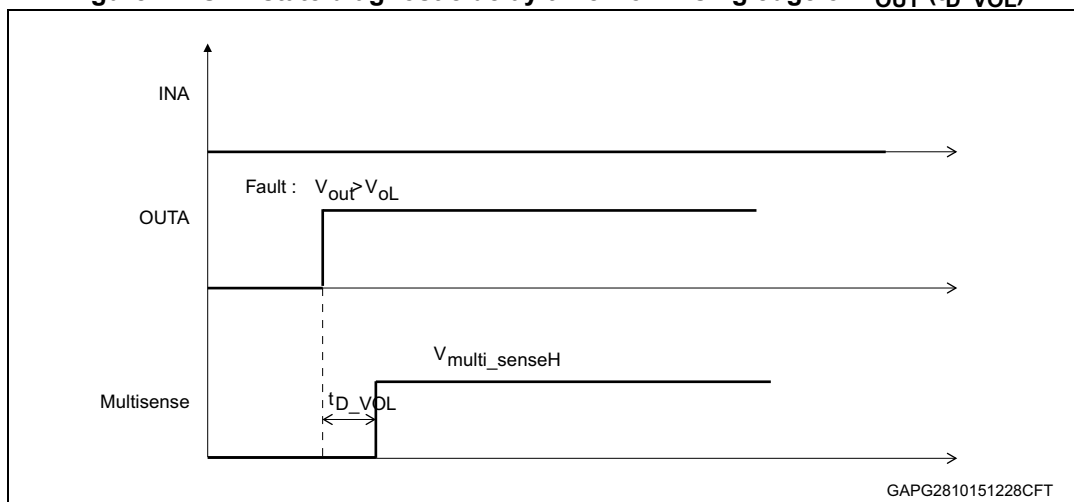
Note: *MultiSense\_EN=1*

Figure 10. Input Reset time for LSD-fault unlatch



Note: *MultiSense\_EN = 1*

Figure 11. OFF-state diagnostic delay time from rising edge of  $V_{OUT}$  ( $t_{D\_VOL}$ )



Note:  $MultiSense\_EN = 1$

Table 12. Operative condition - truth table

| INA              | INB | PWM | SEL0 | SEL1 | MS_EN | MS                        | HSA | LSA | HSB | LSB |
|------------------|-----|-----|------|------|-------|---------------------------|-----|-----|-----|-----|
| 0                | 0   | 1   | 0    | 0    | 1     | High-Z                    | OFF | ON  | OFF | ON  |
|                  |     | 1   | 1    | 0    | 1     | High-Z                    | OFF | ON  | OFF | ON  |
| 0                | 1   | 0   | 0    | 0    | 1     | Current Monitoring HSB    | OFF | OFF | ON  | OFF |
|                  |     | 1   | 0    | 0    | 1     | Current Monitoring HSB    | OFF | ON  | ON  | OFF |
| 0                | 1   | 0   | 1    | 0    | 1     | High-Z                    | OFF | OFF | ON  | OFF |
|                  |     | 1   | 1    | 0    | 1     | High-Z                    | OFF | ON  | ON  | OFF |
| 1                | 0   | 0   | 0    | 0    | 1     | High-Z                    | ON  | OFF | OFF | OFF |
|                  |     | 1   | 0    | 0    | 1     | High-Z                    | ON  | OFF | OFF | ON  |
| 1                | 0   | 0   | 1    | 0    | 1     | Current Monitoring HSA    | ON  | OFF | OFF | OFF |
|                  |     | 1   | 1    | 0    | 1     | Current Monitoring HSA    | ON  | OFF | OFF | ON  |
| 1                | 1   | X   | 0    | 0    | 1     | Current Monitoring HSB    | ON  | OFF | ON  | OFF |
|                  |     |     | 1    | 0    | 1     | Current Monitoring HSA    |     |     |     |     |
| 0                | 0   | 0   | 1    | 0    | 1     | Off state diagnostic OUTA | OFF | OFF | OFF | OFF |
| 0                | 0   | 0   | 0    | 0    | 1     | Off state diagnostic OUTB | OFF | OFF | OFF | OFF |
| X <sup>(1)</sup> | X   | X   | 0    | 1    | 1     | Tchip Monitoring          | —   | —   | —   | —   |
| X                | X   | X   | 1    | 1    | 1     | Vcc Monitoring            | —   | —   | —   | —   |
| X                | X   | X   | X    | X    | 0     | High-Z <sup>(2)</sup>     | —   | —   | —   | —   |

1. X means that the value of the pin can be 0 or 1.

2. When  $IN_A = IN_B = PWM = SEL_0 = SEL_1 = MultiSense\_EN = 0$  device enters standby after  $T_{DSTBY}$ .

Table 13. On-state fault conditions - truth table

| Digital Input pins <sup>(1)</sup> |     |     |      | MultiSense | Comment                                   |
|-----------------------------------|-----|-----|------|------------|-------------------------------------------|
| INA                               | INB | PWM | SEL0 |            |                                           |
| 0                                 | 0   | 1   | 0    | VsenseH    | LSB protection triggered; LSB latched off |
| 0                                 | 0   | 1   | 1    | VsenseH    | LSA protection triggered; LSA latched off |
| 0                                 | 1   | X   | 0    | VsenseH    | HSB protection triggered; HSB latched off |
| 0                                 | 1   | 1   | 1    | VsenseH    | LSA protection triggered; LSA latched off |
| 1                                 | 0   | 1   | 0    | VsenseH    | LSB protection triggered; LSB latched off |
| 1                                 | 0   | X   | 1    | VsenseH    | HSA protection triggered; HSA latched off |
| 1                                 | 1   | X   | 0    | VsenseH    | HSB protection triggered; HSB latched off |
| 1                                 | 1   | X   | 1    | VsenseH    | HSA protection triggered; HSA latched off |

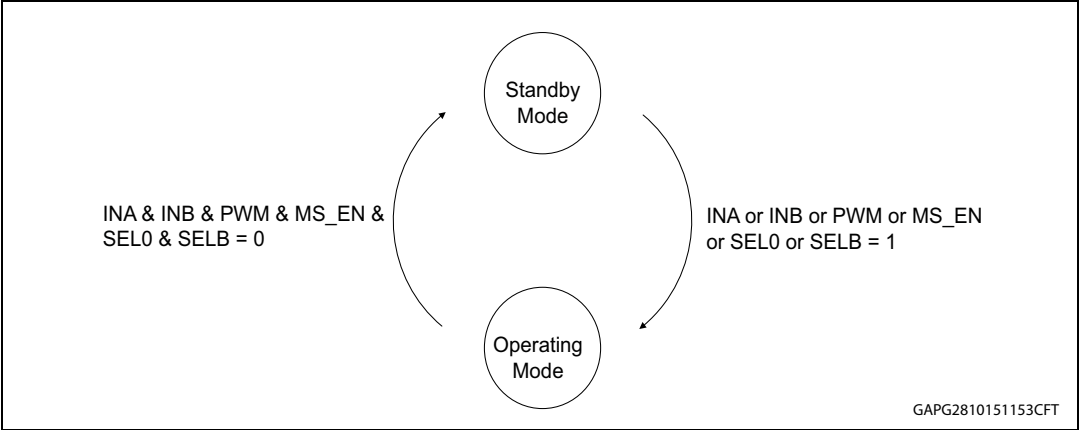
1. MultiSense\_EN = 1 and SEL1 = 0 are mandatory for fault detection. Other logic combinations on digital input pins not reported on the above table do not allow to detect a latched-off channel.

Table 14. Off-state — truth table

| INA                  | INB | SEL0         | SEL1         | PWM | OUTA                | OUTB                | MultiSense_EN | MultiSense   | Description                                                                                                                                                                                                                                                                                                |
|----------------------|-----|--------------|--------------|-----|---------------------|---------------------|---------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Off-state diagnostic |     |              |              |     |                     |                     |               |              |                                                                                                                                                                                                                                                                                                            |
| 0                    | 0   | 1            | 0            | 0   | $V_{OUTA} > V_{OL}$ | X                   | 1             | $V_{SENSEH}$ | <b>Case 1:</b> $OUT_A$ shorted to $V_{CC}$ if no pull-up is applied.<br><b>Case 2: NO open-load</b> in full bridge configuration with an external pull-up on $OUT_B$<br><b>Case 3: open-load</b> in half bridge configuration with an external pull-up on $OUT_A$ (motor connected between Out and Ground) |
|                      |     |              |              |     | $V_{OUTA} < V_{OL}$ | X                   | 1             | Hi-Z         | <b>Case 1: open-load</b> in full Bridge configuration with an external pull-up on $OUT_B$<br><b>Case 2: NO open-load</b> in half Bridge configuration with external pull-up on $OUT_A$ (motor connected between Out and Ground)                                                                            |
|                      |     | $0^{(1)(2)}$ | $0^{(1)(2)}$ |     | X                   | $V_{OUTB} > V_{OL}$ | 1             | $V_{SENSEH}$ | <b>Case 1:</b> $OUT_B$ shorted to $V_{CC}$ if no pull-up is applied<br><b>Case 2: NO open-load</b> in full bridge configuration with external pull-up on $OUT_A$<br><b>Case 3: open-load</b> in half bridge configuration with external pull-up on $OUT_B$ (motor connected between Out and Ground)        |
|                      |     |              |              |     | X                   | $V_{OUTB} < V_{OL}$ | 1             | Hi-Z         | <b>Case1: open-load</b> in full Bridge configuration with an external pull-up on $OUT_A$<br><b>Case 2. NO open-load</b> in half Bridge configuration with external pull-up on $OUT_B$ (motor connected between Out and Ground)                                                                             |

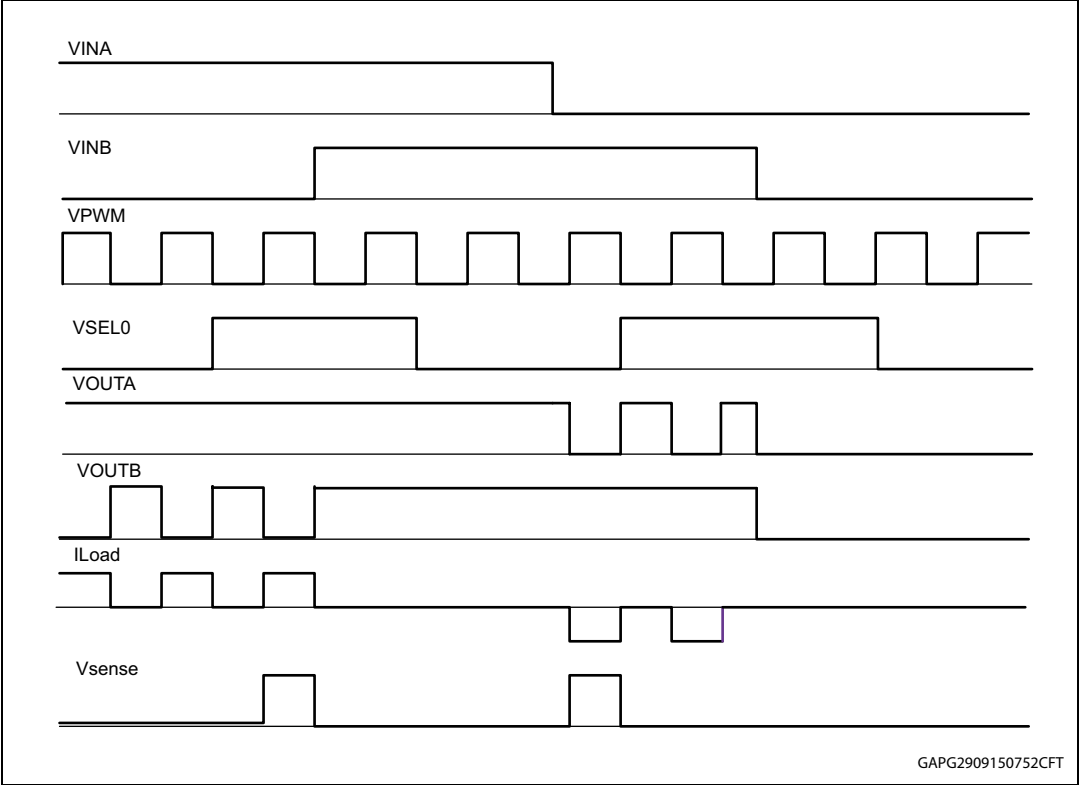
1. The device enters standby mode after  $TD_{sdbv}$ .
2. To power on the device from standby, it is recommended to: toggle INA or INB or SEL0 or SEL1 from 0 to 1 first to come out from STBY mode; toggle PWM from 0 to 1 with a delay of 20  $\mu s$  this avoids any overstress on the device in case of existing short-to-battery.

Figure 12. State diagram



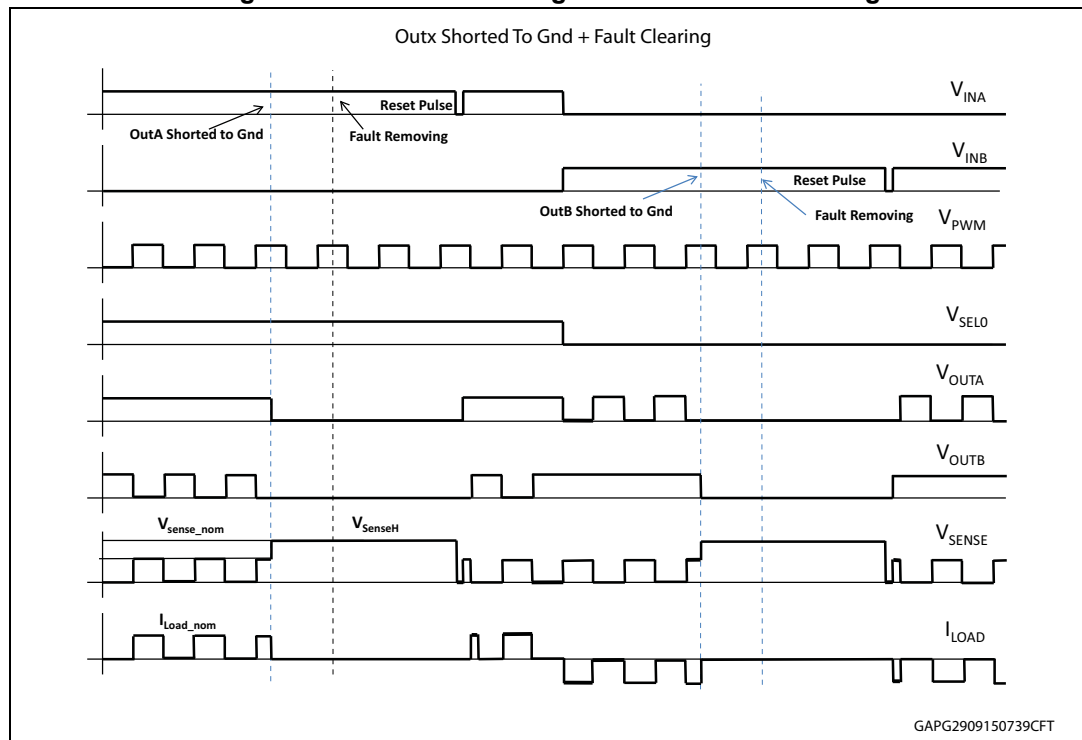
2.4 Waveforms

Figure 13. Normal operative conditions

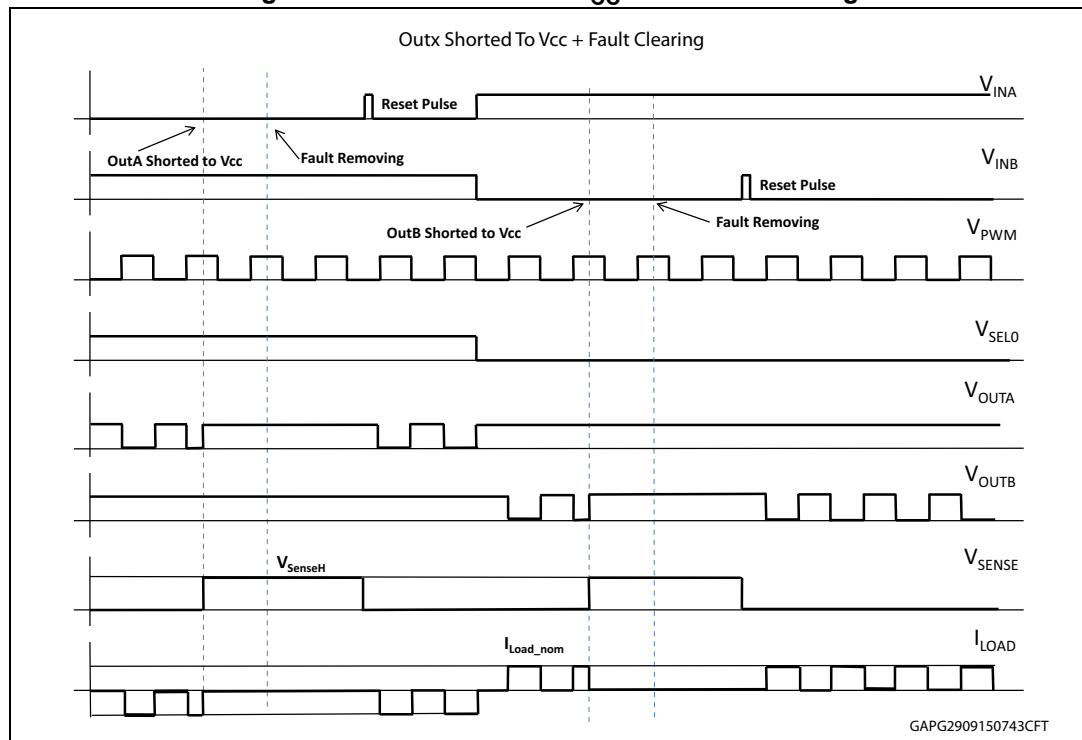


Note: *MultiSense\_EN* = 1.

Figure 14. OUT shorted to ground and short clearing



Note: *MultiSense\_EN* = 1

Figure 15. OUT shorted to V<sub>CC</sub> and short clearing

Note: *MultiSense\_EN* = 1

## 3 Protections

### 3.1 Power limitation (high-side driver)

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing  $\Delta T_j$  through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as  $\Delta T_j$  exceeds the safety level of  $\Delta T_{j\_SD}$ . The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue. When Power Limitation is reached, The device enters in latch mode and generates the Fault Flag on Multisense=VsenseH when the faulty leg diagnostic is selected (please refer to [Table 13](#)).

### 3.2 Thermal shutdown (high-side and low-side)

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175 °C), the device enters in latch mode and generates the Fault Flag on Multisense = VsenseH (please refer to [Table 13](#)). The concerned high side can be switched ON again as soon as  $T_j$  drops below  $T_{TR\_HSD}$ , INX is set low for a duration >  $T_{LATCH\_RST\_HS}$  and set high again.

### 3.3 Current limitation and over current detector

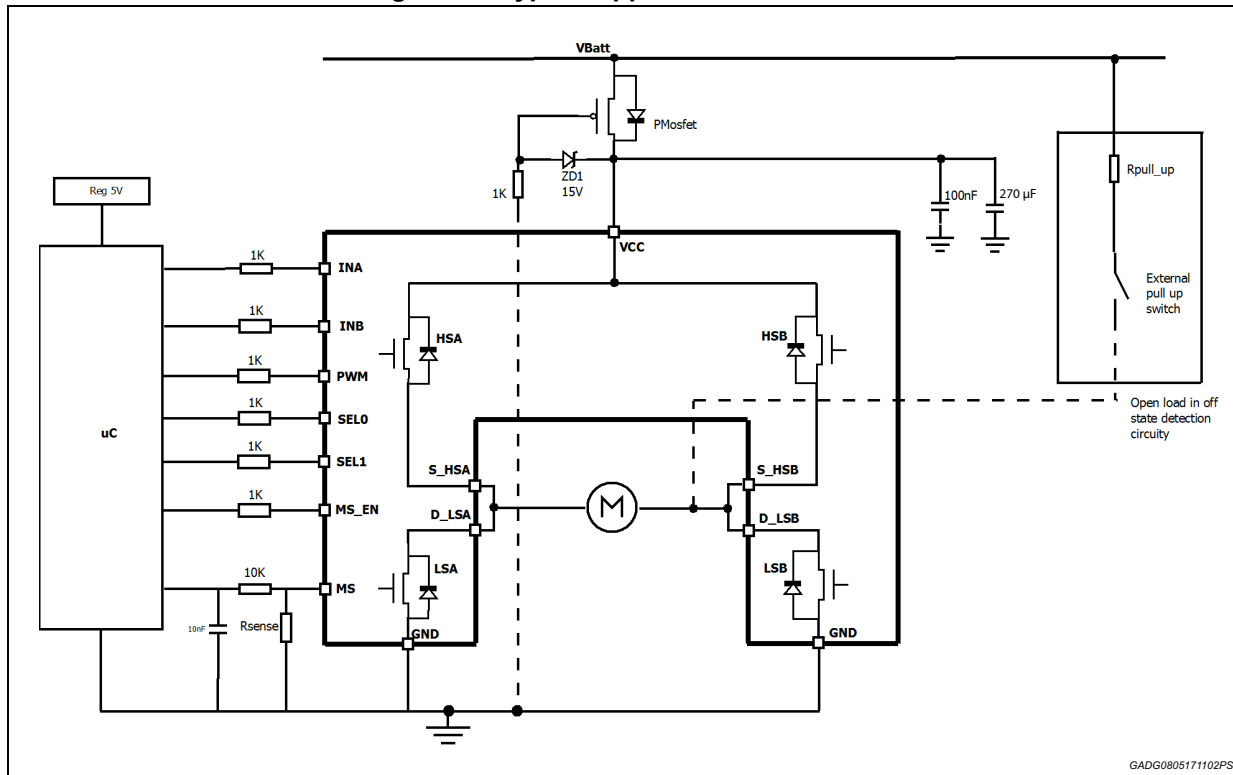
The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. High-side current limitation: in case of short-circuit, overload or during load power-up, the output current is clamped to a safety level,  $I_{LIM\_HSD}$ , by operating the output power MOSFET in the active region.

Low-side overcurrent detector: this protection senses the current flowing in the low-side. If the current exceeds a safety level  $I_{SD\_LS}$ , the device will switch off after a filtering time  $t_{sd\_ld}$ .

In case of fault conditions caused by Power Limitation or overtemperature or open load/short to VCC in OFF state, the fault is indicated by the MultiSense pin being internally switched to a "current limited" voltage source pulled to level VSENSEH (please refer to [Table 13](#)).

## 4 Typical application schematic

Figure 16. Typical application schematic



Note: To protect the device against Battery disconnection with energized inductive load when the bridge driver goes into 3-state, suggested  $C(V_{cc})$  is:

$$C(V_{cc}) = \frac{E_{motor}}{0.5 \cdot DV_{cc, max}^2}$$

where:

$E_{motor} = 19.4 \text{ mJ}$ ;

$DV_{cc, max} = V_{cc\_AMR} - V_{cc\_max}$ ;

$V_{cc\_AMR} = 38 \text{ V}$ ;

$V_{cc\_max} = 26 \text{ V}$  ( $V_{cc}$  at jump start);

$C(V_{cc}) = 270 \mu\text{F}$ .

## 5 MultiSense operation

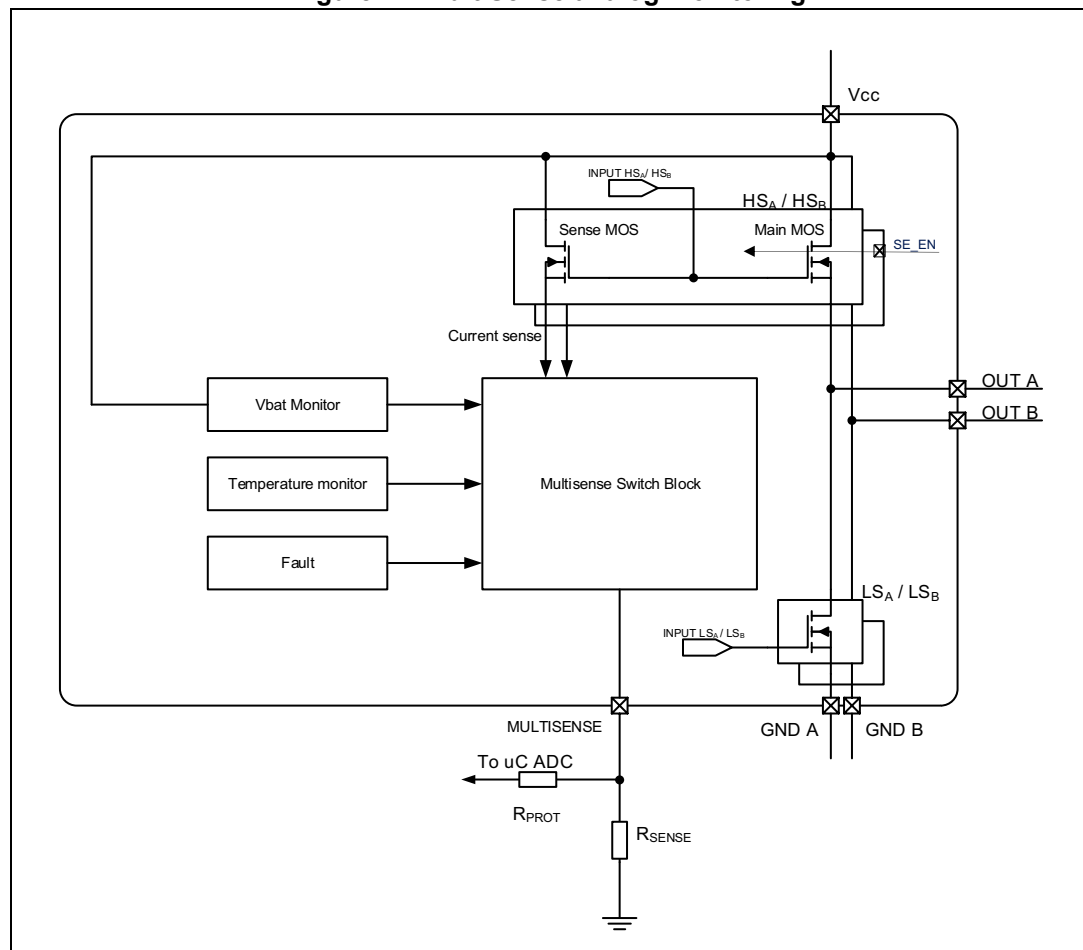
### 5.1 MultiSense analog monitoring

Diagnostic information on device and load status are provided by an analog output pin (MultiSense) delivering the following signals:

- Current monitor: current mirror of channel output current
- $V_{CC}$  monitor: voltage proportional to  $V_{CC}$
- $T_{CASE}$ : voltage proportional to chip temperature

Those signals are routed through an analog multiplexer which is configured and controlled by means of SELx and SEn pins, according to the address map in MultiSense multiplexer addressing table.

**Figure 17. MultiSense analog monitoring**



## 5.2 Multisense diagnostics flag in fault conditions

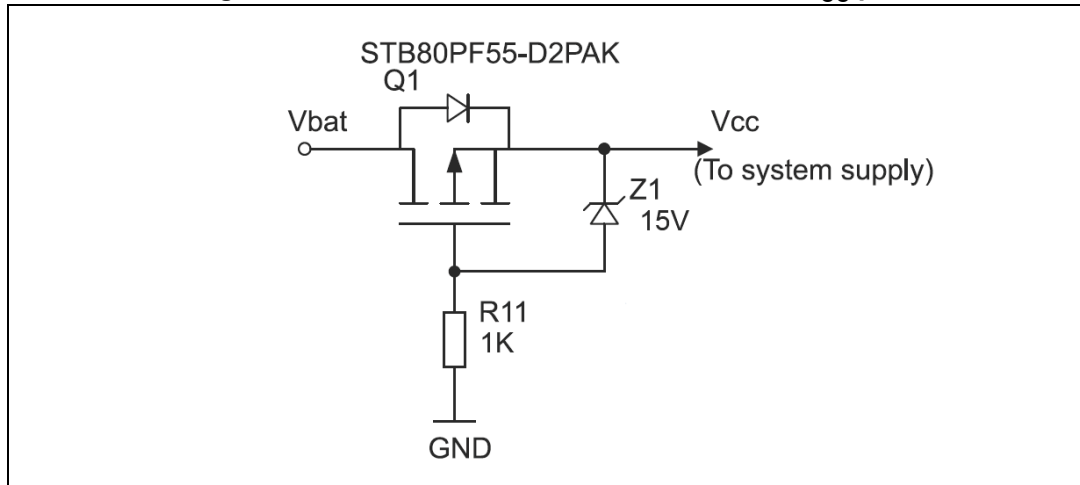
Multisense pin delivers fixed voltage (VSENSEH) with a certain current capability in case of:

- Fault condition on **activated high-side** (in ON state) triggered by Power Limitation, overtemperature protection, where MultiSense output is selected by SEL0 to high-side in fault state.
- Fault condition on **activated low-side** (in ON state) triggered by overcurrent shutdown, overtemperature protection, where MultiSense output is selected by SEL0 to the same leg (of high-side) where low-side is in fault state.
- Short-circuit to VCC on **OUT in OFF state** (INA = INB = PWM = 0) selected by SEL0; Special care must be taken for the OUTB (SEL0 = 0) because the fixed voltage is available only before the device enters its stand-by mode after TD\_STDBY (because all control signals are set to 0).
- In the configuration of **half bridge** (load connected between OUT and ground), when open-load appears on OUT in OFF state (selected by SEL0) with activated external pull-up resistor. Such condition causes an effect similar to the short circuit to  $V_{CC}$  on leg in OFF state (as mentioned in the above case, output voltage exceeds open-load threshold  $V_{OL}$ ).

## 6 Reverse battery protection

The picture below shows a P-Channel MOSFET connected to the  $V_{CC}$  pin.

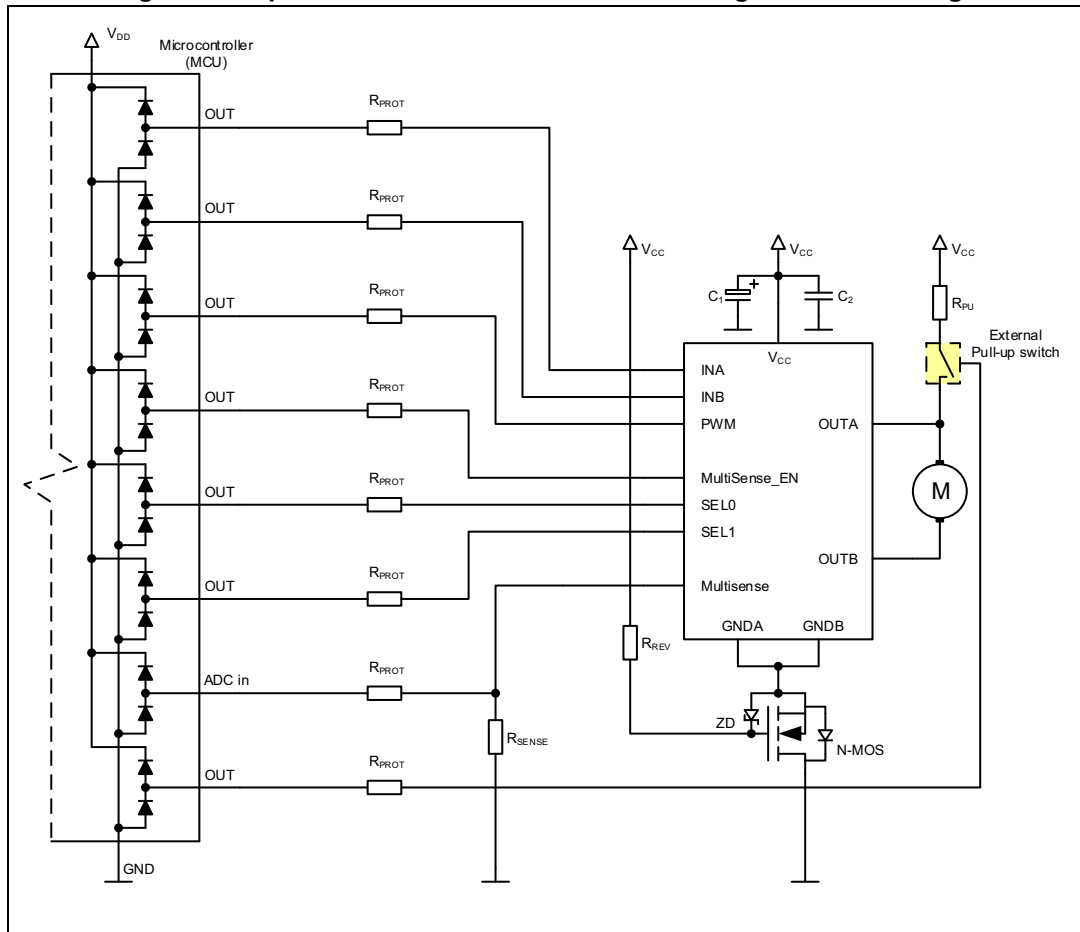
**Figure 18. P-channel MOSFET connected to the  $V_{CC}$  pin**



In normal operation the Zener diode plus the resistor generate a gate-source voltage enough to switch on the P-MOSFET. In case of reverse battery polarity: the P-Ch is switched off since its gate voltage is low. No current can flow in this state.



**Figure 20. Open load detection in off-state - configuration full-bridge**



if the device is used in H-bridge configuration, the equation is:

$$R_{pull\_up} < \frac{V_{BATTmin} - V_{OLmax}}{2 \times I_{L(off2)min}[@VOLmax]}$$

## 8 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the VCC pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in [Table 15: ISO 7637-2 electrical transient conduction along supply line](#).

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), Section 4. The DUT is intended as the present device only, without components and accessed through VCC and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: "The function does not perform as designed during the test but returns automatically to normal operation after the test".

**Table 15. ISO 7637-2 electrical transient conduction along supply line**

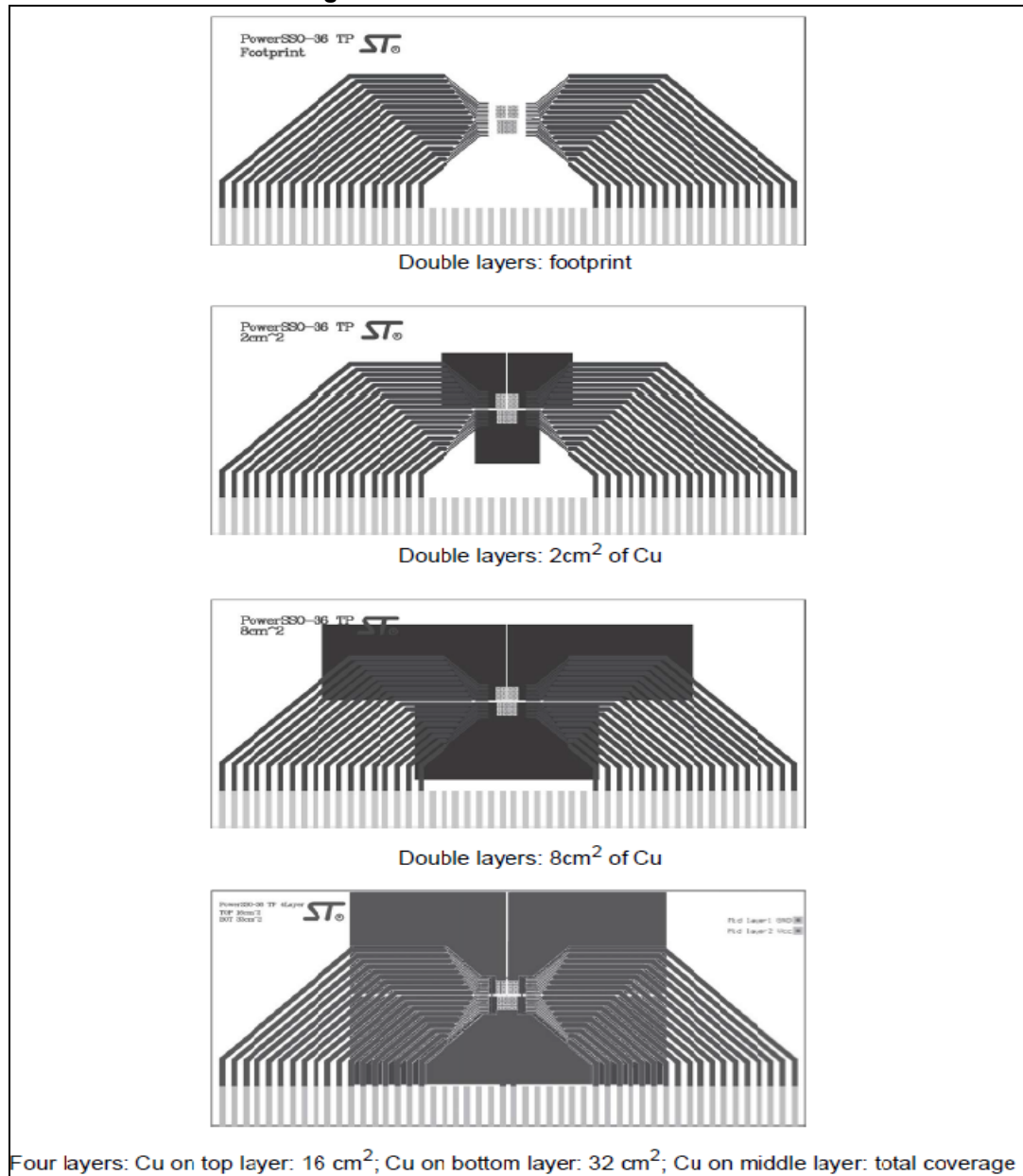
| Test pulse<br>2011(E)                          | Test pulse severity level<br>with status II functional<br>performance status |             | Minimum<br>number of<br>pulses or<br>test time | Burst cycle/pulse<br>repetition time |        | Pulse duration<br>and pulse<br>generator<br>internal<br>impedance |
|------------------------------------------------|------------------------------------------------------------------------------|-------------|------------------------------------------------|--------------------------------------|--------|-------------------------------------------------------------------|
|                                                | Level                                                                        | $U_S^{(1)}$ |                                                | min.                                 | max.   |                                                                   |
| 1                                              | III                                                                          | -112 V      | 500 pulses                                     | 0.5 s                                |        | 2 ms, 10 $\Omega$                                                 |
| 2a                                             | III                                                                          | +55         | 500 pulses                                     | 0.2 s                                | 5 s    | 50 $\mu$ s, 2 $\Omega$                                            |
| 3a                                             | IV                                                                           | -220 V      | 1h                                             | 90 ms                                | 100 ms | 0.1 $\mu$ s, 50 $\Omega$                                          |
| 3b                                             | IV                                                                           | +150 V      | 1h                                             | 90 ms                                | 100 ms | 0.1 $\mu$ s, 50 $\Omega$                                          |
| 4 <sup>(2)</sup>                               | IV                                                                           | -7 V        | 1 pulse                                        |                                      |        | 100 ms, 0.01 $\Omega$                                             |
| <b>Load dump according to ISO 16750-2:2010</b> |                                                                              |             |                                                |                                      |        |                                                                   |
| Test B <sup>(3)</sup>                          |                                                                              | 40 V        | 5 pulse                                        | 1 min                                |        | 400 ms, 2 $\Omega$                                                |

1.  $U_S$  is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E)
2. Test pulse from ISO 7637-2:2004(E)
3. With 40 V external suppressor referred to ground ( $-40^\circ\text{C} < T_J < 150^\circ\text{C}$ )

## 9 Package and PCB thermal data

### 9.1 PowerSSO-36 thermal data

Figure 21. PowerSSO-36™ PC board



**Note:** Board finish thickness 1.6 mm +/- 10%, board double layers and four layers, board dimension 129x60, board material FR4, Cu thickness 0.070 mm (front and back side), thermal vias spaced on a 1.2 mm x 1.2 mm grid, Vias pad clearance thickness 0.2 mm, thermal via diameter 0.3 mm ± 0.08 mm, Cu thickness on vias 0.025 mm, footprint dimension 4.1 mm x 6.5 mm.

Figure 22. Chipset configuration

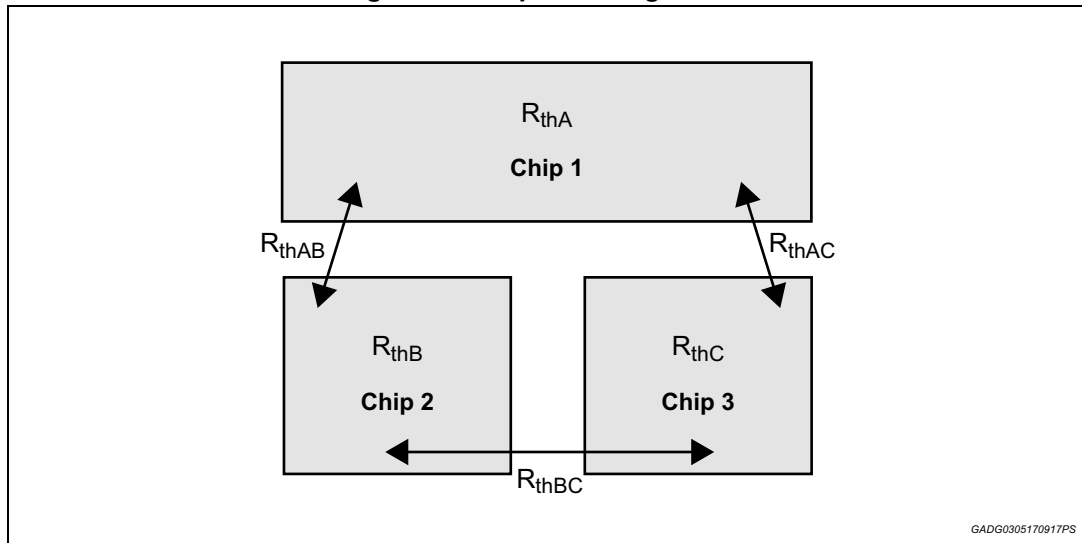
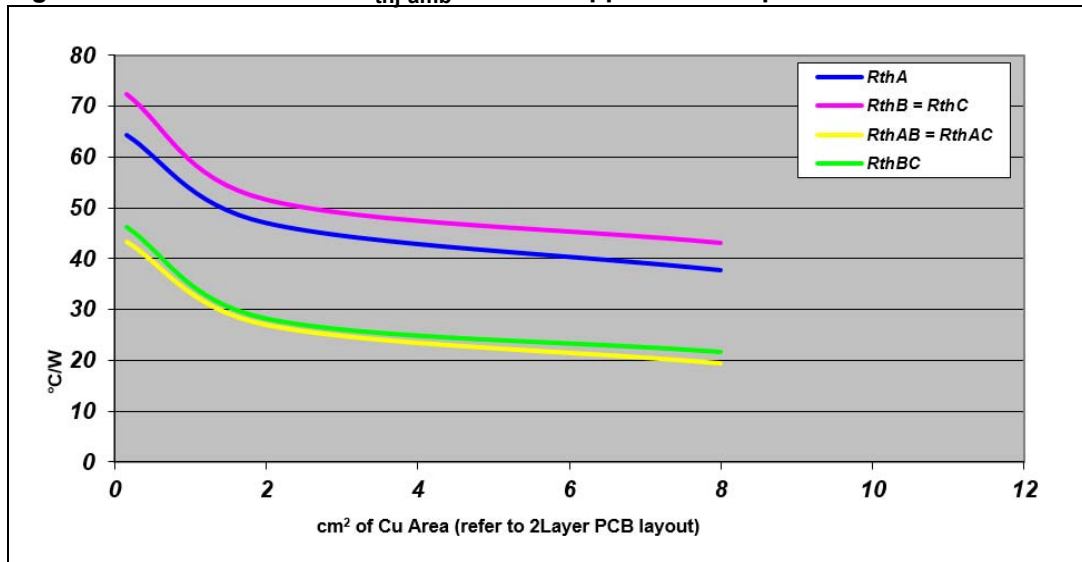
Figure 23. Auto and mutual  $R_{thj-amb}$  vs PCB copper area in open box free air condition

Table 16. Thermal resistance junction-ambient

|                    | Footprint | Cu 2 cm <sup>2</sup> | Cu 8 cm <sup>2</sup> | 4Layer |
|--------------------|-----------|----------------------|----------------------|--------|
|                    | °C/W      |                      |                      |        |
| <b>RthA</b>        | 64.4      | 47.1                 | 37.8                 | 24.1   |
| <b>RthB=RthC</b>   | 72.4      | 51.7                 | 43.2                 | 30.2   |
| <b>RthAB=RthAC</b> | 43.3      | 26.8                 | 19.3                 | 10.8   |
| <b>RthBC</b>       | 46.3      | 28.2                 | 21.6                 | 13.8   |

### 9.1.1 Thermal resistances definition (values according to the PCB heatsink area)

- $R_{thHS} = R_{thHSA} = R_{thHSB}$  = high-side chip thermal resistance junction to ambient (HSA or HSB in ON state)
- $R_{thLS} = R_{thLSA} = R_{thLSB}$  = low-side chip thermal resistance junction to ambient
- $R_{thHSLS} = R_{thHSALSB} = R_{thHSBLSA}$  = mutual thermal resistance junction to ambient between high-side and low-side chips
- $R_{thLSLS} = R_{thLSALSB} = R_{thLSBLSA}$  = mutual thermal resistance junction to ambient between low-side chip.

**Table 17. Thermal model for junction temperature calculation in steady-state conditions**

| Chip 1 | Chip 2 | Chip 3 | Tjchip1                                                          | Tjchip2                                                           | Tjchip3                                                           |
|--------|--------|--------|------------------------------------------------------------------|-------------------------------------------------------------------|-------------------------------------------------------------------|
| ON     | OFF    | ON     | $P_{dchip1} \cdot R_{thA} + P_{dchip3} \cdot R_{thAC} + T_{amb}$ | $P_{dchip1} \cdot R_{thAB} + P_{dchip3} \cdot R_{thBC} + T_{amb}$ | $P_{dchip1} \cdot R_{thAC} + P_{dchip3} \cdot R_{thC} + T_{amb}$  |
| ON     | ON     | OFF    | $P_{dchip1} \cdot R_{thA} + P_{dchip2} \cdot R_{thAB} + T_{amb}$ | $P_{dchip1} \cdot R_{thAB} + P_{dchip2} \cdot R_{thB} + T_{amb}$  | $P_{dchip1} \cdot R_{thAC} + P_{dchip2} \cdot R_{thBC} + T_{amb}$ |
| ON     | OFF    | OFF    | $P_{dchip1} \cdot R_{thA} + T_{amb}$                             | $P_{dchip1} \cdot R_{thAB} + T_{amb}$                             | $P_{dchip1} \cdot R_{thAC} + T_{amb}$                             |
| OFF    | ON     | ON     | $(P_{dchip2} + P_{dchip3}) \cdot R_{thAB} + T_{amb}$             | $P_{dchip2} \cdot R_{thB} + P_{dchip3} \cdot R_{thBC} + T_{amb}$  | $P_{dchip2} \cdot R_{thBC} + P_{dchip3} \cdot R_{thC} + T_{amb}$  |

## 9.2 Thermal Characterization during transients

$$T_{hs} = P_{D_{hs}} \cdot Z_{hs} + Z_{hsIs} \cdot (P_{dIsA} + P_{dIsB}) + T_{amb}$$

$$T_{IsA} = P_{dIsA} \cdot Z_{Is} + P_{D_{hs}} \cdot Z_{hsIs} + P_{dIsB} \cdot Z_{IsIs} + T_{amb}$$

$$T_{IsB} = P_{dIsB} \cdot Z_{Is} + P_{D_{hs}} \cdot Z_{hsIs} + P_{dIsA} \cdot Z_{IsIs} + T_{amb}$$

Figure 24. HSD thermal impedance junction ambient single pulse

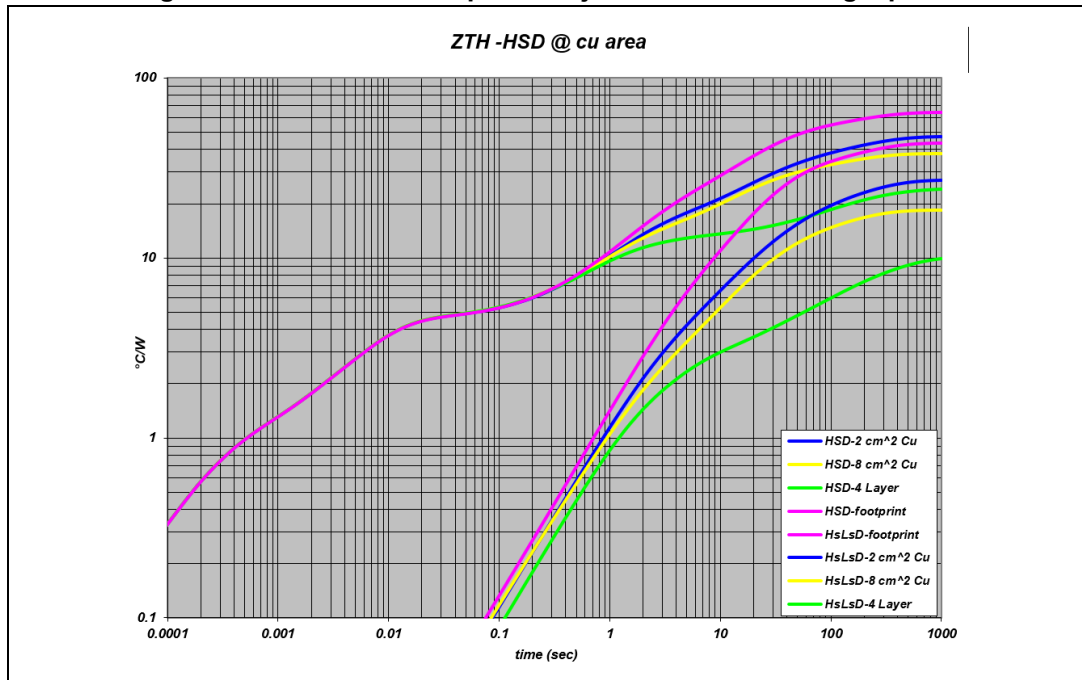


Figure 25. LSD thermal impedance junction ambient single pulse

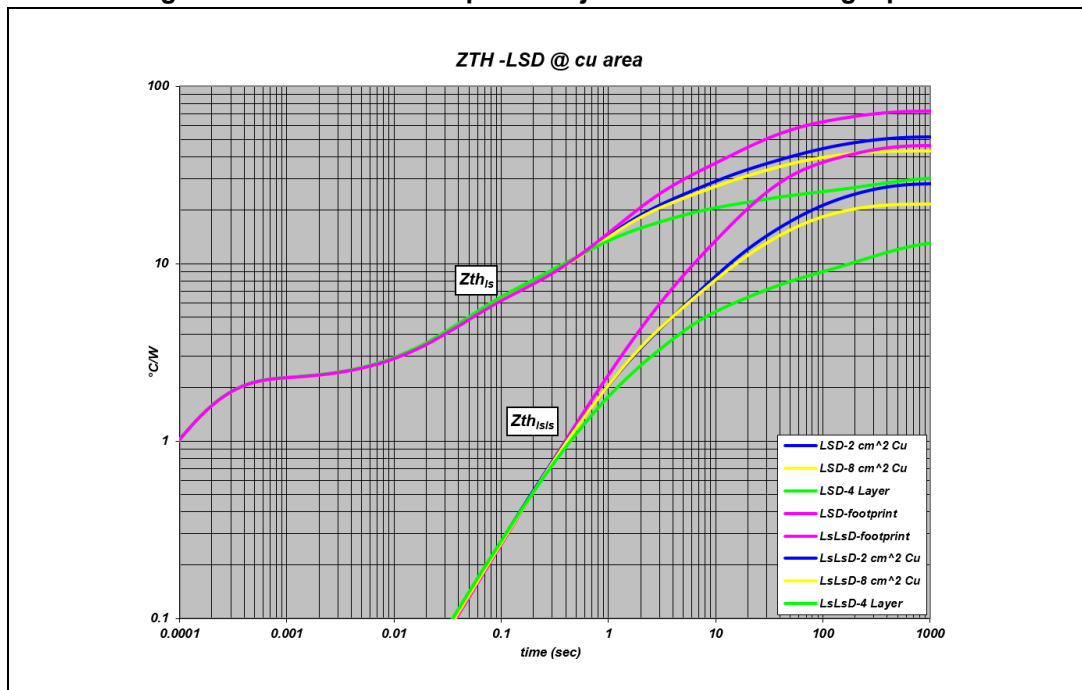


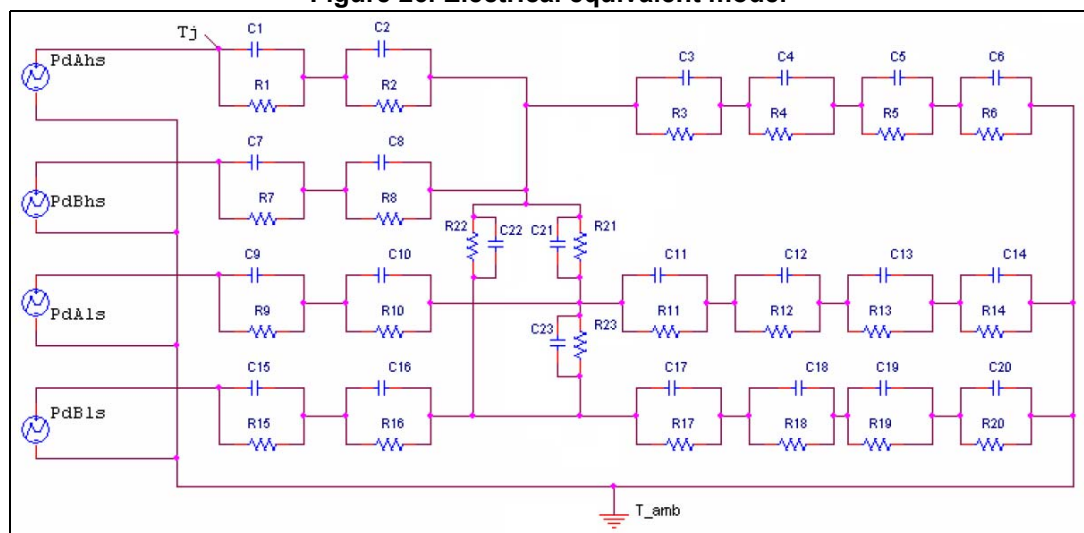
Table 18. Thermal parameters

| Area/island (cm <sup>2</sup> ) | FP      | 2    | 8    | 4L   |
|--------------------------------|---------|------|------|------|
| R1 (°C/W)                      | 0.8     |      |      |      |
| R2 (°C/W)                      | 3.7     |      |      |      |
| R3 (°C/W)                      | 13      | 12   | 8.8  | 5.5  |
| R4 (°C/W)                      | 28      | 14   | 13   | 5    |
| R5 (°C/W)                      | 37      | 21   | 14   | 7    |
| R6 (°C/W)                      | 36      | 36   | 22   | 13   |
| R7 (°C/W)                      | 0.8     |      |      |      |
| R8 (°C/W)                      | 3.7     |      |      |      |
| R9 (°C/W)                      | 2.2     |      |      |      |
| R10 (°C/W)                     | 3.2     |      |      |      |
| R11 (°C/W)                     | 24      | 15.5 | 15.5 | 8.8  |
| R12 (°C/W)                     | 49      | 32   | 20   | 13   |
| R13 (°C/W)                     | 54      | 33   | 25   | 16   |
| R14 (°C/W)                     | 56      | 30   | 27   | 20   |
| R15 (°C/W)                     | 2.2     |      |      |      |
| R16 (°C/W)                     | 3.2     |      |      |      |
| R17 (°C/W)                     | 24      | 15.5 | 15.5 | 8.8  |
| R18 (°C/W)                     | 49      | 32   | 20   | 13   |
| R19 (°C/W)                     | 54      | 33   | 25   | 16   |
| R20 (°C/W)                     | 56      | 30   | 27   | 20   |
| R21 (°C/W)                     | 70      | 64   | 70   | 55   |
| R22 (°C/W)                     | 70      | 64   | 70   | 55   |
| R23 (°C/W)                     | 70      | 66   | 55   | 40   |
| C1 (W·s/°C)                    | 0.00028 |      |      |      |
| C2 (W·s/°C)                    | 0.0018  |      |      |      |
| C3 (W·s/°C)                    | 0.15    | 0.13 | 0.12 | 0.14 |
| C4 (W·s/°C)                    | 0.7     | 1.45 | 1.4  | 0.4  |
| C5 (W·s/°C)                    | 0.8     | 1.8  | 1.5  | 14   |
| C6 (W·s/°C)                    | 5       | 6    | 7.5  | 18   |
| C7 (W·s/°C)                    | 0.00028 |      |      |      |
| C8 (W·s/°C)                    | 0.0018  |      |      |      |
| C9 (W·s/°C)                    | 0.00007 |      |      |      |
| C10 (W·s/°C)                   | 0.015   |      |      |      |
| C11 (W·s/°C)                   | 0.08    | 0.07 | 0.07 | 0.06 |
| C12 (W·s/°C)                   | 0.35    | 0.3  | 0.37 | 0.26 |

Table 18. Thermal parameters (continued)

| Area/island (cm <sup>2</sup> ) | FP      | 2     | 8     | 4L    |
|--------------------------------|---------|-------|-------|-------|
| C13 (W·s/°C)                   | 0.55    | 1.4   | 1.2   | 1.4   |
| C14 (W·s/°C)                   | 2.8     | 5.4   | 3.2   | 20    |
| C15 (W·s/°C)                   | 0.00007 |       |       |       |
| C16 (W·s/°C)                   | 0.015   |       |       |       |
| C17 (W·s/°C)                   | 0.08    | 0.07  | 0.07  | 0.06  |
| C18 (W·s/°C)                   | 0.35    | 0.3   | 0.37  | 0.26  |
| C19 (W·s/°C)                   | 0.55    | 1.4   | 1.2   | 1.4   |
| C20 (W·s/°C)                   | 2.8     | 5.4   | 3.2   | 20    |
| C21 (W·s/°C)                   | 0.011   | 0.009 | 0.009 | 0.005 |
| C22 (W·s/°C)                   | 0.011   | 0.009 | 0.009 | 0.005 |
| C23 (W·s/°C)                   | 0.017   | 0.016 | 0.016 | 0.011 |

Figure 26. Electrical equivalent model



## 10 Package and packing information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).

ECOPACK<sup>®</sup> is an ST trademark.

### 10.1 PowerSSO-36 TP package information

Figure 27. PowerSSO-36 TP package dimensions

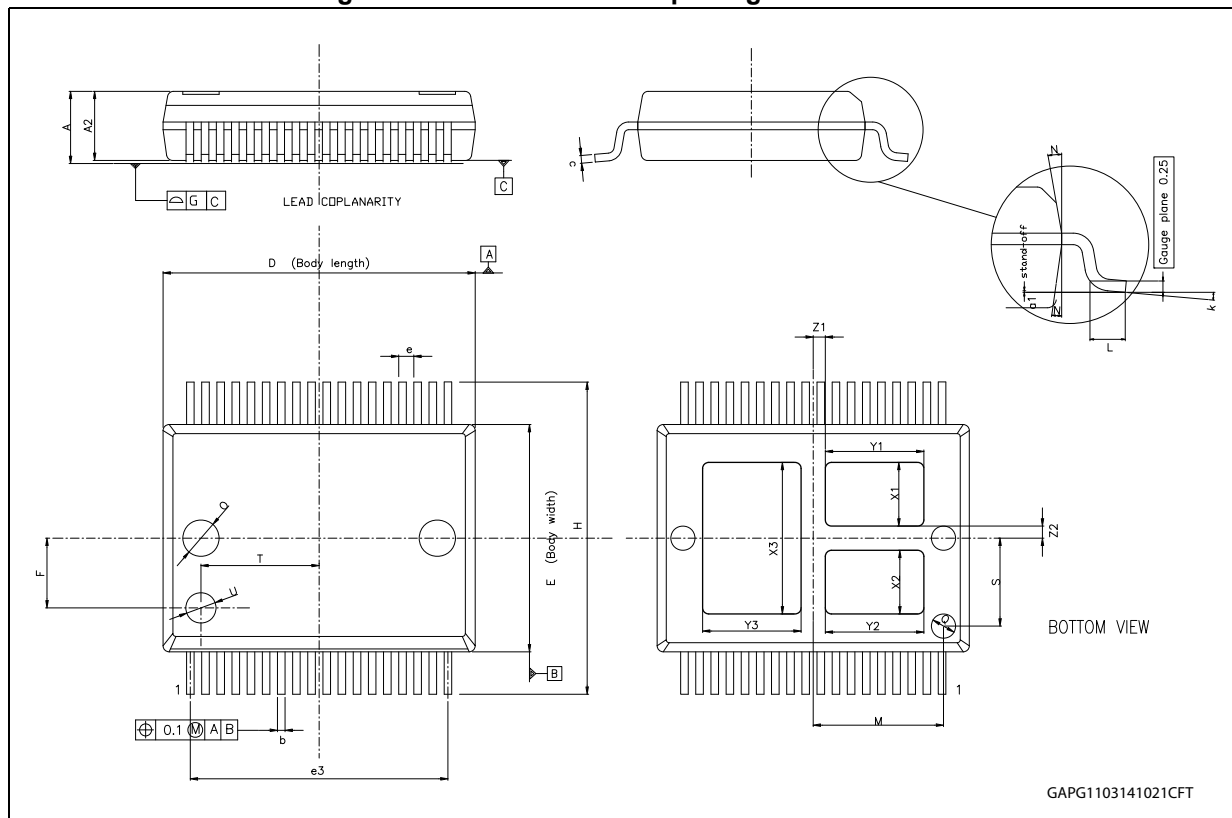


Table 19. PowerSSO-36 TP mechanical data

| Symbol | Millimeters |      |        |
|--------|-------------|------|--------|
|        | Min.        | Typ. | Max.   |
| A      | 2.15        |      | 2.47   |
| A2     | 2.15        |      | 2.40   |
| a1     | 0           |      | 0.1    |
| b      | 0.18        |      | 0.36   |
| c      | 0.23        |      | 0.32   |
| D      | 10.10       |      | 10.50  |
| E      | 7.4         |      | 7.6    |
| e      |             | 0.5  |        |
| e3     |             | 8.5  |        |
| F      |             | 2.3  |        |
| G      |             |      | 0.1    |
| H      | 10.1        |      | 10.5   |
| h      |             |      | 0.4    |
| k      | 0 deg       |      | 8 deg  |
| L      | 0.6         |      | 1      |
| M      |             | 4.3  |        |
| N      |             |      | 10 deg |
| O      |             | 1.2  |        |
| Q      |             | 0.8  |        |
| S      |             | 2.9  |        |
| T      |             | 3.65 |        |
| U      |             | 1.0  |        |
| X1     | 1.85        |      | 2.35   |
| Y1     | 3           |      | 3.5    |
| X2     | 1.85        |      | 2.35   |
| Y2     | 3           |      | 3.5    |
| X3     | 4.7         |      | 5.2    |
| Y3     | 3           |      | 3.5    |
| Z1     |             | 0.4  |        |
| Z2     |             | 0.4  |        |

## 10.2 PowerSSO-36 TP packing information

Figure 28. PowerSSO-36 TP tube shipment (no suffix)

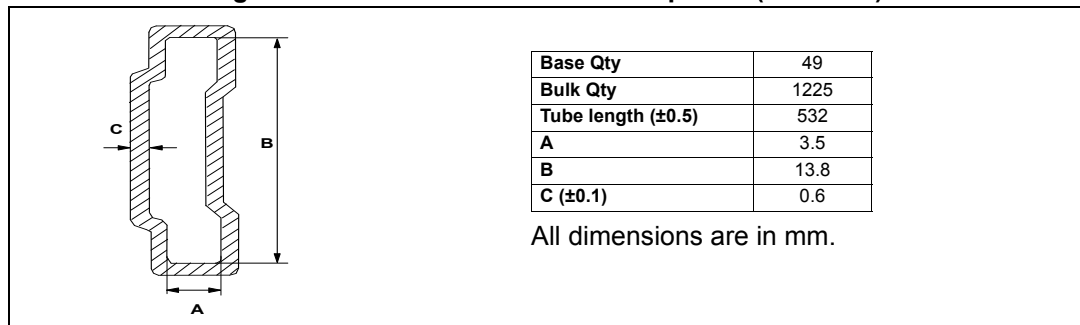
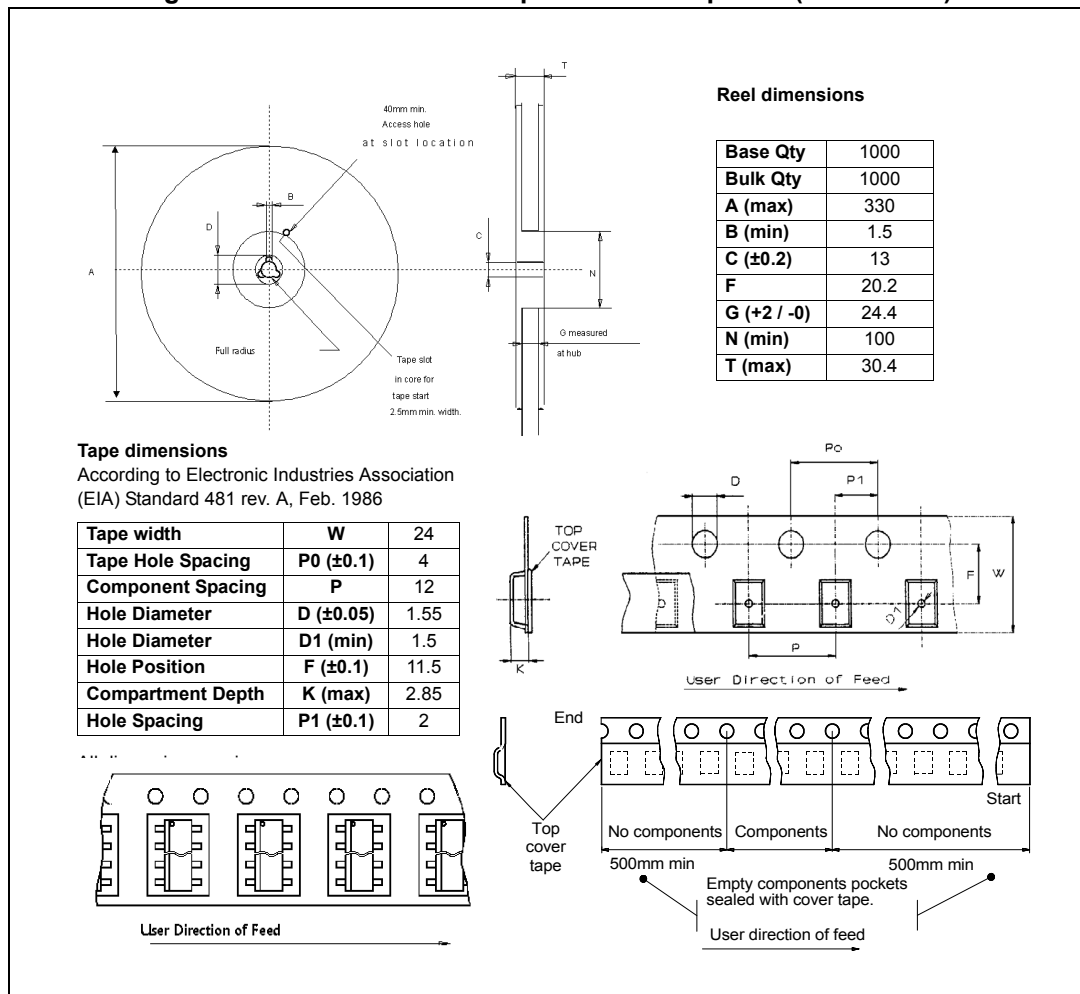
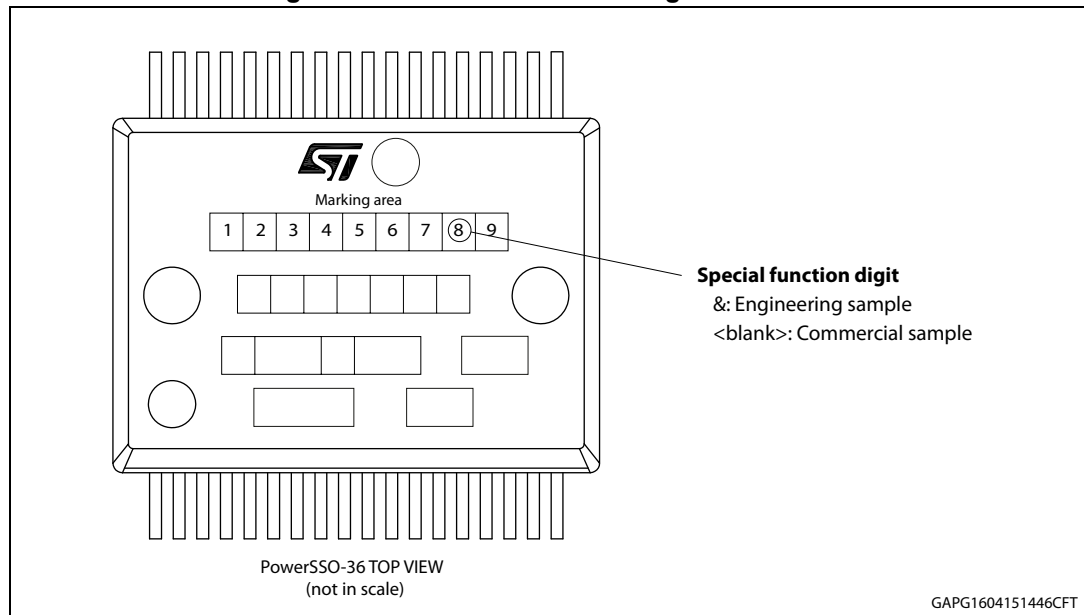


Figure 29. PowerSSO-36 TP tape and reel shipment (suffix "TR")



### 10.3 PowerSSO-36 marking information

Figure 30. PowerSSO-36 marking information



Parts marked as '&' are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

## 11 Order codes

**Table 20. Device summary**

| Package        | Order codes |               |
|----------------|-------------|---------------|
|                | Tube        | Tape and reel |
| PowerSSO-36 TP | VNH7070AY   | VNH7070AYTR   |

## 12 Revision history

**Table 21. Document revision history**

| Date        | Revision | Description of changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13-Jul-2017 | 1        | Initial release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 17-May-2018 | 2        | Updated <a href="#">Table 7: Power section</a> ; <a href="#">Table 10: Protections and diagnostics</a> ( $7\text{ V} < V_{CC} < 18\text{ V}$ ; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$ ); <a href="#">Table 11: MultiSense</a> ( $7\text{ V} < V_{CC} < 18\text{ V}$ ; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$ ).<br>Updated <a href="#">Section 3.1: Power limitation (high-side driver)</a> and <a href="#">Section 3.2: Thermal shutdown (high-side and low-side)</a> . |
| 25-Jan-2019 | 3        | Updated in cover page the first feature with "AEC-Q100 qualified".<br>Updated <a href="#">Table 6</a> , <a href="#">Table 11</a> , <a href="#">Table 17</a> and <a href="#">Figure 16</a> .<br>Added <a href="#">Figure 23</a> , <a href="#">Table 16</a> , <a href="#">Figure 24</a> , <a href="#">Figure 25</a> and <a href="#">Table 18</a> .                                                                                                                                                                               |
| 11-Feb-2019 | 4        | In <a href="#">Table 7</a> updated Typ. value for $R_{ONHS}$ parameter.<br>In <a href="#">Table 11</a> updated Min. value for $I_{OUT\_SAT}$ parameter.                                                                                                                                                                                                                                                                                                                                                                        |
| 14-Mar-2019 | 5        | Updated <a href="#">Figure 23</a> , <a href="#">Figure 24</a> and <a href="#">Figure 25</a> .<br>Updated <a href="#">Table 16</a> and <a href="#">Table 18</a> .                                                                                                                                                                                                                                                                                                                                                               |

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