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## 1. Overview

### 1.1 Features

The R8C/LA3A Group, R8C/LA5A Group, R8C/LA6A Group, and R8C/LA8A Group of single-chip MCUs incorporate the R8C CPU core, which implements a powerful instruction set for a high level of efficiency and supports a 1 Mbyte address space, allowing execution of instructions at high speed. In addition, the CPU core integrates a multiplier for high-speed operation processing.

Power consumption is low, and the supported operating modes allow additional power control. These MCUs are designed to maximize EMI/EMS performance.

Integration of many peripheral functions, including multifunction timer and serial interface, helps reduce the number of system components.

The R8C/LA3A Group, R8C/LA5A Group, R8C/LA6A Group, and R8C/LA8A Group have data flash.

#### 1.1.1 Applications

Household appliances, office equipment, audio equipment, consumer products, etc.

## 1.1.2 Differences between Groups

Table 1.1 lists the Differences between Groups, Tables 1.2 and 1.3 list the Programmable I/O Ports Provided for Each Group, and Tables 1.4 and 1.5 list the LCD Display Function Pins Provided for Each Group.

Figures 1.9 to 1.12 show the pin assignment for each group, and Tables 1.9 to 1.12 list product information.

The explanations in the chapters which follow apply to the R8C/LA8A Group only. Note the differences shown below.

**Table 1.1 Differences between Groups**

| Item                      | Function                               | R8C/LA3A Group       | R8C/LA5A Group | R8C/LA6A Group | R8C/LA8A Group |
|---------------------------|--|----------------------|----------------|----------------|----------------|
| I/O Ports                 | Programmable I/O ports                 | 26 pins              | 44 pins        | 56 pins        | 72 pins        |
|                           | High current drive ports               | 8 pins               | 8 pins         | 8 pins         | 10 pins        |
| Interrupts                | $\overline{\text{INT}}$ interrupt pins | 5 pins               | 6 pins         | 8 pins         | 8 pins         |
| Timer RJ                  | Timer RJ0 output pin                   | None                 | None           | None           | 1 pin          |
|                           | Timer RJ1 output pin                   | None                 | None           | None           | 1 pin          |
|                           | Timer RJ2 I/O pin                      | None                 | None           | None           | 1 pin          |
|                           | Timer RJ2 output pin                   | None                 | None           | None           | 1 pin          |
| Timer RH                  | Timer RH output pin                    | None                 | 1 pin          | 1 pin          | 1 pin          |
| Serial interface          | UART2                                  | None                 | None           | 1 pin          | 1 pin          |
| A/D Converter             | Analog input pins                      | 5 pins               | 7 pins         | 8 pins         | 12 pins        |
| LCD Drive Control Circuit | Segment output pins                    | Max. 11 pins         | Max. 27 pins   | Max. 32 pins   | Max. 40 pins   |
| Comparator B              | Analog input voltage                   | 1 pin                | 2 pins         | 2 pins         | 2 pins         |
|                           | Reference input voltage                | 1 pin                | 2 pins         | 2 pins         | 2 pins         |
| Clock                     | XCIN pin                               | Shared with XIN pin  | Dedicated pin  | Dedicated pin  | Dedicated pin  |
|                           | XCOUT pin                              | Shared with XOUT pin | Dedicated pin  | Dedicated pin  | Dedicated pin  |
| Packages                  |  | 32-pin LQFP          | 52-pin LQFP    | 64-pin LQFP    | 80-pin LQFP    |

Note:

- I/O ports are shared with I/O functions, such as interrupts or timers. Refer to Tables 1.13 to 1.17, Pin Name Information by Pin Number, for details.

**Table 1.2 Programmable I/O Ports Provided for Each Group (R8C/LA3A Group, R8C/LA5A Group)**

| Programmable I/O Port | R8C/LA3A Group<br>Total: 26 I/O pins |       |       |       |       |       |       |       | R8C/LA5A Group<br>Total: 44 I/O pins |       |       |       |       |       |       |       |
|-----------------------|--------------------------------------|-------|-------|-------|-------|-------|-------|-------|--------------------------------------|-------|-------|-------|-------|-------|-------|-------|
|                       | Bit 7                                | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Bit 7                                | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| P0                    | —                                    | —     | —     | —     | —     | —     | —     | —     | ✓                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     |
| P2                    | ✓                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     |
| P3                    | —                                    | —     | —     | —     | —     | —     | —     | —     | ✓                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     |
| P5                    | —                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | —                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     |
| P7                    | —                                    | —     | —     | —     | —     | —     | ✓     | —     | —                                    | —     | —     | —     | —     | ✓     | ✓     | ✓     |
| P8                    | ✓                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     |
| P9                    | —                                    | —     | —     | —     | —     | —     | ✓     | ✓     | —                                    | —     | —     | —     | —     | —     | ✓     | ✓     |

Notes:

1. The symbol “✓” indicates a programmable I/O port.
2. The symbol “—” indicates the settings should be made as follows:
  - Set 0 to the corresponding bits in the PDi (i = 0, 3, 5, 7, 9) register. When read, the content is 0.
  - Set 0 to the corresponding bits in the Pi (i = 0, 3, 5, 7, 9) register. When read, the content is 0.

**Table 1.3 Programmable I/O Ports Provided for Each Group (R8C/LA6A Group, R8C/LA8A Group)**

| Programmable I/O Port | R8C/LA6A Group<br>Total: 56 I/O pins |       |       |       |       |       |       |       | R8C/LA8A Group<br>Total: 72 I/O pins |       |       |       |       |       |       |       |
|-----------------------|--------------------------------------|-------|-------|-------|-------|-------|-------|-------|--------------------------------------|-------|-------|-------|-------|-------|-------|-------|
|                       | Bit 7                                | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Bit 7                                | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| P0                    | ✓                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     |
| P1                    | ✓                                    | ✓     | ✓     | ✓     | ✓     | ✓     | —     | —     | ✓                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     |
| P2                    | ✓                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     |
| P3                    | ✓                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     |
| P4                    | ✓                                    | ✓     | —     | —     | —     | —     | —     | —     | ✓                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     |
| P5                    | —                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | —                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     |
| P6                    | ✓                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | —     | ✓                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     |
| P7                    | —                                    | —     | —     | —     | —     | —     | —     | —     | —                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     |
| P8                    | ✓                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓                                    | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     |
| P9                    | —                                    | —     | —     | —     | —     | —     | ✓     | ✓     | —                                    | —     | —     | —     | —     | —     | ✓     | ✓     |

Notes:

1. The symbol “✓” indicates a programmable I/O port.
2. The symbol “—” indicates the settings should be made as follows:
  - Set 0 to the corresponding bits in the PDi (i = 1, 4 to 7, 9) register. When read, the content is 0.
  - Set 0 to the corresponding bits in the Pi (i = 1, 4 to 7, 9) register. When read, the content is 0.
  - Set 0 to the corresponding bits in the P7DRR register. When read, the content is 0.

**Table 1.4 LCD Display Function Pins Provided for Each Group  
(R8C/LA3A Group, R8C/LA5A Group)**

| Shared I/O Port | R8C/LA3A Group<br>Common output: Max. 4<br>Segment output: Max. 11 |         |         |         |        |                 |                 |                 | R8C/LA5A Group<br>Common output: Max. 4<br>Segment output: Max. 27 |         |         |         |        |                 |                 |                 |
|-----------------|--|---------|---------|---------|--------|-----------------|-----------------|-----------------|--|---------|---------|---------|--------|-----------------|-----------------|-----------------|
|                 | SEG 15   | SEG 14  | SEG 13  | SEG 12  | SEG 11 | SEG 10          | SEG 9           | SEG 8           | SEG 15   | SEG 14  | SEG 13  | SEG 12  | SEG 11 | SEG 10          | SEG 9           | SEG 8           |
| P0              | —  | —       | —       | —       | —      | —               | —               | —               | SEG 7  | SEG 6   | SEG 5   | SEG 4   | SEG 3  | SEG 2           | SEG 1           | SEG 0           |
| P2              | SEG 15   | SEG 14  | SEG 13  | SEG 12  | SEG 11 | SEG 10          | SEG 9           | SEG 8           | SEG 15   | SEG 14  | SEG 13  | SEG 12  | SEG 11 | SEG 10          | SEG 9           | SEG 8           |
| P3              | —  | —       | —       | —       | —      | —               | —               | —               | SEG 23   | SEG 22  | SEG 21  | SEG 20  | SEG 19 | SEG 18          | SEG 17          | SEG 16          |
| P5              | —  | VL3 (2) | VL2 (2) | VL1 (2) | COM 0  | COM 1<br>SEG 26 | COM 2<br>SEG 25 | COM 3<br>SEG 24 | —  | VL3 (2) | VL2 (2) | VL1 (2) | COM 0  | COM 1<br>SEG 26 | COM 2<br>SEG 25 | COM 3<br>SEG 24 |

## Notes:

1. The symbol “—” indicates there is no LCD display function. Set the corresponding bits to 0 by setting registers LSE0, LSE2, and LSE5 for these pins.
2. When using the LCD drive control circuit, set the corresponding bit in the LSE5 register to 1.

**Table 1.5 LCD Display Function Pins Provided for Each Group  
(R8C/LA6A Group, R8C/LA8A Group)**

| Shared I/O Port | R8C/LA6A Group<br>Common output: Max. 4<br>Segment output: Max. 32 |         |         |         |        |        |        |        | R8C/LA8A Group<br>Common output: Max. 4<br>Segment output: Max. 40 |         |         |         |        |        |        |        |
|-----------------|--|---------|---------|---------|--------|--------|--------|--------|--|---------|---------|---------|--------|--------|--------|--------|
|                 | SEG 7  | SEG 6   | SEG 5   | SEG 4   | SEG 3  | SEG 2  | SEG 1  | SEG 0  | SEG 7  | SEG 6   | SEG 5   | SEG 4   | SEG 3  | SEG 2  | SEG 1  | SEG 0  |
| P0              | SEG 7  | SEG 6   | SEG 5   | SEG 4   | SEG 3  | SEG 2  | SEG 1  | SEG 0  | SEG 7  | SEG 6   | SEG 5   | SEG 4   | SEG 3  | SEG 2  | SEG 1  | SEG 0  |
| P1              | SEG 15   | SEG 14  | SEG 13  | SEG 12  | SEG 11 | SEG 10 | —      | —      | SEG 15   | SEG 14  | SEG 13  | SEG 12  | SEG 11 | SEG 10 | SEG 9  | SEG 8  |
| P2              | SEG 23   | SEG 22  | SEG 21  | SEG 20  | SEG 19 | SEG 18 | SEG 17 | SEG 16 | SEG 23   | SEG 22  | SEG 21  | SEG 20  | SEG 19 | SEG 18 | SEG 17 | SEG 16 |
| P3              | SEG 31   | SEG 30  | SEG 29  | SEG 28  | SEG 27 | SEG 26 | SEG 25 | SEG 24 | SEG 31   | SEG 30  | SEG 29  | SEG 28  | SEG 27 | SEG 26 | SEG 25 | SEG 24 |
| P4              | SEG 39   | SEG 38  | —       | —       | —      | —      | —      | —      | SEG 39   | SEG 38  | SEG 37  | SEG 36  | SEG 35 | SEG 34 | SEG 33 | SEG 32 |
| P5              | —  | VL3 (2) | VL2 (2) | VL1 (2) | COM 0  | COM 1  | COM 2  | COM 3  | —  | VL3 (2) | VL2 (2) | VL1 (2) | COM 0  | COM 1  | COM 2  | COM 3  |

## Notes:

1. The symbol “—” indicates there is no LCD display function. Set the corresponding bits to 0 by setting registers LSE1, LSE4 and LSE5 for these pins.
2. When using the LCD drive control circuit, set the corresponding bit in the LSE5 register to 1.

### 1.1.3 Specifications

Tables 1.6 to 1.8 list the specifications.

**Table 1.6 Specifications (1)**

| Item                           | Function                  | Specification   |
|--------------------------------|---------------------------|---|
| CPU                            | Central processing unit   | R8C CPU core <ul style="list-style-type: none"> <li>• Number of fundamental instructions: 89</li> <li>• Minimum instruction execution time:<br/>50 ns (f(XIN) = 20 MHz, VCC = 2.7 V to 5.5 V)<br/>125 ns (f(XIN) = 8 MHz, VCC = 1.8 V to 5.5 V)</li> <li>• Multiplier: 16 bits × 16 bits → 32 bits</li> <li>• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits</li> <li>• Operating mode: Single-chip mode (address space: 1 Mbyte)</li> </ul>  |
| Memory                         | ROM/RAM<br>Data flash     | Refer to Tables 1.9 to 1.12 Product Lists.  |
| Power Supply Voltage Detection | Voltage detection circuit | <ul style="list-style-type: none"> <li>• Power-on reset</li> <li>• Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)</li> </ul>   |
| I/O Ports                      | Programmable I/O ports    | R8C/LA3A Group <ul style="list-style-type: none"> <li>• CMOS I/O ports: 26, selectable pull-up resistor <sup>(1)</sup></li> <li>• High current drive ports: 8</li> </ul>  |
|                                |                           | R8C/LA5A Group <ul style="list-style-type: none"> <li>• CMOS I/O ports: 44, selectable pull-up resistor <sup>(1)</sup></li> <li>• High current drive ports: 8</li> </ul>  |
|                                |                           | R8C/LA6A Group <ul style="list-style-type: none"> <li>• CMOS I/O ports: 56, selectable pull-up resistor <sup>(1)</sup></li> <li>• High current drive ports: 8</li> </ul>  |
|                                |                           | R8C/LA8A Group <ul style="list-style-type: none"> <li>• CMOS I/O ports: 72, selectable pull-up resistor <sup>(1)</sup></li> <li>• High current drive ports: 10</li> </ul>   |
| Clock                          | Clock generation circuits | 4 circuits: XIN clock oscillation circuit<br>XCIN clock oscillation circuit (32 kHz)<br>High-speed on-chip oscillator (with frequency adjustment function)<br>Low-speed on-chip oscillator <ul style="list-style-type: none"> <li>• Oscillation stop detection:<br/>XIN clock oscillation stop detection function</li> <li>• Frequency divider circuit:<br/>Division ratio selectable from 1, 2, 4, 8, and 16</li> <li>• Low-power-consumption modes:<br/>Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode, power-off mode</li> </ul> |
|                                |                           | Real-time clock (timer RH)  |
| Interrupts                     | R8C/LA3A Group            | <ul style="list-style-type: none"> <li>• Number of interrupt vectors: 69</li> <li>• External Interrupt: 13 (<math>\overline{\text{INT}} \times 5</math>, key input × 8)</li> <li>• Priority levels: 7 levels</li> </ul>   |
|                                | R8C/LA5A Group            | <ul style="list-style-type: none"> <li>• Number of interrupt vectors: 69</li> <li>• External Interrupt: 14 (<math>\overline{\text{INT}} \times 6</math>, key input × 8)</li> <li>• Priority levels: 7 levels</li> </ul>   |
|                                | R8C/LA6A Group            | <ul style="list-style-type: none"> <li>• Number of interrupt vectors: 69</li> </ul>   |
|                                | R8C/LA8A Group            | <ul style="list-style-type: none"> <li>• External Interrupt: 16 (<math>\overline{\text{INT}} \times 8</math>, key input × 8)</li> <li>• Priority levels: 7 levels</li> </ul>  |
| Watchdog Timer                 |                           | <ul style="list-style-type: none"> <li>• 14 bits × 1 (with prescaler)</li> <li>• Selectable reset start function</li> <li>• Selectable low-speed on-chip oscillator for watchdog timer</li> </ul>   |

Note:

1. No pull-up resistor is provided in the pins P5\_4 to P5\_6.

**Table 1.7 Specifications (2)**

| Item  | Function                            | Specification   |  |                                    |
|---|-------------------------------------|---|--|------------------------------------|
| Timer                                       | Timer RB0, Timer RB1                | 8 bits × 2 (with 8-bit prescaler)<br>Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |  |                                    |
|   | Timer RC                            | 16 bits × 1 (with 4 capture/compare registers)<br>Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin)                              |  |                                    |
|   | Timer RH                            | Real-time clock mode (counting of seconds, minutes, hours, day of the week, date, month, year), output compare mode   |  |                                    |
|   | Timer RJ0<br>Timer RJ1<br>Timer RJ2 | R8C/LA3A Group<br>R8C/LA5A Group<br>R8C/LA6A Group<br>R8C/LA8A Group  | Timer RJ0,<br>Timer RJ1<br><br>Timer RJ0,<br>Timer RJ1,<br>Timer RJ2 | 16 bits × 2<br><br><br>16 bits × 3 |
| Serial Interface                            | UART0                               | 1 channel<br>Clock synchronous serial I/O/UART  |  |                                    |
|   | UART2                               | 1 channel<br>Clock synchronous serial I/O/UART, I <sup>2</sup> C mode (I <sup>2</sup> C-bus), multiprocessor communication function   |  |                                    |
| Synchronous Serial Communication Unit (SSU) |                                     | 1 (shared with I <sup>2</sup> C-bus)  |  |                                    |
| I <sup>2</sup> C bus                        |                                     | 1 (shared with SSU)   |  |                                    |
| A/D Converter                               | R8C/LA3A Group                      | 10-bit resolution × 5 channels, including sample and hold function, with sweep mode, temperature sensor included (measurement temperature range: –20 to 85 °C (N version)/ –40 to 85 °C (D version))  |  |                                    |
|   | R8C/LA5A Group                      | 10-bit resolution × 7 channels, including sample and hold function, with sweep mode, temperature sensor included (measurement temperature range: –20 to 85 °C (N version)/ –40 to 85 °C (D version))  |  |                                    |
|   | R8C/LA6A Group                      | 10-bit resolution × 8 channels, including sample and hold function, with sweep mode, temperature sensor included (measurement temperature range: –20 to 85 °C (N version)/ –40 to 85 °C (D version))  |  |                                    |
|   | R8C/LA8A Group                      | 10-bit resolution × 12 channels, including sample and hold function, with sweep mode, temperature sensor included (measurement temperature range: –20 to 85 °C (N version)/ –40 to 85 °C (D version)) |  |                                    |
| Comparator B                                | R8C/LA3A Group                      | 1 circuit (comparator B1)   |  |                                    |
|   | R8C/LA5A Group                      | 2 circuits (comparator B1, comparator B3)   |  |                                    |
|   | R8C/LA6A Group                      |   |  |                                    |
|   | R8C/LA8A Group                      |   |  |                                    |

**Table 1.8 Specifications (3)**

| Item                                   | Function       | Specification  |
|--|----------------|--|
| LCD Drive Control Circuit              | R8C/LA3A Group | Common output: Max. 4 pins<br>Segment output: Max. 11 pins   |
|  | R8C/LA5A Group | Common output: Max. 4 pins<br>Segment output: Max. 27 pins   |
|  | R8C/LA6A Group | Common output: Max. 4 pins<br>Segment output: Max. 32 pins   |
|  | R8C/LA8A Group | Common output: Max. 4 pins<br>Segment output: Max. 40 pins   |
|  |                | <ul style="list-style-type: none"> <li>• Bias: 1/2, 1/3</li> <li>• Duty: static, 1/2, 1/3, 1/4</li> </ul>  |
| Flash Memory                           |                | <ul style="list-style-type: none"> <li>• Programming and erasure voltage: VCC = 1.8 V to 5.5 V (data flash VCC = 1.8 V to 5.5 V)</li> <li>• Programming and erasure endurance: 10,000 times (data flash)<br/>10,000 times (program ROM)</li> <li>• Program security: ROM code protect, ID code check</li> <li>• On-chip debug function</li> <li>• On-board flash rewrite function</li> </ul> |
| Operating Frequency/<br>Supply Voltage |                | f(XIN) = 20 MHz (VCC = 2.7 V to 5.5 V)<br>f(XIN) = 8 MHz (VCC = 1.8 V to 5.5 V)  |
| Current Consumption                    |                | Typ. 4.7 mA (VCC = 5.0 V, f(XIN) = 20 MHz)<br>Typ. 2.3 mA (VCC = 3.0 V, f(XIN) = 10 MHz)<br>Typ. 1.7 $\mu$ A (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz))<br>Typ. 0.5 $\mu$ A (VCC = 3.0 V, stop mode)<br>Typ. 1.3 $\mu$ A (VCC = 3.0 V, power-off 2 mode, timer RH enabled)<br>Typ. 0.01 $\mu$ A (VCC = 3.0 V, power-off 0 mode, timer RH disabled)  |
| Operating Ambient Temperature          |                | -20 to 85°C (N version)<br>-40 to 85°C (D version) (1)   |

Note:

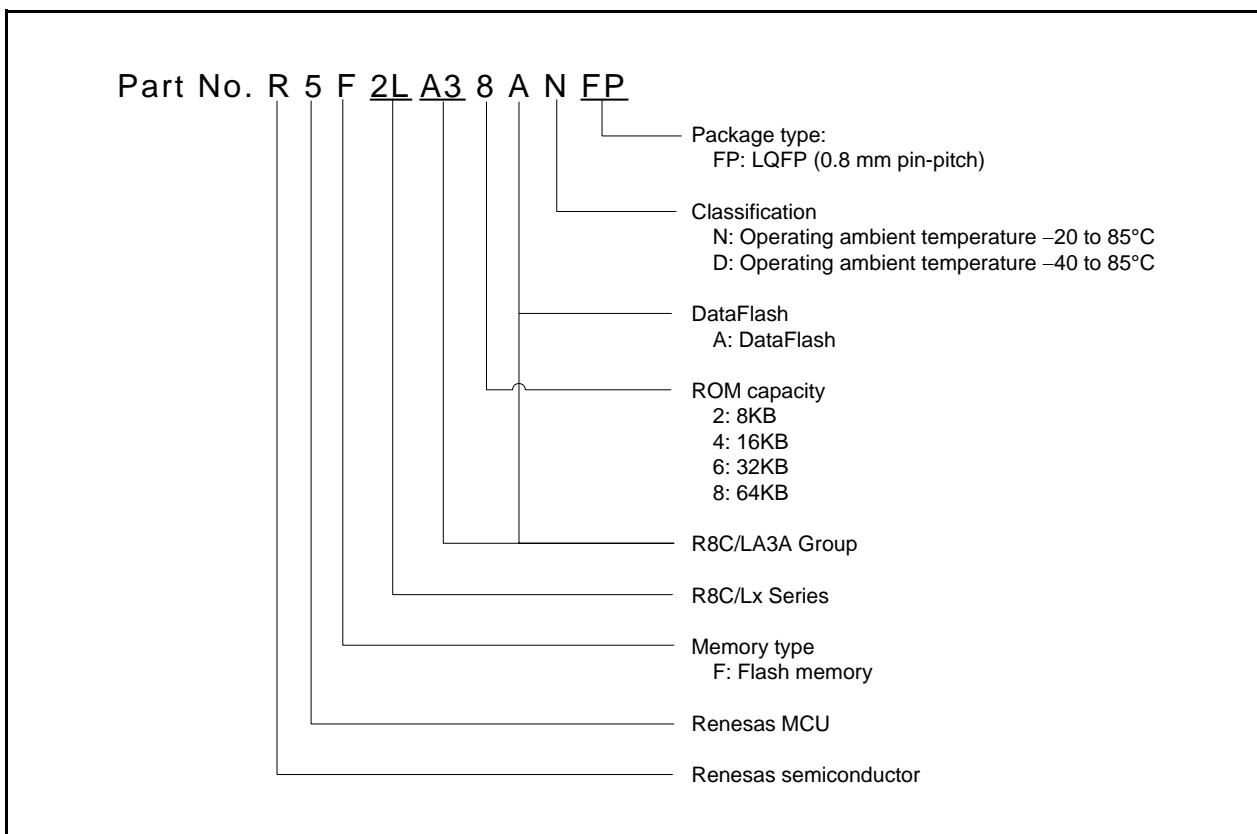
1. Specify the D version if D version functions are to be used.

## 1.2 Product Lists

Tables 1.9 to 1.12 list product information for each group. Figures 1.1 to 1.4 show the Correspondence of Part No., with Memory Size and Package for each group.

**Table 1.9 Product List for R8C/LA3A Group** **Current of Oct 2011**

| Part No.     | Internal ROM Capacity |             | Internal RAM Capacity | Package Type | Remarks   |
|--------------|-----------------------|-------------|-----------------------|--------------|-----------|
|              | Program ROM           | Data Flash  |                       |              |           |
| R5F2LA32ANFP | 8 Kbytes              | 1 Kbyte × 2 | 2 Kbytes              | PLQP0032GB-A | N Version |
| R5F2LA34ANFP | 16 Kbytes             | 1 Kbyte × 2 | 2 Kbytes              | PLQP0032GB-A |           |
| R5F2LA36ANFP | 32 Kbytes             | 1 Kbyte × 2 | 2 Kbytes              | PLQP0032GB-A |           |
| R5F2LA38ANFP | 64 Kbytes             | 1 Kbyte × 2 | 3.5 Kbytes            | PLQP0032GB-A |           |
| R5F2LA32ADFP | 8 Kbytes              | 1 Kbyte × 2 | 2 Kbytes              | PLQP0032GB-A | D Version |
| R5F2LA34ADFP | 16 Kbytes             | 1 Kbyte × 2 | 2 Kbytes              | PLQP0032GB-A |           |
| R5F2LA36ADFP | 32 Kbytes             | 1 Kbyte × 2 | 2 Kbytes              | PLQP0032GB-A |           |
| R5F2LA38ADFP | 64 Kbytes             | 1 Kbyte × 2 | 3.5 Kbytes            | PLQP0032GB-A |           |



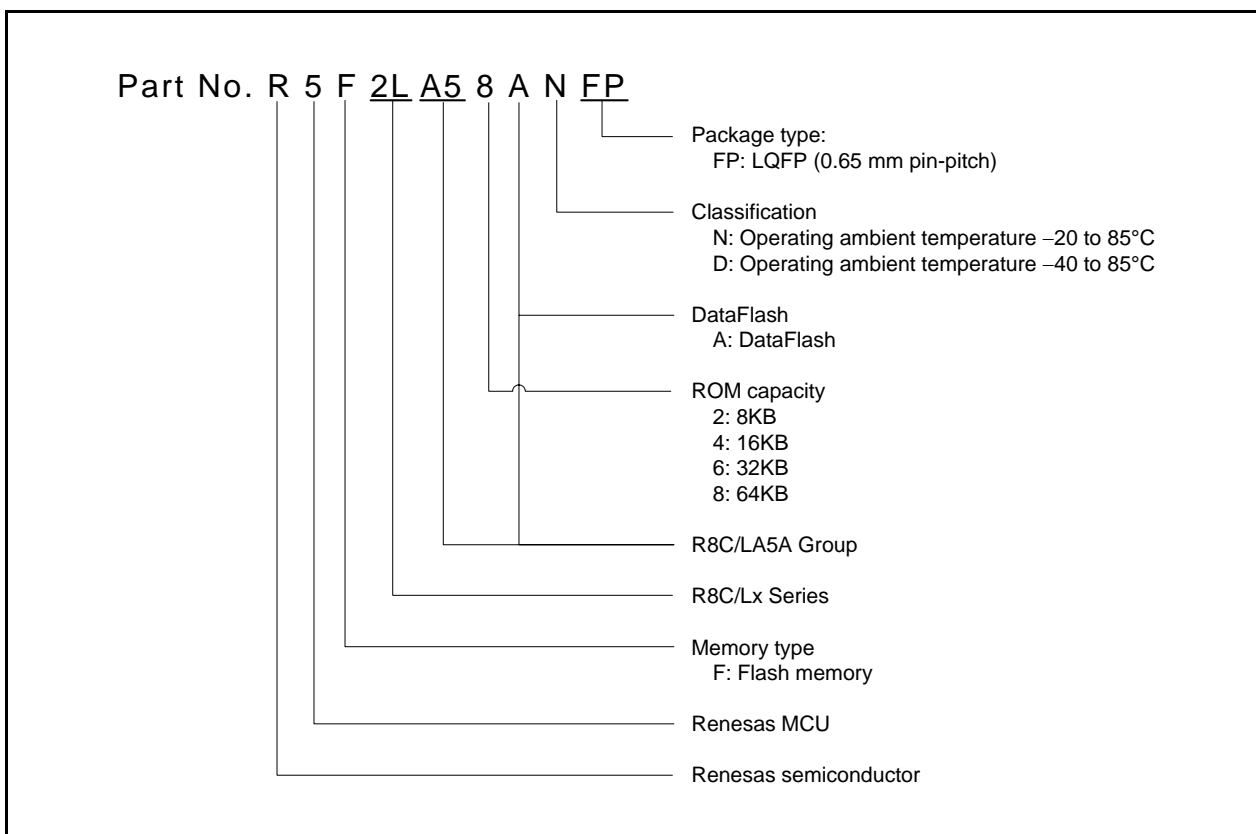
**Figure 1.1 Correspondence of Part No., with Memory Size and Package of R8C/LA3A Group**



**Table 1.10 Product List for R8C/LA5A Group**

**Current of Oct 2011**

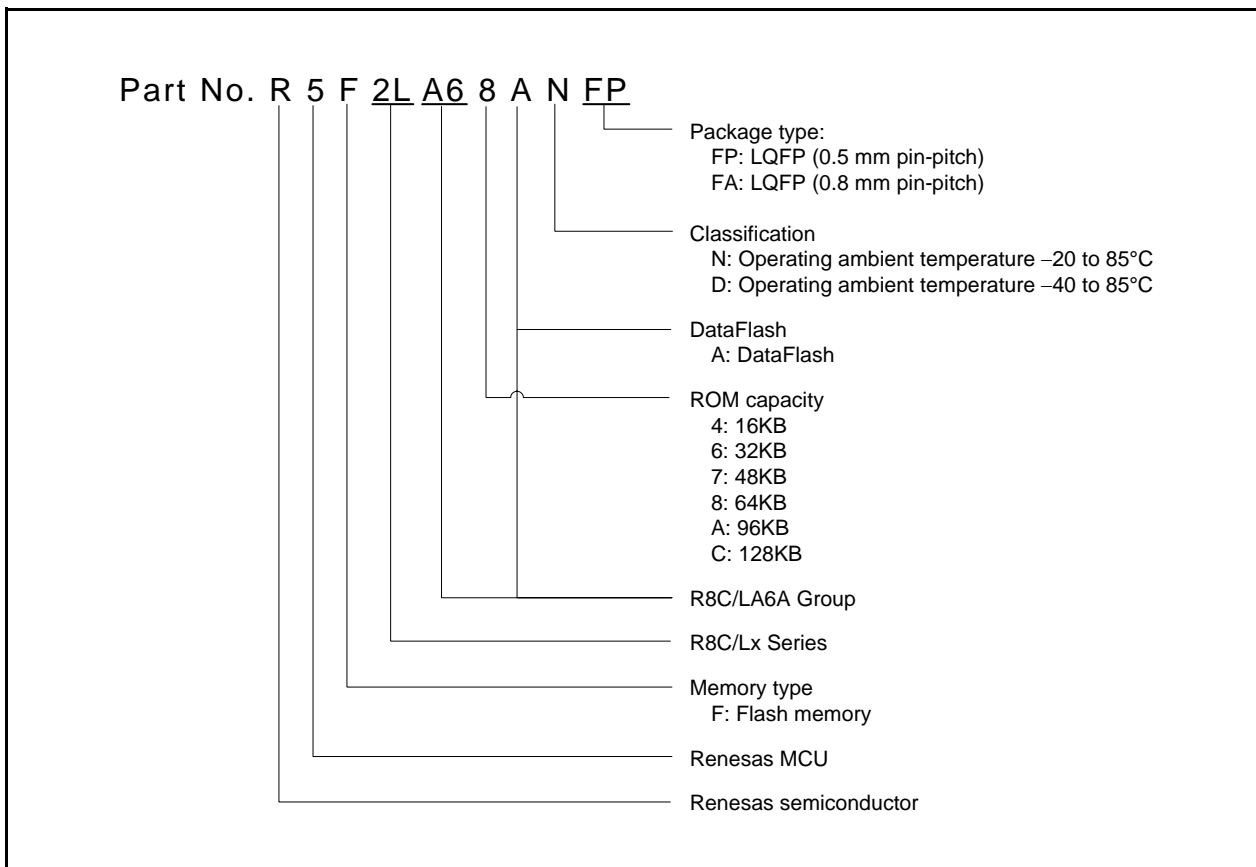
| Part No.     | Internal ROM Capacity |             | Internal RAM Capacity | Package Type | Remarks   |
|--------------|-----------------------|-------------|-----------------------|--------------|-----------|
|              | Program ROM           | Data Flash  |                       |              |           |
| R5F2LA52ANFP | 8 Kbytes              | 1 Kbyte × 2 | 2 Kbytes              | PLQP0052JA-A | N Version |
| R5F2LA54ANFP | 16 Kbytes             | 1 Kbyte × 2 | 2 Kbytes              | PLQP0052JA-A |           |
| R5F2LA56ANFP | 32 Kbytes             | 1 Kbyte × 2 | 2 Kbytes              | PLQP0052JA-A |           |
| R5F2LA58ANFP | 64 Kbytes             | 1 Kbyte × 2 | 3.5 Kbytes            | PLQP0052JA-A |           |
| R5F2LA52ADFP | 8 Kbytes              | 1 Kbyte × 2 | 2 Kbytes              | PLQP0052JA-A | D Version |
| R5F2LA54ADFP | 16 Kbytes             | 1 Kbyte × 2 | 2 Kbytes              | PLQP0052JA-A |           |
| R5F2LA56ADFP | 32 Kbytes             | 1 Kbyte × 2 | 2 Kbytes              | PLQP0052JA-A |           |
| R5F2LA58ADFP | 64 Kbytes             | 1 Kbyte × 2 | 3.5 Kbytes            | PLQP0052JA-A |           |



**Figure 1.2 Correspondence of Part No., with Memory Size and Package of R8C/LA5A Group**

**Table 1.11 Product List for R8C/LA6A Group** **Current of Oct 2011**

| Part No.     | Internal ROM Capacity |              | Internal RAM Capacity | Package Type | Remarks   |           |
|--------------|-----------------------|--------------|-----------------------|--------------|-----------|-----------|
|              | Program ROM           | Data Flash   |                       |              |           |           |
| R5F2LA64ANFP | 16 Kbytes             | 1 Kbyte × 2  | 2 Kbytes              | PLQP0064KB-A | N Version |           |
| R5F2LA64ANFA | 16 Kbytes             | 1 Kbyte × 2  | 2 Kbytes              | PLQP0064GA-A |           |           |
| R5F2LA66ANFP | 32 Kbytes             | 1 Kbyte × 2  | 2 Kbytes              | PLQP0064KB-A |           |           |
| R5F2LA66ANFA | 32 Kbytes             | 1 Kbyte × 2  | 2 Kbytes              | PLQP0064GA-A |           |           |
| R5F2LA67ANFP | 48 Kbytes             | 1 Kbyte × 2  | 3.5 Kbytes            | PLQP0064KB-A |           |           |
| R5F2LA67ANFA | 48 Kbytes             | 1 Kbyte × 2  | 3.5 Kbytes            | PLQP0064GA-A |           |           |
| R5F2LA68ANFP | 64 Kbytes             | 1 Kbyte × 2  | 3.5 Kbytes            | PLQP0064KB-A |           |           |
| R5F2LA68ANFA | 64 Kbytes             | 1 Kbyte × 2  | 3.5 Kbytes            | PLQP0064GA-A |           |           |
| R5F2LA6AANFP | 96 Kbytes             | 2 Kbytes × 2 | 5.5 Kbytes            | PLQP0064KB-A |           |           |
| R5F2LA6AANFA | 96 Kbytes             | 2 Kbytes × 2 | 5.5 Kbytes            | PLQP0064GA-A |           |           |
| R5F2LA6CANFP | 128 Kbytes            | 2 Kbytes × 2 | 5.5 Kbytes            | PLQP0064KB-A |           |           |
| R5F2LA6CANFA | 128 Kbytes            | 2 Kbytes × 2 | 5.5 Kbytes            | PLQP0064GA-A |           |           |
| R5F2LA64ADFP | 16 Kbytes             | 1 Kbyte × 2  | 2 Kbytes              | PLQP0064KB-A |           | D Version |
| R5F2LA64ADFA | 16 Kbytes             | 1 Kbyte × 2  | 2 Kbytes              | PLQP0064GA-A |           |           |
| R5F2LA66ADFP | 32 Kbytes             | 1 Kbyte × 2  | 2 Kbytes              | PLQP0064KB-A |           |           |
| R5F2LA66ADFA | 32 Kbytes             | 1 Kbyte × 2  | 2 Kbytes              | PLQP0064GA-A |           |           |
| R5F2LA67ADFP | 48 Kbytes             | 1 Kbyte × 2  | 3.5 Kbytes            | PLQP0064KB-A |           |           |
| R5F2LA67ADFA | 48 Kbytes             | 1 Kbyte × 2  | 3.5 Kbytes            | PLQP0064GA-A |           |           |
| R5F2LA68ADFP | 64 Kbytes             | 1 Kbyte × 2  | 3.5 Kbytes            | PLQP0064KB-A |           |           |
| R5F2LA68ADFA | 64 Kbytes             | 1 Kbyte × 2  | 3.5 Kbytes            | PLQP0064GA-A |           |           |
| R5F2LA6AADFP | 96 Kbytes             | 2 Kbytes × 2 | 5.5 Kbytes            | PLQP0064KB-A |           |           |
| R5F2LA6AADFA | 96 Kbytes             | 2 Kbytes × 2 | 5.5 Kbytes            | PLQP0064GA-A |           |           |
| R5F2LA6CADFP | 128 Kbytes            | 2 Kbytes × 2 | 5.5 Kbytes            | PLQP0064KB-A |           |           |
| R5F2LA6CADFA | 128 Kbytes            | 2 Kbytes × 2 | 5.5 Kbytes            | PLQP0064GA-A |           |           |



**Figure 1.3 Correspondence of Part No., with Memory Size and Package of R8C/LA6A Group**

Table 1.12 Product List for R8C/LA8A Group

Current of Oct 2011

| Part No.     | Internal ROM Capacity |              | Internal RAM Capacity | Package Type | Remarks   |
|--------------|-----------------------|--------------|-----------------------|--------------|-----------|
|              | Program ROM           | Data Flash   |                       |              |           |
| R5F2LA84ANFP | 16 Kbytes             | 1 Kbyte × 2  | 2 Kbytes              | PLQP0080KB-A | N Version |
| R5F2LA84ANFA | 16 Kbytes             | 1 Kbyte × 2  | 2 Kbytes              | PLQP0080JA-A |           |
| R5F2LA86ANFP | 32 Kbytes             | 1 Kbyte × 2  | 2 Kbytes              | PLQP0080KB-A |           |
| R5F2LA86ANFA | 32 Kbytes             | 1 Kbyte × 2  | 2 Kbytes              | PLQP0080JA-A |           |
| R5F2LA87ANFP | 48 Kbytes             | 1 Kbyte × 2  | 3.5 Kbytes            | PLQP0080KB-A |           |
| R5F2LA87ANFA | 48 Kbytes             | 1 Kbyte × 2  | 3.5 Kbytes            | PLQP0080JA-A |           |
| R5F2LA88ANFP | 64 Kbytes             | 1 Kbyte × 2  | 3.5 Kbytes            | PLQP0080KB-A |           |
| R5F2LA88ANFA | 64 Kbytes             | 1 Kbyte × 2  | 3.5 Kbytes            | PLQP0080JA-A |           |
| R5F2LA8AANFP | 96 Kbytes             | 2 Kbytes × 2 | 5.5 Kbytes            | PLQP0080KB-A |           |
| R5F2LA8AANFA | 96 Kbytes             | 2 Kbytes × 2 | 5.5 Kbytes            | PLQP0080JA-A |           |
| R5F2LA8CANFP | 128 Kbytes            | 2 Kbytes × 2 | 5.5 Kbytes            | PLQP0080KB-A |           |
| R5F2LA8CANFA | 128 Kbytes            | 2 Kbytes × 2 | 5.5 Kbytes            | PLQP0080JA-A |           |
| R5F2LA84ADFP | 16 Kbytes             | 1 Kbyte × 2  | 2 Kbytes              | PLQP0080KB-A | D Version |
| R5F2LA84ADFA | 16 Kbytes             | 1 Kbyte × 2  | 2 Kbytes              | PLQP0080JA-A |           |
| R5F2LA86ADFP | 32 Kbytes             | 1 Kbyte × 2  | 2 Kbytes              | PLQP0080KB-A |           |
| R5F2LA86ADFA | 32 Kbytes             | 1 Kbyte × 2  | 2 Kbytes              | PLQP0080JA-A |           |
| R5F2LA87ADFP | 48 Kbytes             | 1 Kbyte × 2  | 3.5 Kbytes            | PLQP0080KB-A |           |
| R5F2LA87ADFA | 48 Kbytes             | 1 Kbyte × 2  | 3.5 Kbytes            | PLQP0080JA-A |           |
| R5F2LA88ADFP | 64 Kbytes             | 1 Kbyte × 2  | 3.5 Kbytes            | PLQP0080KB-A |           |
| R5F2LA88ADFA | 64 Kbytes             | 1 Kbyte × 2  | 3.5 Kbytes            | PLQP0080JA-A |           |
| R5F2LA8AADFP | 96 Kbytes             | 2 Kbytes × 2 | 5.5 Kbytes            | PLQP0080KB-A |           |
| R5F2LA8AADFA | 96 Kbytes             | 2 Kbytes × 2 | 5.5 Kbytes            | PLQP0080JA-A |           |
| R5F2LA8CADFP | 128 Kbytes            | 2 Kbytes × 2 | 5.5 Kbytes            | PLQP0080KB-A |           |
| R5F2LA8CADFA | 128 Kbytes            | 2 Kbytes × 2 | 5.5 Kbytes            | PLQP0080JA-A |           |

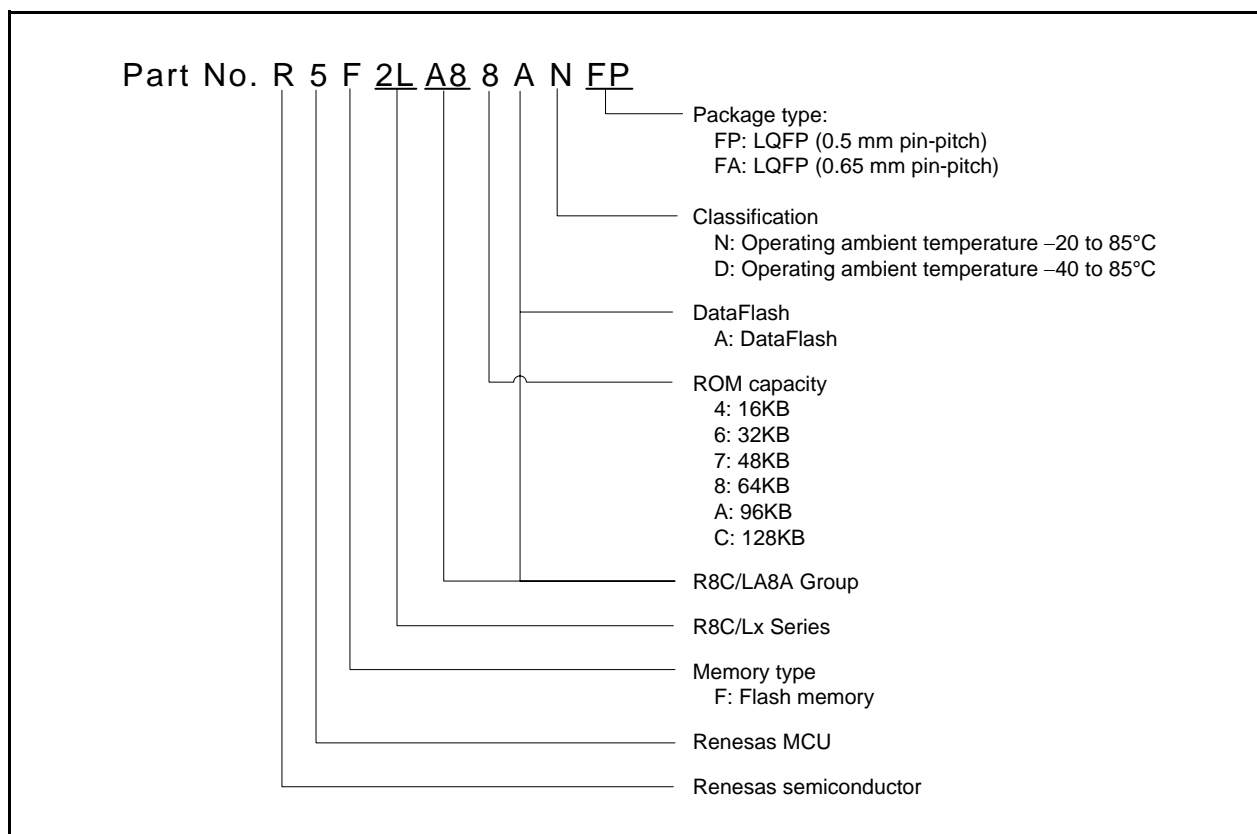


Figure 1.4 Correspondence of Part No., with Memory Size and Package of R8C/LA8A Group

### 1.3 Block Diagrams

Figure 1.5 shows a Block Diagram of R8C/LA3A Group. Figure 1.6 shows a Block Diagram of R8C/LA5A Group. Figure 1.7 shows a Block Diagram of R8C/LA6A Group. Figure 1.8 shows a Block Diagram of R8C/LA8A Group.

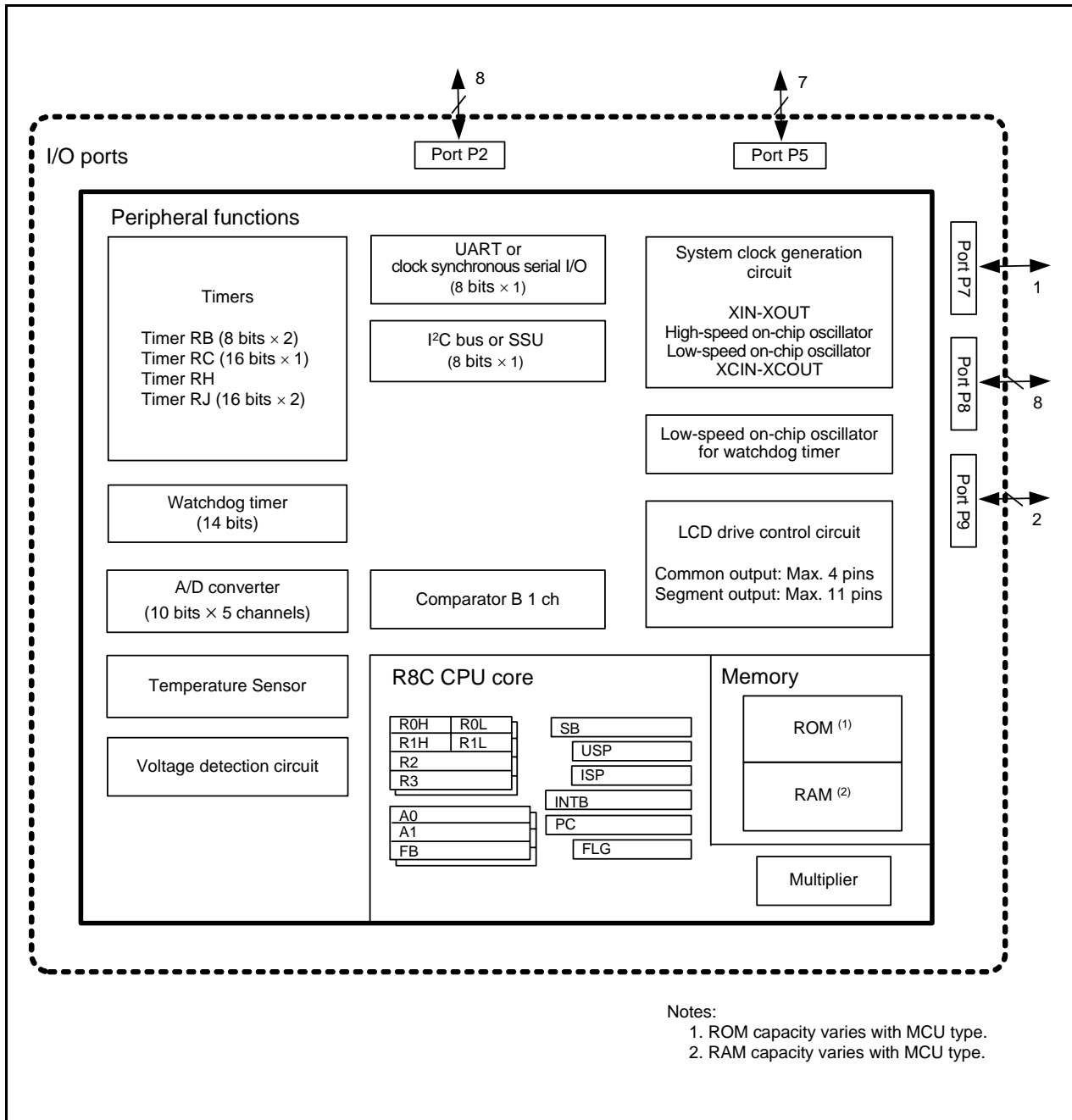


Figure 1.5 Block Diagram of R8C/LA3A Group

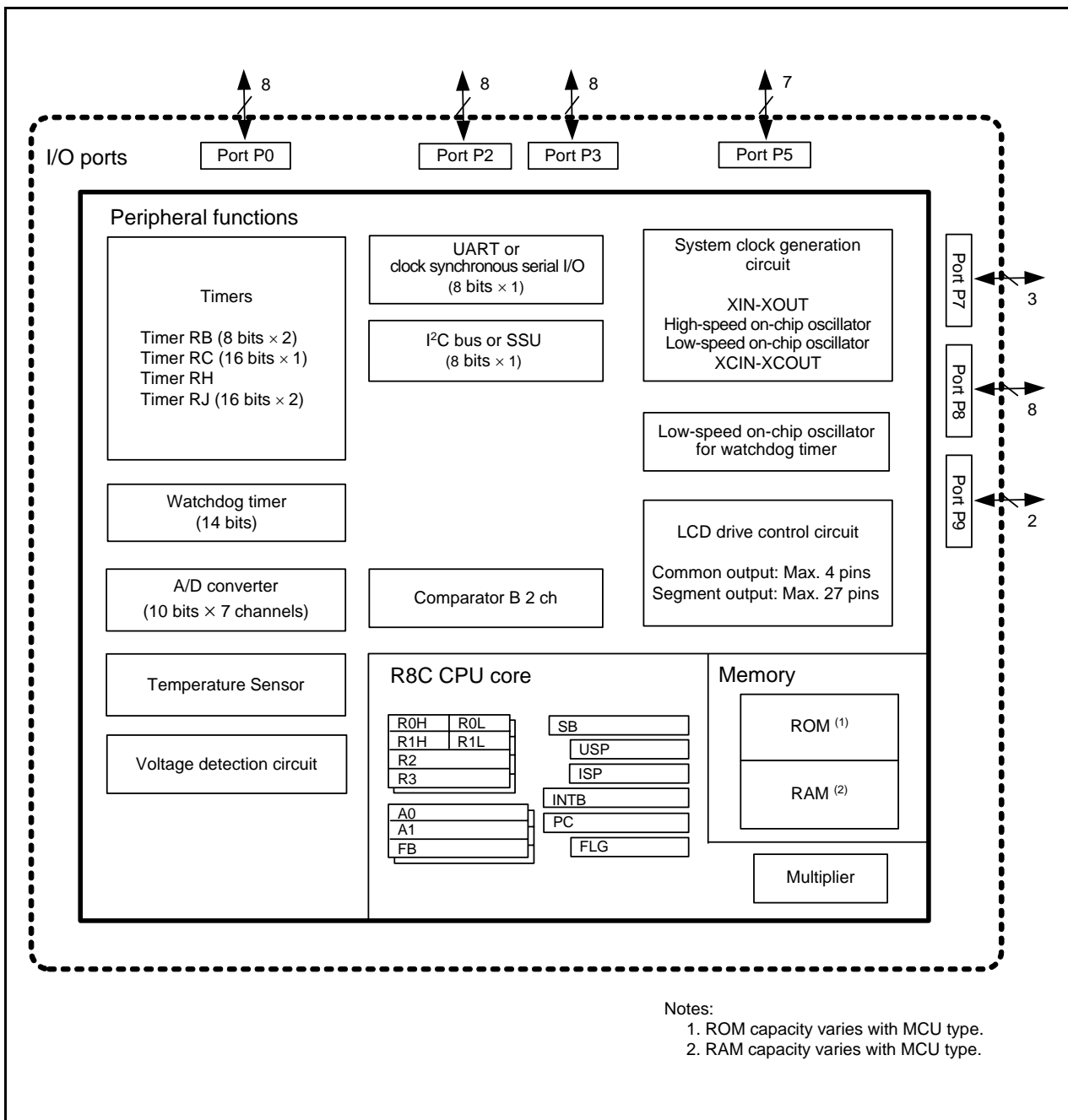


Figure 1.6 Block Diagram of R8C/LA5A Group

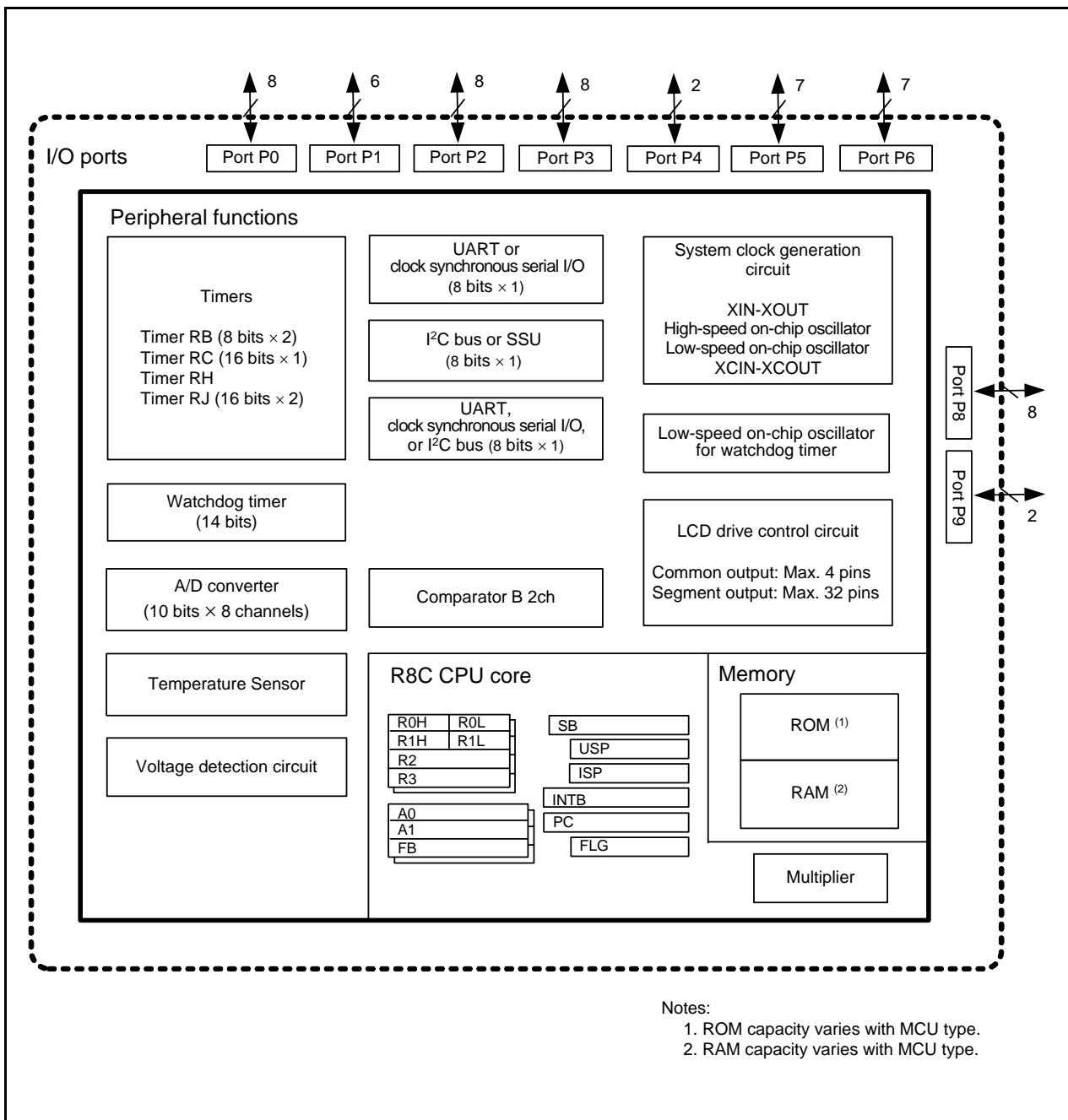


Figure 1.7 Block Diagram of R8C/LA6A Group

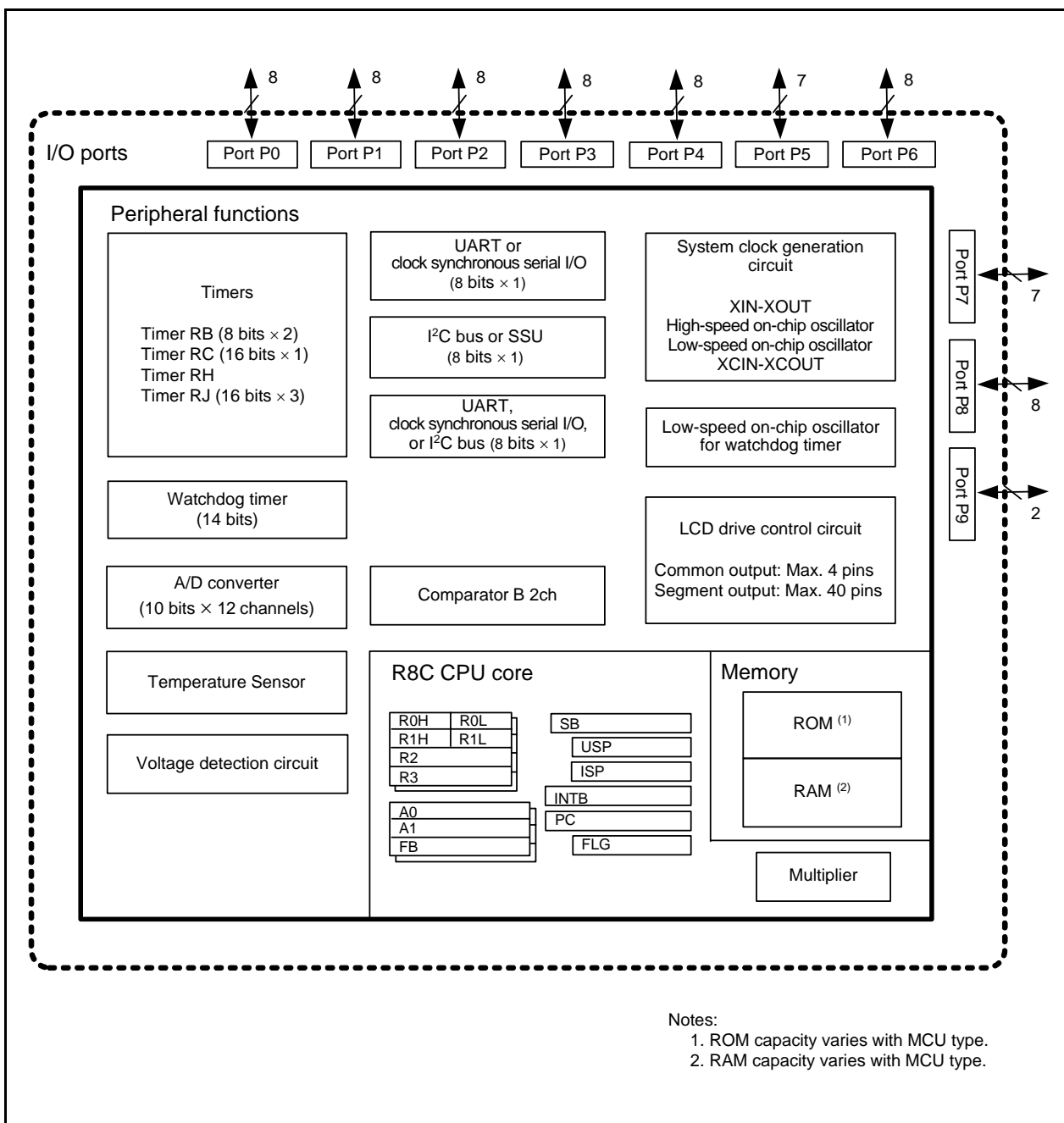
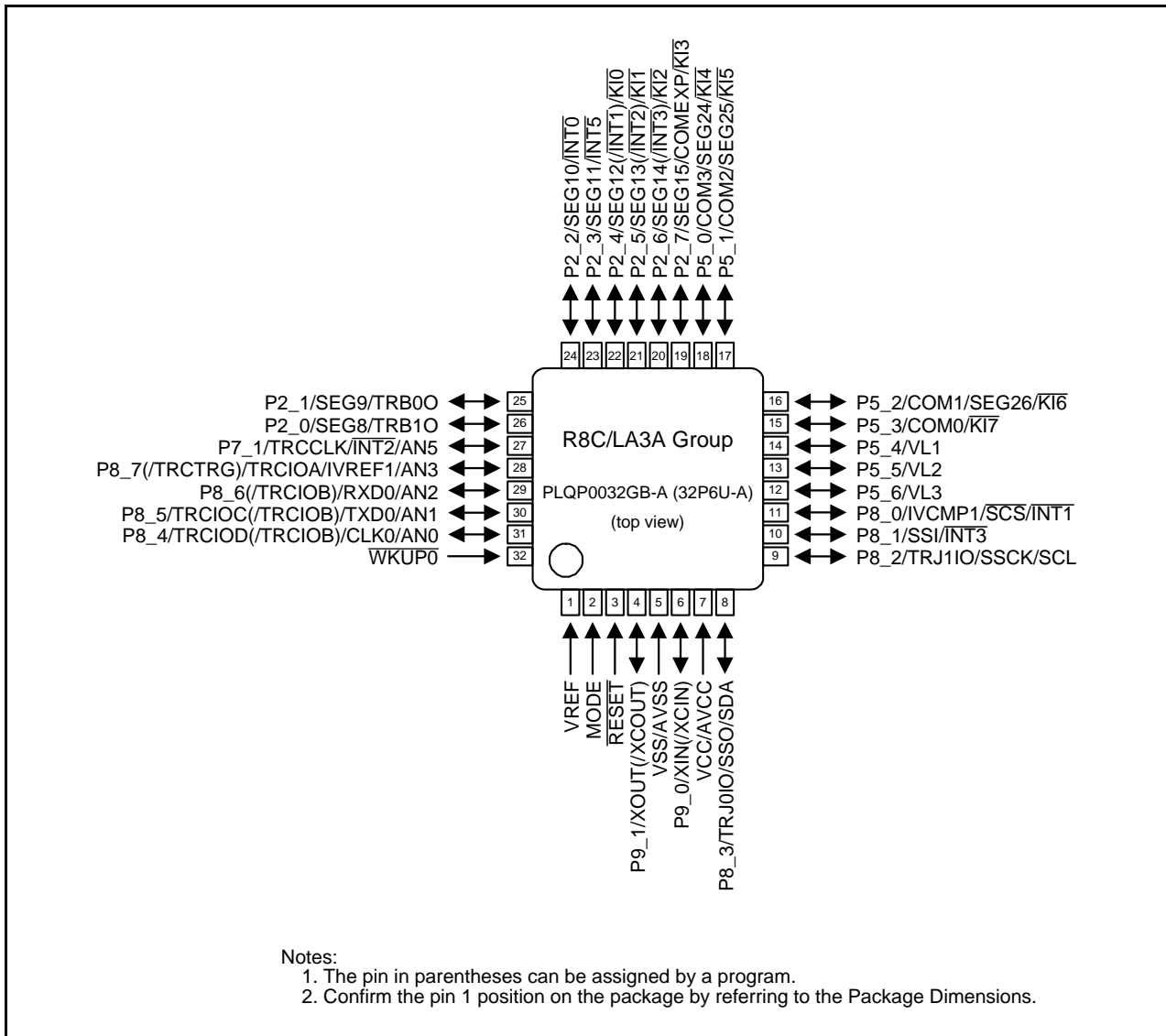


Figure 1.8 Block Diagram of R8C/LA8A Group

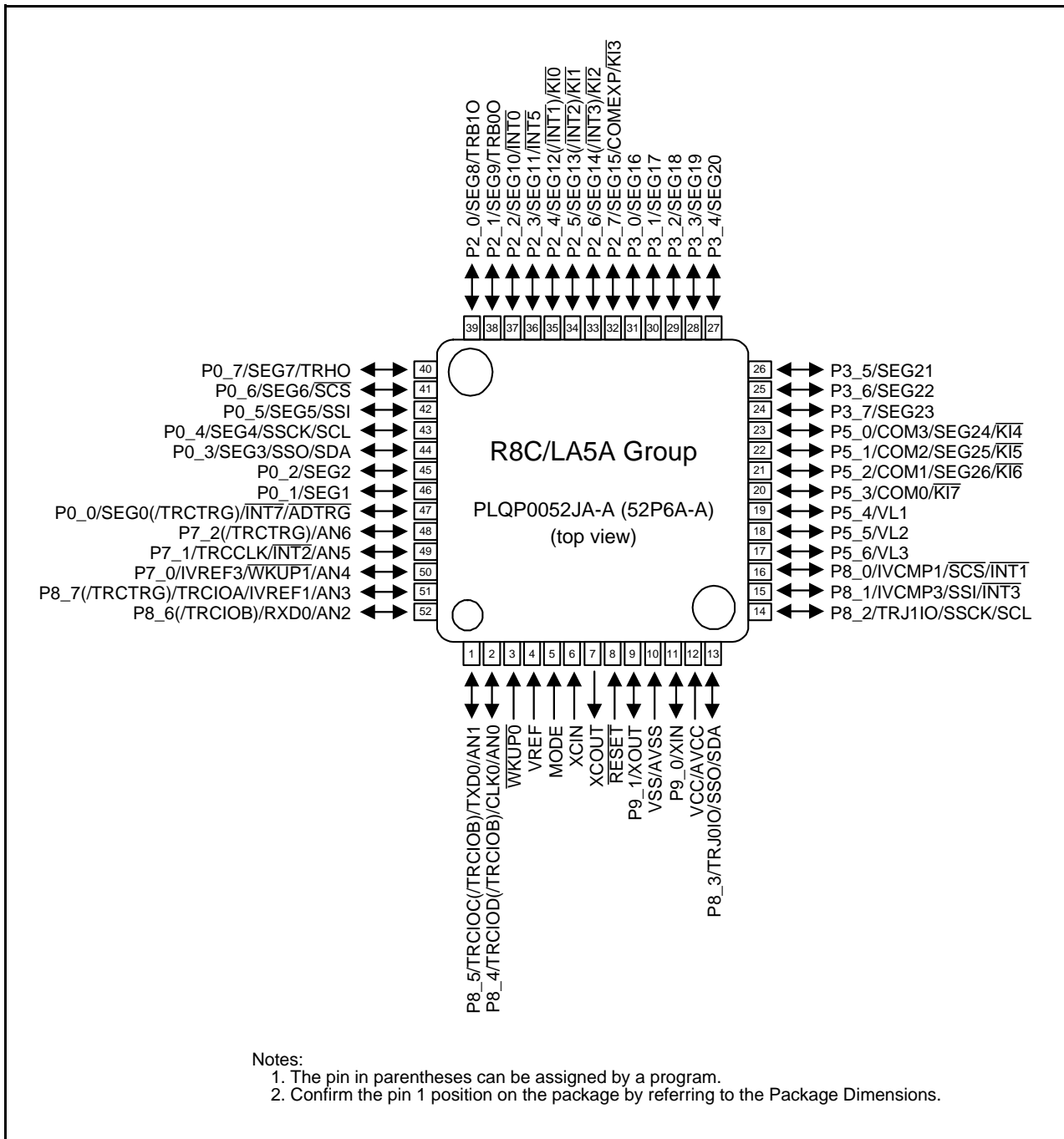
### 1.4 Pin Assignments

Figures 1.9 to 1.12 show pin assignments (top view). Tables 1.13 to 1.17 list the pin name information by pin number.



**Figure 1.9 Pin Assignment (Top View) of PLQP0032GB-A Package**





**Figure 1.10 Pin Assignment (Top View) of PLQP0052JA-A Package**

**Table 1.13 Pin Name Information by Pin Number (R8C/LA3A Group, R8C/LA5A Group)(1)**

| Pin Number |      | Control Pin         | Port | I/O Pin Functions for Peripheral Modules |                     |                  |                  |                      |                             |                           |
|------------|------|---------------------|------|--|---------------------|------------------|------------------|----------------------|-----------------------------|---------------------------|
| LA5A       | LA3A |                     |      | Interrupt                                | Timer               | Serial Interface | SSU              | I <sup>2</sup> C bus | A/D Converter, Comparator B | LCD drive Control Circuit |
| 1          | 30   |                     | P8_5 |  | TRCIOC/<br>(TRCIOB) | TXD0             |                  |                      | AN1                         |                           |
| 2          | 31   |                     | P8_4 |  | TRCIOD/<br>(TRCIOB) | CLK0             |                  |                      | AN0                         |                           |
| 3          | 32   | $\overline{WKUP0}$  |      |  |                     |                  |                  |                      |                             |                           |
| 4          | 1    | VREF                |      |  |                     |                  |                  |                      |                             |                           |
| 5          | 2    | MODE                |      |  |                     |                  |                  |                      |                             |                           |
| 6          |      | XCIN                |      |  |                     |                  |                  |                      |                             |                           |
| 7          |      | XCOUT               |      |  |                     |                  |                  |                      |                             |                           |
| 8          | 3    | $\overline{RESET}$  |      |  |                     |                  |                  |                      |                             |                           |
| 9          | 4    | XOUT<br>(XCOUT) (2) | P9_1 |  |                     |                  |                  |                      |                             |                           |
| 10         | 5    | VSS/AVSS            |      |  |                     |                  |                  |                      |                             |                           |
| 11         | 6    | XIN<br>(XCIN) (2)   | P9_0 |  |                     |                  |                  |                      |                             |                           |
| 12         | 7    | VCC/AVCC            |      |  |                     |                  |                  |                      |                             |                           |
| 13         | 8    |                     | P8_3 |  | TRJ0IO              |                  | SSO              | SDA                  |                             |                           |
| 14         | 9    |                     | P8_2 |  | TRJ1IO              |                  | SSCK             | SCL                  |                             |                           |
| 15         | 10   |                     | P8_1 | $\overline{INT3}$                        |                     |                  | SSI              |                      | IVCMP3 (3)                  |                           |
| 16         | 11   |                     | P8_0 | $\overline{INT1}$                        |                     |                  | $\overline{SCS}$ |                      | IVCMP1                      |                           |
| 17         | 12   |                     | P5_6 |  |                     |                  |                  |                      |                             | VL3                       |
| 18         | 13   |                     | P5_5 |  |                     |                  |                  |                      |                             | VL2                       |
| 19         | 14   |                     | P5_4 |  |                     |                  |                  |                      |                             | VL1                       |
| 20         | 15   |                     | P5_3 | $\overline{KI7}$                         |                     |                  |                  |                      |                             | COM0                      |
| 21         | 16   |                     | P5_2 | $\overline{KI6}$                         |                     |                  |                  |                      |                             | SEG26/<br>COM1            |
| 22         | 17   |                     | P5_1 | $\overline{KI5}$                         |                     |                  |                  |                      |                             | SEG25/<br>COM2            |
| 23         | 18   |                     | P5_0 | $\overline{KI4}$                         |                     |                  |                  |                      |                             | SEG24/<br>COM3            |
| 24         |      |                     | P3_7 |  |                     |                  |                  |                      |                             | SEG23                     |
| 25         |      |                     | P3_6 |  |                     |                  |                  |                      |                             | SEG22                     |
| 26         |      |                     | P3_5 |  |                     |                  |                  |                      |                             | SEG21                     |
| 27         |      |                     | P3_4 |  |                     |                  |                  |                      |                             | SEG20                     |
| 28         |      |                     | P3_3 |  |                     |                  |                  |                      |                             | SEG19                     |
| 29         |      |                     | P3_2 |  |                     |                  |                  |                      |                             | SEG18                     |
| 30         |      |                     | P3_1 |  |                     |                  |                  |                      |                             | SEG17                     |

Note:

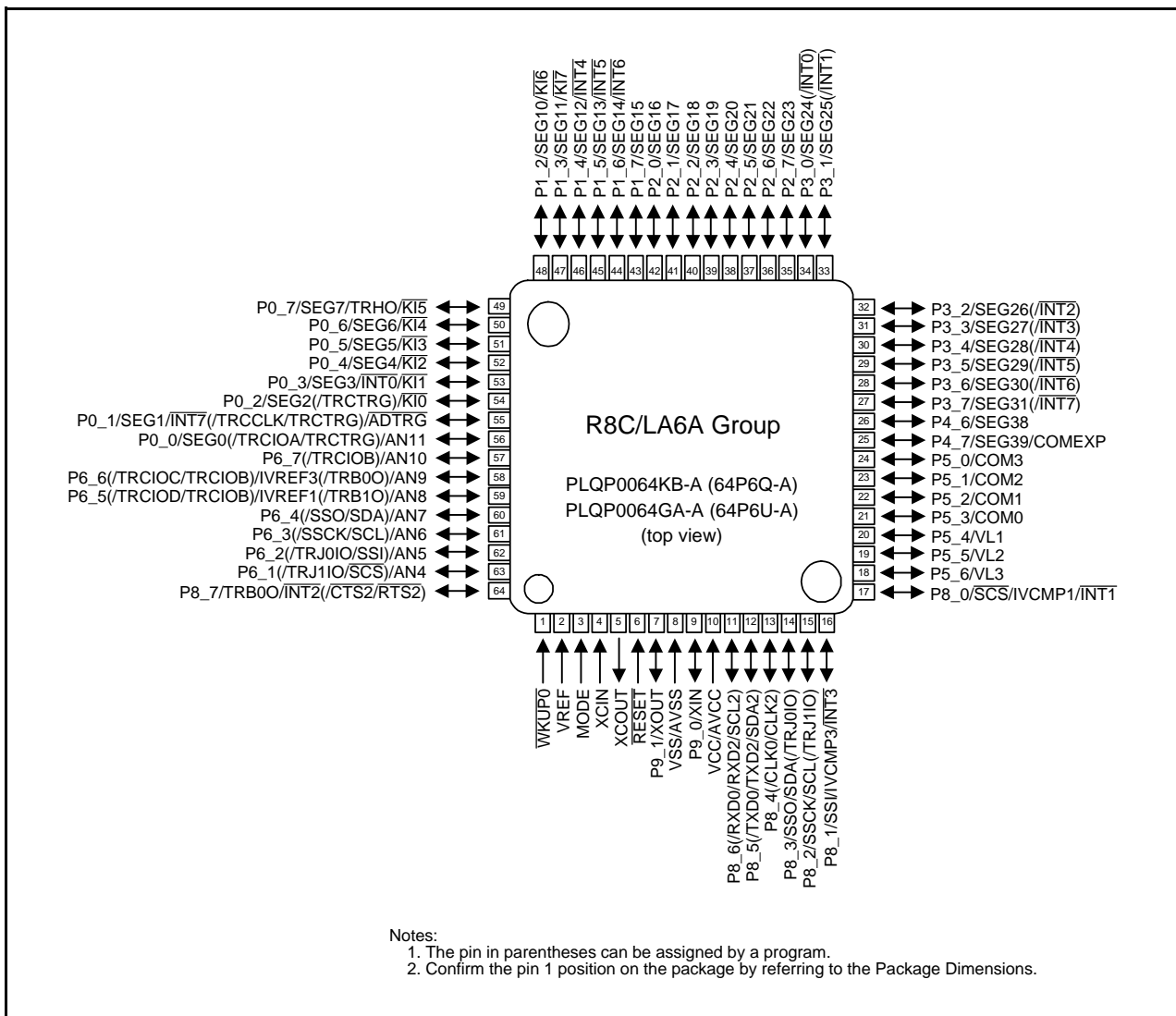
1. The pin in parentheses can be assigned by a program.
2. Pins (XCOUT) and (XCIN) are not available in the R8C/LA5A Group.
3. The IVCMP3 pin is not available in the R8C/LA3A Group.

**Table 1.14 Pin Name Information by Pin Number (R8C/LA3A Group, R8C/LA5A Group)(2)**

| Pin Number |      | Control Pin        | Port | I/O Pin Functions for Peripheral Modules |                     |                  |     |                      |                             |                           |
|------------|------|--------------------|------|--|---------------------|------------------|-----|----------------------|-----------------------------|---------------------------|
| LA5A       | LA3A |                    |      | Interrupt                                | Timer               | Serial Interface | SSU | I <sup>2</sup> C bus | A/D Converter, Comparator B | LCD drive Control Circuit |
| 31         |      |                    | P3_0 |  |                     |                  |     |                      |                             | SEG16                     |
| 32         | 19   |                    | P2_7 | $\overline{KI3}$                         |                     |                  |     |                      |                             | SEG15/COMEXP              |
| 33         | 20   |                    | P2_6 | $\overline{(INT3)/KI2}$                  |                     |                  |     |                      |                             | SEG14                     |
| 34         | 21   |                    | P2_5 | $\overline{(INT2)/KI1}$                  |                     |                  |     |                      |                             | SEG13                     |
| 35         | 22   |                    | P2_4 | $\overline{(INT1)/KI0}$                  |                     |                  |     |                      |                             | SEG12                     |
| 36         | 23   |                    | P2_3 | $\overline{INT5}$                        |                     |                  |     |                      |                             | SEG11                     |
| 37         | 24   |                    | P2_2 | $\overline{INT0}$                        |                     |                  |     |                      |                             | SEG10                     |
| 38         | 25   |                    | P2_1 |  | TRB00               |                  |     |                      |                             | SEG9                      |
| 39         | 26   |                    | P2_0 |  | TRB10               |                  |     |                      |                             | SEG8                      |
| 40         |      |                    | P0_7 |  | TRHO                |                  |     |                      |                             | SEG7                      |
| 41         |      |                    | P0_6 |  |                     |                  |     | $\overline{SCS}$     |                             | SEG6                      |
| 42         |      |                    | P0_5 |  |                     |                  |     | SSI                  |                             | SEG5                      |
| 43         |      |                    | P0_4 |  |                     |                  |     | SSCK                 | SCL                         | SEG4                      |
| 44         |      |                    | P0_3 |  |                     |                  |     | SSO                  | SDA                         | SEG3                      |
| 45         |      |                    | P0_2 |  |                     |                  |     |                      |                             | SEG2                      |
| 46         |      |                    | P0_1 |  |                     |                  |     |                      |                             | SEG1                      |
| 47         |      |                    | P0_0 | $\overline{INT7}$                        | (TRCTRG)            |                  |     |                      | $\overline{ADTRG}$          | SEG0                      |
| 48         |      |                    | P7_2 |  | (TRCTRG)            |                  |     |                      | AN6                         |                           |
| 49         | 27   |                    | P7_1 | $\overline{INT2}$                        | TRCCLK              |                  |     |                      | AN5                         |                           |
| 50         |      | $\overline{WKUP1}$ | P7_0 |  |                     |                  |     |                      | AN4/IVREF3                  |                           |
| 51         | 28   |                    | P8_7 |  | TRCIOA/<br>(TRCTRG) |                  |     |                      | AN3/IVREF1                  |                           |
| 52         | 29   |                    | P8_6 |  | (TRCIOB)            | RXD0             |     |                      | AN2                         |                           |

Note:

1. The pin in parentheses can be assigned by a program.



- Notes:
1. The pin in parentheses can be assigned by a program.
  2. Confirm the pin 1 position on the package by referring to the Package Dimensions.

Figure 1.11 Pin Assignment (Top View) of PLQP0064KB-A and PLQP0064GA-A Packages

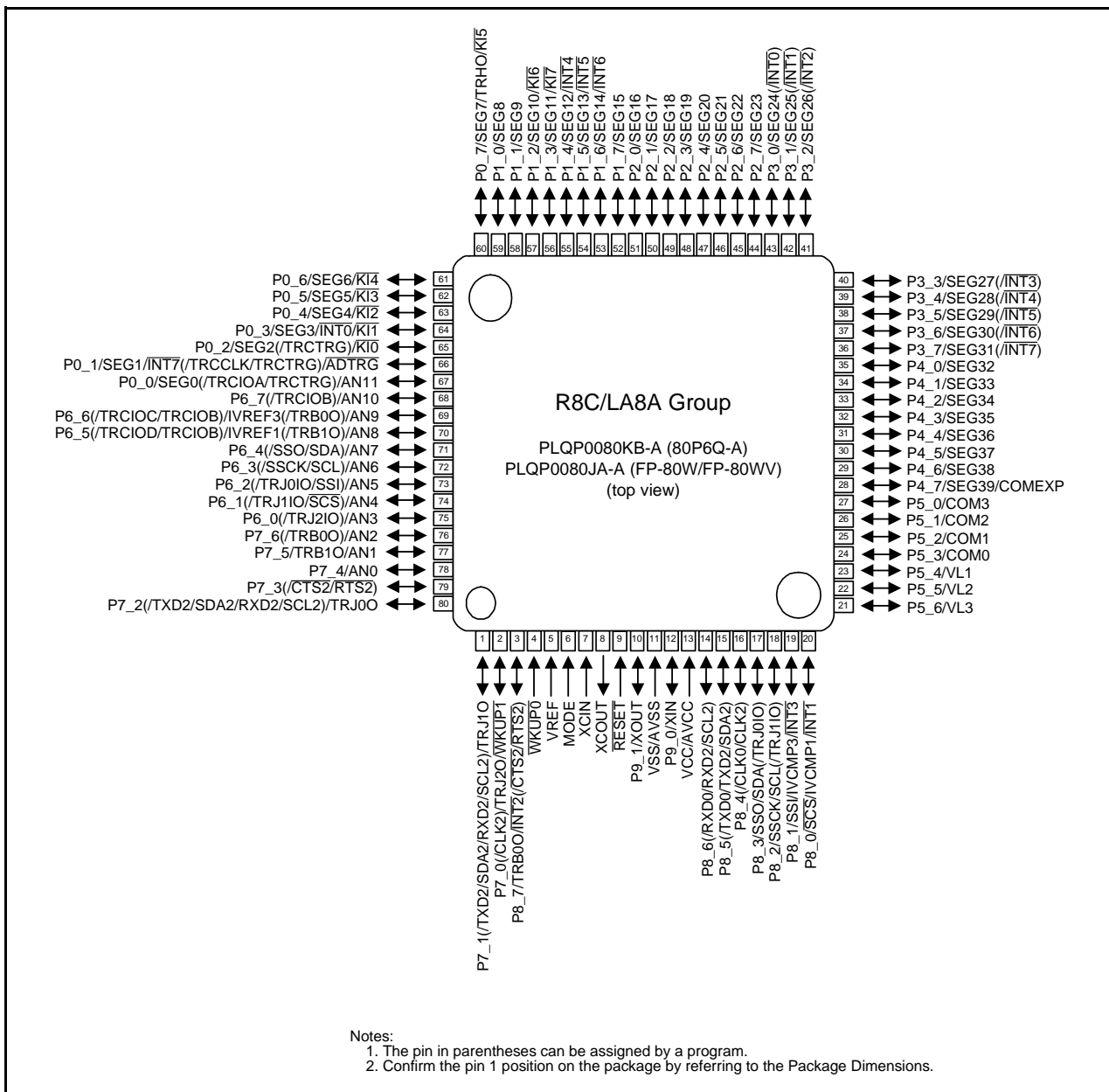


Figure 1.12 Pin Assignment (Top View) of PLQP0080KB-A and PLQP0080JA-A Packages

**Table 1.15 Pin Name Information by Pin Number (R8C/LA6A Group, R8C/LA8A Group)(1)**

| Pin Number |      | Control Pin               | Port | I/O Pin Functions for Peripheral Modules |          |                       |                         |                      |                             |                           |
|------------|------|---------------------------|------|--|----------|-----------------------|-------------------------|----------------------|-----------------------------|---------------------------|
| LA8A       | LA6A |                           |      | Interrupt                                | Timer    | Serial Interface      | SSU                     | I <sup>2</sup> C bus | A/D Converter, Comparator B | LCD drive Control Circuit |
| 1          |      |                           | P7_1 |  | TRJ1O    | (TXD2/SDA2/RXD2/SCL2) |                         |                      |                             |                           |
| 2          |      | $\overline{\text{WKUP1}}$ | P7_0 |  | TRJ2O    | (CLK2)                |                         |                      |                             |                           |
| 3          | 64   |                           | P8_7 | $\overline{\text{INT2}}$                 | TRB0O    | (CTS2/RTS2)           |                         |                      |                             |                           |
| 4          | 1    | $\overline{\text{WKUP0}}$ |      |  |          |                       |                         |                      |                             |                           |
| 5          | 2    | VREF                      |      |  |          |                       |                         |                      |                             |                           |
| 6          | 3    | MODE                      |      |  |          |                       |                         |                      |                             |                           |
| 7          | 4    | XCIN                      |      |  |          |                       |                         |                      |                             |                           |
| 8          | 5    | XCOUT                     |      |  |          |                       |                         |                      |                             |                           |
| 9          | 6    | $\overline{\text{RESET}}$ |      |  |          |                       |                         |                      |                             |                           |
| 10         | 7    | XOUT                      | P9_1 |  |          |                       |                         |                      |                             |                           |
| 11         | 8    | VSS/<br>AVSS              |      |  |          |                       |                         |                      |                             |                           |
| 12         | 9    | XIN                       | P9_0 |  |          |                       |                         |                      |                             |                           |
| 13         | 10   | VCC/<br>AVCC              |      |  |          |                       |                         |                      |                             |                           |
| 14         | 11   |                           | P8_6 |  |          | (RXD0/RXD2/SCL2)      |                         |                      |                             |                           |
| 15         | 12   |                           | P8_5 |  |          | (TXD0/TXD2/SDA2)      |                         |                      |                             |                           |
| 16         | 13   |                           | P8_4 |  |          | (CLK0/CLK2)           |                         |                      |                             |                           |
| 17         | 14   |                           | P8_3 |  | (TRJ0IO) |                       | SSO                     | SDA                  |                             |                           |
| 18         | 15   |                           | P8_2 |  | (TRJ1IO) |                       | SSCK                    | SCL                  |                             |                           |
| 19         | 16   |                           | P8_1 | $\overline{\text{INT3}}$                 |          |                       | SSI                     |                      | IVCMP3                      |                           |
| 20         | 17   |                           | P8_0 | $\overline{\text{INT1}}$                 |          |                       | $\overline{\text{SCS}}$ |                      | IVCMP1                      |                           |
| 21         | 18   |                           | P5_6 |  |          |                       |                         |                      |                             | VL3                       |
| 22         | 19   |                           | P5_5 |  |          |                       |                         |                      |                             | VL2                       |
| 23         | 20   |                           | P5_4 |  |          |                       |                         |                      |                             | VL1                       |
| 24         | 21   |                           | P5_3 |  |          |                       |                         |                      |                             | COM0                      |
| 25         | 22   |                           | P5_2 |  |          |                       |                         |                      |                             | COM1                      |
| 26         | 23   |                           | P5_1 |  |          |                       |                         |                      |                             | COM2                      |
| 27         | 24   |                           | P5_0 |  |          |                       |                         |                      |                             | COM3                      |
| 28         | 25   |                           | P4_7 |  |          |                       |                         |                      |                             | SEG39/<br>COMEXP          |
| 29         | 26   |                           | P4_6 |  |          |                       |                         |                      |                             | SEG38                     |
| 30         |      |                           | P4_5 |  |          |                       |                         |                      |                             | SEG37                     |

Note:

1. The pin in parentheses can be assigned by a program.

**Table 1.16 Pin Name Information by Pin Number (R8C/LA6A Group, R8C/LA8A Group)(2)**

| Pin Number |      | Control Pin | Port | I/O Pin Functions for Peripheral Modules              |   |                  |     |                      |                             |                           |
|------------|------|-------------|------|---|---|------------------|-----|----------------------|-----------------------------|---------------------------|
| LA8A       | LA6A |             |      | Interrupt   | Timer                                     | Serial Interface | SSU | I <sup>2</sup> C bus | A/D Converter, Comparator B | LCD drive Control Circuit |
| 31         |      |             | P4_4 |   |   |                  |     |                      |                             | SEG36                     |
| 32         |      |             | P4_3 |   |   |                  |     |                      |                             | SEG35                     |
| 33         |      |             | P4_2 |   |   |                  |     |                      |                             | SEG34                     |
| 34         |      |             | P4_1 |   |   |                  |     |                      |                             | SEG33                     |
| 35         |      |             | P4_0 |   |   |                  |     |                      |                             | SEG32                     |
| 36         | 27   |             | P3_7 | ( $\overline{\text{INT7}}$ )                          |   |                  |     |                      |                             | SEG31                     |
| 37         | 28   |             | P3_6 | ( $\overline{\text{INT6}}$ )                          |   |                  |     |                      |                             | SEG30                     |
| 38         | 29   |             | P3_5 | ( $\overline{\text{INT5}}$ )                          |   |                  |     |                      |                             | SEG29                     |
| 39         | 30   |             | P3_4 | ( $\overline{\text{INT4}}$ )                          |   |                  |     |                      |                             | SEG28                     |
| 40         | 31   |             | P3_3 | ( $\overline{\text{INT3}}$ )                          |   |                  |     |                      |                             | SEG27                     |
| 41         | 32   |             | P3_2 | ( $\overline{\text{INT2}}$ )                          |   |                  |     |                      |                             | SEG26                     |
| 42         | 33   |             | P3_1 | ( $\overline{\text{INT1}}$ )                          |   |                  |     |                      |                             | SEG25                     |
| 43         | 34   |             | P3_0 | ( $\overline{\text{INT0}}$ )                          |   |                  |     |                      |                             | SEG24                     |
| 44         | 35   |             | P2_7 |   |   |                  |     |                      |                             | SEG23                     |
| 45         | 36   |             | P2_6 |   |   |                  |     |                      |                             | SEG22                     |
| 46         | 37   |             | P2_5 |   |   |                  |     |                      |                             | SEG21                     |
| 47         | 38   |             | P2_4 |   |   |                  |     |                      |                             | SEG20                     |
| 48         | 39   |             | P2_3 |   |   |                  |     |                      |                             | SEG19                     |
| 49         | 40   |             | P2_2 |   |   |                  |     |                      |                             | SEG18                     |
| 50         | 41   |             | P2_1 |   |   |                  |     |                      |                             | SEG17                     |
| 51         | 42   |             | P2_0 |   |   |                  |     |                      |                             | SEG16                     |
| 52         | 43   |             | P1_7 |   |   |                  |     |                      |                             | SEG15                     |
| 53         | 44   |             | P1_6 | $\overline{\text{INT6}}$                              |   |                  |     |                      |                             | SEG14                     |
| 54         | 45   |             | P1_5 | $\overline{\text{INT5}}$                              |   |                  |     |                      |                             | SEG13                     |
| 55         | 46   |             | P1_4 | $\overline{\text{INT4}}$                              |   |                  |     |                      |                             | SEG12                     |
| 56         | 47   |             | P1_3 | $\overline{\text{KI7}}$                               |   |                  |     |                      |                             | SEG11                     |
| 57         | 48   |             | P1_2 | $\overline{\text{KI6}}$                               |   |                  |     |                      |                             | SEG10                     |
| 58         |      |             | P1_1 |   |   |                  |     |                      |                             | SEG9                      |
| 59         |      |             | P1_0 |   |   |                  |     |                      |                             | SEG8                      |
| 60         | 49   |             | P0_7 | $\overline{\text{KI5}}$                               | TRHO                                      |                  |     |                      |                             | SEG7                      |
| 61         | 50   |             | P0_6 | $\overline{\text{KI4}}$                               |   |                  |     |                      |                             | SEG6                      |
| 62         | 51   |             | P0_5 | $\overline{\text{KI3}}$                               |   |                  |     |                      |                             | SEG5                      |
| 63         | 52   |             | P0_4 | $\overline{\text{KI2}}$                               |   |                  |     |                      |                             | SEG4                      |
| 64         | 53   |             | P0_3 | $\overline{\text{KI1}}$ /<br>$\overline{\text{INT0}}$ |   |                  |     |                      |                             | SEG3                      |
| 65         | 54   |             | P0_2 | $\overline{\text{KI0}}$                               | (TRCTR $\overline{\text{G}}$ )            |                  |     |                      |                             | SEG2                      |
| 66         | 55   |             | P0_1 | $\overline{\text{INT7}}$                              | (TRCTR $\overline{\text{G}}$ /<br>TRCCLK) |                  |     |                      | $\overline{\text{ADTRG}}$   | SEG1                      |
| 67         | 56   |             | P0_0 |   | (TRCIOA/<br>TRCTR $\overline{\text{G}}$ ) |                  |     |                      | AN11                        | SEG0                      |
| 68         | 57   |             | P6_7 |   | (TRCIOB)                                  |                  |     |                      | AN10                        |                           |

Note:

1. The pin in parentheses can be assigned by a program.

**Table 1.17 Pin Name Information by Pin Number (R8C/LA6A Group, R8C/LA8A Group)(3)**

| Pin Number |      | Control Pin | Port | I/O Pin Functions for Peripheral Modules |                               |                           |        |                      |                             |                           |
|------------|------|-------------|------|--|-------------------------------|---------------------------|--------|----------------------|-----------------------------|---------------------------|
| LA8A       | LA6A |             |      | Interrupt                                | Timer                         | Serial Interface          | SSU    | I <sup>2</sup> C bus | A/D Converter, Comparator B | LCD drive Control Circuit |
| 69         | 58   |             | P6_6 |  | (TRB00/<br>TRCIOB/<br>TRCIOA) |                           |        |                      | AN9/IVREF3                  |                           |
| 70         | 59   |             | P6_5 |  | (TRB10/<br>TRCIOB/<br>TRCIOD) |                           |        |                      | AN8/IVREF1                  |                           |
| 71         | 60   |             | P6_4 |  |                               |                           | (SSO)  | (SDA)                | AN7                         |                           |
| 72         | 61   |             | P6_3 |  |                               |                           | (SSCK) | (SCL)                | AN6                         |                           |
| 73         | 62   |             | P6_2 |  | (TRJ0IO)                      |                           | (SSI)  |                      | AN5                         |                           |
| 74         | 63   |             | P6_1 |  | (TRJ1IO)                      |                           | (SCS)  |                      | AN4                         |                           |
| 75         |      |             | P6_0 |  | (TRJ2IO)                      |                           |        |                      | AN3                         |                           |
| 76         |      |             | P7_6 |  | (TRB00)                       |                           |        |                      | AN2                         |                           |
| 77         |      |             | P7_5 |  | TRB10                         |                           |        |                      | AN1                         |                           |
| 78         |      |             | P7_4 |  |                               |                           |        |                      | AN0                         |                           |
| 79         |      |             | P7_3 |  |                               | (CTS2/RTS2)               |        |                      |                             |                           |
| 80         |      |             | P7_2 |  | TRJ0O                         | (RXD2/SCL2/<br>TXD2/SDA2) |        |                      |                             |                           |

Note:

1. The pin in parentheses can be assigned by a program.



## 1.5 Pin Functions

Tables 1.18 and 1.19 list Pin Functions for R8C/LA5A Group, and Tables 1.20 and 1.21 list Pin Functions for R8C/LA8A Group.

**Table 1.18 Pin Functions for R8C/LA5A Group (1)**

| Item                                    | Pin Name  | I/O Type | Description   |
|---|---|----------|---|
| Power supply input                      | VCC, VSS  | —        | Apply 1.8 V to 5.5 V to the VCC pin.<br>Apply 0 V to the VSS pin.   |
| Analog power supply input               | AVCC, AVSS  | —        | Power supply for the A/D converter.<br>Connect a capacitor between AVCC and AVSS.   |
| Reset input                             | $\overline{\text{RESET}}$   | I        | Driving this pin low resets the MCU.  |
| MODE                                    | MODE  | I        | Connect this pin to VCC via a resistor.   |
| Power-off 0 mode exit input             | $\overline{\text{WKUP0}}$   | I        | This pin is provided for input to exit the mode used in power-off 0 mode. Connect to VSS when not using power-off 0 mode.   |
|   | $\overline{\text{WKUP1}}$   | I        | This pin is provided for input to exit the mode used in power-off 0 mode.   |
| XIN clock input                         | XIN   | I        | These pins are provided for XIN clock generation circuit I/O. Connect a ceramic oscillator or a crystal oscillator between pins XIN and XOUT. <sup>(1)</sup> To use an external clock, input it to the XIN pin and set XOUT as the I/O port P9_1. When the pin is not used, treat it as an unassigned pin and use the appropriate handling. |
| XIN clock output                        | XOUT  | O        |   |
| XCIN clock input                        | XCIN  | I        | These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between pins XCIN and XCOU. <sup>(1)</sup> To use an external clock, input it to the XCIN pin and leave the XCOU pin open.  |
| XCIN clock output                       | XCOU  | O        |   |
| $\overline{\text{INT}}$ interrupt input | $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ ,<br>$\overline{\text{INT5}}$ , $\overline{\text{INT7}}$ | I        | $\overline{\text{INT}}$ interrupt input pins.   |
| Key input interrupt                     | $\overline{\text{KI0}}$ to $\overline{\text{KI7}}$  | I        | Key input interrupt input pins.   |
| Timer RB                                | TRB00, TRB10  | O        | Timer RB output pins.   |
| Timer RC                                | TRCCLK  | I        | External clock input pin.   |
|   | TRCTRG  | I        | External trigger input pin.   |
|   | TRCIOA, TRCIOB,<br>TRCIOC, TRCIOD   | I/O      | Timer RC I/O pins.  |
| Timer RH                                | TRHO  | O        | Timer RH output pin.  |
| Timer RJ                                | TRJ0IO, TRJ1IO  | I/O      | Timer RJ I/O pins.  |
| Serial interface                        | CLK0  | I/O      | Transfer clock I/O pin.   |
|   | RXD0  | I        | Serial data input pin.  |
|   | TXD0  | O        | Serial data output pin.   |

I: Input      O: Output      I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

**Table 1.19 Pin Functions for R8C/LA5A Group (2)**

| Item                    | Pin Name   | I/O Type | Description  |
|-------------------------|--|----------|--|
| I <sup>2</sup> C bus    | SCL  | I/O      | Clock I/O pin.   |
|                         | SDA  | I/O      | Data I/O pin.  |
| SSU                     | SSI  | I/O      | Data I/O pin.  |
|                         | $\overline{\text{SCS}}$  | I/O      | Chip-select signal I/O pin.  |
|                         | SSCK   | I/O      | Clock I/O pin.   |
|                         | SSO  | I/O      | Data I/O pin.  |
| Reference voltage input | VREF   | I        | Reference voltage input pin for the A/D converter.   |
| A/D converter           | AN0 to AN6   | I        | A/D converter analog input pins.   |
|                         | $\overline{\text{ADTRG}}$  | I        | AD external trigger input pin.   |
| Comparator B            | IVCMP1, IVCMP3   | I        | Comparator B analog voltage input pins.  |
|                         | IVREF1, IVREF3   | I        | Comparator B reference voltage input pins.   |
| I/O ports               | P0_0 to P0_7,<br>P2_0 to P2_7,<br>P3_0 to P3_7,<br>P5_0 to P5_6,<br>P7_0 to P7_2,<br>P8_0 to P8_7,<br>P9_0, P9_1 | I/O      | CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually.<br>Any port set to input can be set to use a pull-up resistor or not by a program.<br>Port P8 can be used as LED drive ports. |
| Segment output          | SEG0 to SEG26  | O        | LCD segment output pins.   |
| Common output           | COM0 to COM3,<br>COMEXP  | O        | LCD common output pins.  |
| LCD power supply        | VL1  | I        | Apply the following voltage: $1\text{ V} \leq \text{VL1} \leq \text{VCC}$ and $\text{VL1} \leq \text{VL2}$ .   |
|                         | VL2  | I        | Apply the following voltage: $\text{VL2} \leq 5.5\text{ V}$ and $\text{VL1} \leq \text{VL2} \leq \text{VL3}$ .   |
|                         | VL3  | I        | Apply the following voltage: $\text{VL3} \leq 5.5\text{ V}$ and $\text{VL2} \leq \text{VL3}$ .   |

I: Input      O: Output      I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

**Table 1.20 Pin Functions for R8C/LA8A Group (1)**

| Item                                    | Pin Name  | I/O Type                            | Description  |
|---|---|-------------------------------------|--|
| Power supply input                      | VCC, VSS  | —                                   | Apply 1.8 V to 5.5 V to the VCC pin.<br>Apply 0 V to the VSS pin.  |
| Analog power supply input               | AVCC, AVSS  | —                                   | Power supply for the A/D converter.<br>Connect a capacitor between AVCC and AVSS.  |
| Reset input                             | $\overline{\text{RESET}}$   | I                                   | Driving this pin low resets the MCU.   |
| MODE                                    | MODE  | I                                   | Connect this pin to VCC via a resistor.  |
| Power-off 0 mode exit input             | $\overline{\text{WKUP0}}$   | I                                   | This pin is provided for input to exit the mode used in power-off 0 mode. Connect to VSS when not using power-off 0 mode.  |
|   | $\overline{\text{WKUP1}}$   | I                                   | This pin is provided for input to exit the mode used in power-off 0 mode.  |
| XIN clock input                         | XIN   | I                                   | These pins are provided for XIN clock generation circuit I/O.<br>Connect a ceramic oscillator or a crystal oscillator between pins XIN and XOUT. <sup>(1)</sup> To use an external clock, input it to the XIN pin and set XOUT as the I/O port P9_1. When the pin is not used, treat it as an unassigned pin and use the appropriate handling. |
| XIN clock output                        | XOUT  | O                                   |  |
| XCIN clock input                        | XCIN  | I                                   | These pins are provided for XCIN clock generation circuit I/O.<br>Connect a crystal oscillator between pins XCIN and XCOU. <sup>(1)</sup> To use an external clock, input it to the XCIN pin and leave the XCOU pin open.  |
| XCIN clock output                       | XCOU  | O                                   |  |
| $\overline{\text{INT}}$ interrupt input | $\overline{\text{INT0}}$ to $\overline{\text{INT7}}$                      | I                                   | $\overline{\text{INT}}$ interrupt input pins.  |
| Key input interrupt                     | $\overline{\text{KI0}}$ to $\overline{\text{KI7}}$                        | I                                   | Key input interrupt input pins.  |
| Timer RB                                | TRB0O, TRB1O  | O                                   | Timer RB output pins.  |
| Timer RC                                | TRCCLK  | I                                   | External clock input pin.  |
|   | TRCTR $\overline{\text{G}}$   | I                                   | External trigger input pin.  |
|   | TRCIOA, TRCIOB, TRCIO $\overline{\text{C}}$ , TRCIO $\overline{\text{D}}$ | I/O                                 | Timer RC I/O pins.   |
| Timer RH                                | TRHO  | O                                   | Timer RH output pin.   |
| Timer RJ                                | TRJ0IO, TRJ1IO, TRJ2IO  | I/O                                 | Timer RJ I/O pins.   |
|   | TRJ0IO, TRJ1IO, TRJ2IO  | O                                   | Timer RJ output pins.  |
| Serial interface                        | CLK0, CLK2  | I/O                                 | Transfer clock I/O pin.  |
|   | RXD0, RXD2  | I                                   | Serial data input pin.   |
|   | TXD0, TXD2  | O                                   | Serial data output pin.  |
|   | $\overline{\text{CTS2}}$  | I                                   | Transmission control input pin.  |
|   | $\overline{\text{RTS2}}$  | O                                   | Reception control output pin.  |
|   | SCL2  | I/O                                 | I <sup>2</sup> C mode clock I/O pin.   |
| SDA2                                    | I/O   | I <sup>2</sup> C mode data I/O pin. |  |

I: Input      O: Output      I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

**Table 1.21 Pin Functions for R8C/LA8A Group (2)**

| Item                    | Pin Name  | I/O Type | Description  |
|-------------------------|---|----------|--|
| I <sup>2</sup> C bus    | SCL   | I/O      | Clock I/O pin.   |
|                         | SDA   | I/O      | Data I/O pin.  |
| SSU                     | SSI   | I/O      | Data I/O pin.  |
|                         | $\overline{\text{SCS}}$   | I/O      | Chip-select signal I/O pin.  |
|                         | SSCK  | I/O      | Clock I/O pin.   |
|                         | SSO   | I/O      | Data I/O pin.  |
| Reference voltage input | VREF  | I        | Reference voltage input pin for the A/D converter.   |
| A/D converter           | AN0 to AN11   | I        | A/D converter analog input pins.   |
|                         | $\overline{\text{ADTRG}}$   | I        | AD external trigger input pin.   |
| Comparator B            | IVCMP1, IVCMP3  | I        | Comparator B analog voltage input pins.  |
|                         | IVREF1, IVREF3  | I        | Comparator B reference voltage input pins.   |
| I/O ports               | P0_0 to P0_7,<br>P1_0 to P1_7,<br>P2_0 to P2_7,<br>P3_0 to P3_7,<br>P4_0 to P4_7,<br>P5_0 to P5_6,<br>P6_0 to P6_7,<br>P7_0 to P7_6,<br>P8_0 to P8_7,<br>P9_0, P9_1 | I/O      | CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually.<br>Any port set to input can be set to use a pull-up resistor or not by a program.<br>Ports P7_0, P7_1 and P8 can be used as LED drive ports. |
| Segment output          | SEG0 to SEG39   | O        | LCD segment output pins.   |
| Common output           | COM0 to COM3,<br>COMEXP   | O        | LCD common output pins.  |
| LCD power supply        | VL1   | I        | Apply the following voltage: $1\text{ V} \leq \text{VL1} \leq \text{VCC}$ and $\text{VL1} \leq \text{VL2}$ .   |
|                         | VL2   | I        | Apply the following voltage: $\text{VL2} \leq 5.5\text{ V}$ and $\text{VL1} \leq \text{VL2} \leq \text{VL3}$ .   |
|                         | VL3   | I        | Apply the following voltage: $\text{VL3} \leq 5.5\text{ V}$ and $\text{VL2} \leq \text{VL3}$ .   |

I: Input      O: Output      I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

## 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register banks.

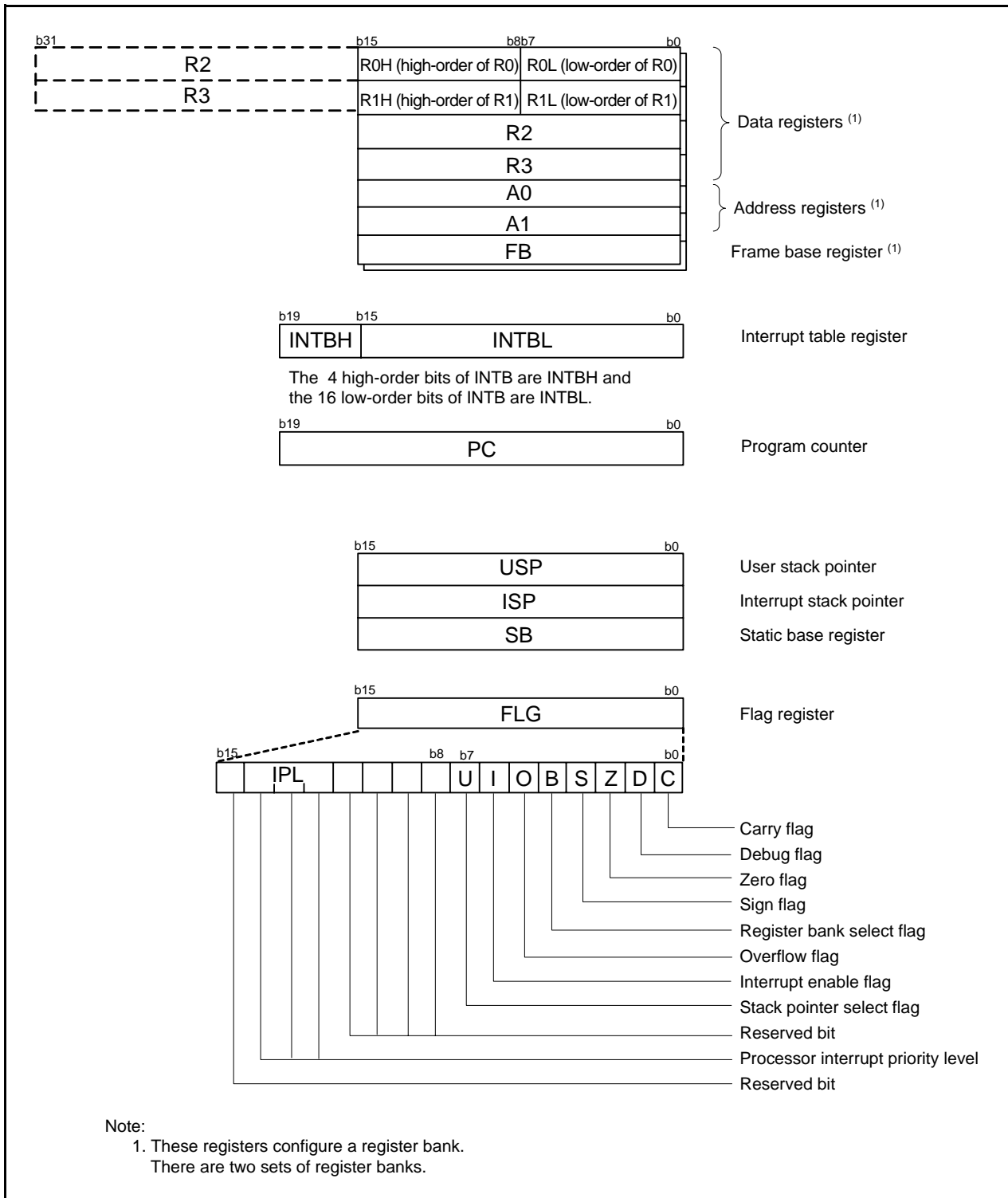


Figure 2.1 CPU Registers

## 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

## 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

### 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

### 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

### 2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

### 2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

### 2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

### 3. Memory

Figure 3.1 shows a Memory Map of each group. Each group has a 1-Mbyte address space from addresses 00000h to FFFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal ROM (data flash) is allocated higher addresses, beginning with address 03000h.

For example, two 1-Kbyte internal ROM (data flash) areas are allocated addresses 03000h to 037FFh. Two 2-Kbyte internal RAM (data flash) areas are allocated addresses 03000h to 03FFFh.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 3.5-Kbyte internal RAM area is allocated addresses 00400h to 011FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.

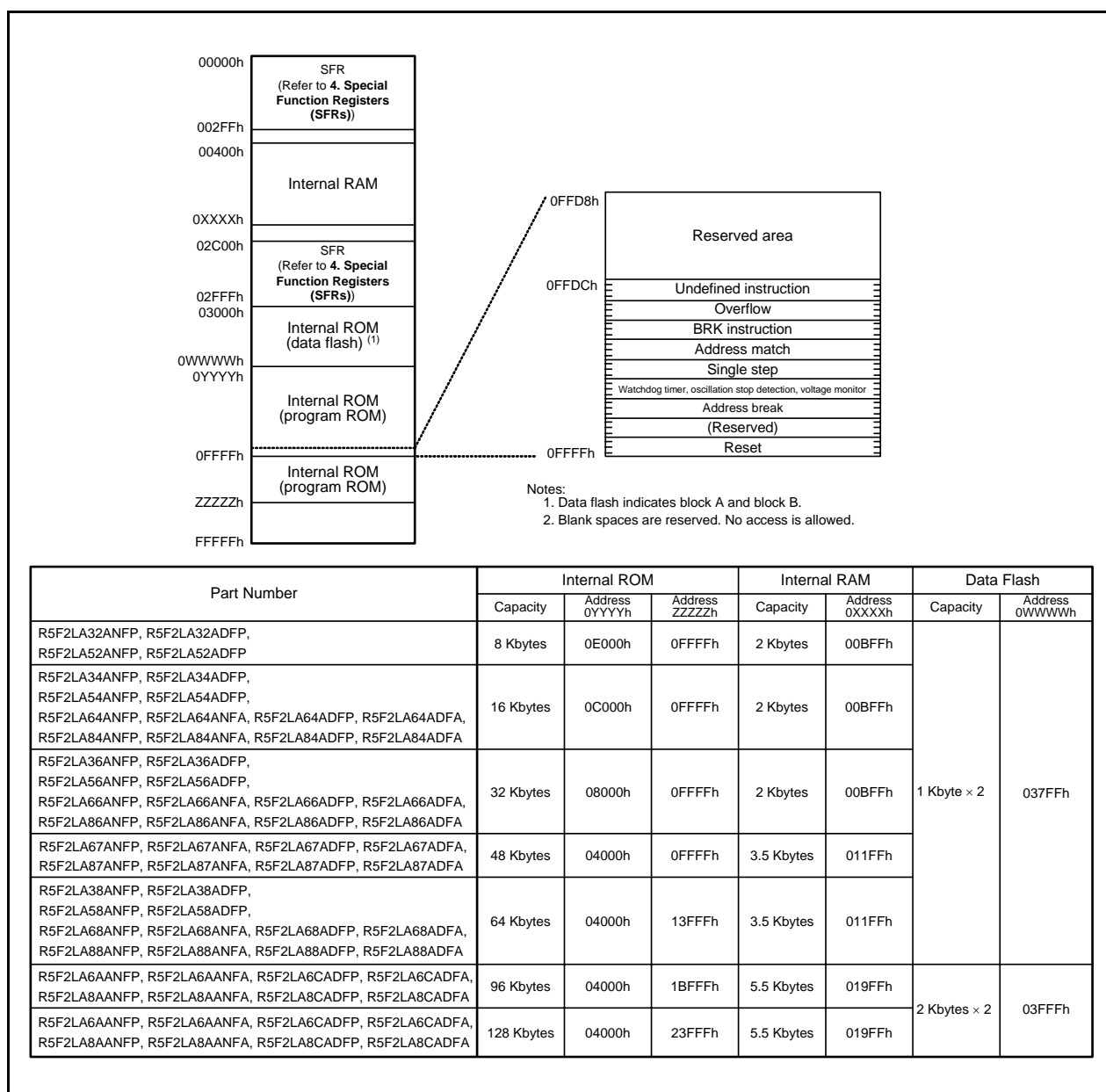


Figure 3.1 Memory Map



## 4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.9 list SFR information for R8C/LA5A Group, Tables 4.10 to 4.18 list SFR information for R8C/LA8A Group, and Table 4.19 lists the ID Code Areas and Option Function Select Area. The description offered in this chapter is based on the R8C/LA8A Group.

**Table 4.1 SFR Information for R8C/LA5A Group (1) (1)**

| Address | Register   | Symbol   | After Reset                    |
|---------|--|----------|--------------------------------|
| 0000h   |  |          |                                |
| 0001h   |  |          |                                |
| 0002h   |  |          |                                |
| 0003h   |  |          |                                |
| 0004h   | Processor Mode Register 0                                  | PM0      | 00h                            |
| 0005h   | Processor Mode Register 1                                  | PM1      | 00h<br>00000100b (2)           |
| 0006h   | System Clock Control Register 0                            | CM0      | 00100000b                      |
| 0007h   | System Clock Control Register 1                            | CM1      | 00100000b                      |
| 0008h   | Module Standby Control Register 0                          | MSTCR0   | 00h                            |
| 0009h   | System Clock Control Register 3                            | CM3      | 00h                            |
| 000Ah   | Protect Register   | PRCR     | 00h                            |
| 000Bh   | Reset Source Determination Register                        | RSTFR    | XXh (3)                        |
| 000Ch   | Oscillation Stop Detection Register                        | OCD      | 00000100b (4)<br>00h (4)       |
| 000Dh   | Watchdog Timer Reset Register                              | WDTR     | XXh                            |
| 000Eh   | Watchdog Timer Start Register                              | WDTS     | XXh                            |
| 000Fh   | Watchdog Timer Control Register                            | WDTC     | 00111111b                      |
| 0010h   | Module Standby Control Register 1                          | MSTCR1   | 00h                            |
| 0011h   |  |          |                                |
| 0012h   |  |          |                                |
| 0013h   |  |          |                                |
| 0014h   |  |          |                                |
| 0015h   |  |          |                                |
| 0016h   |  |          |                                |
| 0017h   |  |          |                                |
| 0018h   |  |          |                                |
| 0019h   |  |          |                                |
| 001Ah   |  |          |                                |
| 001Bh   |  |          |                                |
| 001Ch   | Count Source Protection Mode Register                      | CSPR     | 00h<br>10000000b (5)           |
| 001Dh   |  |          |                                |
| 001Eh   |  |          |                                |
| 001Fh   |  |          |                                |
| 0020h   | Power-Off Mode Control Register 0                          | POMCR0   | XXXXXX00b                      |
| 0021h   |  |          |                                |
| 0022h   |  |          |                                |
| 0023h   | High-Speed On-Chip Oscillator Control Register 0           | FRA0     | 00h                            |
| 0024h   | High-Speed On-Chip Oscillator Frequency Control Register 0 | FRC0     | When shipping                  |
| 0025h   | High-Speed On-Chip Oscillator Control Register 2           | FRA2     | 00h                            |
| 0026h   | On-Chip Reference Voltage Control Register                 | OCVREFCR | 00h                            |
| 0027h   |  |          |                                |
| 0028h   |  |          |                                |
| 0029h   | High-Speed On-Chip Oscillator 18 MHz Set Value Register 0  | FR18S0   | XXh                            |
| 002Ah   | High-Speed On-Chip Oscillator 18 MHz Set Value Register 1  | FR18S1   | XXh                            |
| 002Bh   |  |          |                                |
| 002Ch   |  |          |                                |
| 002Dh   |  |          |                                |
| 002Eh   |  |          |                                |
| 002Fh   | High-Speed On-Chip Oscillator Frequency Control Register 1 | FRC1     | When shipping                  |
| 0030h   | Voltage Monitor Circuit Control Register                   | CMPA     | 00h                            |
| 0031h   | Voltage Monitor Circuit Edge Select Register               | VCAC     | 00h                            |
| 0032h   |  |          |                                |
| 0033h   | Voltage Detect Register 1                                  | VCA1     | 00001000b                      |
| 0034h   | Voltage Detect Register 2                                  | VCA2     | 00h (6)<br>00100000b (7)       |
| 0035h   |  |          |                                |
| 0036h   | Voltage Detection 1 Level Select Register                  | VD1LS    | 00000111b                      |
| 0037h   |  |          |                                |
| 0038h   | Voltage Monitor 0 Circuit Control Register                 | VW0C     | 1100X010b (6)<br>1100X011b (7) |
| 0039h   | Voltage Monitor 1 Circuit Control Register                 | VW1C     | 10001010b                      |

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- The CSPRO bit in the CSPR register is set to 1.
- The CWR bit in the RSTFR register is set to 0 after power-on, voltage monitor 0 reset, or exit from power-off 0 mode. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
- The reset value differs depending on the mode.
- The CSPROINI bit in the OFS register is set to 0.
- The LVDAS bit in the OFS register is set to 1.
- The LVDAS bit in the OFS register is set to 0.

**Table 4.2 SFR Information for R8C/LA5A Group (2) (1)**

| Address | Register  | Symbol      | After Reset |
|---------|---|-------------|-------------|
| 003Ah   | Voltage Monitor 2 Circuit Control Register                              | VW2C        | 10000010b   |
| 003Bh   |   |             |             |
| 003Ch   |   |             |             |
| 003Dh   |   |             |             |
| 003Eh   |   |             |             |
| 003Fh   |   |             |             |
| 0040h   |   |             |             |
| 0041h   | Flash Memory Ready Interrupt Control Register                           | FMRDYIC     | XXXXX000b   |
| 0042h   |   |             |             |
| 0043h   | INT7 Interrupt Control Register   | INT7IC      | XX00X000b   |
| 0044h   |   |             |             |
| 0045h   | INT5 Interrupt Control Register   | INT5IC      | XX00X000b   |
| 0046h   |   |             |             |
| 0047h   | Timer RC Interrupt Control Register                                     | TRCIC       | XXXXX000b   |
| 0048h   |   |             |             |
| 0049h   |   |             |             |
| 004Ah   | Timer RH Interrupt Control Register                                     | TRHIC       | XXXXX000b   |
| 004Bh   |   |             |             |
| 004Ch   |   |             |             |
| 004Dh   | Key Input Interrupt Control Register                                    | KUPIC       | XXXXX000b   |
| 004Eh   | A/D Conversion Interrupt Control Register                               | ADIC        | XXXXX000b   |
| 004Fh   | SSU Interrupt Control Register / IIC bus Interrupt Control Register (2) | SSUIC/IICIC | XXXXX000b   |
| 0050h   |   |             |             |
| 0051h   | UART0 Transmit Interrupt Control Register                               | S0TIC       | XXXXX000b   |
| 0052h   | UART0 Receive Interrupt Control Register                                | S0RIC       | XXXXX000b   |
| 0053h   |   |             |             |
| 0054h   |   |             |             |
| 0055h   | INT2 Interrupt Control Register   | INT2IC      | XX00X000b   |
| 0056h   | Timer RJ0 Interrupt Control Register                                    | TRJ0IC      | XXXXX000b   |
| 0057h   | Timer RB1 Interrupt Control Register                                    | TRB1IC      | XXXXX000b   |
| 0058h   | Timer RB0 Interrupt Control Register                                    | TRB0IC      | XXXXX000b   |
| 0059h   | INT1 Interrupt Control Register   | INT1IC      | XX00X000b   |
| 005Ah   | INT3 Interrupt Control Register   | INT3IC      | XX00X000b   |
| 005Bh   | Timer RJ1 Interrupt Control Register                                    | TRJ1IC      | XXXXX000b   |
| 005Ch   |   |             |             |
| 005Dh   | INT0 Interrupt Control Register   | INT0IC      | XX00X000b   |
| 005Eh   |   |             |             |
| 005Fh   |   |             |             |
| 0060h   |   |             |             |
| 0061h   |   |             |             |
| 0062h   |   |             |             |
| 0063h   |   |             |             |
| 0064h   |   |             |             |
| 0065h   |   |             |             |
| 0066h   |   |             |             |
| 0067h   |   |             |             |
| 0068h   |   |             |             |
| 0069h   |   |             |             |
| 006Ah   | LCD Interrupt Control Register  | LCDIC       | XXXXX000b   |
| 006Bh   |   |             |             |
| 006Ch   |   |             |             |
| 006Dh   |   |             |             |
| 006Eh   |   |             |             |
| 006Fh   |   |             |             |
| 0070h   |   |             |             |
| 0071h   |   |             |             |
| 0072h   | Voltage monitor 1 Interrupt Control Register                            | VCMP1IC     | XXXXX000b   |
| 0073h   | Voltage monitor 2 Interrupt Control Register                            | VCMP2IC     | XXXXX000b   |
| 0074h   |   |             |             |
| 0075h   |   |             |             |
| 0076h   |   |             |             |
| 0077h   |   |             |             |
| 0078h   |   |             |             |
| 0079h   |   |             |             |
| 007Ah   |   |             |             |
| 007Bh   |   |             |             |
| 007Ch   |   |             |             |
| 007Dh   |   |             |             |
| 007Eh   |   |             |             |
| 007Fh   |   |             |             |

X: Undefined

Notes:

1. Blank spaces are reserved. No access is allowed.
2. Selectable by the IICSEL bit in the SSUICSR register.

**Table 4.3 SFR Information for R8C/LA5A Group (3) (1)**

| Address | Register                                  | Symbol  | After Reset |
|---------|---|---------|-------------|
| 0080h   | Timer RJ0 Control Register                | TRJ0CR  | 00h         |
| 0081h   | Timer RJ0 I/O Control Register            | TRJ0IOC | 00h         |
| 0082h   | Timer RJ0 Mode Register                   | TRJ0MR  | 00h         |
| 0083h   | Timer RJ0 Event Pin Select Register       | TRJ0ISR | 00h         |
| 0084h   | Timer RJ0 Register                        | TRJ0    | FFh         |
| 0085h   |   |         | FFh         |
| 0086h   |   |         |             |
| 0087h   |   |         |             |
| 0088h   | Timer RJ1 Control Register                | TRJ1CR  | 00h         |
| 0089h   | Timer RJ1 I/O Control Register            | TRJ1IOC | 00h         |
| 008Ah   | Timer RJ1 Mode Register                   | TRJ1MR  | 00h         |
| 008Bh   | Timer RJ1 Event Pin Select Register       | TRJ1ISR | 00h         |
| 008Ch   | Timer RJ1 Register                        | TRJ1    | FFh         |
| 008Dh   |   |         | FFh         |
| 008Eh   |   |         |             |
| 008Fh   |   |         |             |
| 0090h   |   |         |             |
| 0091h   |   |         |             |
| 0092h   |   |         |             |
| 0093h   |   |         |             |
| 0094h   |   |         |             |
| 0095h   |   |         |             |
| 0096h   |   |         |             |
| 0097h   |   |         |             |
| 0098h   | Timer RB1 Control Register                | TRB1CR  | 00h         |
| 0099h   | Timer RB1 One-Shot Control Register       | TRB1OCR | 00h         |
| 009Ah   | Timer RB1 I/O Control Register            | TRB1IOC | 00h         |
| 009Bh   | Timer RB1 Mode Register                   | TRB1MR  | 00h         |
| 009Ch   | Timer RB1 Prescaler Register              | TRB1PRE | FFh         |
| 009Dh   | Timer RB1 Secondary Register              | TRB1SC  | FFh         |
| 009Eh   | Timer RB1 Primary Register                | TRB1PR  | FFh         |
| 009Fh   |   |         |             |
| 00A0h   | UART0 Transmit/Receive Mode Register      | U0MR    | 00h         |
| 00A1h   | UART0 Bit Rate Register                   | U0BRG   | XXh         |
| 00A2h   | UART0 Transmit Buffer Register            | U0TB    | XXh         |
| 00A3h   |   |         | XXh         |
| 00A4h   | UART0 Transmit/Receive Control Register 0 | U0C0    | 00001000b   |
| 00A5h   | UART0 Transmit/Receive Control Register 1 | U0C1    | 00000010b   |
| 00A6h   | UART0 Receive Buffer Register             | U0RB    | XXh         |
| 00A7h   |   |         | XXh         |
| 00A8h   |   |         |             |
| 00A9h   |   |         |             |
| 00AAh   |   |         |             |
| 00ABh   |   |         |             |
| 00ACh   |   |         |             |
| 00ADh   |   |         |             |
| 00AEh   |   |         |             |
| 00AFh   |   |         |             |
| 00B0h   |   |         |             |
| 00B1h   |   |         |             |
| 00B2h   |   |         |             |
| 00B3h   |   |         |             |
| 00B4h   |   |         |             |
| 00B5h   |   |         |             |
| 00B6h   |   |         |             |
| 00B7h   |   |         |             |
| 00B8h   |   |         |             |
| 00B9h   |   |         |             |
| 00BAh   |   |         |             |
| 00BBh   |   |         |             |
| 00BCh   |   |         |             |
| 00BDh   |   |         |             |
| 00BEh   |   |         |             |
| 00BFh   |   |         |             |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

**Table 4.4 SFR Information for R8C/LA5A Group (4) (1)**

| Address | Register                   | Symbol  | After Reset |
|---------|----------------------------|---------|-------------|
| 00C0h   | A/D Register 0             | AD0     | XXh         |
| 00C1h   |                            |         | 000000XXb   |
| 00C2h   | A/D Register 1             | AD1     | XXh         |
| 00C3h   |                            |         | 000000XXb   |
| 00C4h   | A/D Register 2             | AD2     | XXh         |
| 00C5h   |                            |         | 000000XXb   |
| 00C6h   | A/D Register 3             | AD3     | XXh         |
| 00C7h   |                            |         | 000000XXb   |
| 00C8h   | A/D Register 4             | AD4     | XXh         |
| 00C9h   |                            |         | 000000XXb   |
| 00CAh   | A/D Register 5             | AD5     | XXh         |
| 00CBh   |                            |         | 000000XXb   |
| 00CCh   | A/D Register 6             | AD6     | XXh         |
| 00CDh   |                            |         | 000000XXb   |
| 00CEh   | A/D Register 7             | AD7     | XXh         |
| 00CFh   |                            |         | 000000XXb   |
| 00D0h   |                            |         |             |
| 00D1h   |                            |         |             |
| 00D2h   |                            |         |             |
| 00D3h   |                            |         |             |
| 00D4h   | A/D Mode Register          | ADMOD   | 00h         |
| 00D5h   | A/D Input Select Register  | ADINSEL | 11000000b   |
| 00D6h   | A/D Control Register 0     | ADCON0  | 00h         |
| 00D7h   | A/D Control Register 1     | ADCON1  | 00h         |
| 00D8h   |                            |         |             |
| 00D9h   |                            |         |             |
| 00DAh   |                            |         |             |
| 00DBh   |                            |         |             |
| 00DCh   |                            |         |             |
| 00DDh   | A/D Control Register 2     | ADCON2  | 00h         |
| 00DEh   |                            |         |             |
| 00DFh   |                            |         |             |
| 00E0h   | Port P0 Register           | P0      | XXh         |
| 00E1h   |                            |         |             |
| 00E2h   | Port P0 Direction Register | PD0     | 00h         |
| 00E3h   |                            |         |             |
| 00E4h   | Port P2 Register           | P2      | XXh         |
| 00E5h   | Port P3 Register           | P3      | XXh         |
| 00E6h   | Port P2 Direction Register | PD2     | 00h         |
| 00E7h   | Port P3 Direction Register | PD3     | 00h         |
| 00E8h   |                            |         |             |
| 00E9h   | Port P5 Register           | P5      | XXh         |
| 00EAh   |                            |         |             |
| 00EBh   | Port P5 Direction Register | PD5     | 00h         |
| 00ECh   |                            |         |             |
| 00EDh   | Port P7 Register           | P7      | XXh         |
| 00EEh   |                            |         |             |
| 00EFh   | Port P7 Direction Register | PD7     | 00h         |
| 00F0h   | Port P8 Register           | P8      | XXh         |
| 00F1h   | Port P9 Register           | P9      | XXh         |
| 00F2h   | Port P8 Direction Register | PD8     | 00h         |
| 00F3h   | Port P9 Direction Register | PD9     | 00h         |
| 00F4h   |                            |         |             |
| 00F5h   |                            |         |             |
| 00F6h   |                            |         |             |
| 00F7h   |                            |         |             |
| 00F8h   |                            |         |             |
| 00F9h   |                            |         |             |
| 00FAh   |                            |         |             |
| 00FBh   |                            |         |             |
| 00FCh   |                            |         |             |
| 00FDh   |                            |         |             |
| 00FEh   |                            |         |             |
| 00FFh   |                            |         |             |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

**Table 4.5 SFR Information for R8C/LA5A Group (5) (1)**

| Address | Register  | Symbol  | After Reset                |
|---------|---|---------|----------------------------|
| 0100h   |   |         |                            |
| 0101h   |   |         |                            |
| 0102h   |   |         |                            |
| 0103h   |   |         |                            |
| 0104h   |   |         |                            |
| 0105h   |   |         |                            |
| 0106h   |   |         |                            |
| 0107h   |   |         |                            |
| 0108h   | Timer RB0 Control Register                            | TRB0CR  | 00h                        |
| 0109h   | Timer RB0 One-Shot Control Register                   | TRB0OCR | 00h                        |
| 010Ah   | Timer RB0 I/O Control Register                        | TRB0IOC | 00h                        |
| 010Bh   | Timer RB0 Mode Register                               | TRB0MR  | 00h                        |
| 010Ch   | Timer RB0 Prescaler Register                          | TRB0PRE | FFh                        |
| 010Dh   | Timer RB0 Secondary Register                          | TRB0SC  | FFh                        |
| 010Eh   | Timer RB0 Primary Register                            | TRB0PR  | FFh                        |
| 010Fh   |   |         |                            |
| 0110h   | Timer RH Second Data Register / Counter Data Register | TRHSEC  | XXh<br>00h (2)             |
| 0111h   | Timer RH Minute Data Register / Compare Data Register | TRHMIN  | XXh<br>00h (2)             |
| 0112h   | Timer RH Hour Data Register                           | TRHHR   | 00XXXXXXb<br>00h (2)       |
| 0113h   | Timer RH Day-of-the-Week Data Register                | TRHWK   | 00000XXXb<br>00h (2)       |
| 0114h   | Timer RH Date Data Register                           | TRHDY   | 00XXXXXXb<br>00000001b (2) |
| 0115h   | Timer RH Month Data Register                          | TRHMON  | 000XXXXXb<br>00000001b (2) |
| 0116h   | Timer RH Year Data Register                           | TRHYR   | XXh<br>00h (2)             |
| 0117h   | Timer RH Control Register                             | TRHCR   | XXX000XXb<br>000XX1X0b (2) |
| 0118h   | Timer RH Count Source Select Register                 | TRHCSR  | X0001000b<br>0XXXXXXXb (2) |
| 0119h   | Timer RH Clock Error Correction Register              | TRHADJ  | XXh<br>00h (2)             |
| 011Ah   | Timer RH Interrupt Flag Register                      | TRHIFR  | 00000XXXb<br>000XX000b (2) |
| 011Bh   | Timer RH Interrupt Enable Register                    | TRHIER  | XXh<br>00h (2)             |
| 011Ch   | Timer RH Alarm Minute Register                        | TRHAMN  | XXh<br>00h (2)             |
| 011Dh   | Timer RH Alarm Hour Register                          | TRHAHR  | XXh<br>00h (2)             |
| 011Eh   | Timer RH Alarm Day-of-the-Week Register               | TRHAWK  | X0000XXXb<br>00h (2)       |
| 011Fh   | Timer RH Protect Register                             | TRHPRC  | 00h<br>X0000000b (2)       |
| 0120h   | Timer RC Mode Register                                | TRCMR   | 01001000b                  |
| 0121h   | Timer RC Control Register 1                           | TRCCR1  | 00h                        |
| 0122h   | Timer RC Interrupt Enable Register                    | TRCIER  | 01110000b                  |
| 0123h   | Timer RC Status Register                              | TRCSR   | 01110000b                  |
| 0124h   | Timer RC I/O Control Register 0                       | TRCIOR0 | 10001000b                  |
| 0125h   | Timer RC I/O Control Register 1                       | TRCIOR1 | 10001000b                  |
| 0126h   | Timer RC Counter                                      | TRC     | 00h<br>00h                 |
| 0127h   |   |         |                            |
| 0128h   | Timer RC General Register A                           | TRCGRA  | FFh<br>FFh                 |
| 0129h   |   |         |                            |
| 012Ah   | Timer RC General Register B                           | TRCGRB  | FFh<br>FFh                 |
| 012Bh   |   |         |                            |
| 012Ch   | Timer RC General Register C                           | TRCGRC  | FFh<br>FFh                 |
| 012Dh   |   |         |                            |
| 012Eh   | Timer RC General Register D                           | TRCGRD  | FFh<br>FFh                 |
| 012Fh   |   |         |                            |
| 0130h   | Timer RC Control Register 2                           | TRCCR2  | 00011000b                  |
| 0131h   | Timer RC Digital Filter Function Select Register      | TRCDF   | 00h                        |
| 0132h   | Timer RC Output Master Enable Register                | TRCOER  | 01111111b                  |
| 0133h   | Timer RC Trigger Control Register                     | TRCADCR | 00h                        |
| 0134h   |   |         |                            |
| 0135h   |   |         |                            |
| 0136h   |   |         |                            |
| 0137h   |   |         |                            |
| 0138h   |   |         |                            |
| 0139h   |   |         |                            |
| 013Ah   |   |         |                            |
| 013Bh   |   |         |                            |
| 013Ch   |   |         |                            |
| 013Dh   |   |         |                            |
| 013Eh   |   |         |                            |
| 013Fh   |   |         |                            |

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- This is the reset value after reset by RTCRST bit in TRHCR register.

**Table 4.6 SFR Information for R8C/LA5A Group (6) (1)**

| Address | Register | Symbol | After Reset |
|---------|----------|--------|-------------|
| 0140h   |          |        |             |
| 0141h   |          |        |             |
| 0142h   |          |        |             |
| 0143h   |          |        |             |
| 0144h   |          |        |             |
| 0145h   |          |        |             |
| 0146h   |          |        |             |
| 0147h   |          |        |             |
| 0148h   |          |        |             |
| 0149h   |          |        |             |
| 014Ah   |          |        |             |
| 014Bh   |          |        |             |
| 014Ch   |          |        |             |
| 014Dh   |          |        |             |
| 014Eh   |          |        |             |
| 014Fh   |          |        |             |
| 0150h   |          |        |             |
| 0151h   |          |        |             |
| 0152h   |          |        |             |
| 0153h   |          |        |             |
| 0154h   |          |        |             |
| 0155h   |          |        |             |
| 0156h   |          |        |             |
| 0157h   |          |        |             |
| 0158h   |          |        |             |
| 0159h   |          |        |             |
| 015Ah   |          |        |             |
| 015Bh   |          |        |             |
| 015Ch   |          |        |             |
| 015Dh   |          |        |             |
| 015Eh   |          |        |             |
| 015Fh   |          |        |             |
| 0160h   |          |        |             |
| 0161h   |          |        |             |
| 0162h   |          |        |             |
| 0163h   |          |        |             |
| 0164h   |          |        |             |
| 0165h   |          |        |             |
| 0166h   |          |        |             |
| 0167h   |          |        |             |
| 0168h   |          |        |             |
| 0169h   |          |        |             |
| 016Ah   |          |        |             |
| 016Bh   |          |        |             |
| 016Ch   |          |        |             |
| 016Dh   |          |        |             |
| 016Eh   |          |        |             |
| 016Fh   |          |        |             |
| 0170h   |          |        |             |
| 0171h   |          |        |             |
| 0172h   |          |        |             |
| 0173h   |          |        |             |
| 0174h   |          |        |             |
| 0175h   |          |        |             |
| 0176h   |          |        |             |
| 0177h   |          |        |             |
| 0178h   |          |        |             |
| 0179h   |          |        |             |
| 017Ah   |          |        |             |
| 017Bh   |          |        |             |
| 017Ch   |          |        |             |
| 017Dh   |          |        |             |
| 017Eh   |          |        |             |
| 017Fh   |          |        |             |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

**Table 4.7 SFR Information for R8C/LA5A Group (7) (1)**

| Address | Register   | Symbol      | After Reset                |
|---------|--|-------------|----------------------------|
| 0180h   | Timer RJ Pin Select Register                                     | TRJSR       | 00h                        |
| 0181h   |  |             |                            |
| 0182h   | Timer RC Pin Select Register 0                                   | TRCPSR0     | 00h                        |
| 0183h   | Timer RC Pin Select Register 1                                   | TRCPSR1     | 00h                        |
| 0184h   |  |             |                            |
| 0185h   |  |             |                            |
| 0186h   |  |             |                            |
| 0187h   |  |             |                            |
| 0188h   | UART0 Pin Select Register  | U0SR        | 00h                        |
| 0189h   |  |             |                            |
| 018Ah   |  |             |                            |
| 018Bh   |  |             |                            |
| 018Ch   | SSU/IIC Pin Select Register                                      | SSUICSR     | 00h                        |
| 018Dh   | Timer RH Second Interrupt Control Register                       | TRHICR      | X0XXXXXXb<br>00000001b (3) |
| 018Eh   | INT Interrupt Input Pin Select Register                          | INTSR       | 00h                        |
| 018Fh   | I/O Function Pin Select Register                                 | PINSR       | 00h                        |
| 0190h   |  |             |                            |
| 0191h   |  |             |                            |
| 0192h   |  |             |                            |
| 0193h   | SS Bit Counter Register  | SSBR        | 11111000b                  |
| 0194h   | SS Transmit Data Register L / IIC bus Transmit Data Register (2) | SSTDR/ICDRT | FFh                        |
| 0195h   | SS Transmit Data Register H (2)                                  | SSTDRH      | FFh                        |
| 0196h   | SS Receive Data Register L / IIC bus Receive Data Register (2)   | SSRDR/ICDRR | FFh                        |
| 0197h   | SS Receive Data Register H (2)                                   | SSRDRH      | FFh                        |
| 0198h   | SS Control Register H / IIC bus Control Register 1 (2)           | SSCRH/ICCR1 | 00h                        |
| 0199h   | SS Control Register L / IIC bus Control Register 2 (2)           | SSCRL/ICCR2 | 01111101b                  |
| 019Ah   | SS Mode Register / IIC bus Mode Register (2)                     | SSMR/ICMR   | 00010000b/00011000b        |
| 019Bh   | SS Enable Register / IIC bus Interrupt Enable Register (2)       | SSER/ICIER  | 00h                        |
| 019Ch   | SS Status Register / IIC bus Status Register (2)                 | SSSR/ICSR   | 00h/0000X000b              |
| 019Dh   | SS Mode Register 2 / Slave Address Register (2)                  | SSMR2/SAR   | 00h                        |
| 019Eh   |  |             |                            |
| 019Fh   |  |             |                            |
| 01A0h   |  |             |                            |
| 01A1h   |  |             |                            |
| 01A2h   |  |             |                            |
| 01A3h   |  |             |                            |
| 01A4h   |  |             |                            |
| 01A5h   |  |             |                            |
| 01A6h   |  |             |                            |
| 01A7h   |  |             |                            |
| 01A8h   |  |             |                            |
| 01A9h   |  |             |                            |
| 01AAh   |  |             |                            |
| 01ABh   |  |             |                            |
| 01ACh   |  |             |                            |
| 01ADh   |  |             |                            |
| 01AEh   |  |             |                            |
| 01AFh   |  |             |                            |
| 01B0h   |  |             |                            |
| 01B1h   |  |             |                            |
| 01B2h   | Flash Memory Status Register                                     | FST         | 10000X00b                  |
| 01B3h   |  |             |                            |
| 01B4h   | Flash Memory Control Register 0                                  | FMR0        | 00h                        |
| 01B5h   | Flash Memory Control Register 1                                  | FMR1        | 000000X0b                  |
| 01B6h   | Flash Memory Control Register 2                                  | FMR2        | 00h                        |
| 01B7h   |  |             |                            |
| 01B8h   |  |             |                            |
| 01B9h   |  |             |                            |
| 01BAh   |  |             |                            |
| 01BBh   |  |             |                            |
| 01BCh   |  |             |                            |
| 01BDh   |  |             |                            |
| 01BEh   |  |             |                            |
| 01BFh   |  |             |                            |

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- Selectable by the IICSEL bit in the SSUICSR register.
- This is the reset value after reset by RTCRST bit in TRHCR register.

**Table 4.8 SFR Information for R8C/LA5A Group (8) (1)**

| Address | Register                                  | Symbol | After Reset |
|---------|---|--------|-------------|
| 01C0h   | Address Match Interrupt Register 0        | RMAD0  | XXh         |
| 01C1h   |   |        | XXh         |
| 01C2h   |   |        | 0000XXXXb   |
| 01C3h   | Address Match Interrupt Enable Register 0 | AIER0  | 00h         |
| 01C4h   | Address Match Interrupt Register 1        | RMAD1  | XXh         |
| 01C5h   |   |        | XXh         |
| 01C6h   |   |        | 0000XXXXb   |
| 01C7h   | Address Match Interrupt Enable Register 1 | AIER1  | 00h         |
| 01C8h   |   |        |             |
| 01C9h   |   |        |             |
| 01CAh   |   |        |             |
| 01CBh   |   |        |             |
| 01CCh   |   |        |             |
| 01CDh   |   |        |             |
| 01CEh   |   |        |             |
| 01CFh   |   |        |             |
| 01D0h   |   |        |             |
| 01D1h   |   |        |             |
| 01D2h   |   |        |             |
| 01D3h   |   |        |             |
| 01D4h   |   |        |             |
| 01D5h   |   |        |             |
| 01D6h   |   |        |             |
| 01D7h   |   |        |             |
| 01D8h   |   |        |             |
| 01D9h   |   |        |             |
| 01DAh   |   |        |             |
| 01DBh   |   |        |             |
| 01DCh   |   |        |             |
| 01DDh   |   |        |             |
| 01DEh   |   |        |             |
| 01DFh   |   |        |             |
| 01E0h   | Port P0 Pull-Up Control Register          | P0PUR  | 00h         |
| 01E1h   |   |        |             |
| 01E2h   | Port P2 Pull-Up Control Register          | P2PUR  | 00h         |
| 01E3h   | Port P3 Pull-Up Control Register          | P3PUR  | 00h         |
| 01E4h   |   |        |             |
| 01E5h   | Port P5 Pull-Up Control Register          | P5PUR  | 00h         |
| 01E6h   |   |        |             |
| 01E7h   | Port P7 Pull-Up Control Register          | P7PUR  | 00h         |
| 01E8h   | Port P8 Pull-Up Control Register          | P8PUR  | 00h         |
| 01E9h   | Port P9 Pull-Up Control Register          | P9PUR  | 00h         |
| 01EAh   |   |        |             |
| 01EBh   |   |        |             |
| 01ECh   |   |        |             |
| 01EDh   |   |        |             |
| 01EEh   |   |        |             |
| 01EFh   |   |        |             |
| 01F0h   |   |        |             |
| 01F1h   | Port P8 Drive Capacity Control Register   | P8DRR  | 00h         |
| 01F2h   |   |        |             |
| 01F3h   |   |        |             |
| 01F4h   |   |        |             |
| 01F5h   | Input Threshold Control Register 0        | VLT0   | 00h         |
| 01F6h   | Input Threshold Control Register 1        | VLT1   | 00h         |
| 01F7h   | Input Threshold Control Register 2        | VLT2   | 00h         |
| 01F8h   | Comparator B Control Register 0           | INTCMP | 00h         |
| 01F9h   |   |        |             |
| 01FAh   | External Input Enable Register 0          | INTEN  | 00h         |
| 01FBh   | External Input Enable Register 1          | INTEN1 | 00h         |
| 01FCh   | INT Input Filter Select Register 0        | INTF   | 00h         |
| 01FDh   | INT Input Filter Select Register 1        | INTF1  | 00h         |
| 01FEh   | Key Input Enable Register 0               | KIEN   | 00h         |
| 01FFh   | Key Input Enable Register 1               | KIEN1  | 00h         |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.



**Table 4.9 SFR Information for R8C/LA5A Group (9) (1)**

| Address | Register                          | Symbol | After Reset |
|---------|-----------------------------------|--------|-------------|
| 0200h   | LCD Control Register              | LCR0   | 00h         |
| 0201h   |                                   |        |             |
| 0202h   | LCD Option Clock Control Register | LCR2   | 00h         |
| 0203h   | LCD Clock Control Register        | LCR3   | 00h         |
| 0204h   | LCD Display Control Register      | LCR4   | 00h         |
| 0205h   |                                   |        |             |
| 0206h   | LCD Port Select Register 0        | LSE0   | 00h         |
| 0207h   | LCD Port Select Register 1        | LSE1   | 00h         |
| 0208h   | LCD Port Select Register 2        | LSE2   | 00h         |
| 0209h   |                                   |        |             |
| 020Ah   |                                   |        |             |
| 020Bh   | LCD Port Select Register 5        | LSE5   | 00h         |
| 020Ch   |                                   |        |             |
| 020Dh   |                                   |        |             |
| 020Eh   |                                   |        |             |
| 020Fh   |                                   |        |             |
| 0210h   | LCD Display Data Register         | LRA0L  | XXh         |
| 0211h   |                                   | LRA1L  | XXh         |
| 0212h   |                                   | LRA2L  | XXh         |
| 0213h   |                                   | LRA3L  | XXh         |
| 0214h   |                                   | LRA4L  | XXh         |
| 0215h   |                                   | LRA5L  | XXh         |
| 0216h   |                                   | LRA6L  | XXh         |
| 0217h   |                                   | LRA7L  | XXh         |
| 0218h   |                                   | LRA8L  | XXh         |
| 0219h   |                                   | LRA9L  | XXh         |
| 021Ah   |                                   | LRA10L | XXh         |
| 021Bh   |                                   | LRA11L | XXh         |
| 021Ch   |                                   | LRA12L | XXh         |
| 021Dh   |                                   | LRA13L | XXh         |
| 021Eh   |                                   | LRA14L | XXh         |
| 021Fh   |                                   | LRA15L | XXh         |
| 0220h   |                                   | LRA16L | XXh         |
| 0221h   |                                   | LRA17L | XXh         |
| 0222h   |                                   | LRA18L | XXh         |
| 0223h   |                                   | LRA19L | XXh         |
| 0224h   |                                   | LRA20L | XXh         |
| 0225h   |                                   | LRA21L | XXh         |
| 0226h   |                                   | LRA22L | XXh         |
| 0227h   |                                   | LRA23L | XXh         |
| 0228h   |                                   | LRA24L | XXh         |
| 0229h   |                                   | LRA25L | XXh         |
| 022Ah   |                                   | LRA26L | XXh         |
| 022Bh   |                                   |        |             |
| 022Ch   |                                   |        |             |
| 022Dh   |                                   |        |             |
| 022Eh   |                                   |        |             |
| 022Fh   |                                   |        |             |
| 0230h   |                                   |        |             |
| 0231h   |                                   |        |             |
| 0232h   |                                   |        |             |
| 0233h   |                                   |        |             |
| 0234h   |                                   |        |             |
| 0235h   |                                   |        |             |
| 0236h   |                                   |        |             |
| 0237h   |                                   |        |             |
| :       |                                   |        |             |
| 2FFh    |                                   |        |             |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

**Table 4.10 SFR Information for R8C/LA8A Group (1) (1)**

| Address | Register   | Symbol   | After Reset                    |
|---------|--|----------|--------------------------------|
| 0000h   |  |          |                                |
| 0001h   |  |          |                                |
| 0002h   |  |          |                                |
| 0003h   |  |          |                                |
| 0004h   | Processor Mode Register 0                                  | PM0      | 00h                            |
| 0005h   | Processor Mode Register 1                                  | PM1      | 00h<br>00000100b (2)           |
| 0006h   | System Clock Control Register 0                            | CM0      | 00100000b                      |
| 0007h   | System Clock Control Register 1                            | CM1      | 00100000b                      |
| 0008h   | Module Standby Control Register 0                          | MSTCR0   | 00h                            |
| 0009h   | System Clock Control Register 3                            | CM3      | 00h                            |
| 000Ah   | Protect Register   | PRCR     | 00h                            |
| 000Bh   | Reset Source Determination Register                        | RSTFR    | XXh (3)                        |
| 000Ch   | Oscillation Stop Detection Register                        | OCD      | 00000100b (4)<br>00h (4)       |
| 000Dh   | Watchdog Timer Reset Register                              | WDTR     | XXh                            |
| 000Eh   | Watchdog Timer Start Register                              | WDTS     | XXh                            |
| 000Fh   | Watchdog Timer Control Register                            | WDTC     | 00111111b                      |
| 0010h   | Module Standby Control Register 1                          | MSTCR1   | 00h                            |
| 0011h   |  |          |                                |
| 0012h   |  |          |                                |
| 0013h   |  |          |                                |
| 0014h   |  |          |                                |
| 0015h   |  |          |                                |
| 0016h   |  |          |                                |
| 0017h   |  |          |                                |
| 0018h   |  |          |                                |
| 0019h   |  |          |                                |
| 001Ah   |  |          |                                |
| 001Bh   |  |          |                                |
| 001Ch   | Count Source Protection Mode Register                      | CSPR     | 00h<br>10000000b (5)           |
| 001Dh   |  |          |                                |
| 001Eh   |  |          |                                |
| 001Fh   |  |          |                                |
| 0020h   | Power-Off Mode Control Register 0                          | POMCR0   | XXXXXX00b                      |
| 0021h   |  |          |                                |
| 0022h   |  |          |                                |
| 0023h   | High-Speed On-Chip Oscillator Control Register 0           | FRA0     | 00h                            |
| 0024h   | High-Speed On-Chip Oscillator Frequency Control Register 0 | FRC0     | When shipping                  |
| 0025h   | High-Speed On-Chip Oscillator Control Register 2           | FRA2     | 00h                            |
| 0026h   | On-Chip Reference Voltage Control Register                 | OCVREFCR | 00h                            |
| 0027h   |  |          |                                |
| 0028h   |  |          |                                |
| 0029h   | High-Speed On-Chip Oscillator 18 MHz Set Value Register 0  | FR18S0   | XXh                            |
| 002Ah   | High-Speed On-Chip Oscillator 18 MHz Set Value Register 1  | FR18S1   | XXh                            |
| 002Bh   |  |          |                                |
| 002Ch   |  |          |                                |
| 002Dh   |  |          |                                |
| 002Eh   |  |          |                                |
| 002Fh   | High-Speed On-Chip Oscillator Frequency Control Register 1 | FRC1     | When shipping                  |
| 0030h   | Voltage Monitor Circuit Control Register                   | CMPA     | 00h                            |
| 0031h   | Voltage Monitor Circuit Edge Select Register               | VCAC     | 00h                            |
| 0032h   |  |          |                                |
| 0033h   | Voltage Detect Register 1                                  | VCA1     | 00001000b                      |
| 0034h   | Voltage Detect Register 2                                  | VCA2     | 00h (6)<br>00100000b (7)       |
| 0035h   |  |          |                                |
| 0036h   | Voltage Detection 1 Level Select Register                  | VD1LS    | 00000111b                      |
| 0037h   |  |          |                                |
| 0038h   | Voltage Monitor 0 Circuit Control Register                 | VW0C     | 1100X010b (6)<br>1100X011b (7) |
| 0039h   | Voltage Monitor 1 Circuit Control Register                 | VW1C     | 10001010b                      |

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- The CSPO bit in the CSPR register is set to 1.
- The CWR bit in the RSTFR register is set to 0 after power-on, voltage monitor 0 reset, or exit from power-off 0 mode. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
- The reset value differs depending on the mode.
- The CSPOINI bit in the OFS register is set to 0.
- The LVDAS bit in the OFS register is set to 1.
- The LVDAS bit in the OFS register is set to 0.

**Table 4.11 SFR Information for R8C/LA8A Group (2) (1)**

| Address | Register  | Symbol      | After Reset |
|---------|---|-------------|-------------|
| 003Ah   | Voltage Monitor 2 Circuit Control Register                              | VW2C        | 10000010b   |
| 003Bh   |   |             |             |
| 003Ch   |   |             |             |
| 003Dh   |   |             |             |
| 003Eh   |   |             |             |
| 003Fh   |   |             |             |
| 0040h   |   |             |             |
| 0041h   | Flash Memory Ready Interrupt Control Register                           | FMRDYIC     | XXXXX000b   |
| 0042h   |   |             |             |
| 0043h   | INT7 Interrupt Control Register   | INT7IC      | XX00X000b   |
| 0044h   | INT6 Interrupt Control Register   | INT6IC      | XX00X000b   |
| 0045h   | INT5 Interrupt Control Register   | INT5IC      | XX00X000b   |
| 0046h   | INT4 Interrupt Control Register   | INT4IC      | XX00X000b   |
| 0047h   | Timer RC Interrupt Control Register                                     | TRCIC       | XXXXX000b   |
| 0048h   |   |             |             |
| 0049h   |   |             |             |
| 004Ah   | Timer RH Interrupt Control Register                                     | TRHIC       | XXXXX000b   |
| 004Bh   | UART2 Transmit Interrupt Control Register                               | S2TIC       | XXXXX000b   |
| 004Ch   | UART2 Receive Interrupt Control Register                                | S2RIC       | XXXXX000b   |
| 004Dh   | Key Input Interrupt Control Register                                    | KUPIC       | XXXXX000b   |
| 004Eh   | A/D Conversion Interrupt Control Register                               | ADIC        | XXXXX000b   |
| 004Fh   | SSU Interrupt Control Register / IIC bus Interrupt Control Register (2) | SSUIC/IICIC | XXXXX000b   |
| 0050h   |   |             |             |
| 0051h   | UART0 Transmit Interrupt Control Register                               | S0TIC       | XXXXX000b   |
| 0052h   | UART0 Receive Interrupt Control Register                                | S0RIC       | XXXXX000b   |
| 0053h   |   |             |             |
| 0054h   |   |             |             |
| 0055h   | INT2 Interrupt Control Register   | INT2IC      | XX00X000b   |
| 0056h   | Timer RJ0 Interrupt Control Register                                    | TRJ0IC      | XXXXX000b   |
| 0057h   | Timer RB1 Interrupt Control Register                                    | TRB1IC      | XXXXX000b   |
| 0058h   | Timer RB0 Interrupt Control Register                                    | TRB0IC      | XXXXX000b   |
| 0059h   | INT1 Interrupt Control Register   | INT1IC      | XX00X000b   |
| 005Ah   | INT3 Interrupt Control Register   | INT3IC      | XX00X000b   |
| 005Bh   | Timer RJ1 Interrupt Control Register                                    | TRJ1IC      | XXXXX000b   |
| 005Ch   | Timer RJ2 Interrupt Control Register                                    | TRJ2IC      | XXXXX000b   |
| 005Dh   | INT0 Interrupt Control Register   | INT0IC      | XX00X000b   |
| 005Eh   | UART2 Bus Collision Detection Interrupt Control Register                | U2BCNIC     | XXXXX000b   |
| 005Fh   |   |             |             |
| 0060h   |   |             |             |
| 0061h   |   |             |             |
| 0062h   |   |             |             |
| 0063h   |   |             |             |
| 0064h   |   |             |             |
| 0065h   |   |             |             |
| 0066h   |   |             |             |
| 0067h   |   |             |             |
| 0068h   |   |             |             |
| 0069h   |   |             |             |
| 006Ah   | LCD Interrupt Control Register  | LCDIC       | XXXXX000b   |
| 006Bh   |   |             |             |
| 006Ch   |   |             |             |
| 006Dh   |   |             |             |
| 006Eh   |   |             |             |
| 006Fh   |   |             |             |
| 0070h   |   |             |             |
| 0071h   |   |             |             |
| 0072h   | Voltage monitor 1 Interrupt Control Register                            | VCMP1IC     | XXXXX000b   |
| 0073h   | Voltage monitor 2 Interrupt Control Register                            | VCMP2IC     | XXXXX000b   |
| 0074h   |   |             |             |
| 0075h   |   |             |             |
| 0076h   |   |             |             |
| 0077h   |   |             |             |
| 0078h   |   |             |             |
| 0079h   |   |             |             |
| 007Ah   |   |             |             |
| 007Bh   |   |             |             |
| 007Ch   |   |             |             |
| 007Dh   |   |             |             |
| 007Eh   |   |             |             |
| 007Fh   |   |             |             |

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- Selectable by the IICSEL bit in the SSUICSR register.

**Table 4.12 SFR Information for R8C/LA8A Group (3) (1)**

| Address | Register                                      | Symbol  | After Reset |
|---------|---|---------|-------------|
| 0080h   | Timer RJ0 Control Register                    | TRJ0CR  | 00h         |
| 0081h   | Timer RJ0 I/O Control Register                | TRJ0IOC | 00h         |
| 0082h   | Timer RJ0 Mode Register                       | TRJ0MR  | 00h         |
| 0083h   | Timer RJ0 Event Pin Select Register           | TRJ0ISR | 00h         |
| 0084h   | Timer RJ0 Register                            | TRJ0    | FFh         |
| 0085h   |   |         | FFh         |
| 0086h   |   |         |             |
| 0087h   |   |         |             |
| 0088h   | Timer RJ1 Control Register                    | TRJ1CR  | 00h         |
| 0089h   | Timer RJ1 I/O Control Register                | TRJ1IOC | 00h         |
| 008Ah   | Timer RJ1 Mode Register                       | TRJ1MR  | 00h         |
| 008Bh   | Timer RJ1 Event Pin Select Register           | TRJ1ISR | 00h         |
| 008Ch   | Timer RJ1 Register                            | TRJ1    | FFh         |
| 008Dh   |   |         | FFh         |
| 008Eh   |   |         |             |
| 008Fh   |   |         |             |
| 0090h   | Timer RJ2 Control Register                    | TRJ2CR  | 00h         |
| 0091h   | Timer RJ2 I/O Control Register                | TRJ2IOC | 00h         |
| 0092h   | Timer RJ2 Mode Register                       | TRJ2MR  | 00h         |
| 0093h   | Timer RJ2 Event Pin Select Register           | TRJ2ISR | 00h         |
| 0094h   | Timer RJ2 Register                            | TRJ2    | FFh         |
| 0095h   |   |         | FFh         |
| 0096h   |   |         |             |
| 0097h   |   |         |             |
| 0098h   | Timer RB1 Control Register                    | TRB1CR  | 00h         |
| 0099h   | Timer RB1 One-Shot Control Register           | TRB1OCR | 00h         |
| 009Ah   | Timer RB1 I/O Control Register                | TRB1IOC | 00h         |
| 009Bh   | Timer RB1 Mode Register                       | TRB1MR  | 00h         |
| 009Ch   | Timer RB1 Prescaler Register                  | TRB1PRE | FFh         |
| 009Dh   | Timer RB1 Secondary Register                  | TRB1SC  | FFh         |
| 009Eh   | Timer RB1 Primary Register                    | TRB1PR  | FFh         |
| 009Fh   |   |         |             |
| 00A0h   | UART0 Transmit/Receive Mode Register          | U0MR    | 00h         |
| 00A1h   | UART0 Bit Rate Register                       | U0BRG   | XXh         |
| 00A2h   | UART0 Transmit Buffer Register                | U0TB    | XXh         |
| 00A3h   |   |         | XXh         |
| 00A4h   | UART0 Transmit/Receive Control Register 0     | U0C0    | 00001000b   |
| 00A5h   | UART0 Transmit/Receive Control Register 1     | U0C1    | 00000010b   |
| 00A6h   | UART0 Receive Buffer Register                 | U0RB    | XXh         |
| 00A7h   |   |         | XXh         |
| 00A8h   | UART2 Transmit/Receive Mode Register          | U2MR    | 00h         |
| 00A9h   | UART2 Bit Rate Register                       | U2BRG   | XXh         |
| 00AAh   | UART2 Transmit Buffer Register                | U2TB    | XXh         |
| 00ABh   |   |         | XXh         |
| 00ACh   | UART2 Transmit/Receive Control Register 0     | U2C0    | 00001000b   |
| 00ADh   | UART2 Transmit/Receive Control Register 1     | U2C1    | 00000010b   |
| 00AEh   | UART2 Receive Buffer Register                 | U2RB    | XXh         |
| 00AFh   |   |         | XXh         |
| 00B0h   | UART2 Digital Filter Function Select Register | URXDF   | 00h         |
| 00B1h   |   |         |             |
| 00B2h   |   |         |             |
| 00B3h   |   |         |             |
| 00B4h   |   |         |             |
| 00B5h   |   |         |             |
| 00B6h   |   |         |             |
| 00B7h   |   |         |             |
| 00B8h   |   |         |             |
| 00B9h   |   |         |             |
| 00BAh   |   |         |             |
| 00BBh   | UART2 Special Mode Register 5                 | U2SMR5  | 00h         |
| 00BCh   | UART2 Special Mode Register 4                 | U2SMR4  | 00h         |
| 00BDh   | UART2 Special Mode Register 3                 | U2SMR3  | 000X0X0Xb   |
| 00BEh   | UART2 Special Mode Register 2                 | U2SMR2  | X0000000b   |
| 00BFh   | UART2 Special Mode Register                   | U2SMR   | X0000000b   |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

**Table 4.13 SFR Information for R8C/LA8A Group (4) (1)**

| Address | Register                   | Symbol  | After Reset |
|---------|----------------------------|---------|-------------|
| 00C0h   | A/D Register 0             | AD0     | XXh         |
| 00C1h   |                            |         | 000000XXb   |
| 00C2h   | A/D Register 1             | AD1     | XXh         |
| 00C3h   |                            |         | 000000XXb   |
| 00C4h   | A/D Register 2             | AD2     | XXh         |
| 00C5h   |                            |         | 000000XXb   |
| 00C6h   | A/D Register 3             | AD3     | XXh         |
| 00C7h   |                            |         | 000000XXb   |
| 00C8h   | A/D Register 4             | AD4     | XXh         |
| 00C9h   |                            |         | 000000XXb   |
| 00CAh   | A/D Register 5             | AD5     | XXh         |
| 00CBh   |                            |         | 000000XXb   |
| 00CCh   | A/D Register 6             | AD6     | XXh         |
| 00CDh   |                            |         | 000000XXb   |
| 00CEh   | A/D Register 7             | AD7     | XXh         |
| 00CFh   |                            |         | 000000XXb   |
| 00D0h   |                            |         |             |
| 00D1h   |                            |         |             |
| 00D2h   |                            |         |             |
| 00D3h   |                            |         |             |
| 00D4h   | A/D Mode Register          | ADMOD   | 00h         |
| 00D5h   | A/D Input Select Register  | ADINSEL | 11000000b   |
| 00D6h   | A/D Control Register 0     | ADCON0  | 00h         |
| 00D7h   | A/D Control Register 1     | ADCON1  | 00h         |
| 00D8h   |                            |         |             |
| 00D9h   |                            |         |             |
| 00DAh   |                            |         |             |
| 00DBh   |                            |         |             |
| 00DCh   |                            |         |             |
| 00DDh   | A/D Control Register 2     | ADCON2  | 00h         |
| 00DEh   |                            |         |             |
| 00DFh   |                            |         |             |
| 00E0h   | Port P0 Register           | P0      | XXh         |
| 00E1h   | Port P1 Register           | P1      | XXh         |
| 00E2h   | Port P0 Direction Register | PD0     | 00h         |
| 00E3h   | Port P1 Direction Register | PD1     | 00h         |
| 00E4h   | Port P2 Register           | P2      | XXh         |
| 00E5h   | Port P3 Register           | P3      | XXh         |
| 00E6h   | Port P2 Direction Register | PD2     | 00h         |
| 00E7h   | Port P3 Direction Register | PD3     | 00h         |
| 00E8h   | Port P4 Register           | P4      | XXh         |
| 00E9h   | Port P5 Register           | P5      | XXh         |
| 00EAh   | Port P4 Direction Register | PD4     | 00h         |
| 00EBh   | Port P5 Direction Register | PD5     | 00h         |
| 00ECh   | Port P6 Register           | P6      | XXh         |
| 00EDh   | Port P7 Register           | P7      | XXh         |
| 00EEh   | Port P6 Direction Register | PD6     | 00h         |
| 00EFh   | Port P7 Direction Register | PD7     | 00h         |
| 00F0h   | Port P8 Register           | P8      | XXh         |
| 00F1h   | Port P9 Register           | P9      | XXh         |
| 00F2h   | Port P8 Direction Register | PD8     | 00h         |
| 00F3h   | Port P9 Direction Register | PD9     | 00h         |
| 00F4h   |                            |         |             |
| 00F5h   |                            |         |             |
| 00F6h   |                            |         |             |
| 00F7h   |                            |         |             |
| 00F8h   |                            |         |             |
| 00F9h   |                            |         |             |
| 00FAh   |                            |         |             |
| 00FBh   |                            |         |             |
| 00FCh   |                            |         |             |
| 00FDh   |                            |         |             |
| 00FEh   |                            |         |             |
| 00FFh   |                            |         |             |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

**Table 4.14 SFR Information for R8C/LA8A Group (5) (1)**

| Address | Register  | Symbol  | After Reset                |
|---------|---|---------|----------------------------|
| 0100h   |   |         |                            |
| 0101h   |   |         |                            |
| 0102h   |   |         |                            |
| 0103h   |   |         |                            |
| 0104h   |   |         |                            |
| 0105h   |   |         |                            |
| 0106h   |   |         |                            |
| 0107h   |   |         |                            |
| 0108h   | Timer RB0 Control Register                            | TRB0CR  | 00h                        |
| 0109h   | Timer RB0 One-Shot Control Register                   | TRB0OCR | 00h                        |
| 010Ah   | Timer RB0 I/O Control Register                        | TRB0IOC | 00h                        |
| 010Bh   | Timer RB0 Mode Register                               | TRB0MR  | 00h                        |
| 010Ch   | Timer RB0 Prescaler Register                          | TRB0PRE | FFh                        |
| 010Dh   | Timer RB0 Secondary Register                          | TRB0SC  | FFh                        |
| 010Eh   | Timer RB0 Primary Register                            | TRB0PR  | FFh                        |
| 010Fh   |   |         |                            |
| 0110h   | Timer RH Second Data Register / Counter Data Register | TRHSEC  | XXh<br>00h (2)             |
| 0111h   | Timer RH Minute Data Register / Compare Data Register | TRHMIN  | XXh<br>00h (2)             |
| 0112h   | Timer RH Hour Data Register                           | TRHHR   | 00XXXXXXb<br>00h (2)       |
| 0113h   | Timer RH Day-of-the-Week Data Register                | TRHWK   | 00000XXXb<br>00h (2)       |
| 0114h   | Timer RH Date Data Register                           | TRHDY   | 00XXXXXXb<br>00000001b (2) |
| 0115h   | Timer RH Month Data Register                          | TRHMON  | 000XXXXXb<br>00000001b (2) |
| 0116h   | Timer RH Year Data Register                           | TRHYR   | XXh<br>00h (2)             |
| 0117h   | Timer RH Control Register                             | TRHCR   | XXX000XXb<br>000XX1X0b (2) |
| 0118h   | Timer RH Count Source Select Register                 | TRHCSR  | X0001000b<br>0XXXXXXXb (2) |
| 0119h   | Timer RH Clock Error Correction Register              | TRHADJ  | XXh<br>00h (2)             |
| 011Ah   | Timer RH Interrupt Flag Register                      | TRHIFR  | 00000XXXb<br>000XX000b (2) |
| 011Bh   | Timer RH Interrupt Enable Register                    | TRHIER  | XXh<br>00h (2)             |
| 011Ch   | Timer RH Alarm Minute Register                        | TRHAMN  | XXh<br>00h (2)             |
| 011Dh   | Timer RH Alarm Hour Register                          | TRHAHR  | XXh<br>00h (2)             |
| 011Eh   | Timer RH Alarm Day-of-the-Week Register               | TRHAWK  | X0000XXXb<br>00h (2)       |
| 011Fh   | Timer RH Protect Register                             | TRHPRC  | 00h<br>X0000000b (2)       |
| 0120h   | Timer RC Mode Register                                | TRCMR   | 01001000b                  |
| 0121h   | Timer RC Control Register 1                           | TRCCR1  | 00h                        |
| 0122h   | Timer RC Interrupt Enable Register                    | TRCIER  | 01110000b                  |
| 0123h   | Timer RC Status Register                              | TRCSR   | 01110000b                  |
| 0124h   | Timer RC I/O Control Register 0                       | TRCIOR0 | 10001000b                  |
| 0125h   | Timer RC I/O Control Register 1                       | TRCIOR1 | 10001000b                  |
| 0126h   | Timer RC Counter                                      | TRC     | 00h<br>00h                 |
| 0127h   |   |         |                            |
| 0128h   | Timer RC General Register A                           | TRCGRA  | FFh<br>FFh                 |
| 0129h   |   |         |                            |
| 012Ah   | Timer RC General Register B                           | TRCGRB  | FFh<br>FFh                 |
| 012Bh   |   |         |                            |
| 012Ch   | Timer RC General Register C                           | TRCGRC  | FFh<br>FFh                 |
| 012Dh   |   |         |                            |
| 012Eh   | Timer RC General Register D                           | TRCGRD  | FFh<br>FFh                 |
| 012Fh   |   |         |                            |
| 0130h   | Timer RC Control Register 2                           | TRCCR2  | 00011000b                  |
| 0131h   | Timer RC Digital Filter Function Select Register      | TRCDF   | 00h                        |
| 0132h   | Timer RC Output Master Enable Register                | TRCOER  | 01111111b                  |
| 0133h   | Timer RC Trigger Control Register                     | TRCADCR | 00h                        |
| 0134h   |   |         |                            |
| 0135h   |   |         |                            |
| 0136h   |   |         |                            |
| 0137h   |   |         |                            |
| 0138h   |   |         |                            |
| 0139h   |   |         |                            |
| 013Ah   |   |         |                            |
| 013Bh   |   |         |                            |
| 013Ch   |   |         |                            |
| 013Dh   |   |         |                            |
| 013Eh   |   |         |                            |
| 013Fh   |   |         |                            |

X: Undefined

Notes:

1. Blank spaces are reserved. No access is allowed.
2. This is the reset value after reset by RTCRST bit in TRHCR register.

**Table 4.15 SFR Information for R8C/LA8A Group (6) (1)**

| Address | Register | Symbol | After Reset |
|---------|----------|--------|-------------|
| 0140h   |          |        |             |
| 0141h   |          |        |             |
| 0142h   |          |        |             |
| 0143h   |          |        |             |
| 0144h   |          |        |             |
| 0145h   |          |        |             |
| 0146h   |          |        |             |
| 0147h   |          |        |             |
| 0148h   |          |        |             |
| 0149h   |          |        |             |
| 014Ah   |          |        |             |
| 014Bh   |          |        |             |
| 014Ch   |          |        |             |
| 014Dh   |          |        |             |
| 014Eh   |          |        |             |
| 014Fh   |          |        |             |
| 0150h   |          |        |             |
| 0151h   |          |        |             |
| 0152h   |          |        |             |
| 0153h   |          |        |             |
| 0154h   |          |        |             |
| 0155h   |          |        |             |
| 0156h   |          |        |             |
| 0157h   |          |        |             |
| 0158h   |          |        |             |
| 0159h   |          |        |             |
| 015Ah   |          |        |             |
| 015Bh   |          |        |             |
| 015Ch   |          |        |             |
| 015Dh   |          |        |             |
| 015Eh   |          |        |             |
| 015Fh   |          |        |             |
| 0160h   |          |        |             |
| 0161h   |          |        |             |
| 0162h   |          |        |             |
| 0163h   |          |        |             |
| 0164h   |          |        |             |
| 0165h   |          |        |             |
| 0166h   |          |        |             |
| 0167h   |          |        |             |
| 0168h   |          |        |             |
| 0169h   |          |        |             |
| 016Ah   |          |        |             |
| 016Bh   |          |        |             |
| 016Ch   |          |        |             |
| 016Dh   |          |        |             |
| 016Eh   |          |        |             |
| 016Fh   |          |        |             |
| 0170h   |          |        |             |
| 0171h   |          |        |             |
| 0172h   |          |        |             |
| 0173h   |          |        |             |
| 0174h   |          |        |             |
| 0175h   |          |        |             |
| 0176h   |          |        |             |
| 0177h   |          |        |             |
| 0178h   |          |        |             |
| 0179h   |          |        |             |
| 017Ah   |          |        |             |
| 017Bh   |          |        |             |
| 017Ch   |          |        |             |
| 017Dh   |          |        |             |
| 017Eh   |          |        |             |
| 017Fh   |          |        |             |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

**Table 4.16 SFR Information for R8C/LA8A Group (7) (1)**

| Address | Register   | Symbol      | After Reset                |
|---------|--|-------------|----------------------------|
| 0180h   | Timer RJ Pin Select Register                                     | TRJSR       | 00h                        |
| 0181h   | Timer RB Pin Select Register                                     | TRBSR       | 00h                        |
| 0182h   | Timer RC Pin Select Register 0                                   | TRCPSR0     | 00h                        |
| 0183h   | Timer RC Pin Select Register 1                                   | TRCPSR1     | 00h                        |
| 0184h   |  |             |                            |
| 0185h   |  |             |                            |
| 0186h   |  |             |                            |
| 0187h   |  |             |                            |
| 0188h   | UART0 Pin Select Register  | U0SR        | 00h                        |
| 0189h   |  |             |                            |
| 018Ah   | UART2 Pin Select Register 0                                      | U2SR0       | 00h                        |
| 018Bh   | UART2 Pin Select Register 1                                      | U2SR1       | 00h                        |
| 018Ch   | SSU/IIC Pin Select Register                                      | SSUICSR     | 00h                        |
| 018Dh   | Timer RH Second Interrupt Control Register                       | TRHICR      | X0XXXXXXb<br>00000001b (3) |
| 018Eh   | INT Interrupt Input Pin Select Register                          | INTSR       | 00h                        |
| 018Fh   | I/O Function Pin Select Register                                 | PINSR       | 00h                        |
| 0190h   |  |             |                            |
| 0191h   |  |             |                            |
| 0192h   |  |             |                            |
| 0193h   | SS Bit Counter Register  | SSBR        | 11111000b                  |
| 0194h   | SS Transmit Data Register L / IIC bus Transmit Data Register (2) | SSTDR/ICDRT | FFh                        |
| 0195h   | SS Transmit Data Register H (2)                                  | SSTDRH      | FFh                        |
| 0196h   | SS Receive Data Register L / IIC bus Receive Data Register (2)   | SSRDR/ICDRR | FFh                        |
| 0197h   | SS Receive Data Register H (2)                                   | SSRDRH      | FFh                        |
| 0198h   | SS Control Register H / IIC bus Control Register 1 (2)           | SSCRH/ICCR1 | 00h                        |
| 0199h   | SS Control Register L / IIC bus Control Register 2 (2)           | SSCRL/ICCR2 | 01111101b                  |
| 019Ah   | SS Mode Register / IIC bus Mode Register (2)                     | SSMR/ICMR   | 00010000b/00011000b        |
| 019Bh   | SS Enable Register / IIC bus Interrupt Enable Register (2)       | SSER/ICIER  | 00h                        |
| 019Ch   | SS Status Register / IIC bus Status Register (2)                 | SSSR/ICSR   | 00h/0000X000b              |
| 019Dh   | SS Mode Register 2 / Slave Address Register (2)                  | SSMR2/SAR   | 00h                        |
| 019Eh   |  |             |                            |
| 019Fh   |  |             |                            |
| 01A0h   |  |             |                            |
| 01A1h   |  |             |                            |
| 01A2h   |  |             |                            |
| 01A3h   |  |             |                            |
| 01A4h   |  |             |                            |
| 01A5h   |  |             |                            |
| 01A6h   |  |             |                            |
| 01A7h   |  |             |                            |
| 01A8h   |  |             |                            |
| 01A9h   |  |             |                            |
| 01AAh   |  |             |                            |
| 01ABh   |  |             |                            |
| 01ACh   |  |             |                            |
| 01ADh   |  |             |                            |
| 01AEh   |  |             |                            |
| 01AFh   |  |             |                            |
| 01B0h   |  |             |                            |
| 01B1h   |  |             |                            |
| 01B2h   | Flash Memory Status Register                                     | FST         | 10000X00b                  |
| 01B3h   |  |             |                            |
| 01B4h   | Flash Memory Control Register 0                                  | FMR0        | 00h                        |
| 01B5h   | Flash Memory Control Register 1                                  | FMR1        | 000000X0b                  |
| 01B6h   | Flash Memory Control Register 2                                  | FMR2        | 00h                        |
| 01B7h   |  |             |                            |
| 01B8h   |  |             |                            |
| 01B9h   |  |             |                            |
| 01BAh   |  |             |                            |
| 01BBh   |  |             |                            |
| 01BCh   |  |             |                            |
| 01BDh   |  |             |                            |
| 01BEh   |  |             |                            |
| 01BFh   |  |             |                            |

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- Selectable by the IICSEL bit in the SSUICSR register.
- This is the reset value after reset by RTCRST bit in TRHCR register.



**Table 4.17 SFR Information for R8C/LA8A Group (8) (1)**

| Address | Register                                  | Symbol | After Reset |
|---------|---|--------|-------------|
| 01C0h   | Address Match Interrupt Register 0        | RMAD0  | XXh         |
| 01C1h   |   |        | XXh         |
| 01C2h   |   |        | 0000XXXXb   |
| 01C3h   | Address Match Interrupt Enable Register 0 | AIER0  | 00h         |
| 01C4h   | Address Match Interrupt Register 1        | RMAD1  | XXh         |
| 01C5h   |   |        | XXh         |
| 01C6h   |   |        | 0000XXXXb   |
| 01C7h   | Address Match Interrupt Enable Register 1 | AIER1  | 00h         |
| 01C8h   |   |        |             |
| 01C9h   |   |        |             |
| 01CAh   |   |        |             |
| 01CBh   |   |        |             |
| 01CCh   |   |        |             |
| 01CDh   |   |        |             |
| 01CEh   |   |        |             |
| 01CFh   |   |        |             |
| 01D0h   |   |        |             |
| 01D1h   |   |        |             |
| 01D2h   |   |        |             |
| 01D3h   |   |        |             |
| 01D4h   |   |        |             |
| 01D5h   |   |        |             |
| 01D6h   |   |        |             |
| 01D7h   |   |        |             |
| 01D8h   |   |        |             |
| 01D9h   |   |        |             |
| 01DAh   |   |        |             |
| 01DBh   |   |        |             |
| 01DCh   |   |        |             |
| 01DDh   |   |        |             |
| 01DEh   |   |        |             |
| 01DFh   |   |        |             |
| 01E0h   | Port P0 Pull-Up Control Register          | P0PUR  | 00h         |
| 01E1h   | Port P1 Pull-Up Control Register          | P1PUR  | 00h         |
| 01E2h   | Port P2 Pull-Up Control Register          | P2PUR  | 00h         |
| 01E3h   | Port P3 Pull-Up Control Register          | P3PUR  | 00h         |
| 01E4h   | Port P4 Pull-Up Control Register          | P4PUR  | 00h         |
| 01E5h   | Port P5 Pull-Up Control Register          | P5PUR  | 00h         |
| 01E6h   | Port P6 Pull-Up Control Register          | P6PUR  | 00h         |
| 01E7h   | Port P7 Pull-Up Control Register          | P7PUR  | 00h         |
| 01E8h   | Port P8 Pull-Up Control Register          | P8PUR  | 00h         |
| 01E9h   | Port P9 Pull-Up Control Register          | P9PUR  | 00h         |
| 01EAh   |   |        |             |
| 01EBh   |   |        |             |
| 01ECh   |   |        |             |
| 01EDh   |   |        |             |
| 01EEh   |   |        |             |
| 01EFh   |   |        |             |
| 01F0h   | Port P7 Drive Capacity Control Register   | P7DRR  | 00h         |
| 01F1h   | Port P8 Drive Capacity Control Register   | P8DRR  | 00h         |
| 01F2h   |   |        |             |
| 01F3h   |   |        |             |
| 01F4h   |   |        |             |
| 01F5h   | Input Threshold Control Register 0        | VLT0   | 00h         |
| 01F6h   | Input Threshold Control Register 1        | VLT1   | 00h         |
| 01F7h   | Input Threshold Control Register 2        | VLT2   | 00h         |
| 01F8h   | Comparator B Control Register 0           | INTCMP | 00h         |
| 01F9h   |   |        |             |
| 01FAh   | External Input Enable Register 0          | INTEN  | 00h         |
| 01FBh   | External Input Enable Register 1          | INTEN1 | 00h         |
| 01FCh   | INT Input Filter Select Register 0        | INTF   | 00h         |
| 01FDh   | INT Input Filter Select Register 1        | INTF1  | 00h         |
| 01FEh   | Key Input Enable Register 0               | KIEN   | 00h         |
| 01FFh   | Key Input Enable Register 1               | KIEN1  | 00h         |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

**Table 4.18 SFR Information for R8C/LA8A Group (9) (1)**

| Address | Register                          | Symbol | After Reset |
|---------|-----------------------------------|--------|-------------|
| 0200h   | LCD Control Register              | LCR0   | 00h         |
| 0201h   |                                   |        |             |
| 0202h   | LCD Option Clock Control Register | LCR2   | 00h         |
| 0203h   | LCD Clock Control Register        | LCR3   | 00h         |
| 0204h   | LCD Display Control Register      | LCR4   | 00h         |
| 0205h   |                                   |        |             |
| 0206h   | LCD Port Select Register 0        | LSE0   | 00h         |
| 0207h   | LCD Port Select Register 1        | LSE1   | 00h         |
| 0208h   | LCD Port Select Register 2        | LSE2   | 00h         |
| 0209h   | LCD Port Select Register 3        | LSE3   | 00h         |
| 020Ah   | LCD Port Select Register 4        | LSE4   | 00h         |
| 020Bh   | LCD Port Select Register 5        | LSE5   | 00h         |
| 020Ch   |                                   |        |             |
| 020Dh   |                                   |        |             |
| 020Eh   |                                   |        |             |
| 020Fh   |                                   |        |             |
| 0210h   | LCD Display Data Register         | LRA0L  | XXh         |
| 0211h   |                                   | LRA1L  | XXh         |
| 0212h   |                                   | LRA2L  | XXh         |
| 0213h   |                                   | LRA3L  | XXh         |
| 0214h   |                                   | LRA4L  | XXh         |
| 0215h   |                                   | LRA5L  | XXh         |
| 0216h   |                                   | LRA6L  | XXh         |
| 0217h   |                                   | LRA7L  | XXh         |
| 0218h   |                                   | LRA8L  | XXh         |
| 0219h   |                                   | LRA9L  | XXh         |
| 021Ah   |                                   | LRA10L | XXh         |
| 021Bh   |                                   | LRA11L | XXh         |
| 021Ch   |                                   | LRA12L | XXh         |
| 021Dh   |                                   | LRA13L | XXh         |
| 021Eh   |                                   | LRA14L | XXh         |
| 021Fh   |                                   | LRA15L | XXh         |
| 0220h   |                                   | LRA16L | XXh         |
| 0221h   |                                   | LRA17L | XXh         |
| 0222h   |                                   | LRA18L | XXh         |
| 0223h   |                                   | LRA19L | XXh         |
| 0224h   |                                   | LRA20L | XXh         |
| 0225h   |                                   | LRA21L | XXh         |
| 0226h   |                                   | LRA22L | XXh         |
| 0227h   |                                   | LRA23L | XXh         |
| 0228h   |                                   | LRA24L | XXh         |
| 0229h   |                                   | LRA25L | XXh         |
| 022Ah   |                                   | LRA26L | XXh         |
| 022Bh   |                                   | LRA27L | XXh         |
| 022Ch   |                                   | LRA28L | XXh         |
| 022Dh   |                                   | LRA29L | XXh         |
| 022Eh   |                                   | LRA30L | XXh         |
| 022Fh   |                                   | LRA31L | XXh         |
| 0230h   |                                   | LRA32L | XXh         |
| 0231h   |                                   | LRA33L | XXh         |
| 0232h   |                                   | LRA34L | XXh         |
| 0233h   |                                   | LRA35L | XXh         |
| 0234h   |                                   | LRA36L | XXh         |
| 0235h   |                                   | LRA37L | XXh         |
| 0236h   |                                   | LRA38L | XXh         |
| 0237h   |                                   | LRA39L | XXh         |
| :       |                                   |        |             |
| 2FFh    |                                   |        |             |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

**Table 4.19 ID Code Areas and Option Function Select Area**

| Address | Area Name                         | Symbol | After Reset |
|---------|-----------------------------------|--------|-------------|
| FFDBh   | Option Function Select Register 2 | OFS2   | (Note 1)    |
| FFDFh   | ID1                               |        | (Note 2)    |
| FFE3h   | ID2                               |        | (Note 2)    |
| FFEBh   | ID3                               |        | (Note 2)    |
| FFEFh   | ID4                               |        | (Note 2)    |
| FFF3h   | ID5                               |        | (Note 2)    |
| FFF7h   | ID6                               |        | (Note 2)    |
| FFFBh   | ID7                               |        | (Note 2)    |
| FFFh    | Option Function Select Register   | OFS    | (Note 1)    |

## Notes:

- The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.  
Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.  
When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.  
When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
- The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.  
Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.  
When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.  
When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

## 5. Electrical Characteristics

### 5.1 Electrical Characteristics (R8C/LA3A Group and R8C/LA5A Group)

#### 5.1.1 Absolute Maximum Ratings

**Table 5.1 Absolute Maximum Ratings**

| Symbol                            | Parameter                     |               | Condition   | Rated Value                                     | Unit |
|-----------------------------------|-------------------------------|---------------|---|---|------|
| V <sub>cc</sub> /AV <sub>cc</sub> | Supply voltage                |               |   | -0.3 to 6.5                                     | V    |
| V <sub>i</sub>                    | Input voltage                 | XIN           | XIN-XOUT oscillation on (oscillation buffer ON) <sup>(1)</sup>  | -0.3 to 1.9                                     | V    |
|                                   |                               | XIN           | XIN-XOUT oscillation on (oscillation buffer OFF) <sup>(1)</sup> | -0.3 to V <sub>cc</sub> + 0.3                   | V    |
|                                   |                               | P5_4/VL1      |   | -0.3 to VL2 <sup>(2)</sup>                      | V    |
|                                   |                               | P5_5/VL2      |   | VL1 to VL3                                      | V    |
|                                   |                               | P5_6/VL3      |   | VL2 to 6.5                                      | V    |
|                                   |                               | Other pins    |   | -0.3 to V <sub>cc</sub> + 0.3                   | V    |
| V <sub>o</sub>                    | Output voltage                | XOUT          | XIN-XOUT oscillation on (oscillation buffer ON) <sup>(1)</sup>  | -0.3 to 1.9                                     | V    |
|                                   |                               | XOUT          | XIN-XOUT oscillation on (oscillation buffer OFF) <sup>(1)</sup> | -0.3 to V <sub>cc</sub> + 0.3                   | V    |
|                                   |                               | COM0 to COM3  |   | -0.3 to VL3                                     | V    |
|                                   |                               | SEG0 to SEG26 |   | -0.3 to VL3                                     | V    |
|                                   |                               | Other pins    |   | -0.3 to V <sub>cc</sub> + 0.3                   | V    |
| P <sub>d</sub>                    | Power dissipation             |               | -40 °C ≤ T <sub>opr</sub> ≤ 85 °C                               | 500   | mW   |
| T <sub>opr</sub>                  | Operating ambient temperature |               |   | -20 to 85 (N version)/<br>-40 to 85 (D version) | °C   |
| T <sub>stg</sub>                  | Storage temperature           |               |   | -65 to 150                                      | °C   |

Notes:

- For the register settings for each operation, refer to **7. I/O Ports** and **9. Clock Generation Circuit** in the User's Manual: Hardware.
- The VL1 voltage should be VCC or below.

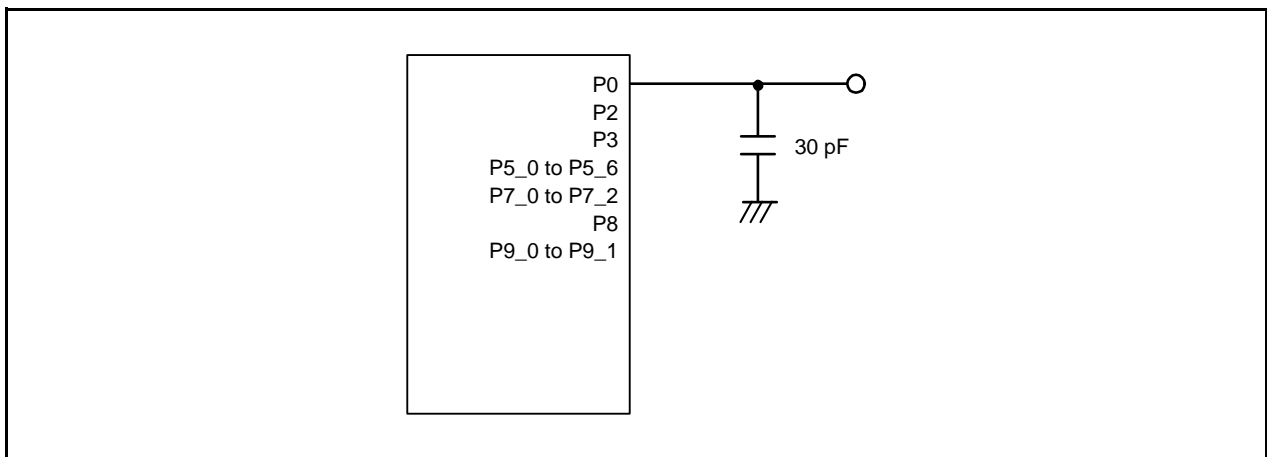
## 5.1.2 Recommended Operating Conditions

**Table 5.2 Recommended Operating Conditions**  
(V<sub>CC</sub> = 1.8 to 5.5 V and T<sub>opr</sub> = -20 to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.)

| Symbol                            | Parameter                                      |                                       |   | Conditions                                   | Standard                        |                      |                      | Unit                 |     |
|-----------------------------------|--|---------------------------------------|---|--|---------------------------------|----------------------|----------------------|----------------------|-----|
|                                   |  |                                       |   |  | Min.                            | Typ.                 | Max.                 |                      |     |
| V <sub>CC</sub> /AV <sub>CC</sub> | Supply voltage                                 |                                       |   |  | 1.8                             | -                    | 5.5                  | V                    |     |
| V <sub>SS</sub> /AV <sub>SS</sub> | Supply voltage                                 |                                       |   |  | -                               | 0                    | -                    | V                    |     |
| V <sub>IH</sub>                   | Input "H" voltage                              | Other than CMOS input                 |   | 4.0 V ≤ V <sub>CC</sub> ≤ 5.5 V              | 0.8 V <sub>CC</sub>             | -                    | V <sub>CC</sub>      | V                    |     |
|                                   |  |                                       |   | 2.7 V ≤ V <sub>CC</sub> < 4.0 V              | 0.8 V <sub>CC</sub>             | -                    | V <sub>CC</sub>      | V                    |     |
|                                   |  |                                       |   | 1.8 V ≤ V <sub>CC</sub> < 2.7 V              | 0.9 V <sub>CC</sub>             | -                    | V <sub>CC</sub>      | V                    |     |
|                                   |  | CMOS input                            | Input level switching function (I/O port) | Input level selection : 0.35 V <sub>CC</sub> | 4.0 V ≤ V <sub>CC</sub> ≤ 5.5 V | 0.5 V <sub>CC</sub>  | -                    | V <sub>CC</sub>      | V   |
|                                   |  |                                       |   |  | 2.7 V ≤ V <sub>CC</sub> < 4.0 V | 0.55 V <sub>CC</sub> | -                    | V <sub>CC</sub>      | V   |
|                                   |  |                                       |   |  | 1.8 V ≤ V <sub>CC</sub> < 2.7 V | 0.65 V <sub>CC</sub> | -                    | V <sub>CC</sub>      | V   |
|                                   |  |                                       |   | Input level selection : 0.5 V <sub>CC</sub>  | 4.0 V ≤ V <sub>CC</sub> ≤ 5.5 V | 0.65 V <sub>CC</sub> | -                    | V <sub>CC</sub>      | V   |
|                                   |  |                                       |   |  | 2.7 V ≤ V <sub>CC</sub> < 4.0 V | 0.7 V <sub>CC</sub>  | -                    | V <sub>CC</sub>      | V   |
|                                   |  |                                       |   |  | 1.8 V ≤ V <sub>CC</sub> < 2.7 V | 0.8 V <sub>CC</sub>  | -                    | V <sub>CC</sub>      | V   |
|                                   |  |                                       |   | Input level selection : 0.7 V <sub>CC</sub>  | 4.0 V ≤ V <sub>CC</sub> ≤ 5.5 V | 0.85 V <sub>CC</sub> | -                    | V <sub>CC</sub>      | V   |
|                                   |  |                                       |   |  | 2.7 V ≤ V <sub>CC</sub> < 4.0 V | 0.85 V <sub>CC</sub> | -                    | V <sub>CC</sub>      | V   |
|                                   |  |                                       |   |  | 1.8 V ≤ V <sub>CC</sub> < 2.7 V | 0.85 V <sub>CC</sub> | -                    | V <sub>CC</sub>      | V   |
| V <sub>IL</sub>                   | Input "L" voltage                              | Other than CMOS input                 |   | 4.0 V ≤ V <sub>CC</sub> ≤ 5.5 V              | 0                               | -                    | 0.2 V <sub>CC</sub>  | V                    |     |
|                                   |  |                                       |   | 2.7 V ≤ V <sub>CC</sub> < 4.0 V              | 0                               | -                    | 0.2 V <sub>CC</sub>  | V                    |     |
|                                   |  |                                       |   | 1.8 V ≤ V <sub>CC</sub> < 2.7 V              | 0                               | -                    | 0.05 V <sub>CC</sub> | V                    |     |
|                                   |  | CMOS input                            | Input level switching function (I/O port) | Input level selection : 0.35 V <sub>CC</sub> | 4.0 V ≤ V <sub>CC</sub> ≤ 5.5 V | 0                    | -                    | 0.2 V <sub>CC</sub>  | V   |
|                                   |  |                                       |   |  | 2.7 V ≤ V <sub>CC</sub> < 4.0 V | 0                    | -                    | 0.2 V <sub>CC</sub>  | V   |
|                                   |  |                                       |   |  | 1.8 V ≤ V <sub>CC</sub> < 2.7 V | 0                    | -                    | 0.2 V <sub>CC</sub>  | V   |
|                                   |  |                                       |   | Input level selection : 0.5 V <sub>CC</sub>  | 4.0 V ≤ V <sub>CC</sub> ≤ 5.5 V | 0                    | -                    | 0.4 V <sub>CC</sub>  | V   |
|                                   |  |                                       |   |  | 2.7 V ≤ V <sub>CC</sub> < 4.0 V | 0                    | -                    | 0.3 V <sub>CC</sub>  | V   |
|                                   |  |                                       |   |  | 1.8 V ≤ V <sub>CC</sub> < 2.7 V | 0                    | -                    | 0.2 V <sub>CC</sub>  | V   |
|                                   |  |                                       |   | Input level selection : 0.7 V <sub>CC</sub>  | 4.0 V ≤ V <sub>CC</sub> ≤ 5.5 V | 0                    | -                    | 0.55 V <sub>CC</sub> | V   |
|                                   |  |                                       |   |  | 2.7 V ≤ V <sub>CC</sub> < 4.0 V | 0                    | -                    | 0.45 V <sub>CC</sub> | V   |
|                                   |  |                                       |   |  | 1.8 V ≤ V <sub>CC</sub> < 2.7 V | 0                    | -                    | 0.35 V <sub>CC</sub> | V   |
| I <sub>OH(sum)</sub>              | Peak sum output "H" current                    | Sum of all pins I <sub>OH(peak)</sub> |   |  | -                               | -                    | -160                 | mA                   |     |
| I <sub>OH(sum)</sub>              | Average sum output "H" current                 | Sum of all pins I <sub>OH(avg)</sub>  |   |  | -                               | -                    | -80                  | mA                   |     |
| I <sub>OH(peak)</sub>             | Peak output "H" current                        | Port P8 (2)                           |   |  | -                               | -                    | -40                  | mA                   |     |
|                                   |  | Other pins                            |   |  | -                               | -                    | -10                  | mA                   |     |
| I <sub>OH(avg)</sub>              | Average output "H" current (1)                 | Port P8 (2)                           |   |  | -                               | -                    | -20                  | mA                   |     |
|                                   |  | Other pins                            |   |  | -                               | -                    | -5                   | mA                   |     |
| I <sub>OL(sum)</sub>              | Peak sum output "L" current                    | Sum of all pins I <sub>OL(peak)</sub> |   |  | -                               | -                    | 160                  | mA                   |     |
| I <sub>OL(sum)</sub>              | Average sum output "L" current                 | Sum of all pins I <sub>OL(avg)</sub>  |   |  | -                               | -                    | 80                   | mA                   |     |
| I <sub>OL(peak)</sub>             | Peak output "L" current                        | Port P8 (2)                           |   |  | -                               | -                    | 40                   | mA                   |     |
|                                   |  | Other pins                            |   |  | -                               | -                    | 10                   | mA                   |     |
| I <sub>OL(avg)</sub>              | Average output "L" current (1)                 | Port P8 (2)                           |   |  | -                               | -                    | 20                   | mA                   |     |
|                                   |  | Other pins                            |   |  | -                               | -                    | 5                    | mA                   |     |
| f <sub>(XIN)</sub>                | XIN clock input oscillation frequency          | 2.7 V ≤ V <sub>CC</sub> ≤ 5.5 V       |   |  | 2                               | -                    | 20                   | MHz                  |     |
|                                   |  | 1.8 V ≤ V <sub>CC</sub> < 2.7 V       |   |  | 2                               | -                    | 8                    | MHz                  |     |
| f <sub>(XCIN)</sub>               | XCIN oscillation frequency                     | 1.8 V ≤ V <sub>CC</sub> ≤ 5.5 V       |   |  | -                               | 32.768               | -                    | kHz                  |     |
|                                   |  | XCIN external clock input frequency   |   |  | 1.8 V ≤ V <sub>CC</sub> ≤ 5.5 V | -                    | -                    | 50                   | kHz |
| f <sub>(OCO20M)</sub>             | When used as the count source for timer RC (3) | 2.7 V ≤ V <sub>CC</sub> ≤ 5.5 V       |   |  | 18.432                          | -                    | 20                   | MHz                  |     |
| f <sub>(OCO-F)</sub>              | f <sub>(OCO-F)</sub> frequency                 | 2.7 V ≤ V <sub>CC</sub> ≤ 5.5 V       |   |  | -                               | -                    | 20                   | MHz                  |     |
|                                   |  | 1.8 V ≤ V <sub>CC</sub> < 2.7 V       |   |  | -                               | -                    | 8                    | MHz                  |     |
| -                                 | System clock frequency                         | 2.7 V ≤ V <sub>CC</sub> ≤ 5.5 V       |   |  | -                               | -                    | 20                   | MHz                  |     |
|                                   |  | 1.8 V ≤ V <sub>CC</sub> < 2.7 V       |   |  | -                               | -                    | 8                    | MHz                  |     |
| f <sub>(BCLK)</sub>               | CPU clock frequency                            | 2.7 V ≤ V <sub>CC</sub> ≤ 5.5 V       |   |  | 0                               | -                    | 20                   | MHz                  |     |
|                                   |  | 1.8 V ≤ V <sub>CC</sub> < 2.7 V       |   |  | 0                               | -                    | 8                    | MHz                  |     |

## Notes:

- The average output current indicates the average value of current measured during 100 ms.
- This applies when the drive capacity of the output transistor is set to High by P8DRR register. When the drive capacity is set to Low, the value of any other pin applies.
- f<sub>(OCO20M)</sub> can be used as the count source for timer RC in the range of V<sub>CC</sub> = 2.7 V to 5.5V.



**Figure 5.1** Ports P0, P2, P3, P5\_0 to P5\_6, P7\_0 to P7\_2, P8, and P9\_0 to P9\_1 Timing Measurement Circuit

### 5.1.3 Peripheral Function Characteristics

**Table 5.3 A/D Converter Characteristics**  
( $V_{CC}/AV_{CC} = V_{ref} = 1.8$  to  $5.5$  V,  $V_{SS} = 0$  V, and  $T_{opr} = -20$  to  $85$  °C (N version)/  
 $-40$  to  $85$  °C (D version), unless otherwise specified.)

| Symbol      | Parameter                           |             | Conditions   | Standard |      |           | Unit       |
|-------------|-------------------------------------|-------------|--|----------|------|-----------|------------|
|             |                                     |             |  | Min.     | Typ. | Max.      |            |
| –           | Resolution                          |             | $V_{ref} = AV_{CC}$                                    | –        | –    | 10        | Bit        |
| –           | Absolute accuracy <sup>(2)</sup>    | 10-bit mode | $V_{ref} = AV_{CC} = 5.0$ V AN0 to AN6 input           | –        | –    | $\pm 3$   | LSB        |
|             |                                     |             | $V_{ref} = AV_{CC} = 2.2$ V AN0 to AN6 input           | –        | –    | $\pm 5$   | LSB        |
|             |                                     |             | $V_{ref} = AV_{CC} = 1.8$ V AN0 to AN6 input           | –        | –    | $\pm 5$   | LSB        |
|             |                                     | 8-bit mode  | $V_{ref} = AV_{CC} = 5.0$ V AN0 to AN6 input           | –        | –    | $\pm 2$   | LSB        |
|             |                                     |             | $V_{ref} = AV_{CC} = 2.2$ V AN0 to AN6 input           | –        | –    | $\pm 2$   | LSB        |
|             |                                     |             | $V_{ref} = AV_{CC} = 1.8$ V AN0 to AN6 input           | –        | –    | $\pm 2$   | LSB        |
| $\phi_{AD}$ | A/D conversion clock                |             | $4.0 \leq V_{ref} = AV_{CC} \leq 5.5$ V <sup>(1)</sup> | 1        | –    | 20        | MHz        |
|             |                                     |             | $3.2 \leq V_{ref} = AV_{CC} \leq 5.5$ V <sup>(1)</sup> | 1        | –    | 16        | MHz        |
|             |                                     |             | $2.7 \leq V_{ref} = AV_{CC} \leq 5.5$ V <sup>(1)</sup> | 1        | –    | 10        | MHz        |
|             |                                     |             | $1.8 \leq V_{ref} = AV_{CC} \leq 5.5$ V <sup>(1)</sup> | 1        | –    | 8         | MHz        |
| –           | Tolerance level impedance           |             |  | –        | 3    | –         | k $\Omega$ |
| $t_{CONV}$  | Conversion time                     | 10-bit mode | $V_{ref} = AV_{CC} = 5.0$ V, $\phi_{AD} = 20$ MHz      | 2.2      | –    | –         | $\mu$ s    |
|             |                                     | 8-bit mode  | $V_{ref} = AV_{CC} = 5.0$ V, $\phi_{AD} = 20$ MHz      | 2.2      | –    | –         | ms         |
| $t_{SAMP}$  | Sampling time                       |             | $\phi_{AD} = 20$ MHz                                   | 0.8      | –    | –         | $\mu$ s    |
| $I_{Vref}$  | V <sub>ref</sub> current            |             | $V_{CC} = 5$ V, $XIN = f1 = \phi_{AD} = 20$ MHz        | –        | 45   | –         | $\mu$ A    |
| $V_{ref}$   | Reference voltage                   |             |  | 1.8      | –    | $AV_{CC}$ | V          |
| $V_{IA}$    | Analog input voltage <sup>(3)</sup> |             |  | 0        | –    | $V_{ref}$ | V          |
| OCVREF      | On-chip reference voltage           |             | $2$ MHz $\leq \phi_{AD} \leq 4$ MHz                    | 1.53     | 1.70 | 1.87      | V          |

Notes:

1. The A/D conversion result will be undefined in wait mode, stop mode, power-off mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
2. This applies when the peripheral functions are stopped.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

**Table 5.4 Temperature Sensor Characteristics**  
( $V_{SS} = 0$  V and  $T_{opr} = -20$  to  $85$  °C (N version)/  $-40$  to  $85$  °C (D version), unless  
otherwise specified.)

| Symbol    | Parameter                         | Conditions   | Standard |        |      | Unit    |
|-----------|-----------------------------------|--|----------|--------|------|---------|
|           |                                   |  | Min.     | Typ.   | Max. |         |
| $V_{TMP}$ | Temperature sensor output voltage | $1.8$ V $\leq V_{ref} = AV_{CC} \leq 5.5$ V<br>$\phi_{AD} = 1.0$ MHz to $5.0$ MHz<br>Ambient temperature = $25$ °C | 550      | 600    | 650  | mV      |
| –         | Temperature coefficient           | $1.8$ V $\leq V_{ref} = AV_{CC} \leq 5.5$ V<br>$\phi_{AD} = 1.0$ MHz to $5.0$ MHz<br>Ambient temperature = $25$ °C | –        | $-2.1$ | –    | mV/°C   |
| –         | Start-up time                     | $1.8$ V $\leq V_{ref} = AV_{CC} \leq 5.5$ V<br>$\phi_{AD} = 1.0$ MHz to $5.0$ MHz                                  | –        | –      | 200  | $\mu$ s |
| $I_{TMP}$ | Operating current                 | $1.8$ V $\leq V_{ref} = AV_{CC} \leq 5.5$ V<br>$\phi_{AD} = 1.0$ MHz to $5.0$ MHz                                  | –        | 100    | –    | $\mu$ A |

**Table 5.5 Gain Amplifier Characteristics**  
**(V<sub>SS</sub> = 0 V and T<sub>opr</sub> = -20 to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.)**

| Symbol            | Parameter                      | Conditions | Standard |      |                        | Unit |
|-------------------|--------------------------------|------------|----------|------|------------------------|------|
|                   |                                |            | Min.     | Typ. | Max.                   |      |
| V <sub>GAIN</sub> | Gain amplifier operating range |            | 0.4      | —    | AV <sub>CC</sub> - 1.0 | V    |
| φ <sub>AD</sub>   | A/D conversion clock           |            | 1        | —    | 5                      | MHz  |

**Table 5.6 Comparator B Characteristics**  
**(V<sub>CC</sub> = 1.8 to 5.5 V and T<sub>opr</sub> = -20 to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.)**

| Symbol           | Parameter                                   | Condition                                  | Standard |      |                       | Unit |
|------------------|---|--|----------|------|-----------------------|------|
|                  |   |  | Min.     | Typ. | Max.                  |      |
| V <sub>ref</sub> | IVREF1, IVREF3 input reference voltage      |  | 0        | —    | V <sub>CC</sub> - 1.4 | V    |
| V <sub>I</sub>   | IVCMP1, IVCMP3 input voltage                |  | -0.3     | —    | V <sub>CC</sub> + 0.3 | V    |
| —                | Offset                                      |  | —        | 5    | 100                   | mV   |
| t <sub>d</sub>   | Comparator output delay time <sup>(1)</sup> | V <sub>I</sub> = V <sub>ref</sub> ± 100 mV | —        | —    | 1                     | μs   |
| I <sub>CMP</sub> | Comparator operating current                | V <sub>CC</sub> = 5.0 V                    | —        | 12   | —                     | μA   |

Note:

1. When the digital filter is disabled.



**Table 5.7 Flash Memory (Program ROM) Characteristics**  
**(V<sub>CC</sub> = 1.8 to 5.5 V and T<sub>opr</sub> = 0 to 60 °C, unless otherwise specified.)**

| Symbol                        | Parameter  | Conditions                  | Standard   |      |                                | Unit  |
|-------------------------------|--|-----------------------------|------------|------|--------------------------------|-------|
|                               |  |                             | Min.       | Typ. | Max.                           |       |
| –                             | Program/erase endurance (1)  |                             | 10,000 (2) | –    | –                              | times |
| –                             | Byte program time  |                             | –          | 80   | –                              | μs    |
| –                             | Block erase time   |                             | –          | 0.12 | –                              | s     |
| t <sub>d</sub> (SR-SUS)       | Time delay from suspend request until suspend                          |                             | –          | –    | 0.25 + CPU clock<br>× 3 cycles | ms    |
| –                             | Time from suspend until erase restart                                  |                             | –          | –    | 30 + CPU clock<br>× 1 cycle    | μs    |
| t <sub>d</sub> (CMDRST-READY) | Time from when command is forcibly terminated until reading is enabled |                             | –          | –    | 30 + CPU clock<br>× 1 cycle    | μs    |
| –                             | Program, erase voltage   |                             | 1.8        | –    | 5.5                            | V     |
| –                             | Read voltage   |                             | 1.8        | –    | 5.5                            | V     |
| –                             | Program, erase temperature   |                             | 0          | –    | 60                             | °C    |
| –                             | Data hold time (6)   | Ambient temperature = 85 °C | 10         | –    | –                              | year  |

## Notes:

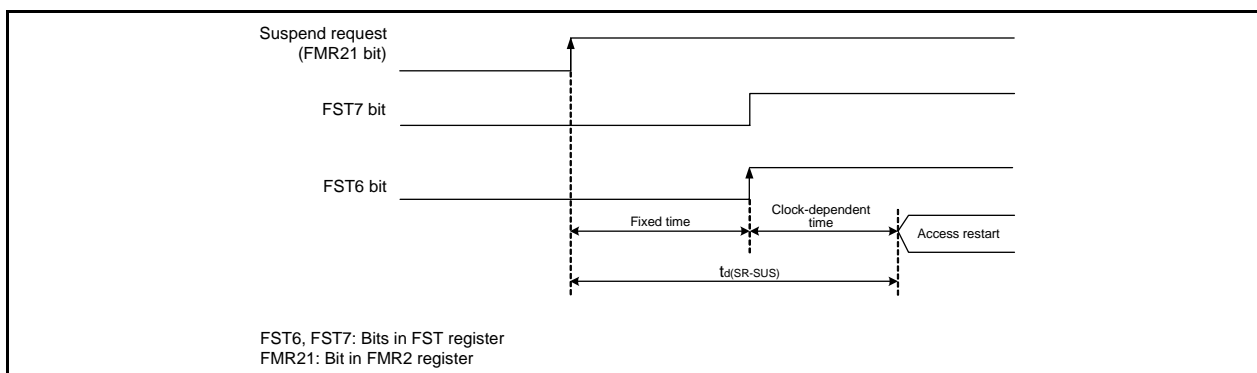
- Definition of programming/erasure endurance  
 The programming and erasure endurance is defined on a per-block basis.  
 If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.  
 However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- The data hold time includes time that the power supply is off or the clock is not supplied.

**Table 5.8 Flash Memory (Data flash Block A and Block B) Characteristics**  
**(VCC = 1.8 to 5.5 V and Topr = -20 to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.)**

| Symbol                        | Parameter  | Conditions                  | Standard   |      |                                | Unit      |
|-------------------------------|--|-----------------------------|------------|------|--------------------------------|-----------|
|                               |  |                             | Min.       | Typ. | Max.                           |           |
| —                             | Program/erase endurance (1)  |                             | 10,000 (2) | —    | —                              | time<br>s |
| —                             | Byte program time<br>(program/erase endurance ≤ 10,000 times)          |                             | —          | 150  | —                              | μs        |
| —                             | Block erase time<br>(program/erase endurance ≤ 10,000 times)           |                             | —          | 0.05 | 1                              | s         |
| t <sub>d</sub> (SR-SUS)       | Time delay from suspend request until suspend                          |                             | —          | —    | 0.25 + CPU clock<br>× 3 cycles | ms        |
| —                             | Time from suspend until erase restart                                  |                             | —          | —    | 30 + CPU clock<br>× 1 cycle    | μs        |
| t <sub>d</sub> (CMDRST-READY) | Time from when command is forcibly terminated until reading is enabled |                             | —          | —    | 30 + CPU clock<br>× 1 cycle    | μs        |
| —                             | Program, erase voltage   |                             | 1.8        | —    | 5.5                            | V         |
| —                             | Read voltage   |                             | 1.8        | —    | 5.5                            | V         |
| —                             | Program, erase temperature   |                             | -20 (6)    | —    | 85                             | °C        |
| —                             | Data hold time (7)   | Ambient temperature = 85 °C | 10         | —    | —                              | year      |

## Notes:

- Definition of programming/erasure endurance  
 The programming and erasure endurance is defined on a per-block basis.  
 If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.  
 However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 40 °C for D version.
- The data hold time includes time that the power supply is off or the clock is not supplied.



**Figure 5.2 Time delay until Suspend**

**Table 5.9 Voltage Detection 0 Circuit Characteristics**  
**(V<sub>CC</sub> = 1.8 to 5.5 V and T<sub>opr</sub> = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)**

| Symbol              | Parameter   | Condition                          | Standard  |      |      | Unit |     |    |
|---------------------|---|------------------------------------|---|------|------|------|-----|----|
|                     |   |                                    | Min.  | Typ. | Max. |      |     |    |
| V <sub>det0</sub>   | Voltage detection level V <sub>det0_0</sub> (1)                   |                                    | 1.8   | 1.90 | 2.05 | V    |     |    |
|                     | Voltage detection level V <sub>det0_1</sub> (1)                   |                                    | 2.15  | 2.35 | 2.50 | V    |     |    |
|                     | Voltage detection level V <sub>det0_2</sub> (1)                   |                                    | 2.70  | 2.85 | 3.05 | V    |     |    |
|                     | Voltage detection level V <sub>det0_3</sub> (1)                   |                                    | 3.55  | 3.80 | 4.05 | V    |     |    |
| –                   | Voltage detection 0 circuit response time (3)                     | In operation                       | At the falling of V <sub>CC</sub> from 5 V to (V <sub>det0_0</sub> – 0.1) V |      | –    | 50   | 500 | μs |
|                     |   | In stop mode                       | At the falling of V <sub>CC</sub> from 5 V to (V <sub>det0_0</sub> – 0.1) V |      | –    | 100  | 500 | μs |
| –                   | Voltage detection circuit self power consumption                  | VCA25 = 1, V <sub>CC</sub> = 5.0 V |   |      | –    | 1.5  | –   | μA |
| t <sub>d(E-A)</sub> | Waiting time until voltage detection circuit operation starts (2) |                                    | –   | –    | 100  | –    | μs  |    |

Notes:

1. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
3. Time until the voltage monitor 0 reset is generated after the voltage passes V<sub>det0</sub>.

**Table 5.10 Voltage Detection 1 Circuit Characteristics**  
**(V<sub>CC</sub> = 1.8 to 5.5 V and T<sub>opr</sub> = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)**

| Symbol              | Parameter  | Condition   | Standard  |      |      | Unit |     |    |
|---------------------|--|---|---|------|------|------|-----|----|
|                     |  |   | Min.  | Typ. | Max. |      |     |    |
| V <sub>det1</sub>   | Voltage detection level V <sub>det1_0</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 2.00  | 2.20 | 2.40 | V    |     |    |
|                     | Voltage detection level V <sub>det1_1</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 2.15  | 2.35 | 2.55 | V    |     |    |
|                     | Voltage detection level V <sub>det1_2</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 2.30  | 2.50 | 2.70 | V    |     |    |
|                     | Voltage detection level V <sub>det1_3</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 2.45  | 2.65 | 2.85 | V    |     |    |
|                     | Voltage detection level V <sub>det1_4</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 2.60  | 2.80 | 3.00 | V    |     |    |
|                     | Voltage detection level V <sub>det1_5</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 2.75  | 2.95 | 3.15 | V    |     |    |
|                     | Voltage detection level V <sub>det1_6</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 2.85  | 3.10 | 3.40 | V    |     |    |
|                     | Voltage detection level V <sub>det1_7</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 3.00  | 3.25 | 3.55 | V    |     |    |
|                     | Voltage detection level V <sub>det1_8</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 3.15  | 3.40 | 3.70 | V    |     |    |
|                     | Voltage detection level V <sub>det1_9</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 3.30  | 3.55 | 3.85 | V    |     |    |
|                     | Voltage detection level V <sub>det1_A</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 3.45  | 3.70 | 4.00 | V    |     |    |
|                     | Voltage detection level V <sub>det1_B</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 3.60  | 3.85 | 4.15 | V    |     |    |
|                     | Voltage detection level V <sub>det1_C</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 3.75  | 4.00 | 4.30 | V    |     |    |
|                     | Voltage detection level V <sub>det1_D</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 3.90  | 4.15 | 4.45 | V    |     |    |
|                     | Voltage detection level V <sub>det1_E</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 4.05  | 4.30 | 4.60 | V    |     |    |
|                     | Voltage detection level V <sub>det1_F</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 4.20  | 4.45 | 4.75 | V    |     |    |
| –                   | Hysteresis width at the rising of V <sub>CC</sub> in voltage detection 1 circuit | V <sub>det1_0</sub> to V <sub>det1_5</sub> selected | –   | 0.07 | –    | V    |     |    |
|                     |  | V <sub>det1_6</sub> to V <sub>det1_F</sub> selected | –   | 0.10 | –    | V    |     |    |
| –                   | Voltage detection 1 circuit response time (2)                                    | In operation  | At the falling of V <sub>CC</sub> from 5 V to (V <sub>det1_0</sub> – 0.1) V |      | –    | 60   | 150 | μs |
|                     |  | In stop mode  | At the falling of V <sub>CC</sub> from 5 V to (V <sub>det1_0</sub> – 0.1) V |      | –    | 250  | 500 | μs |
| –                   | Voltage detection circuit self power consumption                                 | VCA26 = 1, V <sub>CC</sub> = 5.0 V                  |   |      | –    | 1.7  | –   | μA |
| t <sub>d(E-A)</sub> | Waiting time until voltage detection circuit operation starts (3)                |   | –   | –    | 100  | –    | μs  |    |

Notes:

1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V<sub>det1</sub>.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

**Table 5.11 Voltage Detection 2 Circuit Characteristics**  
**(V<sub>CC</sub> = 1.8 to 5.5 V and T<sub>opr</sub> = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)**

| Symbol              | Parameter  | Condition                          | Standard |      |      | Unit |
|---------------------|--|------------------------------------|----------|------|------|------|
|                     |  |                                    | Min.     | Typ. | Max. |      |
| V <sub>det2</sub>   | Voltage detection level V <sub>det2_0</sub> <sup>(1)</sup>                       | At the falling of V <sub>CC</sub>  | 3.70     | 4.0  | 4.30 | V    |
| –                   | Hysteresis width at the rising of V <sub>CC</sub> in voltage detection 2 circuit |                                    | –        | 0.10 | –    | V    |
| –                   | Voltage detection 2 circuit response time <sup>(2)</sup>                         | In operation                       |          | 20   | 150  | μs   |
|                     |  | In stop mode                       |          | –    | 200  | 500  |
| –                   | Voltage detection circuit self power consumption                                 | VCA27 = 1, V <sub>CC</sub> = 5.0 V | –        | 1.7  | –    | μA   |
| t <sub>d(E-A)</sub> | Waiting time until voltage detection circuit operation starts <sup>(3)</sup>     |                                    | –        | –    | 100  | μs   |

Notes:

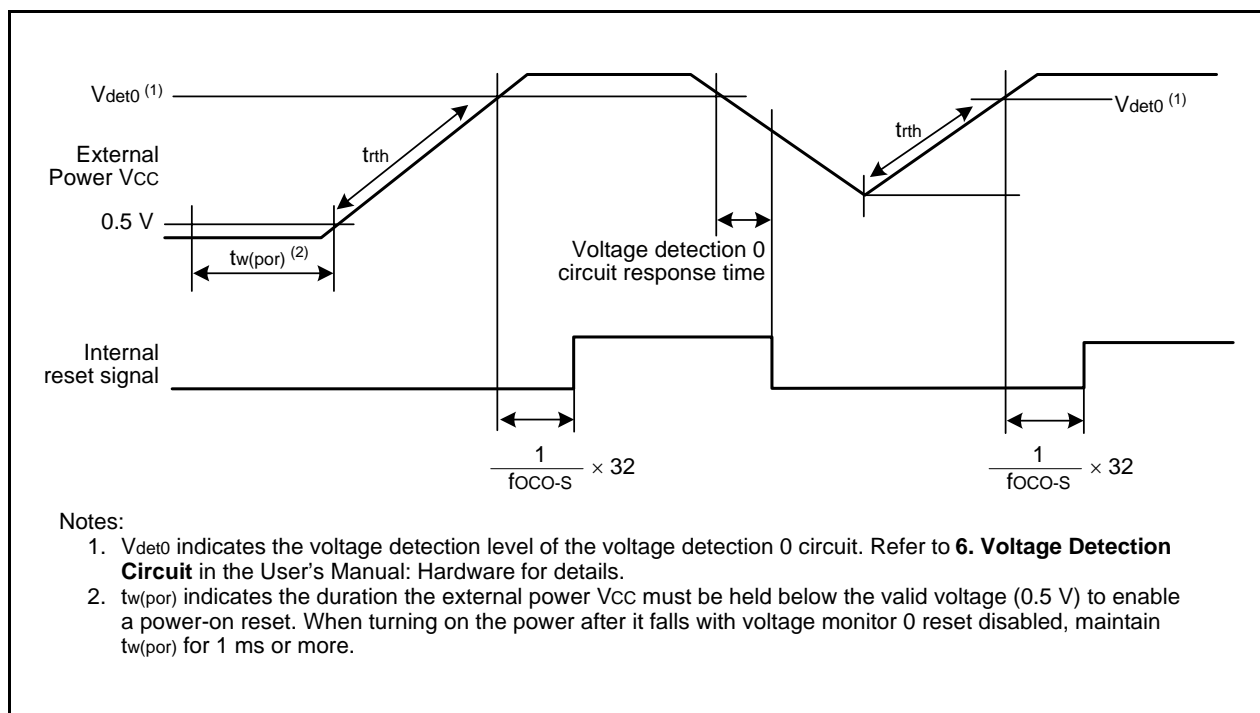
1. The voltage detection level varies with detection targets. Select the level with the VCA24 bit in the VCA2 register.
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V<sub>det2</sub>.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

**Table 5.12 Power-on Reset Circuit Characteristics<sup>(1)</sup>**  
**(T<sub>opr</sub> = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)**

| Symbol           | Parameter                                    | Condition | Standard |      |       | Unit  |
|------------------|--|-----------|----------|------|-------|-------|
|                  |  |           | Min.     | Typ. | Max.  |       |
| t <sub>rth</sub> | External power V <sub>CC</sub> rise gradient |           | 0        | –    | 50000 | mV/ms |

Note:

1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



**Figure 5.3 Power-on Reset Circuit Characteristics**

**Table 5.13 High-speed On-Chip Oscillator Circuit Characteristics**  
( $V_{CC} = 1.8$  to  $5.5$  V and  $T_{opr} = -20$  to  $85$  °C (N version)/  $-40$  to  $85$  °C (D version), unless otherwise specified.)

| Symbol | Parameter  | Condition   | Standard |        |        | Unit    |
|--------|--|---|----------|--------|--------|---------|
|        |  |   | Min.     | Typ.   | Max.   |         |
| –      | High-speed on-chip oscillator frequency after reset  | $V_{CC} = 1.8$ V to $5.5$ V<br>$-20$ °C $\leq T_{opr} \leq 85$ °C | 19.2     | 20     | 20.8   | MHz     |
|        |  | $V_{CC} = 1.8$ V to $5.5$ V<br>$-40$ °C $\leq T_{opr} \leq 85$ °C | 19.0     | 20     | 21.0   | MHz     |
| –      | High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register <sup>(1)</sup> | $V_{CC} = 1.8$ V to $5.5$ V<br>$-20$ °C $\leq T_{opr} \leq 85$ °C | 17.694   | 18.432 | 19.169 | MHz     |
|        |  | $V_{CC} = 1.8$ V to $5.5$ V<br>$-40$ °C $\leq T_{opr} \leq 85$ °C | 17.510   | 18.432 | 19.353 | MHz     |
| –      | Oscillation stability time   |   | –        | 5      | 30     | $\mu$ s |
| –      | Self power consumption at oscillation  | $V_{CC} = 5.0$ V, $T_{opr} = 25$ °C                               | –        | 530    | –      | $\mu$ A |

Note:

1. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

**Table 5.14 Low-speed On-Chip Oscillator Circuit Characteristics**  
( $V_{CC} = 1.8$  to  $5.5$  V and  $T_{opr} = -20$  to  $85$  °C (N version)/  $-40$  to  $85$  °C (D version), unless otherwise specified.)

| Symbol   | Parameter   | Condition                           | Standard |      |      | Unit    |
|----------|---|-------------------------------------|----------|------|------|---------|
|          |   |                                     | Min.     | Typ. | Max. |         |
| fOCO-S   | Low-speed on-chip oscillator frequency                        |                                     | 60       | 125  | 250  | kHz     |
| –        | Oscillation stability time                                    |                                     | –        | –    | 35   | $\mu$ s |
| –        | Self power consumption at oscillation                         | $V_{CC} = 5.0$ V, $T_{opr} = 25$ °C | –        | 2    | –    | $\mu$ A |
| fOCO-WDT | Low-speed on-chip oscillator frequency for the watchdog timer |                                     | 60       | 125  | 250  | kHz     |
| –        | Oscillation stability time                                    |                                     | –        | –    | 35   | $\mu$ s |
| –        | Self power consumption at oscillation                         | $V_{CC} = 5.0$ V, $T_{opr} = 25$ °C | –        | 2    | –    | $\mu$ A |

**Table 5.15 Power Supply Circuit Characteristics**  
( $V_{CC} = 1.8$  to  $5.5$  V,  $V_{SS} = 0$  V, and  $T_{opr} = 25$  °C, unless otherwise specified.)

| Symbol               | Parameter   | Condition | Standard |      |      | Unit    |
|----------------------|---|-----------|----------|------|------|---------|
|                      |   |           | Min.     | Typ. | Max. |         |
| t <sub>d</sub> (P-R) | Time for internal power supply stabilization during power-on <sup>(1)</sup> |           | –        | –    | 2000 | $\mu$ s |

Note:

1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

**Table 5.16 LCD Drive Control Circuit Characteristics**  
**(V<sub>CC</sub> = 1.8 to 5.5 V, V<sub>SS</sub> = 0 V, and T<sub>opr</sub> = -20 to 85 °C (N version)/**  
**-40 to 85 °C (D version), unless otherwise specified.)**

| Symbol | Parameter                         | Condition  | Standard |      |         | Unit |
|--------|-----------------------------------|------------|----------|------|---------|------|
|        |                                   |            | Min.     | Typ. | Max.    |      |
| VLCD   | LCD power supply voltage          | VLCD = VL3 | 2.2      | –    | 5.5     | V    |
| VL2    | VL2 voltage                       |            | VL1      | –    | VL3     | V    |
| VL1    | VL1 voltage                       |            | 1        | –    | VL2 (2) | V    |
| f(FR)  | Frame frequency                   |            | 50       | –    | 180     | Hz   |
| ILCD   | LCD drive control circuit current |            | –        | (1)  | –       | μA   |

Notes:

1. Refer to Table 5.19 DC Characteristics (2), Table 5.21 DC Characteristics (4), and Table 5.23 DC Characteristics (6).
2. The VL1 voltage should be VCC or below.

**Table 5.17 Power-Off Mode Characteristics**  
**(V<sub>CC</sub> = 1.8 to 5.5 V, V<sub>SS</sub> = 0 V, and T<sub>opr</sub> = -20 to 85 °C (N version)/**  
**-40 to 85 °C (D version), unless otherwise specified.)**

| Symbol | Parameter                               | Condition | Standard |      |      | Unit |
|--------|---|-----------|----------|------|------|------|
|        |   |           | Min.     | Typ. | Max. |      |
| –      | Power-off mode operating supply voltage |           | 1.8      | –    | 5.5  | V    |

### 5.1.4 DC Characteristics

**Table 5.18 DC Characteristics (1) [4.0 V ≤ V<sub>CC</sub> ≤ 5.5 V]**  
(T<sub>opr</sub> = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

| Symbol                           | Parameter           |   | Condition                                   |                      |                          | Standard              |      |                 | Unit |
|----------------------------------|---------------------|---|---|----------------------|--------------------------|-----------------------|------|-----------------|------|
|                                  |                     |   |   |                      |                          | Min.                  | Typ. | Max.            |      |
| V <sub>OH</sub>                  | Output "H" voltage  |   | Port P8 (1)                                 | V <sub>CC</sub> = 5V | I <sub>OH</sub> = –20 mA | V <sub>CC</sub> – 2.0 | –    | V <sub>CC</sub> | V    |
|                                  |                     |   | Other pins                                  | V <sub>CC</sub> = 5V | I <sub>OH</sub> = –5 mA  | V <sub>CC</sub> – 2.0 | –    | V <sub>CC</sub> | V    |
| V <sub>OL</sub>                  | Output "L" voltage  |   | Port P8 (1)                                 | V <sub>CC</sub> = 5V | I <sub>OL</sub> = 20 mA  | –                     | –    | 2.0             | V    |
|                                  |                     |   | Other pins                                  | V <sub>CC</sub> = 5V | I <sub>OL</sub> = 5 mA   | –                     | –    | 2.0             | V    |
| V <sub>T+</sub> –V <sub>T–</sub> | Hysteresis          | $\overline{\text{INT0}}$ , $\overline{\text{INT1}}$ , $\overline{\text{INT2}}$ ,<br>$\overline{\text{INT3}}$ , $\overline{\text{INT5}}$ , $\overline{\text{INT7}}$ ,<br>$\overline{\text{KI0}}$ , $\overline{\text{KI1}}$ , $\overline{\text{KI2}}$ , $\overline{\text{KI3}}$ ,<br>$\overline{\text{KI4}}$ , $\overline{\text{KI5}}$ , $\overline{\text{KI6}}$ , $\overline{\text{KI7}}$ ,<br>TRCIOA, TRCIOB,<br>TRCIOC, TRCIOD,<br>TRJ0IO, TRJ1IO,<br>TRCTRG, TRCCLK,<br>ADTRG,<br>RXD0, CLK0, SSI,<br>SCL, SDA, SSO |   |                      |                          | 0.05                  | 0.5  | –               | V    |
|                                  |                     | $\overline{\text{RESET}}$ , $\overline{\text{WKUP0}}$   |   |                      |                          | 0.1                   | 0.8  | –               | V    |
| I <sub>IH</sub>                  | Input "H" current   |   | V <sub>I</sub> = 5 V, V <sub>CC</sub> = 5 V |                      |                          | –                     | –    | 5.0             | μA   |
| I <sub>IL</sub>                  | Input "L" current   |   | V <sub>I</sub> = 0 V, V <sub>CC</sub> = 5 V |                      |                          | –                     | –    | –5.0            | μA   |
| R <sub>PULLUP</sub>              | Pull-up resistance  |   | V <sub>I</sub> = 0 V, V <sub>CC</sub> = 5 V |                      |                          | 20                    | 40   | 80              | kΩ   |
| R <sub>I<sub>XIN</sub></sub>     | Feedback resistance | XIN   |   |                      |                          | –                     | 2.0  | –               | MΩ   |
| R <sub>I<sub>XCIN</sub></sub>    | Feedback resistance | XCIN  |   |                      |                          | –                     | 14   | –               | MΩ   |
| V <sub>RAM</sub>                 | RAM hold voltage    |   | During stop mode                            |                      |                          | 1.8                   | –    | –               | V    |

Note:

1. This applies when the drive capacity of the output transistor is set to High by P8DRR register. When the drive capacity is set to Low, the value of any other pin applies.

**Table 5.19 DC Characteristics (2) [4.0 V ≤ V<sub>CC</sub> ≤ 5.5 V]**  
**(T<sub>opr</sub> = −20 to 85 °C (N version)/ −40 to 85 °C (D version), unless otherwise specified.)**

| Symbol          | Parameter                           |                                    | Condition           |        |                    |           |              |  |  | Standard  |                     |      | Unit |    |
|-----------------|-------------------------------------|------------------------------------|---------------------|--------|--------------------|-----------|--------------|--|--|---|---------------------|------|------|----|
|                 |                                     |                                    | Oscillation Circuit |        | On-Chip Oscillator |           | CPU Clock    | Low-Power-Consumption Setting  | Other  | Min.  | Typ. <sup>(3)</sup> | Max. |      |    |
|                 |                                     |                                    | XIN <sup>(2)</sup>  | XCIN   | High-Speed         | Low-Speed |              |  |  |   |                     |      |      |    |
| I <sub>CC</sub> | Power supply current <sup>(1)</sup> | High-speed clock mode              | 20 MHz              | Off    | Off                | 125 kHz   | No division  | –  |  | –   | 4.7                 | 10   | mA   |    |
|                 |                                     |                                    | 16 MHz              | Off    | Off                | 125 kHz   | No division  | –  |  | –   | 3.9                 | 8    | mA   |    |
|                 |                                     |                                    | 10 MHz              | Off    | Off                | 125 kHz   | No division  | –  |  | –   | 2.3                 | –    | mA   |    |
|                 |                                     |                                    | 20 MHz              | Off    | Off                | Off       | No division  | FMR27 = 1<br>MSTCR0 = BEh<br>MSTCR1 = 3Fh                                | Flash memory off<br>Program operation on RAM<br>Module standby setting enabled                             | –   | 3.1                 | –    | mA   |    |
|                 |                                     |                                    | 20 MHz              | Off    | Off                | 125 kHz   | Divide-by-8  | –  |  | –   | 1.8                 | –    | mA   |    |
|                 |                                     |                                    | 16 MHz              | Off    | Off                | 125 kHz   | Divide-by-8  | –  |  | –   | 1.5                 | –    | mA   |    |
|                 |                                     | High-speed on-chip oscillator mode | 10 MHz              | Off    | Off                | 125 kHz   | Divide-by-8  | –  |  | –   | 1.0                 | –    | mA   |    |
|                 |                                     |                                    | Off                 | Off    | 20 MHz             | 125 kHz   | No division  | –  |  | –   | 5.0                 | 11   | mA   |    |
|                 |                                     |                                    | Off                 | Off    | 20 MHz             | 125 kHz   | Divide-by-8  | –  |  | –   | 2.1                 | –    | mA   |    |
|                 |                                     | Low-speed on-chip oscillator mode  | Off                 | Off    | 4 MHz              | 125 kHz   | Divide-by-16 | MSTCR0 = BEh<br>MSTCR1 = 3Fh   |  | –   | 0.9                 | –    | mA   |    |
|                 |                                     |                                    | Off                 | Off    | Off                | 125 kHz   | No division  | FMR27 = 1<br>VCA20 = 0   |  | –   | 110                 | 320  | μA   |    |
|                 |                                     | Low-speed clock mode               | Off                 | Off    | Off                | 125 kHz   | Divide-by-8  | FMR27 = 1<br>VCA20 = 0   |  | –   | 63                  | 220  | μA   |    |
|                 |                                     |                                    | Off                 | 32 kHz | Off                | Off       | No division  | FMR27 = 1<br>VCA20 = 0   |  | –   | 60                  | 220  | μA   |    |
|                 |                                     | Wait mode                          | Off                 | 32 kHz | Off                | Off       | No division  | FMSTP = 1<br>VCA20 = 0   | Flash memory off<br>Program operation on RAM   | –   | 46                  | –    | μA   |    |
|                 |                                     |                                    | Off                 | Off    | Off                | 125 kHz   | –            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1                         | While a WAIT instruction is executed<br>Peripheral clock operation   | –   | 9.0                 | 50   | μA   |    |
|                 |                                     | Stop mode                          | Off                 | Off    | Off                | 125 kHz   | –            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | While a WAIT instruction is executed<br>Peripheral clock off   | –   | 2.8                 | 33   | μA   |    |
|                 |                                     |                                    | Off                 | 32 kHz | Off                | Off       | –            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 0 | While a WAIT instruction is executed<br>Peripheral clock off<br>Timer RH operation in real-time clock mode | LCD drive control circuit <sup>(4)</sup><br>When external division resistors are used | –                   | 4.6  | –    | μA |
|                 |                                     |                                    | Off                 | 32 kHz | Off                | Off       | –            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | While a WAIT instruction is executed<br>Peripheral clock off<br>Timer RH operation in real-time clock mode | –   | 2.4                 | –    | μA   |    |
|                 |                                     |                                    | Off                 | Off    | Off                | Off       | –            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM10 = 1             | Topr = 25 °C<br>Peripheral clock off   | –   | 0.5                 | 2.2  | μA   |    |
|                 |                                     | Power-off mode                     | Off                 | Off    | Off                | Off       | –            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM10 = 1             | Topr = 85 °C<br>Peripheral clock off   | –   | 1.2                 | –    | μA   |    |
|                 |                                     |                                    | Off                 | Off    | Off                | Off       | –            | –  | Power-off 0<br>Topr = 25 °C  | –   | 0.01                | 0.1  | μA   |    |
|                 |                                     |                                    | Off                 | Off    | Off                | Off       | –            | –  | Power-off 0<br>Topr = 85 °C  | –   | 0.03                | –    | μA   |    |
|                 |                                     |                                    | Off                 | 32 kHz | Off                | Off       | –            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1                          | Power-off 2<br>Topr = 25 °C  | –   | 1.8                 | 6.4  | μA   |    |
|                 |                                     |                                    | Off                 | 32 kHz | Off                | Off       | –            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM10 = 1             | Power-off 2<br>Topr = 85 °C  | –   | 2.7                 | –    | μA   |    |

## Notes:

- V<sub>CC</sub> = 4.0 V to 5.5 V, single chip mode, output pins are open, and other pins are V<sub>SS</sub>.
- XIN is set to square wave input.
- V<sub>CC</sub> = 5.0 V
- VLCD = V<sub>CC</sub>, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG26 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.



**Table 5.20 DC Characteristics (3) [2.7 V ≤ V<sub>CC</sub> < 4.0 V]**  
**(T<sub>opr</sub> = -20 to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.)**

| Symbol                           | Parameter           |   | Condition                                   |                         | Standard              |      |                 | Unit |
|----------------------------------|---------------------|---|---|-------------------------|-----------------------|------|-----------------|------|
|                                  |                     |   |   |                         | Min.                  | Typ. | Max.            |      |
| V <sub>OH</sub>                  | Output "H" voltage  |   | Port P8 (1)                                 | I <sub>OH</sub> = -5 mA | V <sub>CC</sub> - 0.5 | -    | V <sub>CC</sub> | V    |
|                                  |                     |   | Other pins                                  | I <sub>OH</sub> = -1 mA | V <sub>CC</sub> - 0.5 | -    | V <sub>CC</sub> | V    |
| V <sub>OL</sub>                  | Output "L" voltage  |   | Port P8 (1)                                 | I <sub>OL</sub> = 5 mA  | -                     | -    | 0.5             | V    |
|                                  |                     |   | Other pins                                  | I <sub>OL</sub> = 1 mA  | -                     | -    | 0.5             | V    |
| V <sub>T+</sub> -V <sub>T-</sub> | Hysteresis          | $\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT2}},$<br>$\overline{\text{INT3}}, \overline{\text{INT5}}, \overline{\text{INT7}},$<br>$\overline{\text{KI0}}, \overline{\text{KI1}}, \overline{\text{KI2}}, \overline{\text{KI3}},$<br>$\overline{\text{KI4}}, \overline{\text{KI5}}, \overline{\text{KI6}}, \overline{\text{KI7}},$<br>TRCIOA, TRCIOB,<br>TRCIOC, TRCIOD,<br>TRJ0IO, TRJ1IO,<br>TRCTRG, TRCCLK,<br>ADTRG,<br>RXD0, CLK0, SSI,<br>SCL, SDA, SSO |   |                         | 0.05                  | 0.4  | -               | V    |
|                                  |                     | $\overline{\text{RESET}}, \overline{\text{WKUP0}}$  |   |                         | 0.1                   | 0.8  | -               | V    |
| I <sub>IH</sub>                  | Input "H" current   |   | V <sub>I</sub> = 3 V, V <sub>CC</sub> = 3 V |                         | -                     | -    | 5.0             | μA   |
| I <sub>IL</sub>                  | Input "L" current   |   | V <sub>I</sub> = 0 V, V <sub>CC</sub> = 3 V |                         | -                     | -    | -5.0            | μA   |
| R <sub>PULLUP</sub>              | Pull-up resistance  |   | V <sub>I</sub> = 0 V, V <sub>CC</sub> = 3 V |                         | 25                    | 80   | 140             | kΩ   |
| R <sub>FXIN</sub>                | Feedback resistance | XIN   |   |                         | -                     | 2.0  | -               | MΩ   |
| R <sub>FXCIN</sub>               | Feedback resistance | XCIN  |   |                         | -                     | 14   | -               | MΩ   |
| V <sub>RAM</sub>                 | RAM hold voltage    |   | During stop mode                            |                         | 1.8                   | -    | -               | V    |

Note:

1. This applies when the drive capacity of the output transistor is set to High by P8DRR register. When the drive capacity is set to Low, the value of any other pin applies.

**Table 5.21 DC Characteristics (4) [2.7 V ≤ Vcc < 4.0 V]**  
**(Topr = −20 to 85 °C (N version)/ −40 to 85 °C (D version), unless otherwise specified.)**

| Symbol | Parameter                         |                                    | Condition           |      |                    |   |  |  |  | Standard |          |      | Unit |
|--------|-----------------------------------|------------------------------------|---------------------|------|--------------------|---|--|--|--|----------|----------|------|------|
|        |                                   |                                    | Oscillation Circuit |      | On-Chip Oscillator |   | CPU Clock  | Low-Power-Consumption Setting  | Other  | Min.     | Typ. (3) | Max. |      |
|        |                                   |                                    | XIN (2)             | XCIN | High-Speed         | Low-Speed                                       |  |  |  |          |          |      |      |
| Icc    | Power supply current (1)          | High-speed clock mode              | 20 MHz              | Off  | Off                | 125 kHz   | No division  | –  | –  | 4.7      | 10       | mA   |      |
|        |                                   |                                    | 10 MHz              | Off  | Off                | 125 kHz   | No division  | –  | –  | 2.3      | 6        | mA   |      |
|        |                                   |                                    | 20 MHz              | Off  | Off                | Off   | No division  | FMR27 = 1<br>MSTCR0 = BEh<br>MSTCR1 = 3Fh  | Flash memory off<br>Program operation on RAM<br>Module standby setting enabled | –        | 2.9      | –    | mA   |
|        |                                   |                                    | 20 MHz              | Off  | Off                | 125 kHz   | Divide-by-8  | –  | –  | –        | 1.8      | –    | mA   |
|        |                                   |                                    | 10 MHz              | Off  | Off                | 125 kHz   | Divide-by-8  | –  | –  | –        | 1.0      | –    | mA   |
|        |                                   | High-speed on-chip oscillator mode | Off                 | Off  | 20 MHz             | 125 kHz   | No division  | –  | –  | –        | 5.0      | 11   | mA   |
|        |                                   |                                    | Off                 | Off  | 20 MHz             | 125 kHz   | Divide-by-8  | –  | –  | –        | 2.1      | –    | mA   |
|        |                                   |                                    | Off                 | Off  | 10 MHz             | 125 kHz   | No division  | –  | –  | –        | 2.9      | –    | mA   |
|        |                                   |                                    | Off                 | Off  | 10 MHz             | 125 kHz   | Divide-by-8  | –  | –  | –        | 1.5      | –    | mA   |
|        |                                   |                                    | Off                 | Off  | 4 MHz              | 125 kHz   | Divide-by-16   | MSTCR0 = BEh<br>MSTCR1 = 3Fh   | –  | –        | 0.9      | –    | mA   |
|        | Low-speed on-chip oscillator mode | Off                                | Off                 | Off  | 125 kHz            | No division                                     | FMR27 = 1<br>VCA20 = 0   | –  | –  | 106      | 300      | μA   |      |
|        |                                   | Off                                | Off                 | Off  | 125 kHz            | Divide-by-8                                     | FMR27 = 1<br>VCA20 = 0   | –  | –  | 54       | 200      | μA   |      |
|        | Low-speed clock mode              | Off                                | 32 kHz              | Off  | Off                | No division                                     | FMR27 = 1<br>VCA20 = 0   | –  | –  | 54       | 200      | μA   |      |
|        |                                   | Off                                | 32 kHz              | Off  | Off                | No division                                     | FMSTP = 1<br>VCA20 = 0   | Flash memory off<br>Program operation on RAM   | –  | 36       | –        | μA   |      |
|        | Wait mode                         | Off                                | Off                 | Off  | 125 kHz            | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1                         | While a WAIT instruction is executed<br>Peripheral clock operation   | –  | 9.0      | 50       | μA   |      |
|        |                                   | Off                                | Off                 | Off  | 125 kHz            | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | While a WAIT instruction is executed<br>Peripheral clock off   | –  | 2.5      | 31       | μA   |      |
|        |                                   | Off                                | 32 kHz              | Off  | Off                | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 0 | While a WAIT instruction is executed<br>Peripheral clock off<br>Timer RH operation in real-time clock mode | LCD drive control circuit (4)<br>When external division resistors are used     | –        | 3.1      | –    | μA   |
|        |                                   | Off                                | 32 kHz              | Off  | Off                | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | While a WAIT instruction is executed<br>Peripheral clock off<br>Timer RH operation in real-time clock mode | –  | 1.7      | –        | μA   |      |
|        |                                   | Off                                | Off                 | Off  | Off                | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1                          | –  | –  | 0.5      | 2.2      | μA   |      |
|        | Stop mode                         | Off                                | Off                 | Off  | Off                | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1                          | –  | –  | –        | –        | μA   |      |
|        |                                   | Off                                | Off                 | Off  | Off                | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1                          | –  | –  | –        | –        | μA   |      |
|        | Power-off mode                    | Off                                | Off                 | Off  | Off                | –   | –  | Power-off 0<br>Topr = 25 °C  | –  | 0.01     | 0.1      | μA   |      |
|        |                                   | Off                                | Off                 | Off  | Off                | –   | –  | Power-off 0<br>Topr = 85 °C  | –  | 0.02     | –        | μA   |      |
|        |                                   | Off                                | 32 kHz              | Off  | Off                | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1                          | Power-off 2<br>Topr = 25 °C  | –  | 1.3      | 4.5      | μA   |      |
| Off    |                                   | 32 kHz                             | Off                 | Off  | –                  | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1 | Power-off 2<br>Topr = 85 °C  | –  | 2.2  | –        | μA       |      |      |

## Notes:

- Vcc = 2.7 V to 4.0 V, single chip mode, output pins are open, and other pins are Vss.
- XIN is set to square wave input.
- Vcc = 3.0 V
- VLCD = Vcc, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG26 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

**Table 5.22 DC Characteristics (5) [1.8 V ≤ V<sub>CC</sub> < 2.7 V]**  
**(T<sub>opr</sub> = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)**

| Symbol                           | Parameter           |   | Condition                                       |                         | Standard              |      |                 | Unit |
|----------------------------------|---------------------|---|---|-------------------------|-----------------------|------|-----------------|------|
|                                  |                     |   |   |                         | Min.                  | Typ. | Max.            |      |
| V <sub>OH</sub>                  | Output "H" voltage  |   | Port P8 (1)                                     | I <sub>OH</sub> = –2 mA | V <sub>CC</sub> – 0.5 | –    | V <sub>CC</sub> | V    |
|                                  |                     |   | Other pins                                      | I <sub>OH</sub> = –1 mA | V <sub>CC</sub> – 0.5 | –    | V <sub>CC</sub> | V    |
| V <sub>OL</sub>                  | Output "L" voltage  |   | Port P8 (1)                                     | I <sub>OL</sub> = 2 mA  | –                     | –    | 0.5             | V    |
|                                  |                     |   | Other pins                                      | I <sub>OL</sub> = 1 mA  | –                     | –    | 0.5             | V    |
| V <sub>T+</sub> –V <sub>T–</sub> | Hysteresis          | $\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT2}},$<br>$\overline{\text{INT3}}, \overline{\text{INT5}}, \overline{\text{INT7}},$<br>$\overline{\text{KI0}}, \overline{\text{KI1}}, \overline{\text{KI2}}, \overline{\text{KI3}},$<br>$\overline{\text{KI4}}, \overline{\text{KI5}}, \overline{\text{KI6}}, \overline{\text{KI7}},$<br>TRCIOA, TRCIOB,<br>TRCIOC, TRCIOD,<br>TRJ0IO, TRJ1IO,<br>TRCTRG, TRCCLK,<br>ADTRG,<br>RXD0, CLK0, SSI,<br>SCL, SDA, SSO |   |                         | 0.05                  | 0.4  | –               | V    |
|                                  |                     | $\overline{\text{RESET}}, \overline{\text{WKUP0}}$  |   |                         | 0.1                   | 0.8  | –               | V    |
| I <sub>IH</sub>                  | Input "H" current   |   | V <sub>I</sub> = 1.8 V, V <sub>CC</sub> = 1.8 V |                         | –                     | –    | 4.0             | μA   |
| I <sub>IL</sub>                  | Input "L" current   |   | V <sub>I</sub> = 0 V, V <sub>CC</sub> = 1.8 V   |                         | –                     | –    | –4.0            | μA   |
| R <sub>PULLUP</sub>              | Pull-up resistance  |   | V <sub>I</sub> = 0 V, V <sub>CC</sub> = 1.8 V   |                         | 85                    | 220  | 500             | kΩ   |
| R <sub>FXIN</sub>                | Feedback resistance | XIN   |   |                         | –                     | 2.0  | –               | MΩ   |
| R <sub>FXCIN</sub>               | Feedback resistance | XCIN  |   |                         | –                     | 14   | –               | MΩ   |
| V <sub>RAM</sub>                 | RAM hold voltage    |   | During stop mode                                |                         | 1.8                   | –    | –               | V    |

Note:

1. This applies when the drive capacity of the output transistor is set to High by P8DRR register. When the drive capacity is set to Low, the value of any other pin applies.

**Table 5.23 DC Characteristics (6) [ $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$ ]**  
**( $T_{opr} = -20\text{ to }85\text{ }^{\circ}\text{C}$  (N version)/  $-40\text{ to }85\text{ }^{\circ}\text{C}$  (D version), unless otherwise specified.)**

| Symbol          | Parameter                |                                    | Condition           |        |                    |   |                             |  |  | Standard   |          |      | Unit |    |
|-----------------|--------------------------|------------------------------------|---------------------|--------|--------------------|---|-----------------------------|--|--|--|----------|------|------|----|
|                 |                          |                                    | Oscillation Circuit |        | On-Chip Oscillator |   | CPU Clock                   | Low-Power-Consumption Setting  | Other  | Min.   | Typ. (3) | Max. |      |    |
|                 |                          |                                    | XIN (2)             | XCIN   | High-Speed         | Low-Speed                                       |                             |  |  |  |          |      |      |    |
| I <sub>cc</sub> | Power supply current (1) | High-speed clock mode              | 8 MHz               | Off    | Off                | 125 kHz   | No division                 | –  | –  | 2.1  | –        | mA   |      |    |
|                 |                          |                                    | 8 MHz               | Off    | Off                | 125 kHz   | Divide-by-8                 | –  | –  | 0.9  | –        | mA   |      |    |
|                 |                          | High-speed on-chip oscillator mode | Off                 | Off    | 5 MHz              | 125 kHz   | No division                 | –  | –  | 1.8  | 5        | mA   |      |    |
|                 |                          |                                    | Off                 | Off    | 5 MHz              | 125 kHz   | Divide-by-8                 | –  | –  | 1.1  | –        | mA   |      |    |
|                 |                          |                                    | Off                 | Off    | 4 MHz              | 125 kHz   | Divide-by-16                | MSTCR0 = BEh<br>MSTCR1 = 3Fh   | –  | –  | 0.9      | –    | mA   |    |
|                 |                          | Low-speed on-chip oscillator mode  | Off                 | Off    | Off                | 125 kHz   | No division                 | FMR27 = 1<br>VCA20 = 0   | –  | 106  | 300      | μA   |      |    |
|                 |                          |                                    | Off                 | Off    | Off                | 125 kHz   | Divide-by-8                 | FMR27 = 1<br>VCA20 = 0   | –  | 54   | 200      | μA   |      |    |
|                 |                          | Low-speed clock mode               | Off                 | 32 kHz | Off                | Off   | No division                 | FMR27 = 1<br>VCA20 = 0   | –  | 54   | 200      | μA   |      |    |
|                 |                          |                                    | Off                 | 32 kHz | Off                | Off   | No division                 | FMSTP = 1<br>VCA20 = 0   | Flash memory off<br>Program operation on RAM   | –  | 36       | –    | μA   |    |
|                 |                          | Wait mode                          | Off                 | Off    | Off                | 125 kHz   | –                           | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1                         | While a WAIT instruction is executed<br>Peripheral clock operation   | –  | 9.0      | 50   | μA   |    |
|                 |                          |                                    | Off                 | Off    | Off                | 125 kHz   | –                           | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | While a WAIT instruction is executed<br>Peripheral clock off   | –  | 2.5      | 31   | μA   |    |
|                 |                          |                                    | Off                 | 32 kHz | Off                | Off   | –                           | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 0 | While a WAIT instruction is executed<br>Peripheral clock off<br>Timer RH operation in real-time clock mode | LCD drive control circuit (4)<br>When external division resistors are used | –        | 2.4  | –    | μA |
|                 |                          |                                    | Off                 | 32 kHz | Off                | Off   | –                           | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | While a WAIT instruction is executed<br>Peripheral clock off<br>Timer RH operation in real-time clock mode | –  | 1.7      | –    | μA   |    |
|                 |                          | Stop mode                          | Off                 | Off    | Off                | Off   | –                           | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1                          | Topr = 25 °C<br>Peripheral clock off   | –  | 0.5      | 2.2  | μA   |    |
|                 |                          |                                    | Off                 | Off    | Off                | Off   | –                           | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1                         | Topr = 85 °C<br>Peripheral clock off   | –  | 1.2      | –    | μA   |    |
|                 |                          | Power-off mode                     | Off                 | Off    | Off                | Off   | –                           | –  | Power-off 0<br>Topr = 25 °C  | –  | 0.01     | 0.1  | μA   |    |
|                 |                          |                                    | Off                 | Off    | Off                | Off   | –                           | –  | Power-off 0<br>Topr = 85 °C  | –  | 0.02     | –    | μA   |    |
| Off             | 32 kHz                   |                                    | Off                 | Off    | –                  | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1 | Power-off 2<br>Topr = 25 °C | –  | 1.2  | 4  | μA       |      |      |    |
| Off             | 32 kHz                   |                                    | Off                 | Off    | –                  | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1 | Power-off 2<br>Topr = 85 °C | –  | 2  | –  | μA       |      |      |    |

## Notes:

1.  $V_{CC} = 1.8\text{ V}$  to  $2.7\text{ V}$ , single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3.  $V_{CC} = 2.2\text{ V}$
4. VLCD = V<sub>CC</sub>, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG26 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

### 5.1.5 AC Characteristics

**Table 5.24 Timing Requirements of Synchronous Serial Communication Unit (SSU)**  
**(V<sub>CC</sub> = 1.8 to 5.5 V, V<sub>SS</sub> = 0 V, and T<sub>opr</sub> = -20 to 85 °C (N version)/**  
**-40 to 85 °C (D version), unless otherwise specified.)**

| Symbol | Parameter                       |        | Conditions                      | Standard   |      |               | Unit     |
|--------|---------------------------------|--------|---------------------------------|------------|------|---------------|----------|
|        |                                 |        |                                 | Min.       | Typ. | Max.          |          |
| tsucyc | SSCK clock cycle time           |        |                                 | 4          | -    | -             | tcyc (1) |
| tHI    | SSCK clock "H" width            |        |                                 | 0.4        | -    | 0.6           | tsucyc   |
| tLO    | SSCK clock "L" width            |        |                                 | 0.4        | -    | 0.6           | tsucyc   |
| tRISE  | SSCK clock rising time          | Master |                                 | -          | -    | 1             | tcyc (1) |
|        |                                 | Slave  |                                 | -          | -    | 1             | μs       |
| tFALL  | SSCK clock falling time         | Master |                                 | -          | -    | 1             | tcyc (1) |
|        |                                 | Slave  |                                 | -          | -    | 1             | μs       |
| tsu    | SSO, SSI data input setup time  |        |                                 | 100        | -    | -             | ns       |
| tH     | SSO, SSI data input hold time   |        |                                 | 1          | -    | -             | tcyc (1) |
| tLEAD  | $\overline{SCS}$ setup time     | Slave  |                                 | 1tcyc + 50 | -    | -             | ns       |
| tLAG   | $\overline{SCS}$ hold time      | Slave  |                                 | 1tcyc + 50 | -    | -             | ns       |
| tOD    | SSO, SSI data output delay time |        |                                 | -          | -    | 1tcyc + 20    | ns       |
| tsa    | SSI slave access time           |        | 2.7 V ≤ V <sub>CC</sub> ≤ 5.5 V | -          | -    | 1.5tcyc + 100 | ns       |
|        |                                 |        | 1.8 V ≤ V <sub>CC</sub> < 2.7 V | -          | -    | 1.5tcyc + 200 | ns       |
| tor    | SSI slave out open time         |        | 2.7 V ≤ V <sub>CC</sub> ≤ 5.5 V | -          | -    | 1.5tcyc + 100 | ns       |
|        |                                 |        | 1.8 V ≤ V <sub>CC</sub> < 2.7 V | -          | -    | 1.5tcyc + 200 | ns       |

Note:

- 1tcyc = 1/f1(s)

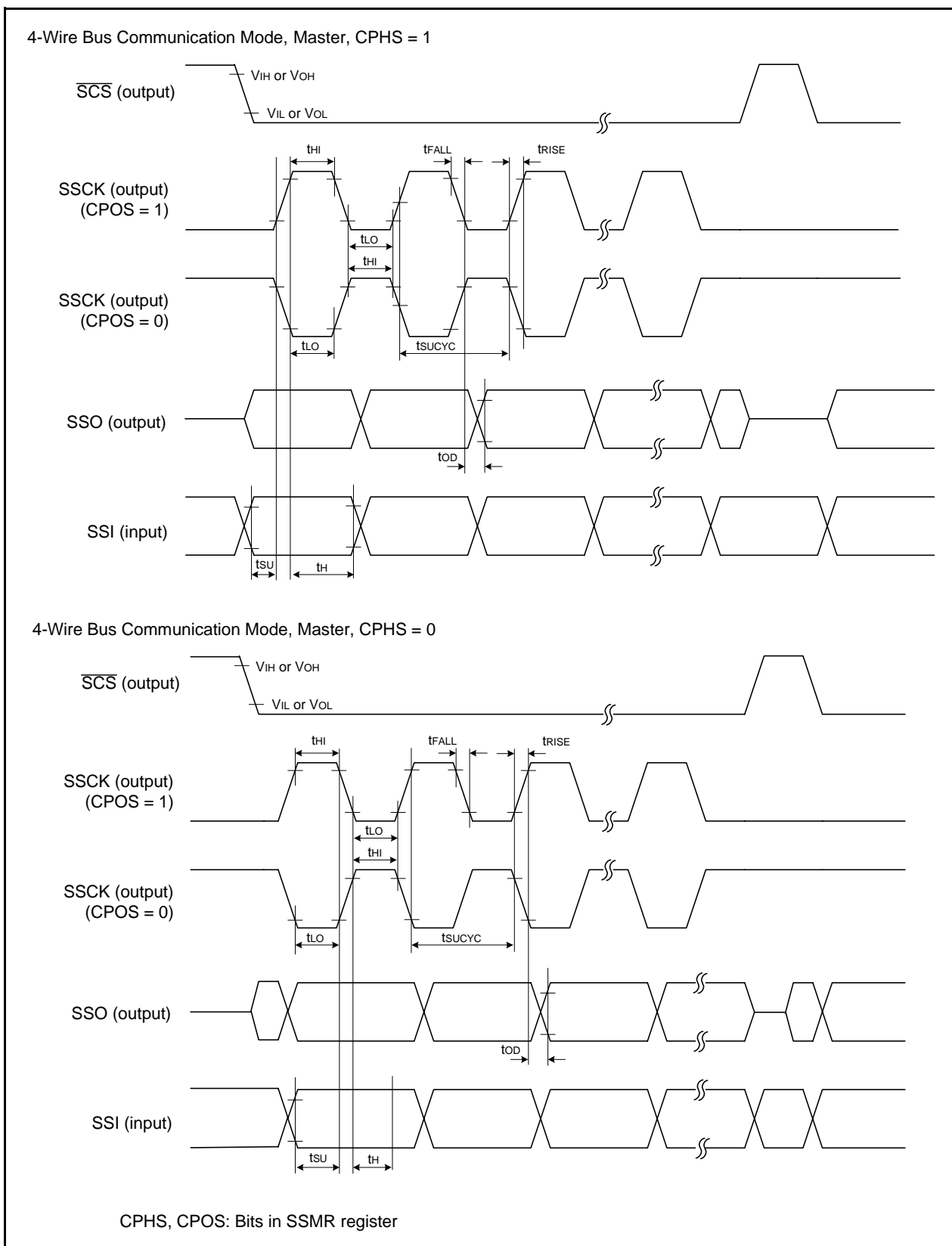


Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

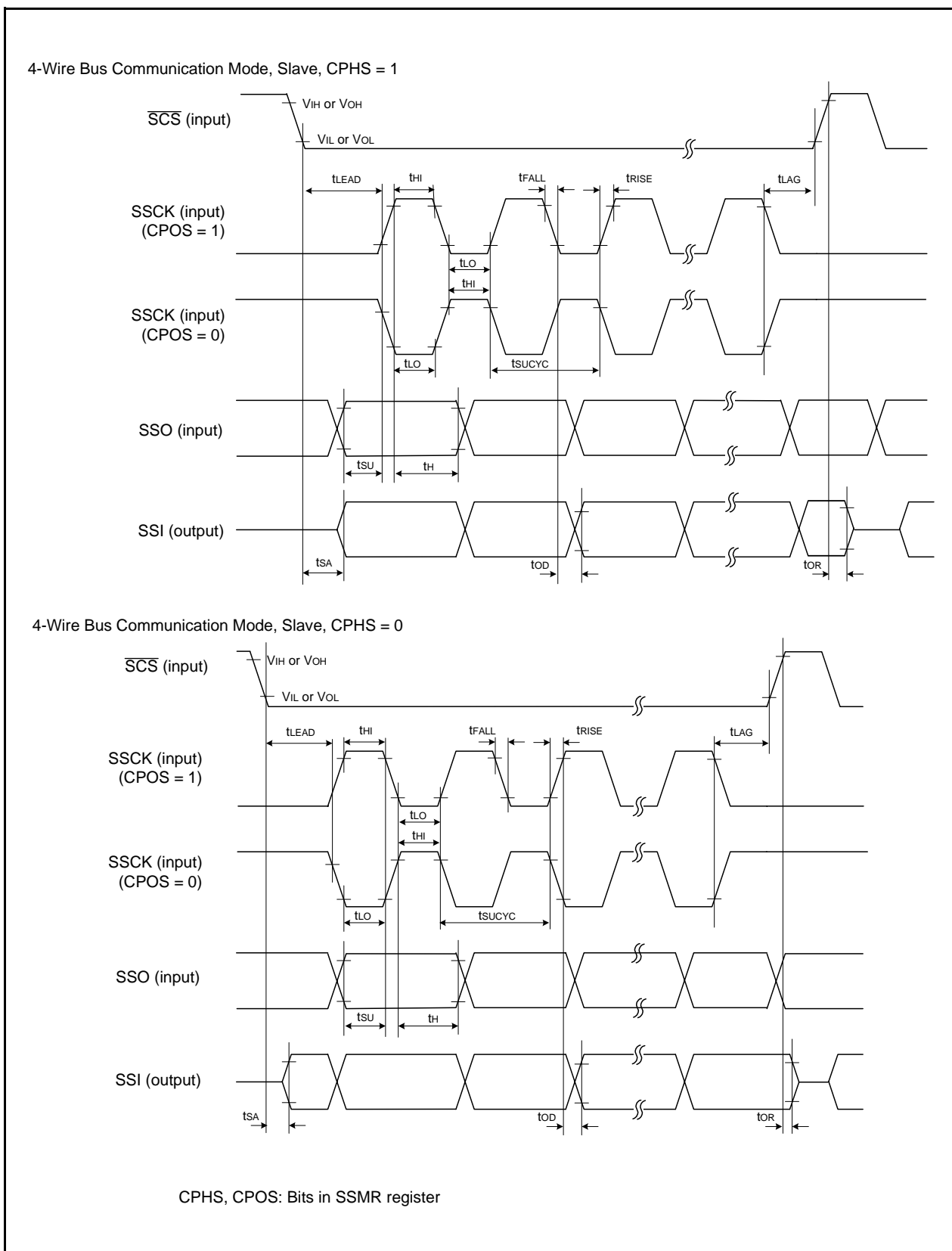


Figure 5.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)



Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

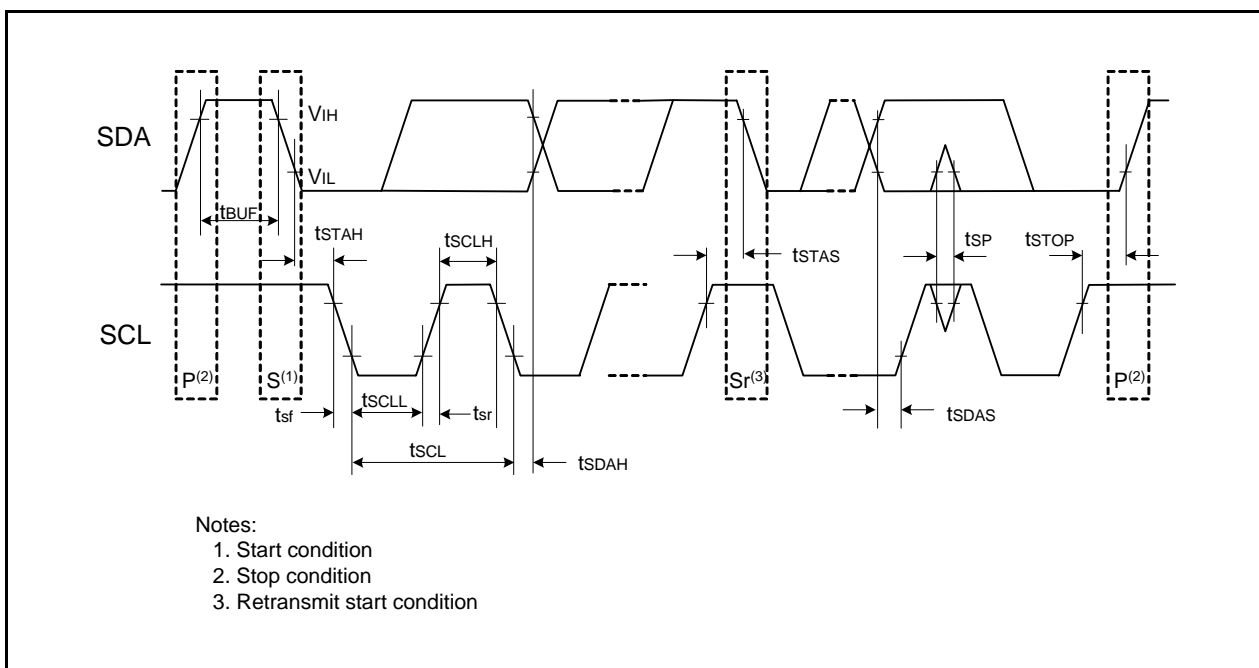


**Table 5.25 Timing Requirements of I<sup>2</sup>C bus Interface (1)**  
**(V<sub>CC</sub> = 1.8 to 5.5 V, V<sub>SS</sub> = 0 V, and T<sub>opr</sub> = -20 to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.)**

| Symbol            | Parameter                                   | Condition | Standard         |      |           | Unit |
|-------------------|---|-----------|------------------|------|-----------|------|
|                   |   |           | Min.             | Typ. | Max.      |      |
| t <sub>SCL</sub>  | SCL input cycle time                        |           | 12tcyc + 600 (1) | –    | –         | ns   |
| t <sub>SCLH</sub> | SCL input “H” width                         |           | 3tcyc + 300 (1)  | –    | –         | ns   |
| t <sub>SCLL</sub> | SCL input “L” width                         |           | 5tcyc + 500 (1)  | –    | –         | ns   |
| t <sub>sf</sub>   | SCL, SDA input fall time                    |           | –                | –    | 300       | ns   |
| t <sub>SP</sub>   | SCL, SDA input spike pulse rejection time   |           | –                | –    | 1tcyc (1) | ns   |
| t <sub>BUF</sub>  | SDA input bus-free time                     |           | 5tcyc (1)        | –    | –         | ns   |
| t <sub>STAH</sub> | Start condition input hold time             |           | 3tcyc (1)        | –    | –         | ns   |
| t <sub>STAS</sub> | Retransmit start condition input setup time |           | 3tcyc (1)        | –    | –         | ns   |
| t <sub>STOP</sub> | Stop condition input setup time             |           | 3tcyc (1)        | –    | –         | ns   |
| t <sub>SDAS</sub> | Data input setup time                       |           | 1tcyc + 40 (1)   | –    | –         | ns   |
| t <sub>SDAH</sub> | Data input hold time                        |           | 10               | –    | –         | ns   |

Note:

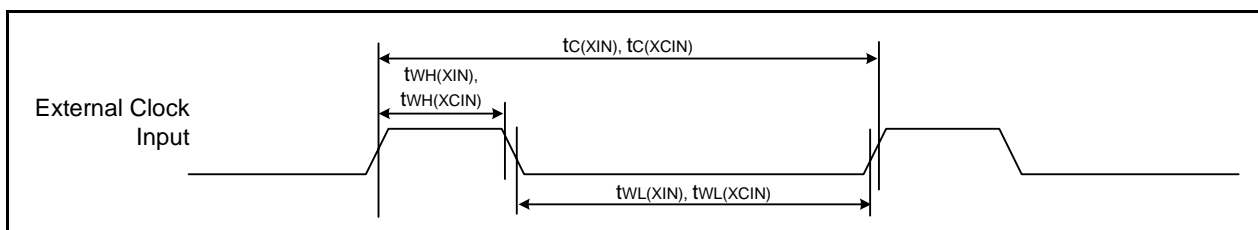
- 1tcyc = 1/f1(s)



**Figure 5.7 I/O Timing of I<sup>2</sup>C bus Interface**

**Table 5.26 Timing Requirements of External Clock Input (XIN, XCIN)**  
( $V_{SS} = 0\text{ V}$  and  $T_{opr} = -20\text{ to }85\text{ }^{\circ}\text{C}$  (N version)/  $-40\text{ to }85\text{ }^{\circ}\text{C}$  (D version), unless otherwise specified.)

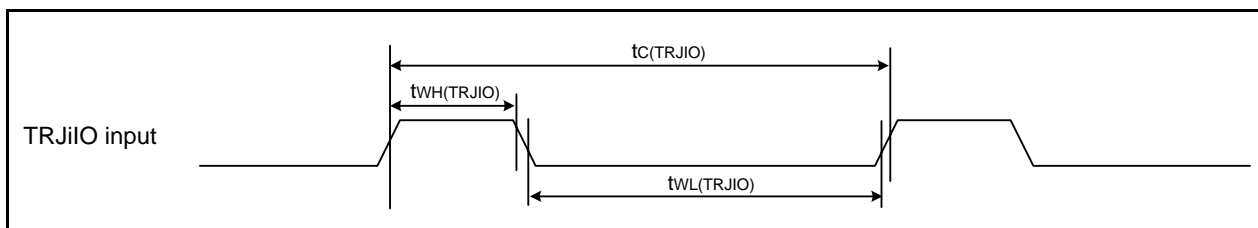
| Symbol         | Parameter             | Standard   |      |  |      |  |      | Unit          |
|----------------|-----------------------|--|------|--|------|--|------|---------------|
|                |                       | $V_{CC} = 2.2\text{V}, T_{opr} = 25^{\circ}\text{C}$ |      | $V_{CC} = 3\text{V}, T_{opr} = 25^{\circ}\text{C}$ |      | $V_{CC} = 5\text{V}, T_{opr} = 25^{\circ}\text{C}$ |      |               |
|                |                       | Min.   | Max. | Min.   | Max. | Min.   | Max. |               |
| $t_{c(XIN)}$   | XIN input cycle time  | 200  | –    | 50   | –    | 50   | –    | ns            |
| $t_{WH(XIN)}$  | XIN input “H” width   | 90   | –    | 24   | –    | 24   | –    | ns            |
| $t_{WL(XIN)}$  | XIN input “L” width   | 90   | –    | 24   | –    | 24   | –    | ns            |
| $t_{c(XCIN)}$  | XCIN input cycle time | 20   | –    | 20   | –    | 20   | –    | $\mu\text{s}$ |
| $t_{WH(XCIN)}$ | XCIN input “H” width  | 10   | –    | 10   | –    | 10   | –    | $\mu\text{s}$ |
| $t_{WL(XCIN)}$ | XCIN input “L” width  | 10   | –    | 10   | –    | 10   | –    | $\mu\text{s}$ |



**Figure 5.8 External Clock Input Timing**

**Table 5.27 Timing Requirements of TRJiIO (i = 0 or 1)**  
( $V_{SS} = 0\text{ V}$  and  $T_{opr} = -20\text{ to }85\text{ }^{\circ}\text{C}$  (N version)/  $-40\text{ to }85\text{ }^{\circ}\text{C}$  (D version), unless otherwise specified.)

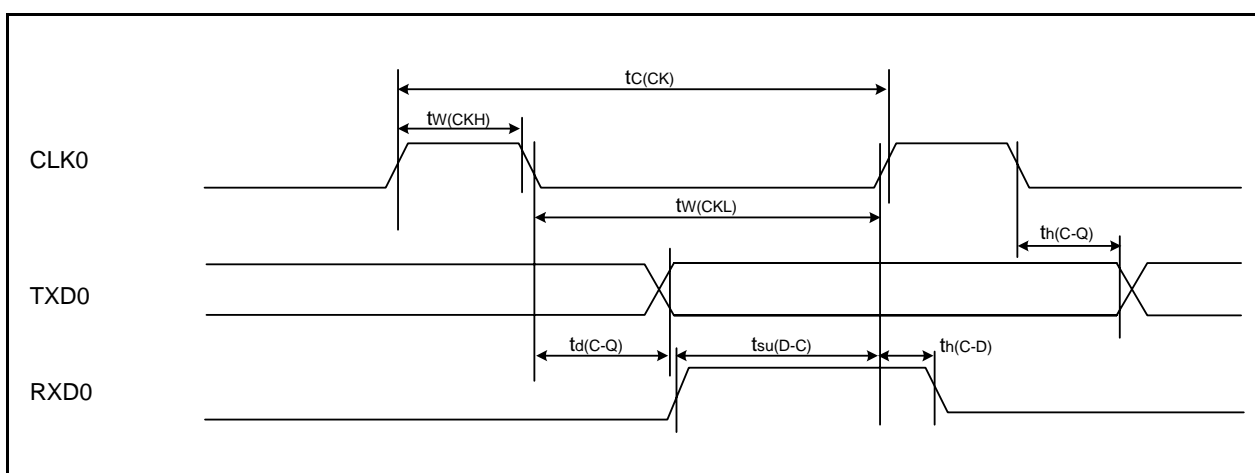
| Symbol          | Parameter               | Standard   |      |  |      |  |      | Unit |
|-----------------|-------------------------|--|------|--|------|--|------|------|
|                 |                         | $V_{CC} = 2.2\text{V}, T_{opr} = 25^{\circ}\text{C}$ |      | $V_{CC} = 3\text{V}, T_{opr} = 25^{\circ}\text{C}$ |      | $V_{CC} = 5\text{V}, T_{opr} = 25^{\circ}\text{C}$ |      |      |
|                 |                         | Min.   | Max. | Min.   | Max. | Min.   | Max. |      |
| $t_{c(TRJIO)}$  | TRJiIO input cycle time | 500  | –    | 300  | –    | 100  | –    | ns   |
| $t_{WH(TRJIO)}$ | TRJiIO input “H” width  | 200  | –    | 120  | –    | 40   | –    | ns   |
| $t_{WL(TRJIO)}$ | TRJiIO input “L” width  | 200  | –    | 120  | –    | 40   | –    | ns   |



**Figure 5.9 Input Timing of TRJiIO**

**Table 5.28 Timing Requirements of Serial Interface**  
( $V_{SS} = 0\text{ V}$  and  $T_{opr} = -20\text{ to }85\text{ }^{\circ}\text{C}$  (N version)/  $-40\text{ to }85\text{ }^{\circ}\text{C}$  (D version), unless otherwise specified.)

| Symbol        | Parameter              | Standard   |      |  |      |  |      | Unit |
|---------------|------------------------|--|------|--|------|--|------|------|
|               |                        | $V_{CC} = 2.2\text{V}, T_{opr} = 25^{\circ}\text{C}$ |      | $V_{CC} = 3\text{V}, T_{opr} = 25^{\circ}\text{C}$ |      | $V_{CC} = 5\text{V}, T_{opr} = 25^{\circ}\text{C}$ |      |      |
|               |                        | Min.   | Max. | Min.   | Max. | Min.   | Max. |      |
| $t_{c(CK)}$   | CLK0 input cycle time  | 800  | –    | 300  | –    | 200  | –    | ns   |
| $t_{w(CKH)}$  | CLK0 input “H” width   | 400  | –    | 150  | –    | 100  | –    | ns   |
| $t_{w(CKL)}$  | CLK0 input “L” width   | 400  | –    | 150  | –    | 100  | –    | ns   |
| $t_{d(C-Q)}$  | TXD0 output delay time | –  | 200  | –  | 80   | –  | 50   | ns   |
| $t_{h(C-Q)}$  | TXD0 hold time         | 0  | –    | 0  | –    | 0  | –    | ns   |
| $t_{su(D-C)}$ | RXD0 input setup time  | 150  | –    | 70   | –    | 50   | –    | ns   |
| $t_{h(C-D)}$  | RXD0 input hold time   | 90   | –    | 90   | –    | 90   | –    | ns   |



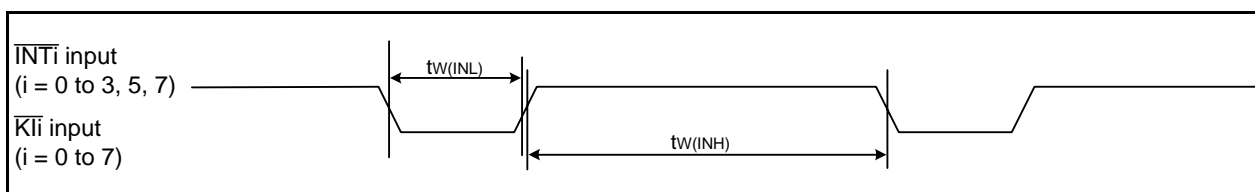
**Figure 5.10 Input and Output Timing of Serial Interface**

**Table 5.29 Timing Requirements of External Interrupt  $\overline{INT}_i$  ( $i = 0\text{ to }3, 5, 7$ ) and Key Input Interrupt  $\overline{KI}_i$  ( $i = 0\text{ to }7$ )**  
( $V_{SS} = 0\text{ V}$  and  $T_{opr} = -20\text{ to }85\text{ }^{\circ}\text{C}$  (N version)/  $-40\text{ to }85\text{ }^{\circ}\text{C}$  (D version), unless otherwise specified.)

| Symbol       | Parameter   | Standard   |      |  |      |  |      | Unit |
|--------------|---|--|------|--|------|--|------|------|
|              |   | $V_{CC} = 2.2\text{V}, T_{opr} = 25^{\circ}\text{C}$ |      | $V_{CC} = 3\text{V}, T_{opr} = 25^{\circ}\text{C}$ |      | $V_{CC} = 5\text{V}, T_{opr} = 25^{\circ}\text{C}$ |      |      |
|              |   | Min.   | Max. | Min.   | Max. | Min.   | Max. |      |
| $t_{w(INH)}$ | $\overline{INT}_i$ input “H” width, $\overline{KI}_i$ input “H” width | 1000 (1)   | –    | 380 (1)  | –    | 250 (1)  | –    | ns   |
| $t_{w(INL)}$ | $\overline{INT}_i$ input “L” width, $\overline{KI}_i$ input “L” width | 1000 (2)   | –    | 380 (2)  | –    | 250 (2)  | –    | ns   |

Notes:

- When selecting the digital filter by the  $\overline{INT}_i$  input filter select bit, use an  $\overline{INT}_i$  input HIGH width of either (1/digital filter clock frequency  $\times$  3) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the  $\overline{INT}_i$  input filter select bit, use an  $\overline{INT}_i$  input LOW width of either (1/digital filter clock frequency  $\times$  3) or the minimum value of standard, whichever is greater.



**Figure 5.11 Input Timing of External Interrupt  $\overline{INT}_i$  and Key Input Interrupt  $\overline{KI}_i$**

## 5.2 Electrical Characteristics (R8C/LA6A Group and R8C/LA8A Group)

### 5.2.1 Absolute Maximum Ratings

**Table 5.30 Absolute Maximum Ratings**

| Symbol                            | Parameter                     |               | Condition   | Rated Value                                     | Unit |
|-----------------------------------|-------------------------------|---------------|---|---|------|
| V <sub>CC</sub> /AV <sub>CC</sub> | Supply voltage                |               |   | -0.3 to 6.5                                     | V    |
| V <sub>I</sub>                    | Input voltage                 | XIN           | XIN-XOUT oscillation on (oscillation buffer ON) <sup>(1)</sup>  | -0.3 to 1.9                                     | V    |
|                                   |                               | XIN           | XIN-XOUT oscillation on (oscillation buffer OFF) <sup>(1)</sup> | -0.3 to V <sub>CC</sub> + 0.3                   | V    |
|                                   |                               | P5_4/VL1      |   | -0.3 to VL2 <sup>(2)</sup>                      | V    |
|                                   |                               | P5_5/VL2      |   | VL1 to VL3                                      | V    |
|                                   |                               | P5_6/VL3      |   | VL2 to 6.5                                      | V    |
|                                   |                               | Other pins    |   | -0.3 to V <sub>CC</sub> + 0.3                   | V    |
| V <sub>O</sub>                    | Output voltage                | XOUT          | XIN-XOUT oscillation on (oscillation buffer ON) <sup>(1)</sup>  | -0.3 to 1.9                                     | V    |
|                                   |                               | XOUT          | XIN-XOUT oscillation on (oscillation buffer OFF) <sup>(1)</sup> | -0.3 to V <sub>CC</sub> + 0.3                   | V    |
|                                   |                               | COM0 to COM3  |   | -0.3 to VL3                                     | V    |
|                                   |                               | SEG0 to SEG39 |   | -0.3 to VL3                                     | V    |
|                                   |                               | Other pins    |   | -0.3 to V <sub>CC</sub> + 0.3                   | V    |
| P <sub>d</sub>                    | Power dissipation             |               | -40°C ≤ T <sub>opr</sub> ≤ 85°C                                 | 500   | mW   |
| T <sub>opr</sub>                  | Operating ambient temperature |               |   | -20 to 85 (N version)/<br>-40 to 85 (D version) | °C   |
| T <sub>stg</sub>                  | Storage temperature           |               |   | -65 to 150                                      | °C   |

Notes:

1. For the register settings for each operation, refer to **7. I/O Ports** and **9. Clock Generation Circuit** in the User's Manual: Hardware.
2. The VL1 voltage should be V<sub>CC</sub> or below.

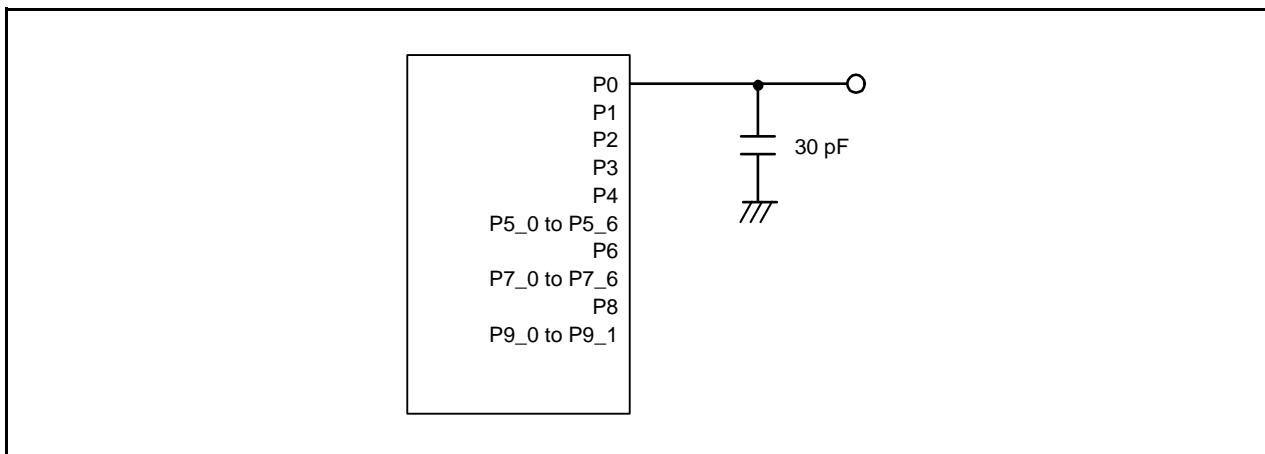
## 5.2.2 Recommended Operating Conditions

**Table 5.31 Recommended Operating Conditions**  
(VCC = 1.8 to 5.5 V and Topr = -20 to 85°C (N version)/ -40 to 85°C (D version), unless otherwise specified.)

| Symbol     | Parameter                                      |                           | Conditions                                | Standard                         |         |                     | Unit     |    |          |    |
|------------|--|---------------------------|---|----------------------------------|---------|---------------------|----------|----|----------|----|
|            |  |                           |   | Min.                             | Typ.    | Max.                |          |    |          |    |
| VCC/AVCC   | Supply voltage                                 |                           |   | 1.8                              | -       | 5.5                 | V        |    |          |    |
| VSS/AVSS   | Supply voltage                                 |                           |   | -                                | 0       | -                   | V        |    |          |    |
| VIH        | Input "H" voltage                              | Other than CMOS input     |   | 4.0 V ≤ VCC ≤ 5.5 V              | 0.8 VCC | -                   | VCC      | V  |          |    |
|            |  |                           |   | 2.7 V ≤ VCC < 4.0 V              | 0.8 VCC | -                   | VCC      | V  |          |    |
|            |  |                           |   | 1.8 V ≤ VCC < 2.7 V              | 0.9 VCC | -                   | VCC      | V  |          |    |
|            |  | CMOS input                | Input level switching function (I/O port) | Input level selection : 0.35 VCC |         | 4.0 V ≤ VCC ≤ 5.5 V | 0.5 VCC  | -  | VCC      | V  |
|            |  |                           |   |                                  |         | 2.7 V ≤ VCC < 4.0 V | 0.55 VCC | -  | VCC      | V  |
|            |  |                           |   |                                  |         | 1.8 V ≤ VCC < 2.7 V | 0.65 VCC | -  | VCC      | V  |
|            |  |                           |   | Input level selection : 0.5 VCC  |         | 4.0 V ≤ VCC ≤ 5.5 V | 0.65 VCC | -  | VCC      | V  |
|            |  |                           |   |                                  |         | 2.7 V ≤ VCC < 4.0 V | 0.7 VCC  | -  | VCC      | V  |
|            |  |                           |   |                                  |         | 1.8 V ≤ VCC < 2.7 V | 0.8 VCC  | -  | VCC      | V  |
|            |  |                           |   | Input level selection : 0.7 VCC  |         | 4.0 V ≤ VCC ≤ 5.5 V | 0.85 VCC | -  | VCC      | V  |
|            |  |                           |   |                                  |         | 2.7 V ≤ VCC < 4.0 V | 0.85 VCC | -  | VCC      | V  |
|            |  |                           |   |                                  |         | 1.8 V ≤ VCC < 2.7 V | 0.85 VCC | -  | VCC      | V  |
| VIL        | Input "L" voltage                              | Other than CMOS input     |   | 4.0 V ≤ VCC ≤ 5.5 V              | 0       | -                   | 0.2 VCC  | V  |          |    |
|            |  |                           |   | 2.7 V ≤ VCC < 4.0 V              | 0       | -                   | 0.2 VCC  | V  |          |    |
|            |  |                           |   | 1.8 V ≤ VCC < 2.7 V              | 0       | -                   | 0.05 VCC | V  |          |    |
|            |  | CMOS input                | Input level switching function (I/O port) | Input level selection : 0.35 VCC |         | 4.0 V ≤ VCC ≤ 5.5 V | 0        | -  | 0.2 VCC  | V  |
|            |  |                           |   |                                  |         | 2.7 V ≤ VCC < 4.0 V | 0        | -  | 0.2 VCC  | V  |
|            |  |                           |   |                                  |         | 1.8 V ≤ VCC < 2.7 V | 0        | -  | 0.2 VCC  | V  |
|            |  |                           |   | Input level selection : 0.5 VCC  |         | 4.0 V ≤ VCC ≤ 5.5 V | 0        | -  | 0.4 VCC  | V  |
|            |  |                           |   |                                  |         | 2.7 V ≤ VCC < 4.0 V | 0        | -  | 0.3 VCC  | V  |
|            |  |                           |   |                                  |         | 1.8 V ≤ VCC < 2.7 V | 0        | -  | 0.2 VCC  | V  |
|            |  |                           |   | Input level selection : 0.7 VCC  |         | 4.0 V ≤ VCC ≤ 5.5 V | 0        | -  | 0.55 VCC | V  |
|            |  |                           |   |                                  |         | 2.7 V ≤ VCC < 4.0 V | 0        | -  | 0.45 VCC | V  |
|            |  |                           |   |                                  |         | 1.8 V ≤ VCC < 2.7 V | 0        | -  | 0.35 VCC | V  |
|            |  | IOH(sum)                  | Peak sum output "H" current               | Sum of all pins IOH(peak)        |         |                     | -        | -  | -160     | mA |
|            |  | IOH(sum)                  | Average sum output "H" current            | Sum of all pins IOH(avg)         |         |                     | -        | -  | -80      | mA |
|            |  | IOH(peak)                 | Peak output "H" current                   | Port P7_0, P7_1, P8 (2)          |         |                     | -        | -  | -40      | mA |
| Other pins |  |                           |   |                                  | -       | -                   | -10      | mA |          |    |
| IOH(avg)   | Average output "H" current (1)                 | Port P7_0, P7_1, P8 (2)   |   |                                  | -       | -                   | -20      | mA |          |    |
|            |  | Other pins                |   |                                  | -       | -                   | -5       | mA |          |    |
| IOI(sum)   | Peak sum output "L" current                    | Sum of all pins IOI(peak) |   |                                  | -       | -                   | 160      | mA |          |    |
| IOI(sum)   | Average sum output "L" current                 | Sum of all pins IOI(avg)  |   |                                  | -       | -                   | 80       | mA |          |    |
| IOI(peak)  | Peak output "L" current                        | Port P7_0, P7_1, P8 (2)   |   |                                  | -       | -                   | 40       | mA |          |    |
|            |  | Other pins                |   |                                  | -       | -                   | 10       | mA |          |    |
| IOI(avg)   | Average output "L" current (1)                 | Port P7_0, P7_1, P8 (2)   |   |                                  | -       | -                   | 20       | mA |          |    |
|            |  | Other pins                |   |                                  | -       | -                   | 5        | mA |          |    |
| f(XIN)     | XIN clock input oscillation frequency          |                           | 2.7 V ≤ VCC ≤ 5.5 V                       | 2                                | -       | 20                  | MHz      |    |          |    |
|            |  |                           | 1.8 V ≤ VCC < 2.7 V                       | 2                                | -       | 8                   | MHz      |    |          |    |
| f(XCIN)    | XCIN oscillation frequency                     |                           | 1.8 V ≤ VCC ≤ 5.5 V                       | -                                | 32.768  | -                   | kHz      |    |          |    |
|            | XCIN external clock input frequency            |                           | 1.8 V ≤ VCC ≤ 5.5 V                       | -                                | -       | 50                  | kHz      |    |          |    |
| fOCO20M    | When used as the count source for timer RC (3) |                           | 2.7 V ≤ VCC ≤ 5.5 V                       | 18.432                           | -       | 20                  | MHz      |    |          |    |
| fOCO-F     | fOCO-F frequency                               |                           | 2.7 V ≤ VCC ≤ 5.5 V                       | -                                | -       | 20                  | MHz      |    |          |    |
|            |  |                           | 1.8 V ≤ VCC < 2.7 V                       | -                                | -       | 8                   | MHz      |    |          |    |
| -          | System clock frequency                         |                           | 2.7 V ≤ VCC ≤ 5.5 V                       | -                                | -       | 20                  | MHz      |    |          |    |
|            |  |                           | 1.8 V ≤ VCC < 2.7 V                       | -                                | -       | 8                   | MHz      |    |          |    |
| f(BCLK)    | CPU clock frequency                            |                           | 2.7 V ≤ VCC ≤ 5.5 V                       | 0                                | -       | 20                  | MHz      |    |          |    |
|            |  |                           | 1.8 V ≤ VCC < 2.7 V                       | 0                                | -       | 8                   | MHz      |    |          |    |

## Notes:

- The average output current indicates the average value of current measured during 100 ms.
- This applies when the drive capacity of the output transistor is set to High by registers P7DRR and P8DRR. When the drive capacity is set to Low, the value of any other pin applies.
- fOCO20M can be used as the count source for timer RC in the range of VCC = 2.7 V to 5.5V.



**Figure 5.12** Ports P0 to P4, P5\_0 to P5\_6, P6, P7\_0 to P7\_6, P8, and P9\_0 to P9\_1 Timing Measurement Circuit

### 5.2.3 Peripheral Function Characteristics

**Table 5.32 A/D Converter Characteristics**  
( $V_{CC}/AV_{CC} = V_{ref} = 1.8$  to  $5.5$  V,  $V_{SS} = 0$  V, and  $T_{opr} = -20$  to  $85^{\circ}\text{C}$  (N version)/  $-40$  to  $85^{\circ}\text{C}$  (D version), unless otherwise specified.)

| Symbol            | Parameter                           |             | Conditions   | Standard |      |                  | Unit          |
|-------------------|-------------------------------------|-------------|--|----------|------|------------------|---------------|
|                   |                                     |             |  | Min.     | Typ. | Max.             |               |
| –                 | Resolution                          |             | $V_{ref} = AV_{CC}$                                    | –        | –    | 10               | Bit           |
| –                 | Absolute accuracy <sup>(2)</sup>    | 10-bit mode | $V_{ref} = AV_{CC} = 5.0$ V AN0 to AN11 input          | –        | –    | $\pm 3$          | LSB           |
|                   |                                     |             | $V_{ref} = AV_{CC} = 2.2$ V AN0 to AN11 input          | –        | –    | $\pm 5$          | LSB           |
|                   |                                     |             | $V_{ref} = AV_{CC} = 1.8$ V AN0 to AN11 input          | –        | –    | $\pm 5$          | LSB           |
|                   |                                     | 8-bit mode  | $V_{ref} = AV_{CC} = 5.0$ V AN0 to AN11 input          | –        | –    | $\pm 2$          | LSB           |
|                   |                                     |             | $V_{ref} = AV_{CC} = 2.2$ V AN0 to AN11 input          | –        | –    | $\pm 2$          | LSB           |
|                   |                                     |             | $V_{ref} = AV_{CC} = 1.8$ V AN0 to AN11 input          | –        | –    | $\pm 2$          | LSB           |
| $\phi_{AD}$       | A/D conversion clock                |             | $4.0 \leq V_{ref} = AV_{CC} \leq 5.5$ V <sup>(1)</sup> | 1        | –    | 20               | MHz           |
|                   |                                     |             | $3.2 \leq V_{ref} = AV_{CC} \leq 5.5$ V <sup>(1)</sup> | 1        | –    | 16               | MHz           |
|                   |                                     |             | $2.7 \leq V_{ref} = AV_{CC} \leq 5.5$ V <sup>(1)</sup> | 1        | –    | 10               | MHz           |
|                   |                                     |             | $1.8 \leq V_{ref} = AV_{CC} \leq 5.5$ V <sup>(1)</sup> | 1        | –    | 8                | MHz           |
| –                 | Tolerance level impedance           |             |  | –        | 3    | –                | k $\Omega$    |
| t <sub>CONV</sub> | Conversion time                     | 10-bit mode | $V_{ref} = AV_{CC} = 5.0$ V, $\phi_{AD} = 20$ MHz      | 2.2      | –    | –                | $\mu\text{s}$ |
|                   |                                     | 8-bit mode  | $V_{ref} = AV_{CC} = 5.0$ V, $\phi_{AD} = 20$ MHz      | 2.2      | –    | –                | ms            |
| t <sub>SAMP</sub> | Sampling time                       |             | $\phi_{AD} = 20$ MHz                                   | 0.8      | –    | –                | $\mu\text{s}$ |
| I <sub>Vref</sub> | V <sub>ref</sub> current            |             | $V_{CC} = 5$ V, XIN = f1 = $\phi_{AD} = 20$ MHz        | –        | 45   | –                | $\mu\text{A}$ |
| V <sub>ref</sub>  | Reference voltage                   |             |  | 1.8      | –    | AV <sub>CC</sub> | V             |
| V <sub>IA</sub>   | Analog input voltage <sup>(3)</sup> |             |  | 0        | –    | V <sub>ref</sub> | V             |
| OCVREF            | On-chip reference voltage           |             | $2 \text{ MHz} \leq \phi_{AD} \leq 4 \text{ MHz}$      | 1.53     | 1.70 | 1.87             | V             |

Notes:

1. The A/D conversion result will be undefined in wait mode, stop mode, power-off mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
2. This applies when the peripheral functions are stopped.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

**Table 5.33 Temperature Sensor Characteristics**  
( $V_{SS} = 0$  V and  $T_{opr} = -20$  to  $85^{\circ}\text{C}$  (N version)/  $-40$  to  $85^{\circ}\text{C}$  (D version), unless otherwise specified.)

| Symbol           | Parameter                         | Conditions   | Standard |      |      | Unit                   |
|------------------|-----------------------------------|--|----------|------|------|------------------------|
|                  |                                   |  | Min.     | Typ. | Max. |                        |
| V <sub>TMP</sub> | Temperature sensor output voltage | $1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$<br>$\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$<br>Ambient temperature = $25^{\circ}\text{C}$ | 550      | 600  | 650  | mV                     |
| –                | Temperature coefficient           | $1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$<br>$\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$<br>Ambient temperature = $25^{\circ}\text{C}$ | –        | –2.1 | –    | mV/ $^{\circ}\text{C}$ |
| –                | Start-up time                     | $1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$<br>$\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$   | –        | –    | 200  | $\mu\text{s}$          |
| I <sub>TMP</sub> | Operating current                 | $1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$<br>$\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$   | –        | 100  | –    | $\mu\text{A}$          |

**Table 5.34 Gain Amplifier Characteristics**  
(VSS = 0 V and Topr = -20 to 85 °C (N version)/-40 to 85 °C (D version), unless otherwise specified.)

| Symbol | Parameter                      | Conditions | Standard |      |            | Unit |
|--------|--------------------------------|------------|----------|------|------------|------|
|        |                                |            | Min.     | Typ. | Max.       |      |
| VGAIN  | Gain amplifier operating range |            | 0.4      | -    | AVCC - 1.0 | V    |
| φAD    | A/D conversion clock           |            | 1        | -    | 5          | MHz  |

**Table 5.35 Comparator B Characteristics**  
(VCC = 1.8 to 5.5 V and Topr = -20 to 85°C (N version)/-40 to 85°C (D version), unless otherwise specified.)

| Symbol | Parameter                                   | Condition          | Standard |      |           | Unit |
|--------|---|--------------------|----------|------|-----------|------|
|        |   |                    | Min.     | Typ. | Max.      |      |
| Vref   | IVREF1, IVREF3 input reference voltage      |                    | 0        | -    | VCC - 1.4 | V    |
| Vi     | IVCMP1, IVCMP3 input voltage                |                    | -0.3     | -    | VCC + 0.3 | V    |
| -      | Offset                                      |                    | -        | 5    | 100       | mV   |
| td     | Comparator output delay time <sup>(1)</sup> | Vi = Vref ± 100 mV | -        | -    | 1         | μs   |
| ICMP   | Comparator operating current                | VCC = 5.0 V        | -        | 12   | -         | μA   |

Note:

1. When the digital filter is disabled.

**Table 5.36 Flash Memory (Program ROM) Characteristics**  
(VCC = 1.8 to 5.5 V and Topr = 0 to 60°C, unless otherwise specified.)

| Symbol           | Parameter  | Conditions   | Standard              |      |                                | Unit  |
|------------------|--|--|-----------------------|------|--------------------------------|-------|
|                  |  |  | Min.                  | Typ. | Max.                           |       |
| -                | Program/erase endurance <sup>(1)</sup>                                 |  | 10,000 <sup>(2)</sup> | -    | -                              | times |
| -                | Byte program time  |  | -                     | 80   | -                              | μs    |
| -                | Block erase time   | Internal ROM Capacity:<br>16 KB, 32 KB, 48 KB, 64 KB | -                     | 0.12 | -                              | s     |
| -                |  | Internal ROM Capacity:<br>96 KB, 128 KB              | -                     | 0.2  | -                              | s     |
| td(SR-SUS)       | Time delay from suspend request until suspend                          |  | -                     | -    | 0.25 + CPU clock<br>× 3 cycles | ms    |
| -                | Time from suspend until erase restart                                  |  | -                     | -    | 30 + CPU clock<br>× 1 cycle    | μs    |
| td(CMDRST-READY) | Time from when command is forcibly terminated until reading is enabled |  | -                     | -    | 30 + CPU clock<br>× 1 cycle    | μs    |
| -                | Program, erase voltage   |  | 1.8                   | -    | 5.5                            | V     |
| -                | Read voltage   |  | 1.8                   | -    | 5.5                            | V     |
| -                | Program, erase temperature   |  | 0                     | -    | 60                             | °C    |
| -                | Data hold time <sup>(6)</sup>  | Ambient temperature = 85°C                           | 10                    | -    | -                              | year  |

Notes:

1. Definition of programming/erasure endurance  
The programming and erasure endurance is defined on a per-block basis.  
If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.  
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

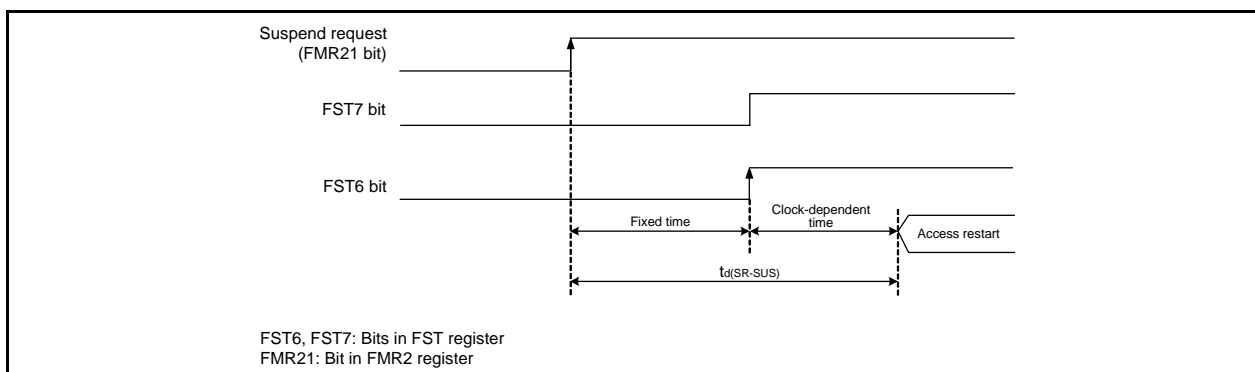


**Table 5.37 Flash Memory (Data flash Block A and Block B) Characteristics**  
**(V<sub>CC</sub> = 1.8 to 5.5 V and T<sub>opr</sub> = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)**

| Symbol                        | Parameter  | Conditions                         | Standard      |       |                                | Unit  |
|-------------------------------|--|------------------------------------|---------------|-------|--------------------------------|-------|
|                               |  |                                    | Min.          | Typ.  | Max.                           |       |
| –                             | Program/erase endurance (1)  |                                    | 10,000<br>(2) | –     | –                              | times |
| –                             | Byte program time<br>(program/erase endurance ≤ 10,000 times)          |                                    | –             | 150   | –                              | μs    |
| –                             | Block erase time<br>(program/erase endurance ≤ 10,000 times)           | Internal ROM Capacity:<br>1 KB × 2 | –             | 0.05  | 1                              | s     |
|                               |  | Internal ROM Capacity:<br>2 KB × 2 | –             | 0.055 | 1                              | s     |
| t <sub>d</sub> (SR-SUS)       | Time delay from suspend request until suspend                          |                                    | –             | –     | 0.25 + CPU clock<br>× 3 cycles | ms    |
| –                             | Time from suspend until erase restart                                  |                                    | –             | –     | 30 + CPU clock<br>× 1 cycle    | μs    |
| t <sub>d</sub> (CMDRST-READY) | Time from when command is forcibly terminated until reading is enabled |                                    | –             | –     | 30 + CPU clock<br>× 1 cycle    | μs    |
| –                             | Program, erase voltage   |                                    | 1.8           | –     | 5.5                            | V     |
| –                             | Read voltage   |                                    | 1.8           | –     | 5.5                            | V     |
| –                             | Program, erase temperature   |                                    | –20 (6)       | –     | 85                             | °C    |
| –                             | Data hold time (7)   | Ambient temperature = 85<br>°C     | 10            | –     | –                              | year  |

## Notes:

- Definition of programming/erasure endurance  
 The programming and erasure endurance is defined on a per-block basis.  
 If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.  
 However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 40°C for D version.
- The data hold time includes time that the power supply is off or the clock is not supplied.



**Figure 5.13 Time delay until Suspend**

**Table 5.38 Voltage Detection 0 Circuit Characteristics**  
(V<sub>CC</sub> = 1.8 to 5.5 V and T<sub>opr</sub> = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

| Symbol              | Parameter   | Condition                          | Standard  |      |      | Unit |     |    |
|---------------------|---|------------------------------------|---|------|------|------|-----|----|
|                     |   |                                    | Min.  | Typ. | Max. |      |     |    |
| V <sub>det0</sub>   | Voltage detection level V <sub>det0_0</sub> (1)                   |                                    | 1.8   | 1.90 | 2.05 | V    |     |    |
|                     | Voltage detection level V <sub>det0_1</sub> (1)                   |                                    | 2.15  | 2.35 | 2.50 | V    |     |    |
|                     | Voltage detection level V <sub>det0_2</sub> (1)                   |                                    | 2.70  | 2.85 | 3.05 | V    |     |    |
|                     | Voltage detection level V <sub>det0_3</sub> (1)                   |                                    | 3.55  | 3.80 | 4.05 | V    |     |    |
| –                   | Voltage detection 0 circuit response time (3)                     | In operation                       | At the falling of V <sub>CC</sub> from 5 V to (V <sub>det0_0</sub> – 0.1) V |      | –    | 50   | 500 | μs |
|                     |   | In stop mode                       | At the falling of V <sub>CC</sub> from 5 V to (V <sub>det0_0</sub> – 0.1) V |      | –    | 100  | 500 | μs |
| –                   | Voltage detection circuit self power consumption                  | VCA25 = 1, V <sub>CC</sub> = 5.0 V |   |      | –    | 1.5  | –   | μA |
| t <sub>d(E-A)</sub> | Waiting time until voltage detection circuit operation starts (2) |                                    | –   | –    | 100  | –    | μs  |    |

Notes:

1. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
3. Time until the voltage monitor 0 reset is generated after the voltage passes V<sub>det0</sub>.

**Table 5.39 Voltage Detection 1 Circuit Characteristics**  
(V<sub>CC</sub> = 1.8 to 5.5 V and T<sub>opr</sub> = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

| Symbol              | Parameter  | Condition   | Standard  |      |      | Unit |     |    |
|---------------------|--|---|---|------|------|------|-----|----|
|                     |  |   | Min.  | Typ. | Max. |      |     |    |
| V <sub>det1</sub>   | Voltage detection level V <sub>det1_0</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 2.00  | 2.20 | 2.40 | V    |     |    |
|                     | Voltage detection level V <sub>det1_1</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 2.15  | 2.35 | 2.55 | V    |     |    |
|                     | Voltage detection level V <sub>det1_2</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 2.30  | 2.50 | 2.70 | V    |     |    |
|                     | Voltage detection level V <sub>det1_3</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 2.45  | 2.65 | 2.85 | V    |     |    |
|                     | Voltage detection level V <sub>det1_4</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 2.60  | 2.80 | 3.00 | V    |     |    |
|                     | Voltage detection level V <sub>det1_5</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 2.75  | 2.95 | 3.15 | V    |     |    |
|                     | Voltage detection level V <sub>det1_6</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 2.85  | 3.10 | 3.40 | V    |     |    |
|                     | Voltage detection level V <sub>det1_7</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 3.00  | 3.25 | 3.55 | V    |     |    |
|                     | Voltage detection level V <sub>det1_8</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 3.15  | 3.40 | 3.70 | V    |     |    |
|                     | Voltage detection level V <sub>det1_9</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 3.30  | 3.55 | 3.85 | V    |     |    |
|                     | Voltage detection level V <sub>det1_A</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 3.45  | 3.70 | 4.00 | V    |     |    |
|                     | Voltage detection level V <sub>det1_B</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 3.60  | 3.85 | 4.15 | V    |     |    |
|                     | Voltage detection level V <sub>det1_C</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 3.75  | 4.00 | 4.30 | V    |     |    |
|                     | Voltage detection level V <sub>det1_D</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 3.90  | 4.15 | 4.45 | V    |     |    |
|                     | Voltage detection level V <sub>det1_E</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 4.05  | 4.30 | 4.60 | V    |     |    |
|                     | Voltage detection level V <sub>det1_F</sub> (1)                                  | At the falling of V <sub>CC</sub>                   | 4.20  | 4.45 | 4.75 | V    |     |    |
| –                   | Hysteresis width at the rising of V <sub>CC</sub> in voltage detection 1 circuit | V <sub>det1_0</sub> to V <sub>det1_5</sub> selected | –   | 0.07 | –    | V    |     |    |
|                     |  | V <sub>det1_6</sub> to V <sub>det1_F</sub> selected | –   | 0.10 | –    | V    |     |    |
| –                   | Voltage detection 1 circuit response time (2)                                    | In operation  | At the falling of V <sub>CC</sub> from 5 V to (V <sub>det1_0</sub> – 0.1) V |      | –    | 60   | 150 | μs |
|                     |  | In stop mode  | At the falling of V <sub>CC</sub> from 5 V to (V <sub>det1_0</sub> – 0.1) V |      | –    | 250  | 500 | μs |
| –                   | Voltage detection circuit self power consumption                                 | VCA26 = 1, V <sub>CC</sub> = 5.0 V                  |   |      | –    | 1.7  | –   | μA |
| t <sub>d(E-A)</sub> | Waiting time until voltage detection circuit operation starts (3)                |   | –   | –    | 100  | –    | μs  |    |

Notes:

1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V<sub>det1</sub>.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

**Table 5.40 Voltage Detection 2 Circuit Characteristics**  
( $V_{CC} = 1.8$  to  $5.5$  V and  $T_{opr} = -20$  to  $85^{\circ}\text{C}$  (N version)/  $-40$  to  $85^{\circ}\text{C}$  (D version), unless otherwise specified.)

| Symbol       | Parameter   | Condition  | Standard |      |      | Unit          |
|--------------|---|--|----------|------|------|---------------|
|              |   |  | Min.     | Typ. | Max. |               |
| $V_{det2}$   | Voltage detection level $V_{det2\_0}$ (1)                                 | At the falling of $V_{CC}$                                       | 3.70     | 4.0  | 4.30 | V             |
| –            | Hysteresis width at the rising of $V_{CC}$ in voltage detection 2 circuit |  | –        | 0.10 | –    | V             |
| –            | Voltage detection 2 circuit response time (2)                             | In operation   |          | 20   | 150  | $\mu\text{s}$ |
|              |   | At the falling of $V_{CC}$ from 5 V to ( $V_{det2\_0} - 0.1$ ) V |          |      |      |               |
| –            | Voltage detection 2 circuit response time (2)                             | In stop mode   |          | 200  | 500  | $\mu\text{s}$ |
|              |   | At the falling of $V_{CC}$ from 5 V to ( $V_{det2\_0} - 0.1$ ) V |          |      |      |               |
| –            | Voltage detection circuit self power consumption                          | $V_{CA27} = 1, V_{CC} = 5.0$ V                                   | –        | 1.7  | –    | $\mu\text{A}$ |
| $t_{d(E-A)}$ | Waiting time until voltage detection circuit operation starts (3)         |  | –        | –    | 100  | $\mu\text{s}$ |

Notes:

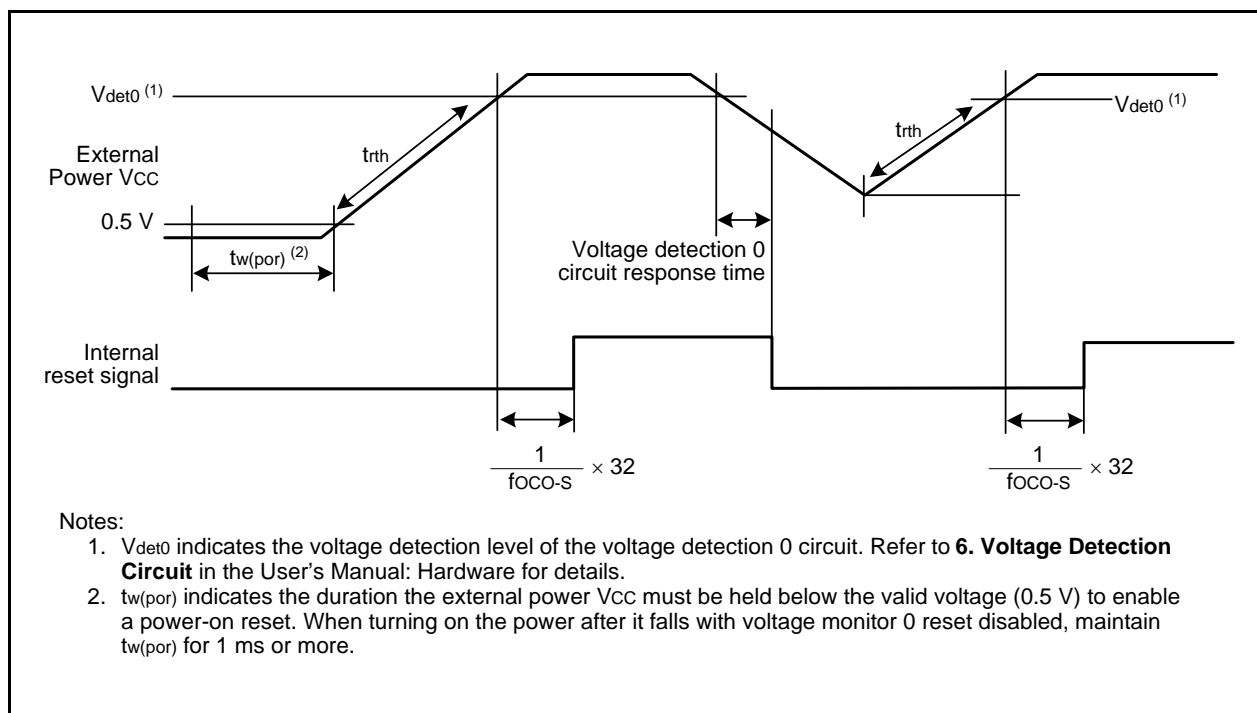
1. The voltage detection level varies with detection targets. Select the level with the  $V_{CA24}$  bit in the  $V_{CA2}$  register.
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes  $V_{det2}$ .
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the  $V_{CA27}$  bit in the  $V_{CA2}$  register to 0.

**Table 5.41 Power-on Reset Circuit Characteristics (1)**  
( $T_{opr} = -20$  to  $85^{\circ}\text{C}$  (N version)/  $-40$  to  $85^{\circ}\text{C}$  (D version), unless otherwise specified.)

| Symbol    | Parameter                             | Condition | Standard |      |       | Unit  |
|-----------|---------------------------------------|-----------|----------|------|-------|-------|
|           |                                       |           | Min.     | Typ. | Max.  |       |
| $t_{rth}$ | External power $V_{CC}$ rise gradient |           | 0        | –    | 50000 | mV/ms |

Note:

1. To use the power-on reset function, enable voltage monitor 0 reset by setting the  $LVDAS$  bit in the  $OFS$  register to 0.



**Figure 5.14 Power-on Reset Circuit Characteristics**

**Table 5.42 High-speed On-Chip Oscillator Circuit Characteristics**  
( $V_{CC} = 1.8$  to  $5.5$  V and  $T_{opr} = -20$  to  $85^{\circ}\text{C}$  (N version)/  $-40$  to  $85^{\circ}\text{C}$  (D version), unless otherwise specified.)

| Symbol | Parameter  | Condition   | Standard |        |        | Unit          |
|--------|--|---|----------|--------|--------|---------------|
|        |  |   | Min.     | Typ.   | Max.   |               |
| –      | High-speed on-chip oscillator frequency after reset  | $V_{CC} = 1.8$ V to $5.5$ V<br>$-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$ | 19.2     | 20     | 20.8   | MHz           |
|        |  | $V_{CC} = 1.8$ V to $5.5$ V<br>$-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$ | 19.0     | 20     | 21.0   | MHz           |
| –      | High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register <sup>(1)</sup> | $V_{CC} = 1.8$ V to $5.5$ V<br>$-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$ | 17.694   | 18.432 | 19.169 | MHz           |
|        |  | $V_{CC} = 1.8$ V to $5.5$ V<br>$-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$ | 17.510   | 18.432 | 19.353 | MHz           |
| –      | Oscillation stability time   |   | –        | 5      | 30     | $\mu\text{s}$ |
| –      | Self power consumption at oscillation  | $V_{CC} = 5.0$ V, $T_{opr} = 25^{\circ}\text{C}$  | –        | 530    | –      | $\mu\text{A}$ |

Note:

1. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

**Table 5.43 Low-speed On-Chip Oscillator Circuit Characteristics**  
( $V_{CC} = 1.8$  to  $5.5$  V and  $T_{opr} = -20$  to  $85^{\circ}\text{C}$  (N version)/  $-40$  to  $85^{\circ}\text{C}$  (D version), unless otherwise specified.)

| Symbol   | Parameter   | Condition  | Standard |      |      | Unit          |
|----------|---|--|----------|------|------|---------------|
|          |   |  | Min.     | Typ. | Max. |               |
| fOCO-S   | Low-speed on-chip oscillator frequency                        |  | 60       | 125  | 250  | kHz           |
| –        | Oscillation stability time                                    |  | –        | –    | 35   | $\mu\text{s}$ |
| –        | Self power consumption at oscillation                         | $V_{CC} = 5.0$ V, $T_{opr} = 25^{\circ}\text{C}$ | –        | 2    | –    | $\mu\text{A}$ |
| fOCO-WDT | Low-speed on-chip oscillator frequency for the watchdog timer |  | 60       | 125  | 250  | kHz           |
| –        | Oscillation stability time                                    |  | –        | –    | 35   | $\mu\text{s}$ |
| –        | Self power consumption at oscillation                         | $V_{CC} = 5.0$ V, $T_{opr} = 25^{\circ}\text{C}$ | –        | 2    | –    | $\mu\text{A}$ |

**Table 5.44 Power Supply Circuit Characteristics**  
( $V_{CC} = 1.8$  to  $5.5$  V,  $V_{SS} = 0$  V, and  $T_{opr} = 25^{\circ}\text{C}$ , unless otherwise specified.)

| Symbol       | Parameter   | Condition | Standard |      |      | Unit          |
|--------------|---|-----------|----------|------|------|---------------|
|              |   |           | Min.     | Typ. | Max. |               |
| $t_{d(P-R)}$ | Time for internal power supply stabilization during power-on <sup>(1)</sup> |           | –        | –    | 2000 | $\mu\text{s}$ |

Note:

1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

**Table 5.45 LCD Drive Control Circuit Characteristics**  
**(V<sub>CC</sub> = 1.8 to 5.5 V, V<sub>SS</sub> = 0 V, and T<sub>opr</sub> = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter                         | Condition  | Standard |      |         | Unit |
|--------|-----------------------------------|------------|----------|------|---------|------|
|        |                                   |            | Min.     | Typ. | Max.    |      |
| VLCD   | LCD power supply voltage          | VLCD = VL3 | 2.2      | –    | 5.5     | V    |
| VL2    | VL2 voltage                       |            | VL1      | –    | VL3     | V    |
| VL1    | VL1 voltage                       |            | 1        | –    | VL2 (2) | V    |
| f(FR)  | Frame frequency                   |            | 50       | –    | 180     | Hz   |
| ILCD   | LCD drive control circuit current |            | –        | (1)  | –       | μA   |

Notes:

1. Refer to Table 5.48 DC Characteristics (2), Table 5.50 DC Characteristics (4), and Table 5.52 DC Characteristics (6).
2. The VL1 voltage should be VCC or below.

**Table 5.46 Power-Off Mode Characteristics**  
**(V<sub>CC</sub> = 1.8 to 5.5 V, V<sub>SS</sub> = 0 V, and T<sub>opr</sub> = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter                               | Condition | Standard |      |      | Unit |
|--------|---|-----------|----------|------|------|------|
|        |   |           | Min.     | Typ. | Max. |      |
| –      | Power-off mode operating supply voltage |           | 1.8      | –    | 5.5  | V    |

## 5.2.4 DC Characteristics

**Table 5.47 DC Characteristics (1) [4.0 V ≤ V<sub>CC</sub> ≤ 5.5 V]**  
(T<sub>opr</sub> = -20 to 85°C (N version)/ -40 to 85°C (D version), unless otherwise specified.)

| Symbol                           | Parameter           |   | Condition                                   |                      |                          | Standard              |      |                 | Unit |
|----------------------------------|---------------------|---|---|----------------------|--------------------------|-----------------------|------|-----------------|------|
|                                  |                     |   |   |                      |                          | Min.                  | Typ. | Max.            |      |
| V <sub>OH</sub>                  | Output "H" voltage  |   | Port P7_0, P7_1, P8 (1)                     | V <sub>CC</sub> = 5V | I <sub>OH</sub> = -20 mA | V <sub>CC</sub> - 2.0 | -    | V <sub>CC</sub> | V    |
|                                  |                     |   | Other pins                                  | V <sub>CC</sub> = 5V | I <sub>OH</sub> = -5 mA  | V <sub>CC</sub> - 2.0 | -    | V <sub>CC</sub> | V    |
| V <sub>OL</sub>                  | Output "L" voltage  |   | Port P7_0, P7_1, P8 (1)                     | V <sub>CC</sub> = 5V | I <sub>OL</sub> = 20 mA  | -                     | -    | 2.0             | V    |
|                                  |                     |   | Other pins                                  | V <sub>CC</sub> = 5V | I <sub>OL</sub> = 5 mA   | -                     | -    | 2.0             | V    |
| V <sub>T+</sub> -V <sub>T-</sub> | Hysteresis          | $\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT2}},$<br>$\overline{\text{INT3}}, \overline{\text{INT4}}, \overline{\text{INT5}},$<br>$\overline{\text{INT6}}, \overline{\text{INT7}},$<br>$\overline{\text{KI0}}, \overline{\text{KI1}}, \overline{\text{KI2}}, \overline{\text{KI3}},$<br>$\overline{\text{KI4}}, \overline{\text{KI5}}, \overline{\text{KI6}}, \overline{\text{KI7}},$<br>TRCIOA, TRCIOB,<br>TRCIOC, TRCIOD,<br>TRJ0IO, TRJ1IO,<br>TRJ2IO, TRCTRG,<br>TRCCLK, ADTRG,<br>RXD0, RXD2, CLK0,<br>CLK2, SSI, SCL,<br>SDA, SSO |   |                      |                          | 0.05                  | 0.5  | -               | V    |
|                                  |                     | $\overline{\text{RESET}}, \overline{\text{WKUP0}}$  |   |                      |                          | 0.1                   | 0.8  | -               | V    |
| I <sub>IH</sub>                  | Input "H" current   |   | V <sub>I</sub> = 5 V, V <sub>CC</sub> = 5 V |                      |                          | -                     | -    | 5.0             | μA   |
| I <sub>IL</sub>                  | Input "L" current   |   | V <sub>I</sub> = 0 V, V <sub>CC</sub> = 5 V |                      |                          | -                     | -    | -5.0            | μA   |
| R <sub>PULLUP</sub>              | Pull-up resistance  |   | V <sub>I</sub> = 0 V, V <sub>CC</sub> = 5 V |                      |                          | 20                    | 40   | 80              | kΩ   |
| R <sub>iXIN</sub>                | Feedback resistance | XIN   |   |                      |                          | -                     | 2.0  | -               | MΩ   |
| R <sub>iXCIN</sub>               | Feedback resistance | XCIN  |   |                      |                          | -                     | 14   | -               | MΩ   |
| V <sub>RAM</sub>                 | RAM hold voltage    |   | During stop mode                            |                      |                          | 1.8                   | -    | -               | V    |

Note:

1. This applies when the drive capacity of the output transistor is set to High by registers P7DRR and P8DRR. When the drive capacity is set to Low, the value of any other pin applies.

**Table 5.48 DC Characteristics (2) [4.0 V ≤ Vcc ≤ 5.5 V]  
(Topr = −20 to 85°C (N version)/ −40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter                |                                    | Condition           |        |                    |           |              |  |  | Standard   |             |      | Unit |    |
|--------|--------------------------|------------------------------------|---------------------|--------|--------------------|-----------|--------------|--|--|--|-------------|------|------|----|
|        |                          |                                    | Oscillation Circuit |        | On-Chip Oscillator |           | CPU Clock    | Low-Power-Consumption Setting  | Other  | Min.   | Typ.<br>(3) | Max. |      |    |
|        |                          |                                    | XIN (2)             | XCIN   | High-Speed         | Low-Speed |              |  |  |  |             |      |      |    |
| Icc    | Power supply current (1) | High-speed clock mode              | 20 MHz              | Off    | Off                | 125 kHz   | No division  | –  |  | –  | 4.7         | 10   | mA   |    |
|        |                          |                                    | 16 MHz              | Off    | Off                | 125 kHz   | No division  | –  |  | –  | 3.9         | 8    | mA   |    |
|        |                          |                                    | 10 MHz              | Off    | Off                | 125 kHz   | No division  | –  |  | –  | 2.3         | –    | mA   |    |
|        |                          |                                    | 20 MHz              | Off    | Off                | Off       | No division  | FMR27 = 1<br>MSTCR0 = BEh<br>MSTCR1 = 3Fh                                | Flash memory off<br>Program operation on RAM<br>Module standby setting enabled                             | –  | 3.1         | –    | mA   |    |
|        |                          |                                    | 20 MHz              | Off    | Off                | 125 kHz   | Divide-by-8  | –  |  | –  | 1.8         | –    | mA   |    |
|        |                          |                                    | 16 MHz              | Off    | Off                | 125 kHz   | Divide-by-8  | –  |  | –  | 1.5         | –    | mA   |    |
|        |                          | High-speed on-chip oscillator mode | 10 MHz              | Off    | Off                | 125 kHz   | Divide-by-8  | –  |  | –  | 1.0         | –    | mA   |    |
|        |                          |                                    | Off                 | Off    | 20 MHz             | 125 kHz   | No division  | –  |  | –  | 5.0         | 11   | mA   |    |
|        |                          |                                    | Off                 | Off    | 20 MHz             | 125 kHz   | Divide-by-8  | –  |  | –  | 2.1         | –    | mA   |    |
|        |                          | Low-speed on-chip oscillator mode  | Off                 | Off    | 4 MHz              | 125 kHz   | Divide-by-16 | MSTCR0 = BEh<br>MSTCR1 = 3Fh   |  | –  | 0.9         | –    | mA   |    |
|        |                          |                                    | Off                 | Off    | Off                | 125 kHz   | No division  | FMR27 = 1<br>VCA20 = 0   |  | –  | 110         | 320  | μA   |    |
|        |                          | Low-speed clock mode               | Off                 | Off    | Off                | 125 kHz   | Divide-by-8  | FMR27 = 1<br>VCA20 = 0   |  | –  | 63          | 220  | μA   |    |
|        |                          |                                    | Off                 | 32 kHz | Off                | Off       | No division  | FMR27 = 1<br>VCA20 = 0   |  | –  | 60          | 220  | μA   |    |
|        |                          | Wait mode                          | Off                 | 32 kHz | Off                | Off       | No division  | FMSTP = 1<br>VCA20 = 0   | Flash memory off<br>Program operation on RAM   | –  | 46          | –    | μA   |    |
|        |                          |                                    | Off                 | Off    | Off                | 125 kHz   | –            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1                         | While a WAIT instruction is executed<br>Peripheral clock operation   | –  | 9.0         | 50   | μA   |    |
|        |                          | Stop mode                          | Off                 | Off    | Off                | 125 kHz   | –            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | While a WAIT instruction is executed<br>Peripheral clock off   | –  | 2.8         | 33   | μA   |    |
|        |                          |                                    | Off                 | 32 kHz | Off                | Off       | –            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 0 | While a WAIT instruction is executed<br>Peripheral clock off<br>Timer RH operation in real-time clock mode | LCD drive control circuit (4)<br>When external division resistors are used | –           | 4.6  | –    | μA |
|        |                          |                                    | Off                 | 32 kHz | Off                | Off       | –            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | While a WAIT instruction is executed<br>Peripheral clock off<br>Timer RH operation in real-time clock mode | –  | 2.4         | –    | μA   |    |
|        |                          |                                    | Off                 | Off    | Off                | Off       | –            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM10 = 1             | Topr = 25°C<br>Peripheral clock off  | –  | 0.5         | 2.2  | μA   |    |
|        |                          | Power-off mode                     | Off                 | Off    | Off                | Off       | –            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM10 = 1             | Topr = 85°C<br>Peripheral clock off  | –  | 1.2         | –    | μA   |    |
|        |                          |                                    | Off                 | Off    | Off                | Off       | –            | –  | Power-off 0<br>Topr = 25°C   | –  | 0.01        | 0.1  | μA   |    |
|        |                          |                                    | Off                 | Off    | Off                | Off       | –            | –  | Power-off 0<br>Topr = 85°C   | –  | 0.03        | –    | μA   |    |
|        |                          |                                    | Off                 | 32 kHz | Off                | Off       | –            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1                          | Power-off 2<br>Topr = 25°C   | –  | 1.8         | 6.4  | μA   |    |
|        |                          |                                    | Off                 | 32 kHz | Off                | Off       | –            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM10 = 1             | Power-off 2<br>Topr = 85°C   | –  | 2.7         | –    | μA   |    |

## Notes:

- Vcc = 4.0 V to 5.5 V, single chip mode, output pins are open, and other pins are Vss.
- XIN is set to square wave input.
- Vcc = 5.0 V
- VLCD = Vcc, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG39 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

**Table 5.49 DC Characteristics (3) [2.7 V ≤ V<sub>CC</sub> < 4.0 V]**  
**(T<sub>opr</sub> = -20 to 85°C (N version)/ -40 to 85°C (D version), unless otherwise specified.)**

| Symbol                           | Parameter           |   | Condition                                   |                         | Standard              |      |                 | Unit |
|----------------------------------|---------------------|---|---|-------------------------|-----------------------|------|-----------------|------|
|                                  |                     |   |   |                         | Min.                  | Typ. | Max.            |      |
| V <sub>OH</sub>                  | Output "H" voltage  |   | Port P7_0, P7_1, P8 (1)                     | I <sub>OH</sub> = -5 mA | V <sub>CC</sub> - 0.5 | -    | V <sub>CC</sub> | V    |
|                                  |                     |   | Other pins                                  | I <sub>OH</sub> = -1 mA | V <sub>CC</sub> - 0.5 | -    | V <sub>CC</sub> | V    |
| V <sub>OL</sub>                  | Output "L" voltage  |   | Port P7_0, P7_1, P8 (1)                     | I <sub>OL</sub> = 5 mA  | -                     | -    | 0.5             | V    |
|                                  |                     |   | Other pins                                  | I <sub>OL</sub> = 1 mA  | -                     | -    | 0.5             | V    |
| V <sub>T+</sub> -V <sub>T-</sub> | Hysteresis          | $\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT2}},$<br>$\overline{\text{INT3}}, \overline{\text{INT4}}, \overline{\text{INT5}},$<br>$\overline{\text{INT6}}, \overline{\text{INT7}},$<br>$\overline{\text{KI0}}, \overline{\text{KI1}}, \overline{\text{KI2}}, \overline{\text{KI3}},$<br>$\overline{\text{KI4}}, \overline{\text{KI5}}, \overline{\text{KI6}}, \overline{\text{KI7}},$<br>TRCIOA, TRCIOB,<br>TRCIOC, TRCIOD,<br>TRJ0IO, TRJ1IO,<br>TRJ2IO, TRCTRG,<br>TRCCLK, ADTRG,<br>RXD0, RXD2, CLK0,<br>CLK2, SSI, SCL,<br>SDA, SSO |   |                         | 0.05                  | 0.4  | -               | V    |
|                                  |                     | RESET, WKUP0  |   |                         | 0.1                   | 0.8  | -               | V    |
| I <sub>IH</sub>                  | Input "H" current   |   | V <sub>I</sub> = 3 V, V <sub>CC</sub> = 3 V |                         | -                     | -    | 5.0             | μA   |
| I <sub>IL</sub>                  | Input "L" current   |   | V <sub>I</sub> = 0 V, V <sub>CC</sub> = 3 V |                         | -                     | -    | -5.0            | μA   |
| R <sub>PULLUP</sub>              | Pull-up resistance  |   | V <sub>I</sub> = 0 V, V <sub>CC</sub> = 3 V |                         | 25                    | 80   | 140             | kΩ   |
| R <sub>iXIN</sub>                | Feedback resistance | XIN   |   |                         | -                     | 2.0  | -               | MΩ   |
| R <sub>iXCIN</sub>               | Feedback resistance | XCIN  |   |                         | -                     | 14   | -               | MΩ   |
| V <sub>RAM</sub>                 | RAM hold voltage    |   | During stop mode                            |                         | 1.8                   | -    | -               | V    |

Note:

1. This applies when the drive capacity of the output transistor is set to High by registers P7DRR and P8DRR. When the drive capacity is set to Low, the value of any other pin applies.



**Table 5.50 DC Characteristics (4) [2.7 V ≤ V<sub>CC</sub> < 4.0 V]**  
**(T<sub>opr</sub> = -20 to 85°C (N version)/ -40 to 85°C (D version), unless otherwise specified.)**

| Symbol          | Parameter                         | Condition                          | Oscillation Circuit |      |         |   | On-Chip Oscillator   |  | CPU Clock  | Low-Power-Consumption Setting | Other | Standard |      |    | Unit |
|-----------------|-----------------------------------|------------------------------------|---------------------|------|---------|---|--|--|--|-------------------------------|-------|----------|------|----|------|
|                 |                                   |                                    | XIN (2)             |      | XCIN    | High-Speed                                      | Low-Speed  | Min.   |  |                               |       | Typ. (3) | Max. |    |      |
|                 |                                   |                                    | XIN                 | XCIN |         |   |  |  |  |                               |       |          |      |    |      |
| I <sub>CC</sub> | Power supply current (1)          | High-speed clock mode              | 20 MHz              | Off  | Off     | 125 kHz   | No division  |  | –  | –                             | –     |          |      | –  | 4.7  |
|                 |                                   |                                    | 10 MHz              | Off  | Off     | 125 kHz   | No division  | –  | –  | –                             | –     | 2.3      | 6    | mA |      |
|                 |                                   |                                    | 20 MHz              | Off  | Off     | Off   | No division  | FMR27 = 1<br>MSTCR0 = BEh<br>MSTCR1 = 3Fh  | Flash memory off<br>Program operation on RAM<br>Module standby setting enabled | –                             | –     | –        | 2.9  | –  | mA   |
|                 |                                   |                                    | 20 MHz              | Off  | Off     | 125 kHz   | Divide-by-8  | –  | –  | –                             | –     | –        | 1.8  | –  | mA   |
|                 |                                   |                                    | 10 MHz              | Off  | Off     | 125 kHz   | Divide-by-8  | –  | –  | –                             | –     | –        | 1.0  | –  | mA   |
|                 |                                   | High-speed on-chip oscillator mode | Off                 | Off  | 20 MHz  | 125 kHz   | No division  | –  | –  | –                             | –     | –        | 5.0  | 11 | mA   |
|                 |                                   |                                    | Off                 | Off  | 20 MHz  | 125 kHz   | Divide-by-8  | –  | –  | –                             | –     | –        | 2.1  | –  | mA   |
|                 |                                   |                                    | Off                 | Off  | 10 MHz  | 125 kHz   | No division  | –  | –  | –                             | –     | –        | 2.9  | –  | mA   |
|                 |                                   |                                    | Off                 | Off  | 10 MHz  | 125 kHz   | Divide-by-8  | –  | –  | –                             | –     | –        | 1.5  | –  | mA   |
|                 |                                   |                                    | Off                 | Off  | 4 MHz   | 125 kHz   | Divide-by-16   | MSTCR0 = BEh<br>MSTCR1 = 3Fh   | –  | –                             | –     | –        | 0.9  | –  | mA   |
|                 | Low-speed on-chip oscillator mode | Off                                | Off                 | Off  | 125 kHz | No division                                     | FMR27 = 1<br>VCA20 = 0   | –  | –  | –                             | –     | 106      | 300  | μA |      |
|                 |                                   | Off                                | Off                 | Off  | 125 kHz | Divide-by-8                                     | FMR27 = 1<br>VCA20 = 0   | –  | –  | –                             | –     | 54       | 200  | μA |      |
|                 | Low-speed clock mode              | Off                                | 32 kHz              | Off  | Off     | No division                                     | FMR27 = 1<br>VCA20 = 0   | –  | –  | –                             | –     | 54       | 200  | μA |      |
|                 |                                   | Off                                | 32 kHz              | Off  | Off     | No division                                     | FMSTP = 1<br>VCA20 = 0   | Flash memory off<br>Program operation on RAM   | –  | –                             | –     | 36       | –    | μA |      |
|                 | Wait mode                         | Off                                | Off                 | Off  | 125 kHz | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1                         | While a WAIT instruction is executed<br>Peripheral clock operation   | –  | –                             | –     | 9.0      | 50   | μA |      |
|                 |                                   | Off                                | Off                 | Off  | 125 kHz | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | While a WAIT instruction is executed<br>Peripheral clock off   | –  | –                             | –     | 2.5      | 31   | μA |      |
|                 |                                   | Off                                | 32 kHz              | Off  | Off     | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 0 | While a WAIT instruction is executed<br>Peripheral clock off<br>Timer RH operation in real-time clock mode | LCD drive control circuit (4)<br>When external division resistors are used     | –                             | –     | 3.1      | –    | μA |      |
|                 |                                   | Off                                | 32 kHz              | Off  | Off     | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | While a WAIT instruction is executed<br>Peripheral clock off<br>Timer RH operation in real-time clock mode | –  | –                             | –     | 1.7      | –    | μA |      |
|                 |                                   | Off                                | Off                 | Off  | Off     | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1                          | –  | –  | –                             | –     | 0.5      | 2.2  | μA |      |
|                 | Stop mode                         | Off                                | Off                 | Off  | Off     | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1                          | –  | –  | –                             | –     | 0.5      | 2.2  | μA |      |
|                 |                                   | Off                                | Off                 | Off  | Off     | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1                          | –  | –  | –                             | –     | 1.2      | –    | μA |      |
|                 | Power-off mode                    | Off                                | Off                 | Off  | Off     | –   | –  | Power-off 0<br>T <sub>opr</sub> = 25°C   | –  | –                             | –     | 0.01     | 0.1  | μA |      |
|                 |                                   | Off                                | Off                 | Off  | Off     | –   | –  | Power-off 0<br>T <sub>opr</sub> = 85°C   | –  | –                             | –     | 0.02     | –    | μA |      |
|                 |                                   | Off                                | 32 kHz              | Off  | Off     | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1                          | Power-off 2<br>T <sub>opr</sub> = 25°C   | –  | –                             | –     | 1.3      | 4.5  | μA |      |
| Off             |                                   | 32 kHz                             | Off                 | Off  | –       | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1 | Power-off 2<br>T <sub>opr</sub> = 85°C                                   | –  | –  | –                             | 2.2   | –        | μA   |    |      |

## Notes:

- V<sub>CC</sub> = 2.7 V to 4.0 V, single chip mode, output pins are open, and other pins are V<sub>SS</sub>.
- XIN is set to square wave input.
- V<sub>CC</sub> = 3.0 V
- VLCD = V<sub>CC</sub>, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG39 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

**Table 5.51 DC Characteristics (5) [1.8 V ≤ V<sub>CC</sub> < 2.7 V]**  
**(T<sub>opr</sub> = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)**

| Symbol                           | Parameter           |   | Condition                                       |                         | Standard              |      |                 | Unit |
|----------------------------------|---------------------|---|---|-------------------------|-----------------------|------|-----------------|------|
|                                  |                     |   |   |                         | Min.                  | Typ. | Max.            |      |
| V <sub>OH</sub>                  | Output "H" voltage  |   | Port P7_0, P7_1, P8 (1)                         | I <sub>OH</sub> = –2 mA | V <sub>CC</sub> – 0.5 | –    | V <sub>CC</sub> | V    |
|                                  |                     |   | Other pins                                      | I <sub>OH</sub> = –1 mA | V <sub>CC</sub> – 0.5 | –    | V <sub>CC</sub> | V    |
| V <sub>OL</sub>                  | Output "L" voltage  |   | Port P7_0, P7_1, P8 (1)                         | I <sub>OL</sub> = 2 mA  | –                     | –    | 0.5             | V    |
|                                  |                     |   | Other pins                                      | I <sub>OL</sub> = 1 mA  | –                     | –    | 0.5             | V    |
| V <sub>T+</sub> –V <sub>T–</sub> | Hysteresis          | $\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT2}},$<br>$\overline{\text{INT3}}, \overline{\text{INT4}}, \overline{\text{INT5}},$<br>$\overline{\text{INT6}}, \overline{\text{INT7}},$<br>$\overline{\text{KI0}}, \overline{\text{KI1}}, \overline{\text{KI2}}, \overline{\text{KI3}},$<br>$\overline{\text{KI4}}, \overline{\text{KI5}}, \overline{\text{KI6}}, \overline{\text{KI7}},$<br>TRCIOA, TRCIOB,<br>TRCIOC, TRCIOD,<br>TRJ0IO, TRJ1IO,<br>TRJ2IO, TRCTRG,<br>TRCCLK, ADTRG,<br>RXD0, RXD2, CLK0,<br>CLK2, SSI, SCL,<br>SDA, SSO |   |                         | 0.05                  | 0.4  | –               | V    |
|                                  |                     | RESET, WKUP0  |   |                         | 0.1                   | 0.8  | –               | V    |
| I <sub>IH</sub>                  | Input "H" current   |   | V <sub>I</sub> = 1.8 V, V <sub>CC</sub> = 1.8 V |                         | –                     | –    | 4.0             | μA   |
| I <sub>IL</sub>                  | Input "L" current   |   | V <sub>I</sub> = 0 V, V <sub>CC</sub> = 1.8 V   |                         | –                     | –    | –4.0            | μA   |
| R <sub>PULLUP</sub>              | Pull-up resistance  |   | V <sub>I</sub> = 0 V, V <sub>CC</sub> = 1.8 V   |                         | 85                    | 220  | 500             | kΩ   |
| R <sub>iXIN</sub>                | Feedback resistance | XIN   |   |                         | –                     | 2.0  | –               | MΩ   |
| R <sub>iXCIN</sub>               | Feedback resistance | XCIN  |   |                         | –                     | 14   | –               | MΩ   |
| V <sub>RAM</sub>                 | RAM hold voltage    |   | During stop mode                                |                         | 1.8                   | –    | –               | V    |

Note:

1. This applies when the drive capacity of the output transistor is set to High by registers P7DRR and P8DRR. When the drive capacity is set to Low, the value of any other pin applies.

**Table 5.52 DC Characteristics (6) [ $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$ ]**  
**( $T_{opr} = -20\text{ to }85^\circ\text{C}$  (N version)/  $-40\text{ to }85^\circ\text{C}$  (D version), unless otherwise specified.)**

| Symbol          | Parameter                |                                    | Condition           |        |                    |   |   |  |  | Standard   |          |      | Unit |    |
|-----------------|--------------------------|------------------------------------|---------------------|--------|--------------------|---|---|--|--|--|----------|------|------|----|
|                 |                          |                                    | Oscillation Circuit |        | On-Chip Oscillator |   | CPU Clock                                   | Low-Power-Consumption Setting  | Other  | Min.   | Typ. (3) | Max. |      |    |
|                 |                          |                                    | XIN (2)             | XCIN   | High-Speed         | Low-Speed                                       |   |  |  |  |          |      |      |    |
| I <sub>CC</sub> | Power supply current (1) | High-speed clock mode              | 8 MHz               | Off    | Off                | 125 kHz   | No division                                 | –  | –  | 2.1  | –        | mA   |      |    |
|                 |                          |                                    | 8 MHz               | Off    | Off                | 125 kHz   | Divide-by-8                                 | –  | –  | 0.9  | –        | mA   |      |    |
|                 |                          | High-speed on-chip oscillator mode | Off                 | Off    | 5 MHz              | 125 kHz   | No division                                 | –  | –  | 1.8  | 5        | mA   |      |    |
|                 |                          |                                    | Off                 | Off    | 5 MHz              | 125 kHz   | Divide-by-8                                 | –  | –  | 1.1  | –        | mA   |      |    |
|                 |                          |                                    | Off                 | Off    | 4 MHz              | 125 kHz   | Divide-by-16                                | MSTCR0 = BEh<br>MSTCR1 = 3Fh   | –  | –  | 0.9      | –    | mA   |    |
|                 |                          | Low-speed on-chip oscillator mode  | Off                 | Off    | Off                | 125 kHz   | No division                                 | FMR27 = 1<br>VCA20 = 0   | –  | 106  | 300      | μA   |      |    |
|                 |                          |                                    | Off                 | Off    | Off                | 125 kHz   | Divide-by-8                                 | FMR27 = 1<br>VCA20 = 0   | –  | 54   | 200      | μA   |      |    |
|                 |                          | Low-speed clock mode               | Off                 | 32 kHz | Off                | Off   | No division                                 | FMR27 = 1<br>VCA20 = 0   | –  | 54   | 200      | μA   |      |    |
|                 |                          |                                    | Off                 | 32 kHz | Off                | Off   | No division                                 | FMSTP = 1<br>VCA20 = 0   | Flash memory off<br>Program operation on RAM   | –  | 36       | –    | μA   |    |
|                 |                          | Wait mode                          | Off                 | Off    | Off                | 125 kHz   | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1                         | While a WAIT instruction is executed<br>Peripheral clock operation   | –  | 9.0      | 50   | μA   |    |
|                 |                          |                                    | Off                 | Off    | Off                | 125 kHz   | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | While a WAIT instruction is executed<br>Peripheral clock off   | –  | 2.5      | 31   | μA   |    |
|                 |                          |                                    | Off                 | 32 kHz | Off                | Off   | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 0 | While a WAIT instruction is executed<br>Peripheral clock off<br>Timer RH operation in real-time clock mode | LCD drive control circuit (4)<br>When external division resistors are used | –        | 2.4  | –    | μA |
|                 |                          |                                    | Off                 | 32 kHz | Off                | Off   | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | While a WAIT instruction is executed<br>Peripheral clock off<br>Timer RH operation in real-time clock mode | –  | 1.7      | –    | μA   |    |
|                 |                          | Stop mode                          | Off                 | Off    | Off                | Off   | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1                          | $T_{opr} = 25^\circ\text{C}$<br>Peripheral clock off   | –  | 0.5      | 2.2  | μA   |    |
|                 |                          |                                    | Off                 | Off    | Off                | Off   | –   | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1                         | $T_{opr} = 85^\circ\text{C}$<br>Peripheral clock off   | –  | 1.2      | –    | μA   |    |
|                 |                          | Power-off mode                     | Off                 | Off    | Off                | Off   | –   | –  | Power-off 0<br>$T_{opr} = 25^\circ\text{C}$  | –  | 0.01     | 0.1  | μA   |    |
| Off             | Off                      |                                    | Off                 | Off    | –                  | –   | Power-off 0<br>$T_{opr} = 85^\circ\text{C}$ | –  | 0.02   | –  | μA       |      |      |    |
| Off             | 32 kHz                   |                                    | Off                 | Off    | –                  | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1 | Power-off 2<br>$T_{opr} = 25^\circ\text{C}$ | –  | 1.2  | 4  | μA       |      |      |    |
| Off             | 32 kHz                   |                                    | Off                 | Off    | –                  | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1 | Power-off 2<br>$T_{opr} = 85^\circ\text{C}$ | –  | 2  | –  | μA       |      |      |    |

## Notes:

1.  $V_{CC} = 1.8\text{ V}$  to  $2.7\text{ V}$ , single chip mode, output pins are open, and other pins are V<sub>SS</sub>.
2. XIN is set to square wave input.
3.  $V_{CC} = 2.2\text{ V}$
4. VLCD = V<sub>CC</sub>, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG39 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

## 5.2.5 AC Characteristics

**Table 5.53 Timing Requirements of Synchronous Serial Communication Unit (SSU)**  
( $V_{CC} = 1.8$  to  $5.5$  V,  $V_{SS} = 0$  V, and  $T_{opr} = -20$  to  $85^{\circ}\text{C}$  (N version)/  $-40$  to  $85^{\circ}\text{C}$  (D version), unless otherwise specified.)

| Symbol | Parameter                          |        | Conditions                                   | Standard            |      |                        | Unit          |
|--------|------------------------------------|--------|--|---------------------|------|------------------------|---------------|
|        |                                    |        |  | Min.                | Typ. | Max.                   |               |
| tsucyc | SSCK clock cycle time              |        |  | 4                   | –    | –                      | tcyc (1)      |
| tHI    | SSCK clock “H” width               |        |  | 0.4                 | –    | 0.6                    | tsucyc        |
| tLO    | SSCK clock “L” width               |        |  | 0.4                 | –    | 0.6                    | tsucyc        |
| trISE  | SSCK clock rising time             | Master |  | –                   | –    | 1                      | tcyc (1)      |
|        |                                    | Slave  |  | –                   | –    | 1                      | $\mu\text{s}$ |
| tFALL  | SSCK clock falling time            | Master |  | –                   | –    | 1                      | tcyc (1)      |
|        |                                    | Slave  |  | –                   | –    | 1                      | $\mu\text{s}$ |
| tsu    | SSO, SSI data input setup time     |        |  | 100                 | –    | –                      | ns            |
| tH     | SSO, SSI data input hold time      |        |  | 1                   | –    | –                      | tcyc (1)      |
| tLEAD  | $\overline{\text{SCS}}$ setup time | Slave  |  | $1\text{tcyc} + 50$ | –    | –                      | ns            |
| tLAG   | $\overline{\text{SCS}}$ hold time  | Slave  |  | $1\text{tcyc} + 50$ | –    | –                      | ns            |
| tOD    | SSO, SSI data output delay time    |        |  | –                   | –    | $1\text{tcyc} + 20$    | ns            |
| tSA    | SSI slave access time              |        | $2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ | –                   | –    | $1.5\text{tcyc} + 100$ | ns            |
|        |                                    |        | $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$    | –                   | –    | $1.5\text{tcyc} + 200$ | ns            |
| tOR    | SSI slave out open time            |        | $2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ | –                   | –    | $1.5\text{tcyc} + 100$ | ns            |
|        |                                    |        | $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$    | –                   | –    | $1.5\text{tcyc} + 200$ | ns            |

Note:

1.  $1\text{tcyc} = 1/f_1(\text{s})$

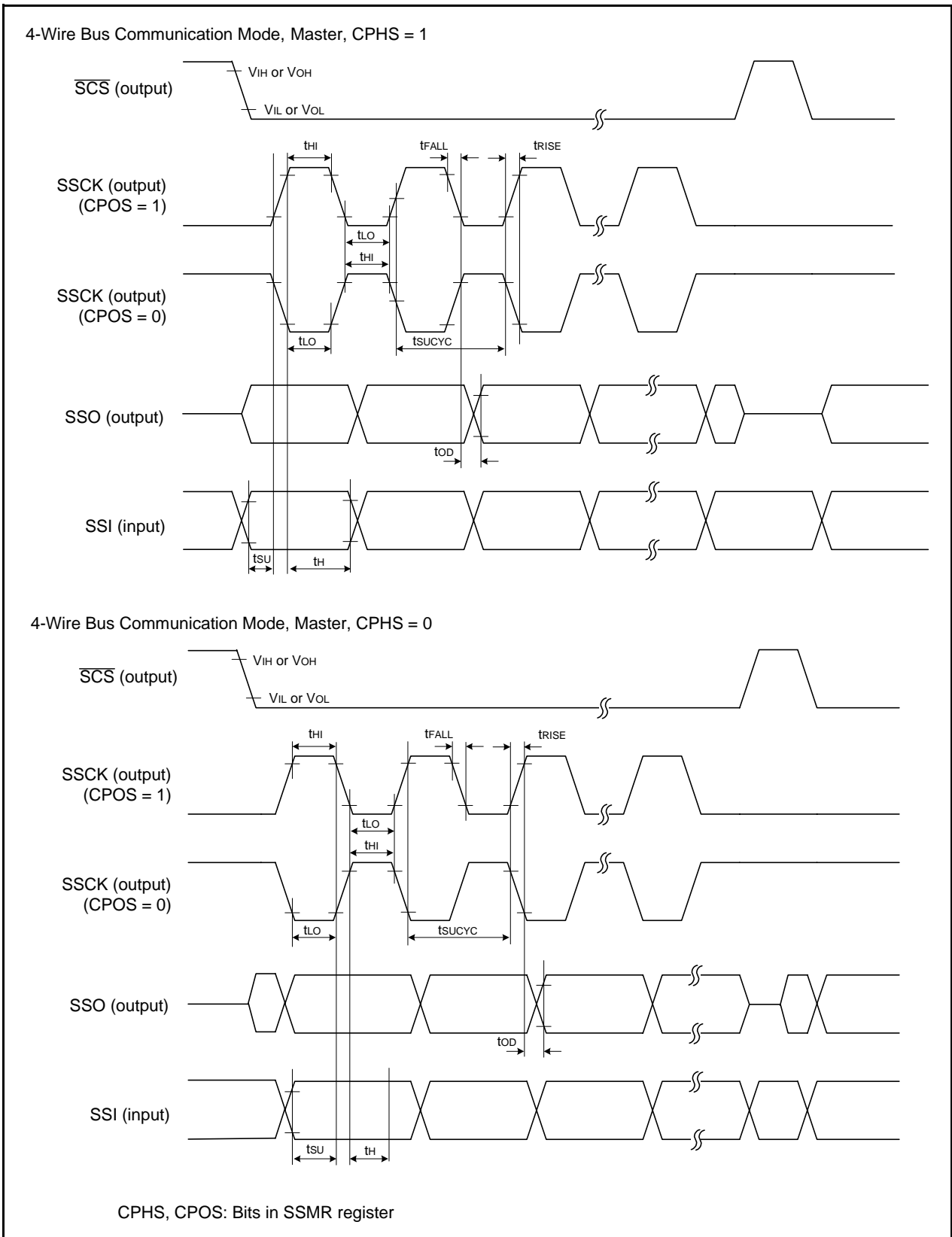


Figure 5.15 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

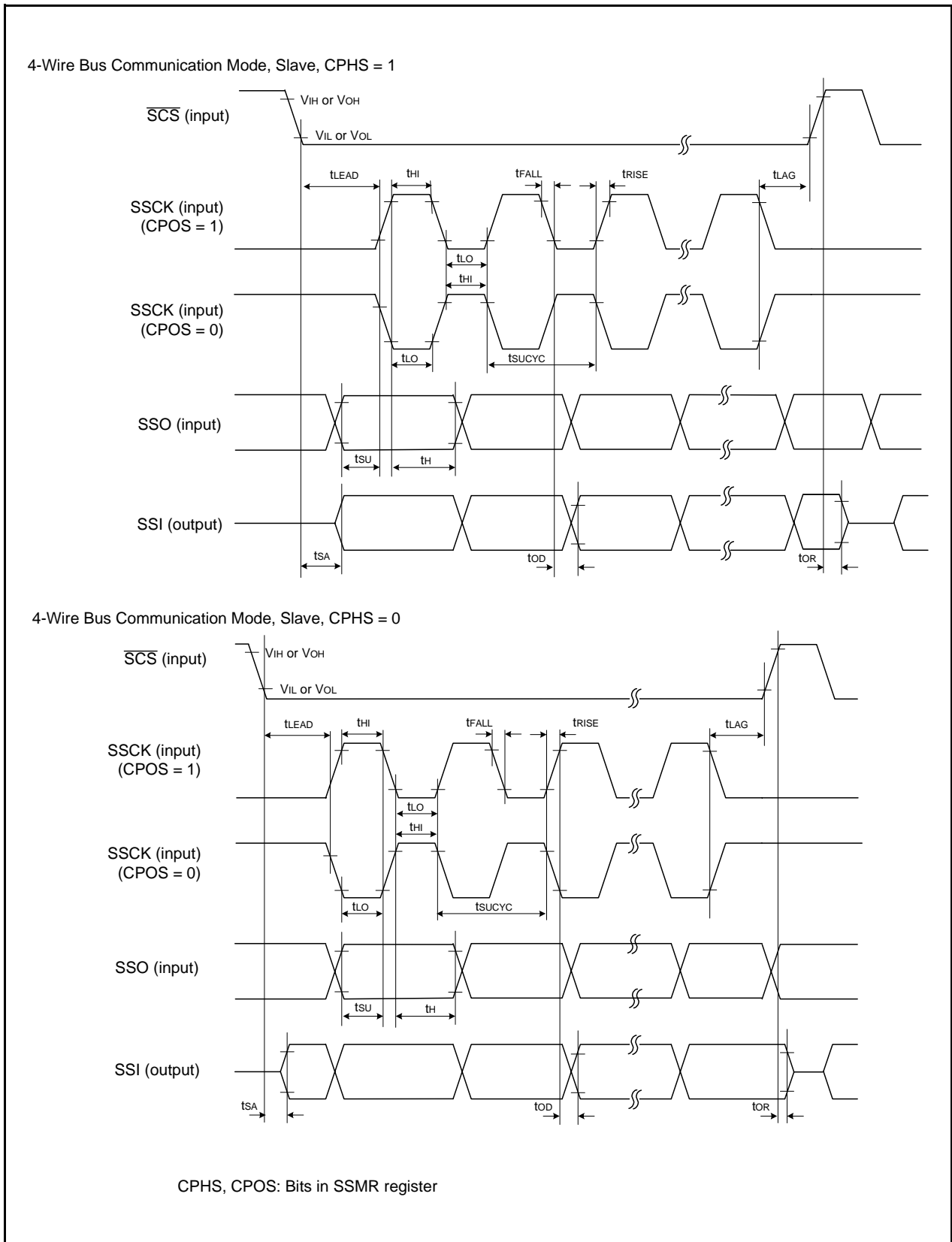


Figure 5.16 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

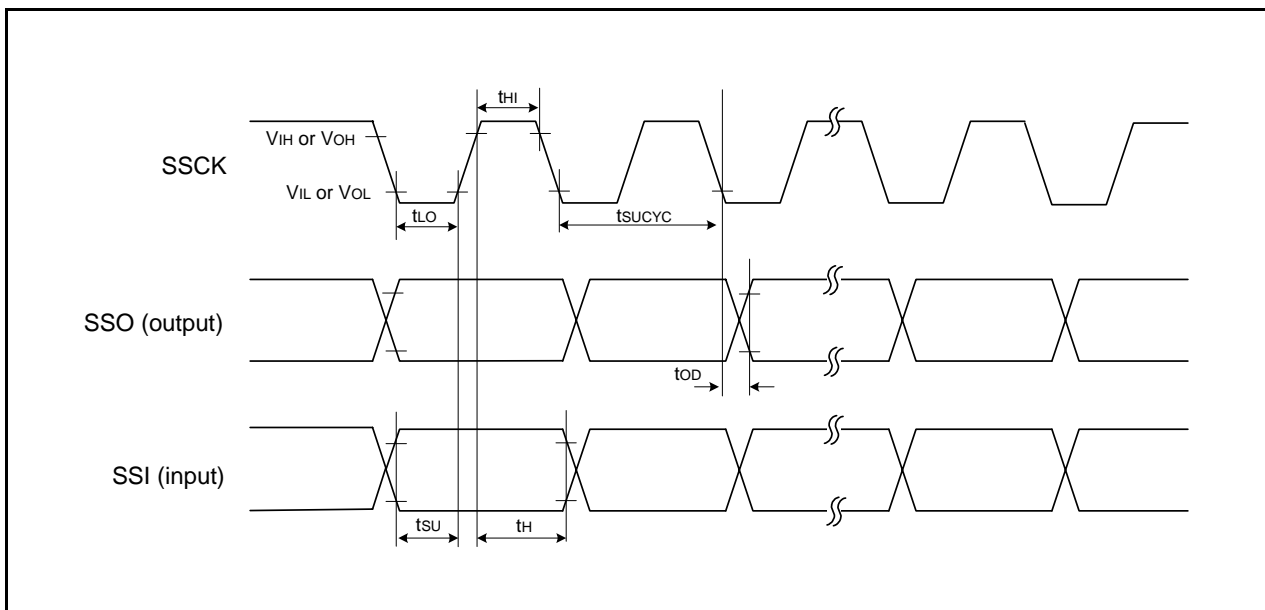


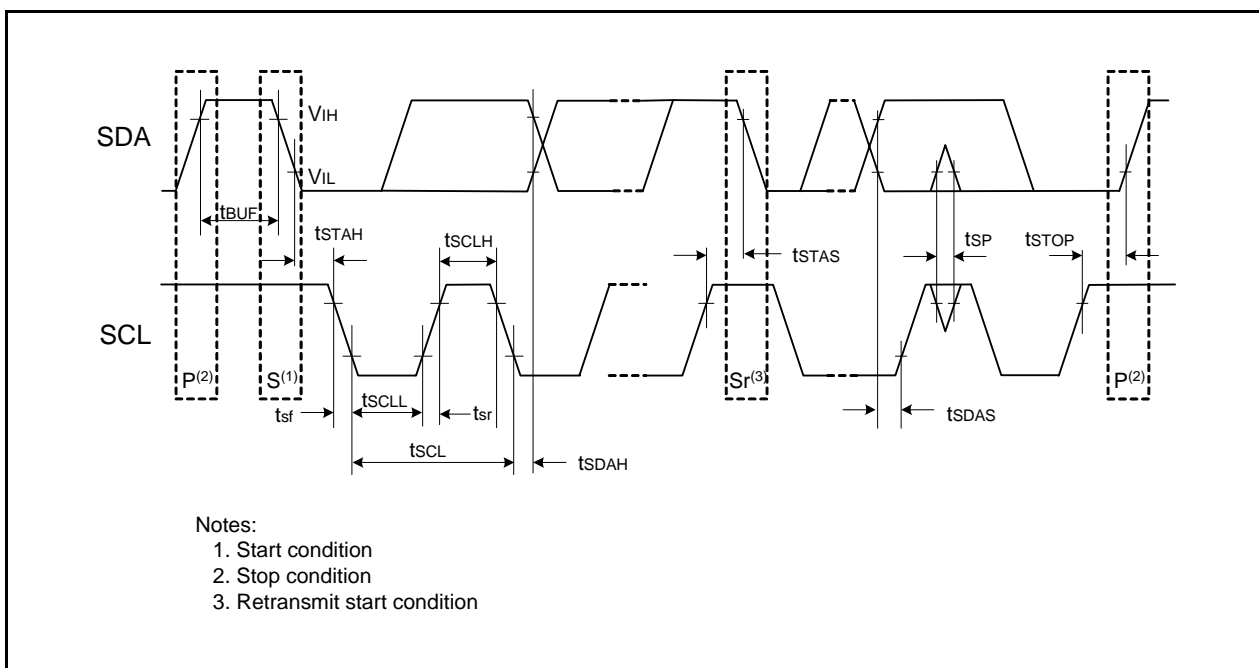
Figure 5.17 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

**Table 5.54 Timing Requirements of I<sup>2</sup>C bus Interface (1)**  
**(V<sub>CC</sub> = 1.8 to 5.5 V, V<sub>SS</sub> = 0 V, and T<sub>opr</sub> = -20 to 85°C (N version)/ -40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter                                   | Condition | Standard         |      |           | Unit |
|--------|---|-----------|------------------|------|-----------|------|
|        |   |           | Min.             | Typ. | Max.      |      |
| tSCL   | SCL input cycle time                        |           | 12tcyc + 600 (1) | –    | –         | ns   |
| tSCLH  | SCL input “H” width                         |           | 3tcyc + 300 (1)  | –    | –         | ns   |
| tSCLL  | SCL input “L” width                         |           | 5tcyc + 500 (1)  | –    | –         | ns   |
| tsf    | SCL, SDA input fall time                    |           | –                | –    | 300       | ns   |
| tSP    | SCL, SDA input spike pulse rejection time   |           | –                | –    | 1tcyc (1) | ns   |
| tBUF   | SDA input bus-free time                     |           | 5tcyc (1)        | –    | –         | ns   |
| tSTAH  | Start condition input hold time             |           | 3tcyc (1)        | –    | –         | ns   |
| tSTAS  | Retransmit start condition input setup time |           | 3tcyc (1)        | –    | –         | ns   |
| tSTOP  | Stop condition input setup time             |           | 3tcyc (1)        | –    | –         | ns   |
| tSDAS  | Data input setup time                       |           | 1tcyc + 40 (1)   | –    | –         | ns   |
| tSDAH  | Data input hold time                        |           | 10               | –    | –         | ns   |

Note:

- 1tcyc = 1/f1(s)

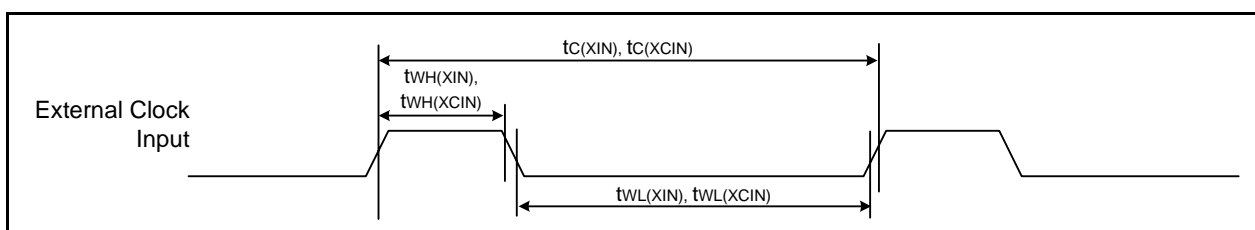


**Figure 5.18 I/O Timing of I<sup>2</sup>C bus Interface**



**Table 5.55 Timing Requirements of External Clock Input (XIN, XCIN)**  
( $V_{SS} = 0\text{ V}$  and  $T_{opr} = -20\text{ to }85^\circ\text{C}$  (N version)/  $-40\text{ to }85^\circ\text{C}$  (D version), unless otherwise specified.)

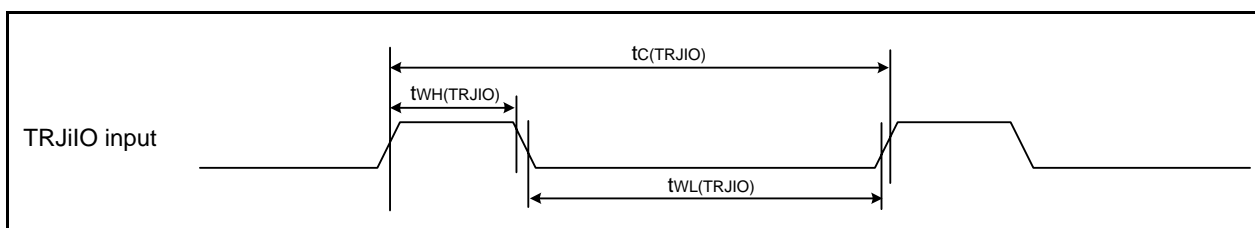
| Symbol         | Parameter             | Standard   |      |  |      |  |      | Unit          |
|----------------|-----------------------|--|------|--|------|--|------|---------------|
|                |                       | $V_{CC} = 2.2\text{V}, T_{opr} = 25^\circ\text{C}$ |      | $V_{CC} = 3\text{V}, T_{opr} = 25^\circ\text{C}$ |      | $V_{CC} = 5\text{V}, T_{opr} = 25^\circ\text{C}$ |      |               |
|                |                       | Min.   | Max. | Min.   | Max. | Min.   | Max. |               |
| $t_{c(XIN)}$   | XIN input cycle time  | 200  | –    | 50   | –    | 50   | –    | ns            |
| $t_{WH(XIN)}$  | XIN input “H” width   | 90   | –    | 24   | –    | 24   | –    | ns            |
| $t_{WL(XIN)}$  | XIN input “L” width   | 90   | –    | 24   | –    | 24   | –    | ns            |
| $t_{c(XCIN)}$  | XCIN input cycle time | 20   | –    | 20   | –    | 20   | –    | $\mu\text{s}$ |
| $t_{WH(XCIN)}$ | XCIN input “H” width  | 10   | –    | 10   | –    | 10   | –    | $\mu\text{s}$ |
| $t_{WL(XCIN)}$ | XCIN input “L” width  | 10   | –    | 10   | –    | 10   | –    | $\mu\text{s}$ |



**Figure 5.19 External Clock Input Timing**

**Table 5.56 Timing Requirements of TRJiIO (i = 0 to 2)**  
( $V_{SS} = 0\text{ V}$  and  $T_{opr} = -20\text{ to }85^\circ\text{C}$  (N version)/  $-40\text{ to }85^\circ\text{C}$  (D version), unless otherwise specified.)

| Symbol          | Parameter               | Standard   |      |  |      |  |      | Unit |
|-----------------|-------------------------|--|------|--|------|--|------|------|
|                 |                         | $V_{CC} = 2.2\text{V}, T_{opr} = 25^\circ\text{C}$ |      | $V_{CC} = 3\text{V}, T_{opr} = 25^\circ\text{C}$ |      | $V_{CC} = 5\text{V}, T_{opr} = 25^\circ\text{C}$ |      |      |
|                 |                         | Min.   | Max. | Min.   | Max. | Min.   | Max. |      |
| $t_{c(TRJIO)}$  | TRJiIO input cycle time | 500  | –    | 300  | –    | 100  | –    | ns   |
| $t_{WH(TRJIO)}$ | TRJiIO input “H” width  | 200  | –    | 120  | –    | 40   | –    | ns   |
| $t_{WL(TRJIO)}$ | TRJiIO input “L” width  | 200  | –    | 120  | –    | 40   | –    | ns   |

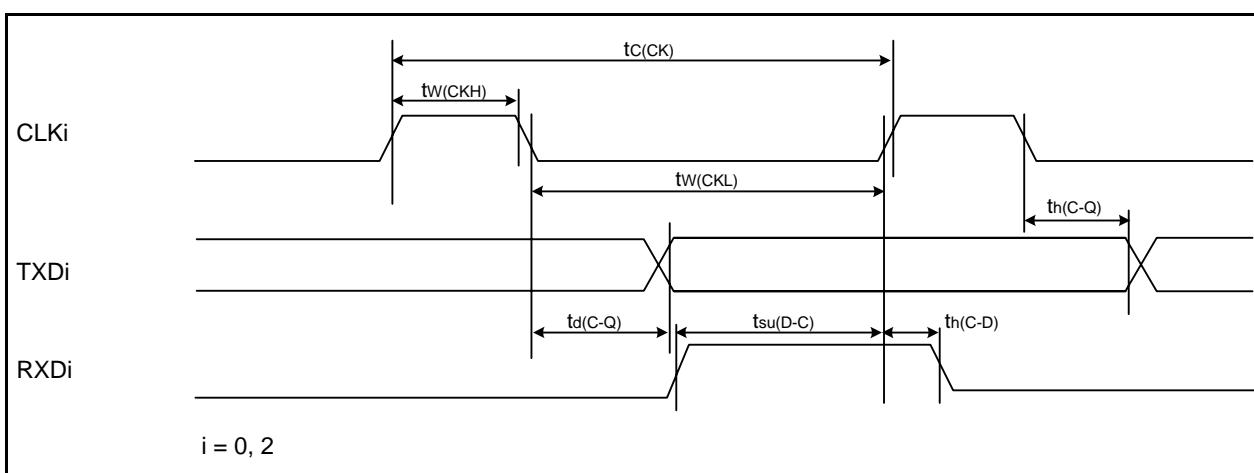


**Figure 5.20 Input Timing of TRJiIO**

**Table 5.57 Timing Requirements of Serial Interface**  
( $V_{SS} = 0\text{ V}$  and  $T_{opr} = -20\text{ to }85^\circ\text{C}$  (N version)/  $-40\text{ to }85^\circ\text{C}$  (D version), unless otherwise specified.)

| Symbol        | Parameter              | Standard   |      |  |      |  |      | Unit |
|---------------|------------------------|--|------|--|------|--|------|------|
|               |                        | $V_{CC} = 2.2\text{V}, T_{opr} = 25^\circ\text{C}$ |      | $V_{CC} = 3\text{V}, T_{opr} = 25^\circ\text{C}$ |      | $V_{CC} = 5\text{V}, T_{opr} = 25^\circ\text{C}$ |      |      |
|               |                        | Min.   | Max. | Min.   | Max. | Min.   | Max. |      |
| $t_{c(CK)}$   | CLKi input cycle time  | 800  | –    | 300  | –    | 200  | –    | ns   |
| $t_{w(CKH)}$  | CLKi input “H” width   | 400  | –    | 150  | –    | 100  | –    | ns   |
| $t_{w(CKL)}$  | CLKi input “L” width   | 400  | –    | 150  | –    | 100  | –    | ns   |
| $t_d(C-Q)$    | TXDi output delay time | –  | 200  | –  | 80   | –  | 50   | ns   |
| $t_h(C-Q)$    | TXDi hold time         | 0  | –    | 0  | –    | 0  | –    | ns   |
| $t_{su}(D-C)$ | RXDi input setup time  | 150  | –    | 70   | –    | 50   | –    | ns   |
| $t_h(C-D)$    | RXDi input hold time   | 90   | –    | 90   | –    | 90   | –    | ns   |

$i = 0, 2$



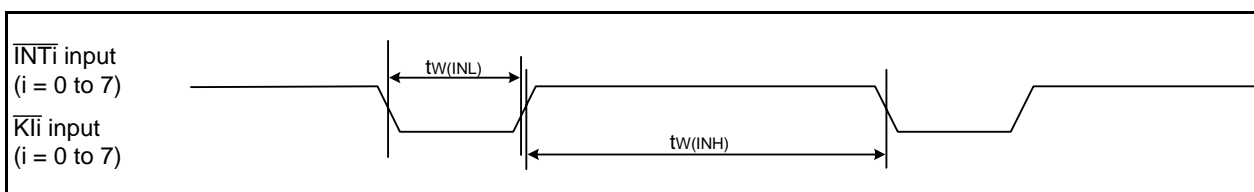
**Figure 5.21 Input and Output Timing of Serial Interface**

**Table 5.58 Timing Requirements of External Interrupt  $\overline{INTi}$  ( $i = 0$  to  $7$ ) and Key Input Interrupt  $\overline{Kli}$  ( $i = 0$  to  $7$ )**  
( $V_{SS} = 0\text{ V}$  and  $T_{opr} = -20\text{ to }85^\circ\text{C}$  (N version)/  $-40\text{ to }85^\circ\text{C}$  (D version), unless otherwise specified.)

| Symbol       | Parameter   | Standard   |      |  |      |  |      | Unit |
|--------------|---|--|------|--|------|--|------|------|
|              |   | $V_{CC} = 2.2\text{V}, T_{opr} = 25^\circ\text{C}$ |      | $V_{CC} = 3\text{V}, T_{opr} = 25^\circ\text{C}$ |      | $V_{CC} = 5\text{V}, T_{opr} = 25^\circ\text{C}$ |      |      |
|              |   | Min.   | Max. | Min.   | Max. | Min.   | Max. |      |
| $t_{w(INH)}$ | $\overline{INTi}$ input “H” width, $\overline{Kli}$ input “H” width | 1000 (1)   | –    | 380 (1)  | –    | 250 (1)  | –    | ns   |
| $t_{w(INL)}$ | $\overline{INTi}$ input “L” width, $\overline{Kli}$ input “L” width | 1000 (2)   | –    | 380 (2)  | –    | 250 (2)  | –    | ns   |

Notes:

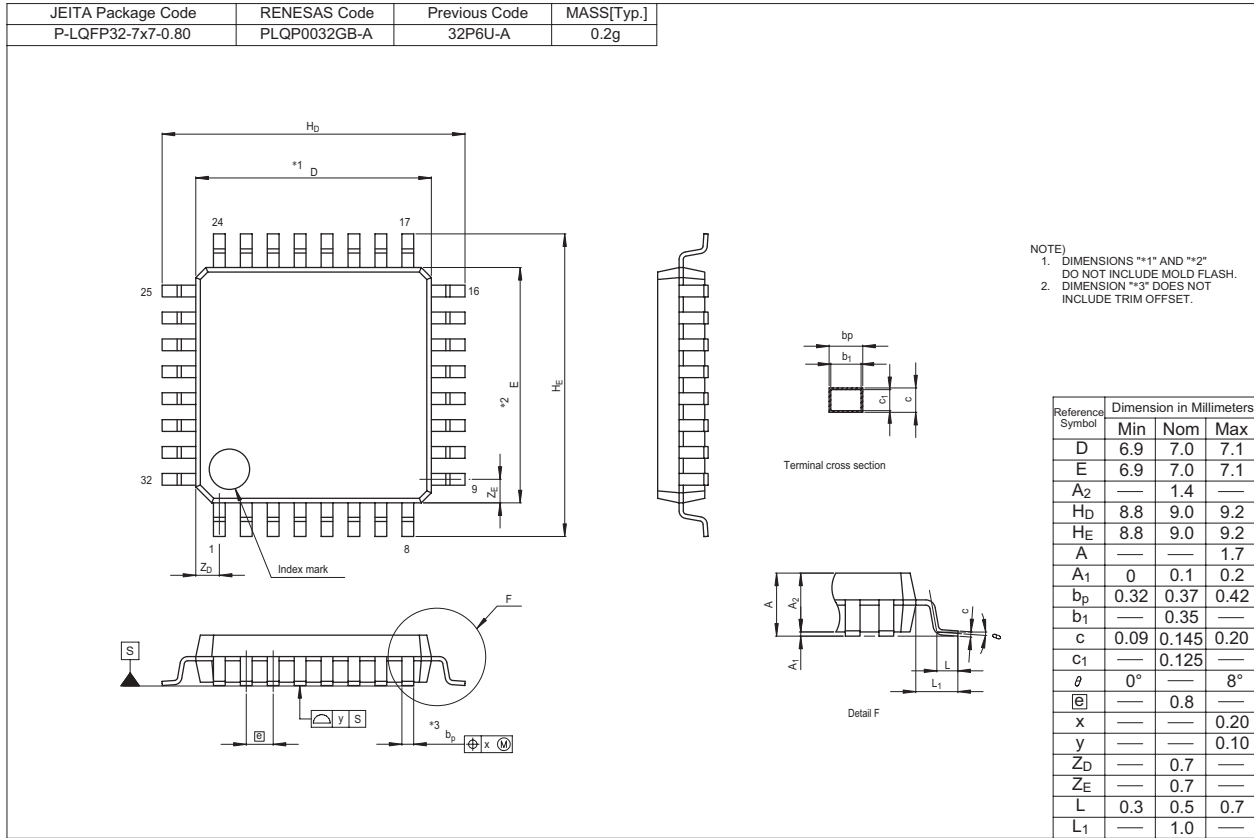
- When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input HIGH width of either (1/digital filter clock frequency  $\times$  3) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input LOW width of either (1/digital filter clock frequency  $\times$  3) or the minimum value of standard, whichever is greater.

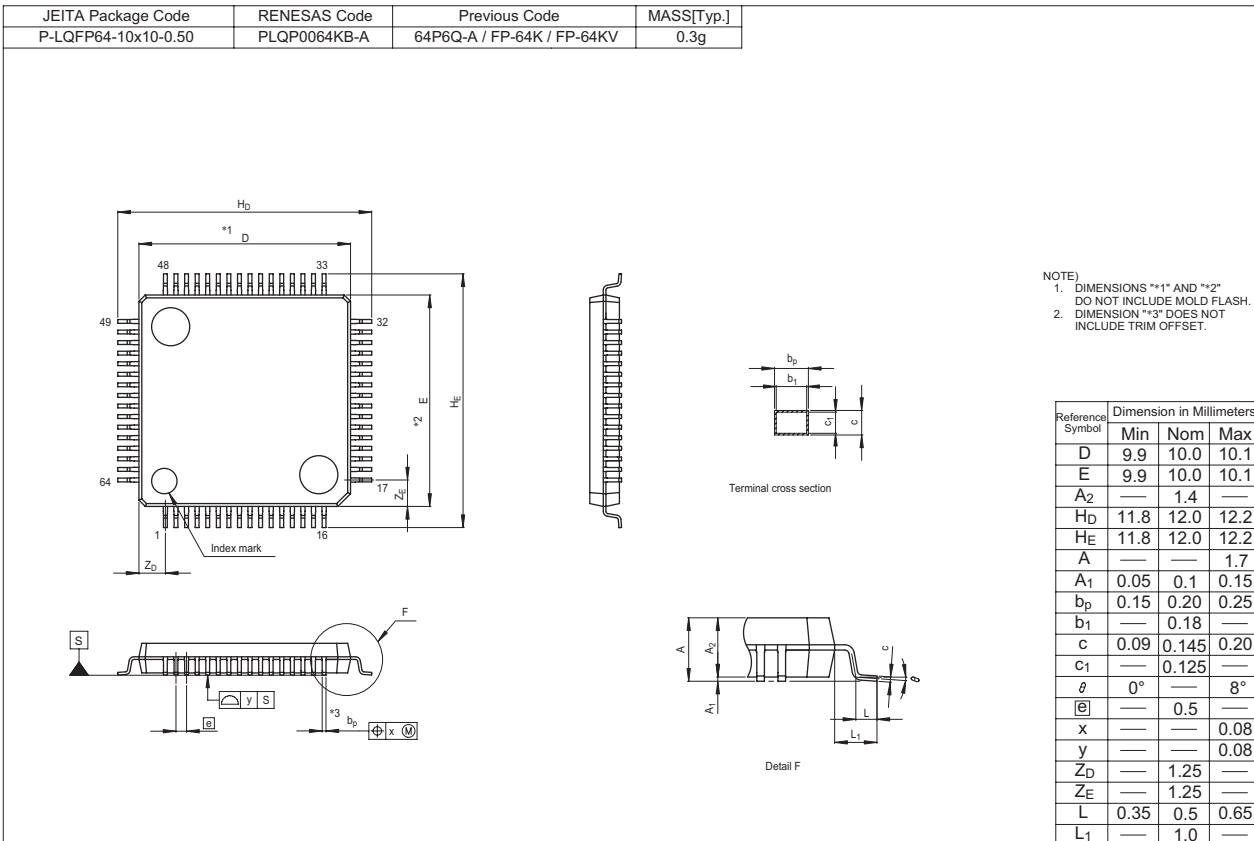
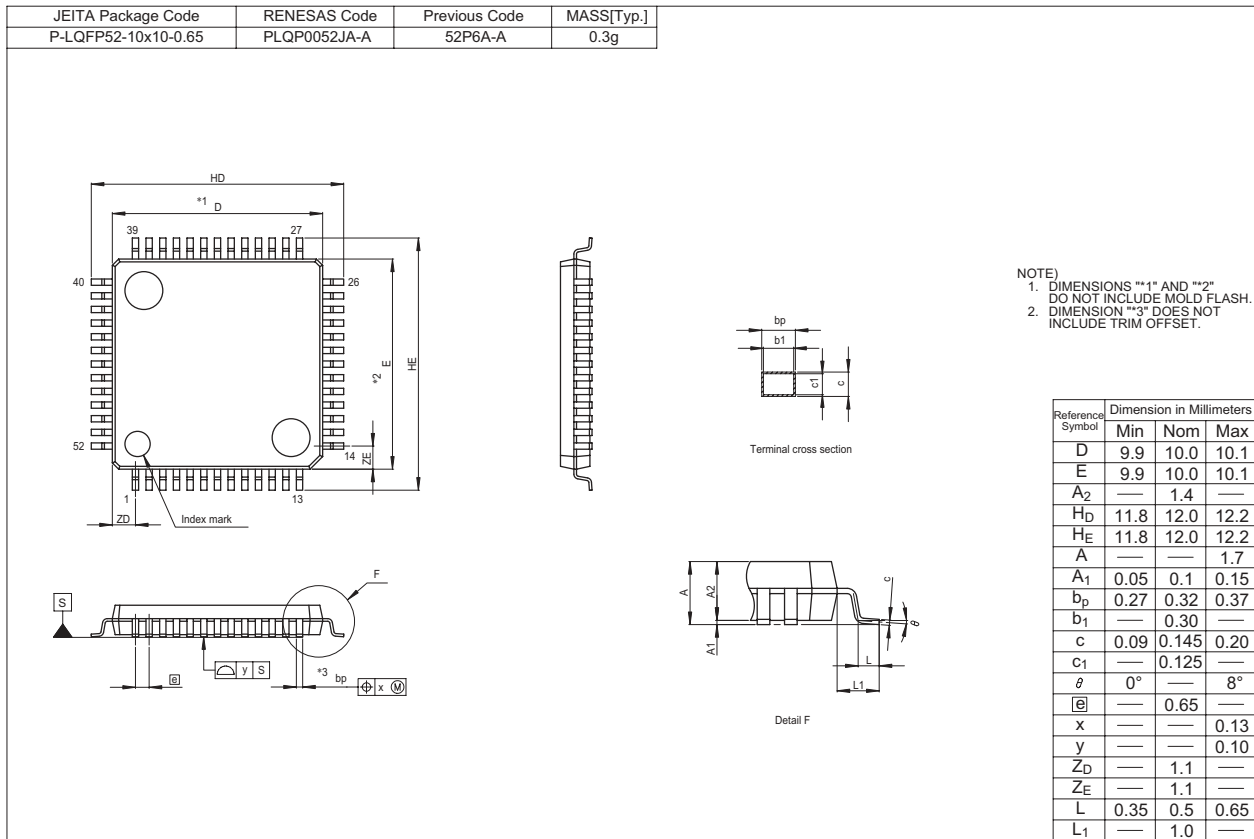


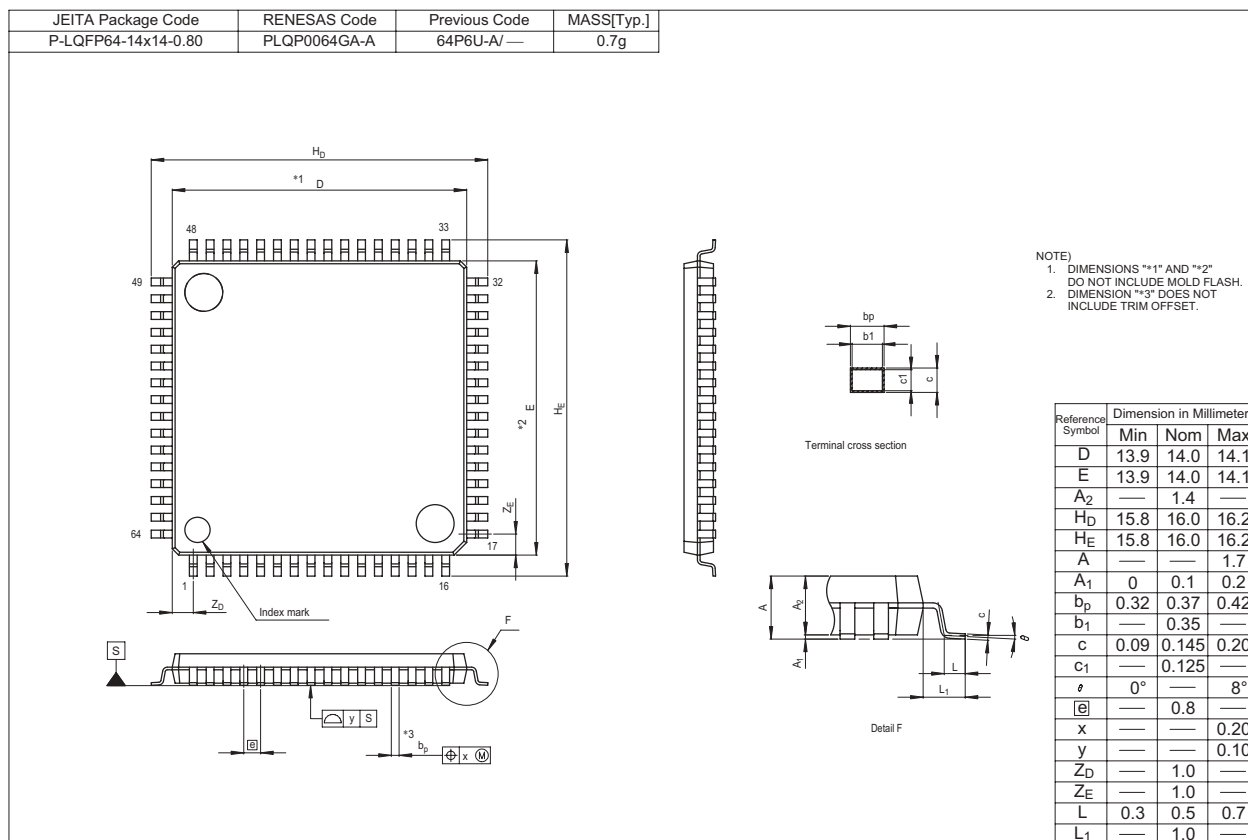
**Figure 5.22 Input Timing of External Interrupt  $\overline{INTi}$  and Key Input Interrupt  $\overline{Kli}$**

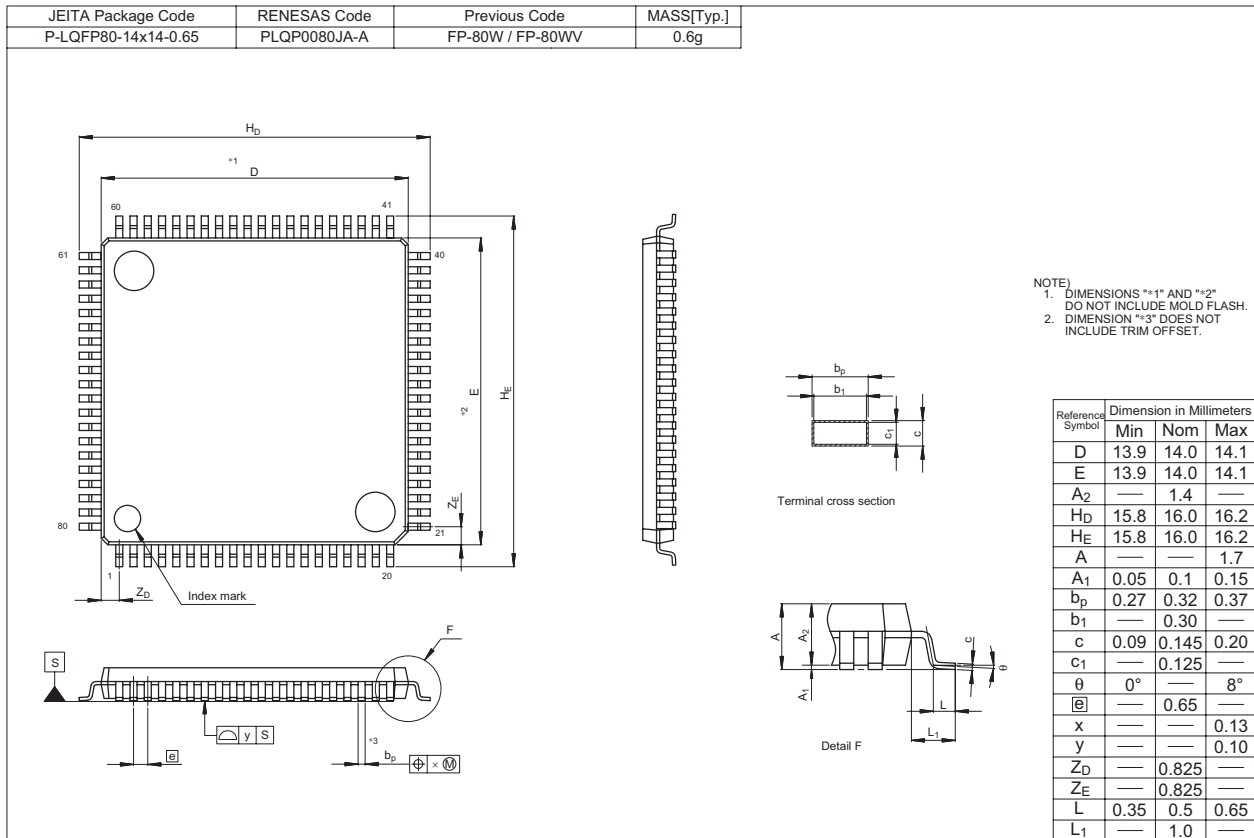
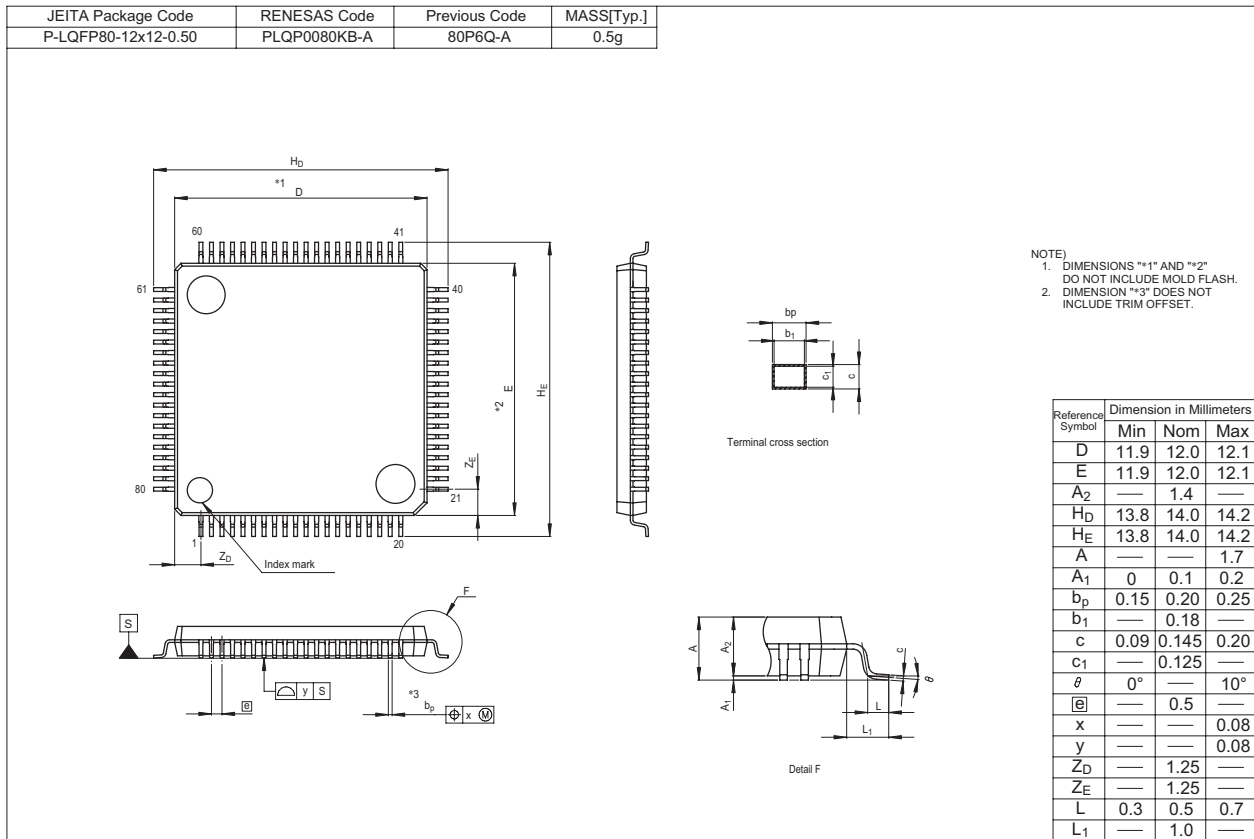
## Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics web site.









**REVISION HISTORY**

R8C/LA3A Group, R8C/LA5A Group, R8C/LA6A Group, R8C/LA8A Group Datasheet

| Rev. | Date                      | Description |   |
|------|---------------------------|-------------|---|
|      |                           | Page        | Summary   |
| 0.01 | Jan 18, 2010              | —           | First Edition issued  |
| 0.02 | Jul 16, 2010              | 2           | Table 1.1 revised   |
|      |                           | 3           | Table 1.2 revised   |
|      |                           | 4           | Tables 1.4 and 1.5 revised                                  |
|      |                           | 5           | Table 1.6 revised   |
|      |                           | 6           | Table 1.7 revised   |
|      |                           | 7           | Table 1.8 revised   |
|      |                           | 8           | Table 1.9 and Figure 1.1 revised                            |
|      |                           | 9           | Table 1.10 and Figure 1.2 revised                           |
|      |                           | 10          | Table 1.11 and Figure 1.3 revised                           |
|      |                           | 11          | Table 1.12 revised  |
|      |                           | 12          | Figure 1.5 revised  |
|      |                           | 13          | Figure 1.6 revised  |
|      |                           | 14          | Figure 1.7 revised  |
|      |                           | 16          | Figure 1.9 revised  |
|      |                           | 17          | Figure 1.10 revised   |
|      |                           | 18          | Table 1.13 revised  |
|      |                           | 19          | Table 1.14 revised  |
|      |                           | 20          | Figure 1.11 revised   |
|      |                           | 21          | Figure 1.12 revised   |
|      |                           | 25          | Table 1.18 revised  |
| 26   | Table 1.19 revised        |             |   |
| 30   | Figure 3.1 revised        |             |   |
| 31   | Table 4.1, Note 3 revised |             |   |
| 35   | Table 4.5 revised         |             |   |
|      |                           | 41 to 44    | Package Dimensions revised                                  |
| 1.00 | Dec 21, 2010              | All         | "Preliminary" and "Under development" deleted               |
|      |                           | 2           | Table 1.1 revised   |
|      |                           | 3           | Tables 1.2 and 1.3 Note 2 revised                           |
|      |                           | 4           | Tables 1.4 and 1.5 Note 1 revised                           |
|      |                           | 6           | Table 1.7 revised   |
|      |                           | 7           | Table 1.8 revised   |
|      |                           | 10          | Table 1.11 and Figure 1.3 revised                           |
|      |                           | 12          | Figure 1.5 revised  |
|      |                           | 13          | Figure 1.6 revised  |
|      |                           | 14          | Figure 1.7 revised  |
|      |                           | 15          | Figure 1.8 revised  |
|      |                           | 16          | Figure 1.9 revised  |
|      |                           | 18          | Table 1.13 revised  |
|      |                           | 19          | Table 1.14 revised  |
|      |                           | 20          | Figure 1.11 revised   |
|      |                           | 22          | Table 1.15 revised  |
| 23   | Table 1.16 revised        |             |   |
| 24   | Table 1.17 revised        |             |   |
|      |                           | 25, 26      | Tables 1.18 and 1.19 Pin Functions for R8C/LA5A Group added |

## REVISION HISTORY

R8C/LA3A Group, R8C/LA5A Group, R8C/LA6A Group, R8C/LA8A Group Datasheet

| Rev. | Date               | Description |   |
|------|--------------------|-------------|---|
|      |                    | Page        | Summary   |
| 1.00 | Dec 21, 2010       | 32          | "The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh." deleted |
|      |                    | 33 to 41    | Figure 3.1 revised  |
|      |                    | 52 to 98    | Tables 4.1 to 4.9 SFR information for R8C/LA5A Group added  |
|      |                    | 92          | "5. Electrical Characteristics" added   |
| 1.01 | Oct 28, 2011       | 92          | Package Dimensions "PVQN0064LB-A" deleted   |
|      |                    | 1           | 1.1 "... data flash (1 KB x 2 blocks)." → "... data flash."   |
|      |                    | 10          | Table 1.11, Figure 1.3 revised  |
|      |                    | 11          | Table 1.12, Figure 1.4 revised  |
|      |                    | 32          | 3 revised, Figure 3.1 revised   |
|      |                    | 60          | Table 5.12 revised  |
|      |                    | 80          | Table 5.36 revised  |
|      |                    | 81          | Table 5.37 revised  |
| 83   | Table 5.41 revised |             |   |

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## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

### 1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

### 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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