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July 2014

# FDMA1024NZ

# **Dual N-Channel PowerTrench® MOSFET**

**20 V, 5.0 A, 54 m**Ω

#### **Features**

- Max  $r_{DS(on)}$  = 54 m $\Omega$  at  $V_{GS}$  = 4.5 V,  $I_D$  = 5.0 A
- Max  $r_{DS(on)}$  = 66 m $\Omega$  at  $V_{GS}$  = 2.5 V,  $I_D$  = 4.2 A
- Max  $r_{DS(on)}$  = 82 m $\Omega$  at  $V_{GS}$  = 1.8 V,  $I_{D}$  = 2.3 A
- Max  $r_{DS(on)}$  = 114 m $\Omega$  at  $V_{GS}$  = 1.5 V,  $I_D$  = 2.0 A
- HBM ESD protection level = 1.6 kV (Note 3)
- Low profile 0.8 mm maximum in the new package MicroFET 2x2 mm
- RoHS Compliant
- Free from halogenated compounds and antimony oxides

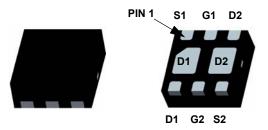
# **General Description**

This device is designed specifically as a single package solution for dual switching requirements in cellular handset and other ultra-portable applications. It features two independent N-Channel MOSFETs with low on-state resistance for minimum conduction losses.

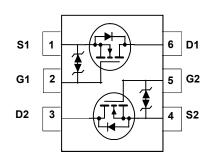
The MicroFET 2X2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

# **Applications**

- Baseband Switch
- Loadswitch
- DC-DC Conversion







# **MOSFET Maximum Ratings** T<sub>A</sub> = 25 °C unless otherwise noted

Symbol	Parameter	Ratings	Units	
V <sub>DS</sub>	Drain to Source Voltage		20	V
$V_{GS}$	Gate to Source Voltage		±8	V
1	Drain Current -Continuous	(Note 1a)	5.0	^
ID	-Pulsed		6.0	A
D	Power Dissipation	(Note 1a)	1.4	W
$P_{D}$	Power Dissipation	(Note 1b)	0.7	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range		-55 to +150	°C

#### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	86 (Single Operation)	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	173 (Single Operation)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1c)	69 (Dual Operation)	C/VV
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1d)	151 (Dual Operation)	

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
024	FDMA1024NZ	MicroFET 2X2	7 "	8 mm	3000 units

# **Electrical Characteristics** T<sub>J</sub> = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25 °C		19		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 16 V, V <sub>GS</sub> = 0 V			1	μА
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±8 V, V <sub>DS</sub> = 0 V			±10	μА

#### **On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	0.4	0.7	1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25 °C		-3		mV/°C
r <sub>DS(on)</sub> Static Drain to Source On-Resistance	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5.0 A		37	54		
		$V_{GS} = 2.5 \text{ V}, I_D = 4.2 \text{ A}$		43	66	
	Static Drain to Source On-Resistance	$V_{GS} = 1.8 \text{ V}, I_D = 2.3 \text{ A}$		52	82	mΩ
		$V_{GS} = 1.5 \text{ V}, I_D = 2.0 \text{ A}$		67	114	
		$V_{GS} = 4.5 \text{ V}, I_D = 5.0 \text{ A}, T_J = 125 \text{ °C}$		51	75	
9 <sub>FS</sub>	Forward Transconductance	$V_{DD} = 5 \text{ V}, I_D = 5.0 \text{ A}$		16		S

# **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V - 40 V V - 0 V	375	500	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	70	95	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 1/11/2	40	65	pF
$R_G$	Gate Resistance	f = 1 MHz	4.3		Ω

# **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		5.3	11	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 10 V, I <sub>D</sub> = 5.0 A	2.2	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS} = 4.5 \text{ V}, R_{GEN} = 6 \Omega$	18	33	ns
t <sub>f</sub>	Fall Time		2.3	10	ns
$Q_g$	Total Gate Charge	V 45V V 40V	5.2	7.3	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	$V_{GS} = 4.5 \text{ V}, V_{DD} = 10 \text{ V},$ $I_{D} = 5.0 \text{ A}$	0.6		nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge	1D = 3.0 A	0.9		nC

### **Drain-Source Diode Characteristics**

Is	Maximum Continuous Source-Drain Diode Forward Current			1.1	Α
$V_{SD}$	Source to Drain Diode Forward Voltage $V_{GS} = 0 \text{ V}, I_S = 1.1 \text{ A}$ (Note 2)		0.7	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>E</sub> = 5.0 A, di/dt = 100 A/μs	19	35	ns
Q <sub>rr</sub>	Reverse Recovery Charge	- 1 <sub>F</sub> = 5.0 A, α//αι = 100 A/μs	5	10	nC

#### Notes:

- 1.  $R_{\theta,JA}$  is determined with the device mounted on a 1 in 2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta,JC}$  is guaranteed by design while  $R_{\theta,JA}$  is determined by the user's board design.

  (a)  $R_{BJA} = 86 \, ^{\circ}\text{C/W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For single operation.

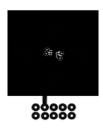
  - (b)  $R_{\theta JA}$  = 173 °C/W when mounted on a minimum pad of 2 oz copper. For single operation.
  - (c)  $R_{\theta JA}$  = 69 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For dual operation.
  - (d)  $R_{\theta,JA}$  = 151 °C/W when mounted on a minimum pad of 2 oz copper. For dual operation.



a) 86 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b) 173  $^{\rm o}$ C/W when mounted on a minimum pad of 2 oz copper.



c) 69 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



d) 151  $^{\rm o}$ C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test : Pulse Width < 300 us, Duty Cycle < 2.0 %
- 3: The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

# Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

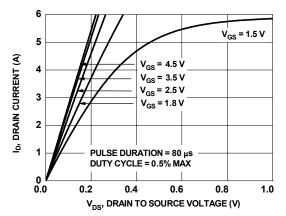


Figure 1. On-Region Characteristics

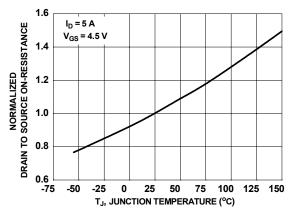


Figure 3. Normalized On-Resistance vs Junction Temperature

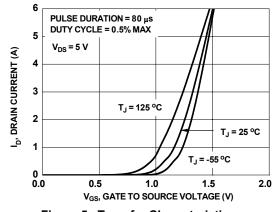


Figure 5. Transfer Characteristics

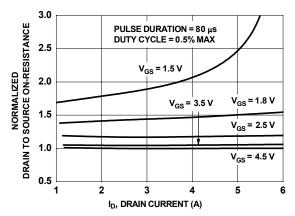


Figure 2 Normalized On-Resistance vs Drain Current and Gate Voltage

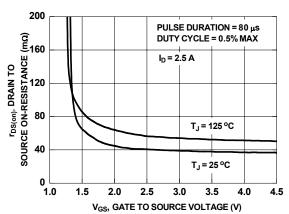


Figure 4. On-Resistance vs Gate to Source Voltage

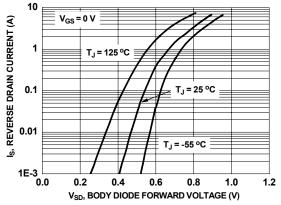


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

# Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

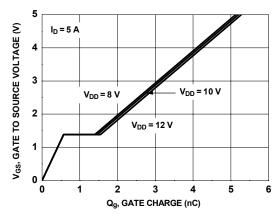


Figure 7. Gate Charge Characteristics

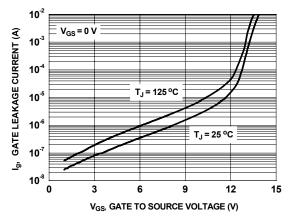


Figure 9. Gate Leakage Current vs Gate to Source Voltage

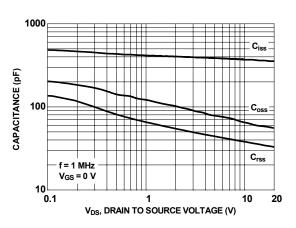


Figure 8.Capacitance vs Drain to Source Voltage

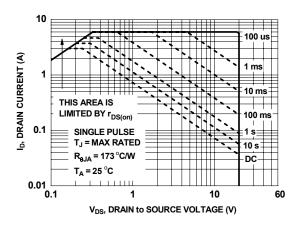


Figure 10. Forward Bias Safe Operating Area

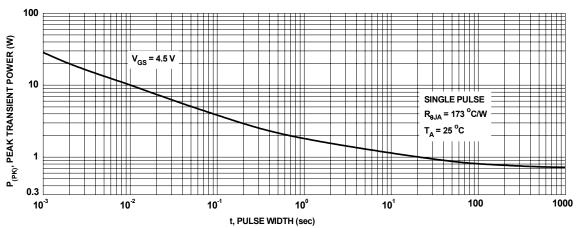


Figure 11. Single Pulse Maximum Power Dissipation

# **Typical Characteristics** $T_J = 25$ °C unless otherwise noted

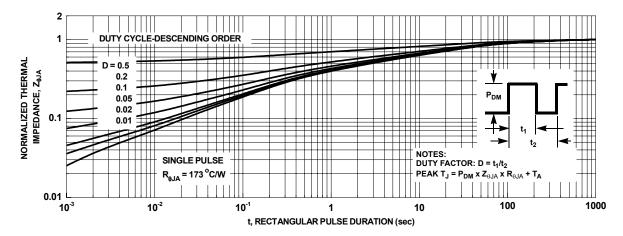
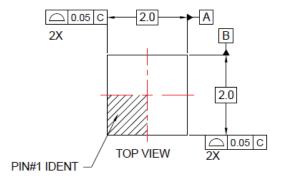
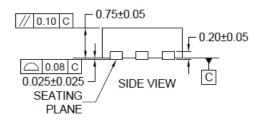
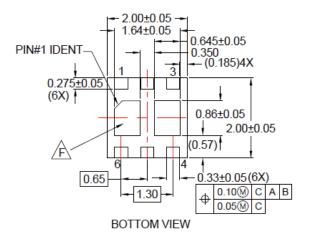


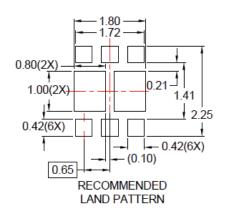
Figure 12. Junction to Ambient Transient Thermal Response Curve

# **Dimensional Outline and Pad Layout**









#### NOTES:

- A. CONFORM TO JADEC REGISTRATIONS MO-229, VARIATION VCCC, EXCEPT WHERE NOTED.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-UMLP16Erev4
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