# MC74LVX4053

# Analog Multiplexer/ Demultiplexer

## High−Performance Silicon−Gate CMOS

The MC74LVX4053 utilizes silicon−gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. This analog multiplexer/demultiplexer controls analog voltages that may vary across the complete power supply range (from $V_{CC}$ to $V_{EE}$).

The LVX4053 is similar in pinout to the LVX8053, the HC4053A, and the metal−gate MC14053B. The Channel−Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel−Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device has been designed so the ON resistance ($R_{ON}$) is more linear over input voltage than the $R_{ON}$ of metal−gate CMOS analog switches and High−Speed CMOS analog switches.

### Features

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Analog Power Supply Range ($V_{CC} - V_{EE}$) = −3.0 V to +3.0 V
- Digital (Control) Power Supply Range ($V_{CC}$ − GND) = 2.5 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal−Gate, HSL, or VHC Counterparts
- Low Noise
- Designed to Operate on a Single Supply with $V_{EE}$ = GND, or Using Split Supplies up to ±3.0 V
- Break−Before−Make Circuitry
- These Devices are Pb−Free and are RoHS Compliant

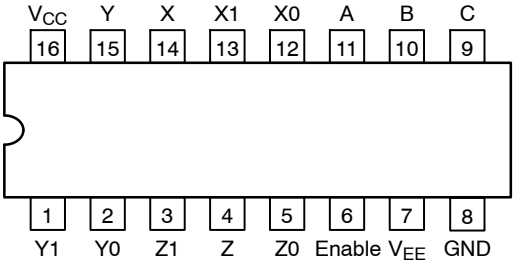


**Figure 1. Pin Connection and Marking Diagram**
(Top View)

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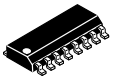
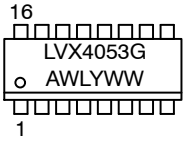
**http://onsemi.com**

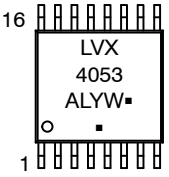
**MARKING DIAGRAMS**

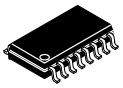


**SOIC−16**
**D SUFFIX**
**CASE 751B**

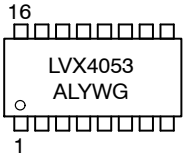


**TSSOP−16**
**DT SUFFIX**
**CASE 948F**



**SOEIAJ−16**
**M SUFFIX**
**CASE 966**




| | |
|---|---|
| LVX4053 | = Specific Device Code |
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| Y | = Year |
| WW, W | = Work Week |
| G or ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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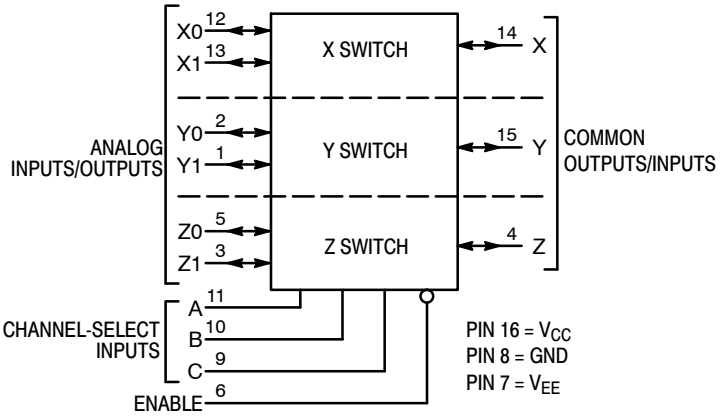
**FUNCTION TABLE**

| Control Inputs | | | | | | |
|---|---|---|---|---|---|---|
| | Select | | | | | |
| Enable | C | B | A | ON Channels | | |
| L | L | L | L | Z0 | Y0 | X0 |
| L | L | L | H | Z0 | Y0 | X1 |
| L | L | H | L | Z0 | Y1 | X0 |
| L | L | H | H | Z0 | Y1 | X1 |
| L | H | L | L | Z1 | Y0 | X0 |
| L | H | L | H | Z1 | Y0 | X1 |
| L | H | H | L | Z1 | Y1 | X0 |
| L | H | H | H | Z1 | Y1 | X1 |
| H | X | X | X | NONE | | |

X = Don't Care




NOTE: This device allows independent control of each switch. Channel−Select Input A controls the X−Switch, Input B controls the Y−Switch and Input C controls the Z−Switch

**Figure 2. Logic Diagram Triple Single−Pole, Double−Position Plus Common Off**

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| MC74LVX4053DG | SOIC−16 (Pb−Free) | 48 Units / Rail |
| MC74LVX4053DR2G | SOIC−16 (Pb−Free) | 2500 Tape & Reel |
| MC74LVX4053DTG | TSSOP−16* | 96 Units / Rail |
| MC74LVX4053DTR2G | TSSOP−16* | 2500 Tape & Reel |
| MC74LVX4053MG | SOEIAJ−16 (Pb−Free) | 50 Units / Rail |
| MC74LVX4053MELG | SOEIAJ−16 (Pb−Free) | 2000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

## MAXIMUM RATINGS

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{EE}$ | Negative DC Supply Voltage | (Referenced to GND) | −7.0 to +0.5 | V |
| $V_{CC}$ | Positive DC Supply Voltage | (Referenced to GND)<br>(Referenced to $V_{EE}$) | −0.5 to +7.0<br>−0.5 to +7.0 | V |
| $V_{IS}$ | Analog Input Voltage | | $V_{EE}$ −0.5 to $V_{CC}$ +0.5 | V |
| $V_{IN}$ | Digital Input Voltage | (Referenced to GND) | −0.5 to 7.0 | V |
| I | DC Current, Into or Out of Any Pin | | ±20 | mA |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds | | 260 | °C |
| $T_J$ | Junction Temperature under Bias | | +150 | °C |
| $\theta_{JA}$ | Thermal Resistance | SOIC<br>TSSOP | 143<br>164 | °C/W |
| $P_D$ | Power Dissipation in Still Air, | SOIC<br>TSSOP | 500<br>450 | mW |
| MSL | Moisture Sensitivity | | Level 1 | |
| $F_R$ | Flammability Rating | Oxygen Index: 30% − 35% | UL−94−VO (0.125 in) | |
| $V_{ESD}$ | ESD Withstand Voltage | Human Body Model (Note 1)<br>Machine Model (Note 2)<br>Charged Device Model (Note 3) | >2000<br>>200<br>>1000 | V |
| $I_{LATCHUP}$ | Latchup Performance | Above $V_{CC}$ and Below GND at 125°C (Note 4) | ±300 | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA/JESD22−A114−A.
2. Tested to EIA/JESD22−A115−A.
3. Tested to JESD22−C101−A.
4. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{EE}$ | Negative DC Supply Voltage | (Referenced to GND) | −6.0 | GND | V |
| $V_{CC}$ | Positive DC Supply Voltage | (Referenced to GND)<br>(Referenced to $V_{EE}$) | 2.5<br>2.5 | 6.0<br>6.0 | V |
| $V_{IS}$ | Analog Input Voltage | | $V_{EE}$ | $V_{CC}$ | V |
| $V_{IN}$ | Digital Input Voltage | (Note 5) (Referenced to GND) | 0 | 6.0 | V |
| $T_A$ | Operating Temperature Range, All Package Types | | −55 | 125 | °C |
| $t_r$, $t_f$ | Input Rise/Fall Time<br>(Channel Select or Enable Inputs) | $V_{CC}$ = 3.0 V ± 0.3 V<br>$V_{CC}$ = 5.0 V ± 0.5 V | 0<br>0 | 100<br>20 | ns/V |

5. Unused inputs may not be left open. All inputs must be tied to a high−logic voltage level or a low−logic input voltage level.

## DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

| Junction Temperature °C | Time, Hours | Time, Years |
|---|---|---|
| 80 | 1,032,200 | 117.8 |
| 90 | 419,300 | 47.9 |
| 100 | 178,700 | 20.4 |
| 110 | 79,600 | 9.4 |
| 120 | 37,000 | 4.2 |
| 130 | 17,800 | 2.0 |
| 140 | 8,900 | 1.0 |

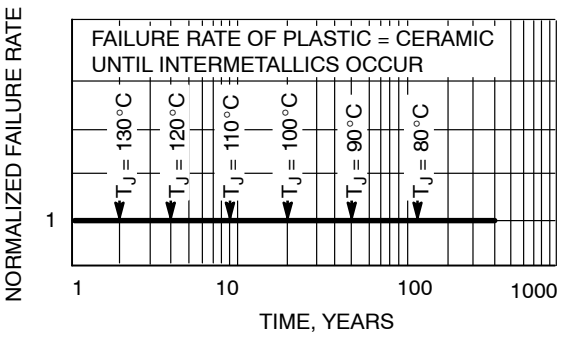



**Figure 3. Failure Rate vs. Time Junction Temperature**

**DC CHARACTERISTICS – Digital Section** (Voltages Referenced to GND)

| Symbol | Parameter | Condition | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | −55 to 25°C | ≤85°C | ≤125°C | |
| $V_{IH}$ | Minimum High−Level Input Voltage, Channel−Select or Enable Inputs | | 2.5<br>3.0<br>4.5<br>6.0 | 1.90<br>2.10<br>3.15<br>4.2 | 1.90<br>2.10<br>3.15<br>4.2 | 1.90<br>2.10<br>3.15<br>4.2 | V |
| $V_{IL}$ | Maximum Low−Level Input Voltage, Channel−Select or Enable Inputs | | 2.5<br>3.0<br>4.5<br>6.0 | 0.6<br>0.9<br>1.35<br>1.8 | 0.6<br>0.9<br>1.35<br>1.8 | 0.6<br>0.9<br>1.35<br>1.8 | V |
| $I_{IN}$ | Maximum Input Leakage Current, Channel−Select or Enable Inputs | $V_{IN}$ = 6.0 or GND | 0 V to 6.0 V | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | Channel Select, Enable and $V_{IS} = V_{CC}$ or GND | 6.0 | 4.0 | 40 | 80 | μA |

**DC ELECTRICAL CHARACTERISTICS – Analog Section**

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | $V_{EE}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | −55 to 25°C | ≤85°C | ≤125°C | |
| $R_{ON}$ | Maximum “ON” Resistance | $V_{IN} = V_{IL}$ or $V_{IH}$<br>$V_{IS}$ = ½ ($V_{CC} - V_{EE}$)<br>$\|I_S\|$ = 2.0 mA<br>(Figure 4) | 3.0<br>4.5<br>3.0 | 0<br>0<br>−3.0 | 86<br>37<br>26 | 108<br>46<br>33 | 120<br>55<br>37 | Ω |
| $\Delta R_{ON}$ | Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package | $V_{IN} = V_{IL}$ or $V_{IH}$<br>$V_{IS}$ = ½ ($V_{CC} - V_{EE}$)<br>$\|I_S\|$ = 2.0 mA | 3.0<br>4.5<br>3.0 | 0<br>0<br>−3.0 | 15<br>13<br>10 | 20<br>18<br>15 | 20<br>18<br>15 | Ω |
| $I_{off}$ | Maximum Off−Channel Leakage Current, Any One Channel | $V_{in} = V_{IL}$ or $V_{IH}$;<br>$V_{IO} = V_{CC}$ or GND;<br>Switch Off (Figure 3) | 5.5<br>+3.0 | 0<br>−3.0 | 0.1<br>0.1 | 0.5<br>0.5 | 1.0<br>1.0 | μA |
| | Maximum Off−Channel Leakage Current, Common Channel | $V_{in} = V_{IL}$ or $V_{IH}$;<br>$V_{IO} = V_{CC}$ or GND;<br>Switch Off (Figure 4) | 5.5<br>+3.0 | 0<br>−3.0 | 0.2<br>0.2 | 2.0<br>2.0 | 4.0<br>4.0 | |
| $I_{on}$ | Maximum On−Channel Leakage Current, Channel−to−Channel | $V_{in} = V_{IL}$ or $V_{IH}$;<br>Switch−to−Switch = $V_{CC}$ or GND; (Figure 5) | 5.5<br>+3.0 | 0<br>−3.0 | 0.2<br>0.2 | 2.0<br>2.0 | 4.0<br>4.0 | μA |

**AC CHARACTERISTICS** (Input $t_r = t_f$ = 3 ns)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | $V_{EE}$ V | Guaranteed Limit | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | −55 to 25°C | | ≤85°C | ≤125°C | |
| | | | | | Min | Typ* | | | |
| $t_{BBM}$ | Min. Break−Before−Make Time | $V_{IN} = V_{IL}$ or $V_{IH}$<br>$V_{IS} = V_{CC}$<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>(Figures 12 and 13) | 3.0<br>4.5<br>3.0 | 0.0<br>0.0<br>−3.0 | 1.0<br>1.0<br>1.0 | 6.5<br>5.0<br>3.5 | –<br>–<br>– | –<br>–<br>– | ns |

*Typical Characteristics are at 25°C.

**AC CHARACTERISTICS** ($C_L$ = 50 pF, Input $t_r = t_f$ = 3 ns)

| Symbol | Parameter | $V_{CC}$ V | $V_{EE}$ V | Guaranteed Limit | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | −55 to 25°C | | | ≤85°C | | ≤125°C | | |
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Channel−Select to Analog Output (Figures 16 and 17) | 2.5 | 0 | | | 40 | | 45 | | 50 | ns |
| | | 3.0 | 0 | | | 28 | | 30 | | 35 | |
| | | 4.5 | 0 | | | 23 | | 25 | | 30 | |
| | | 3.0 | −3.0 | | | 23 | | 25 | | 28 | |
| $t_{PLZ}$, $t_{PHZ}$ | Maximum Propagation Delay, Enable to Analog Output (Figures 14 and 15) | 2.5 | 0 | | | 40 | | 45 | | 50 | ns |
| | | 3.0 | 0 | | | 28 | | 30 | | 35 | |
| | | 4.5 | 0 | | | 23 | | 25 | | 30 | |
| | | 3.0 | −3.0 | | | 23 | | 25 | | 28 | |
| $t_{PZL}$, $t_{PZH}$ | Maximum Propagation Delay, Enable to Analog Output (Figures 14 and 15) | 2.5 | 0 | | | 40 | | 45 | | 50 | ns |
| | | 3.0 | 0 | | | 28 | | 30 | | 35 | |
| | | 4.5 | 0 | | | 23 | | 25 | | 30 | |
| | | 3.0 | −3.0 | | | 23 | | 25 | | 28 | |

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V, $V_{EE}$ = 0V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Figure 18) (Note 6) | 45 | pF |
| $C_{IN}$ | Maximum Input Capacitance, Channel−Select or Enable Inputs | 10 | pF |
| $C_{I/O}$ | Maximum Capacitance (All Switches Off) — Analog I/O | 10 | pF |
| | Common O/I | 10 | |
| | Feedthrough | 1.0 | |

6. Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

**ADDITIONAL APPLICATION CHARACTERISTICS** (GND = 0 V)

| Symbol | Parameter | Condition | $V_{CC}$ V | $V_{EE}$ V | Typ 25°C | Unit |
|---|---|---|---|---|---|---|
| BW | Maximum On−Channel Bandwidth or Minimum Frequency Response | $V_{IS}$ = ½ ($V_{CC}$ − $V_{EE}$)<br>Ref and Test Attn = 10 dB<br>Source Amplitude = 0 dB<br>(Figure 7) | 3.0 | 0.0 | 80 | MHz |
| | | | 4.5 | 0.0 | 80 | |
| | | | 6.0 | 0.0 | 80 | |
| | | | 3.0 | −3.0 | 80 | |
| $V_{ISO}$ | Off−Channel Feedthrough Isolation | f = 1 MHz; $V_{IS}$ = ½ ($V_{CC}$ − $V_{EE}$)<br>Adjust Network Analyzer output to 10 dBm on each output from the power splitter<br>(Figures 8 and 9) | 3.0 | 0.0 | −70 | dB |
| | | | 4.5 | 0.0 | −70 | |
| | | | 6.0 | 0.0 | −70 | |
| | | | 3.0 | −3.0 | −70 | |
| $V_{ONL}$ | Maximum Feedthrough On Loss | $V_{IS}$ = ½ ($V_{CC}$ − $V_{EE}$)<br>Adjust Network Analyzer output to 10 dBm on each output from the power splitter<br>(Figure 11) | 3.0 | 0.0 | −2 | dB |
| | | | 4.5 | 0.0 | −2 | |
| | | | 6.0 | 0.0 | −2 | |
| | | | 3.0 | −3.0 | −2 | |
| Q | Charge Injection | $V_{IN}$ = $V_{CC}$ to $V_{EE}$, $f_{IS}$ = 1 kHz, $t_r = t_f$ = 3 ns<br>$R_{IS}$ = 0 Ω, $C_L$= 1000 pF, Q = $C_L$ * $\Delta V_{OUT}$<br>(Figure 10) | 5.0 | 0.0 | 9.0 | pC |
| | | | 3.0 | −3.0 | 12 | |
| THD | Total Harmonic Distortion THD + Noise | $f_{IS}$ = 1 MHz, $R_L$ = 10 KΩ, $C_L$ = 50 pF,<br>$V_{IS}$ = 5.0 $V_{PP}$ sine wave<br>$V_{IS}$ = 6.0 $V_{PP}$ sine wave<br>(Figure 19) | 6.0 | 0.0 | 0.10 | % |
| | | | 3.0 | −3.0 | 0.05 | |

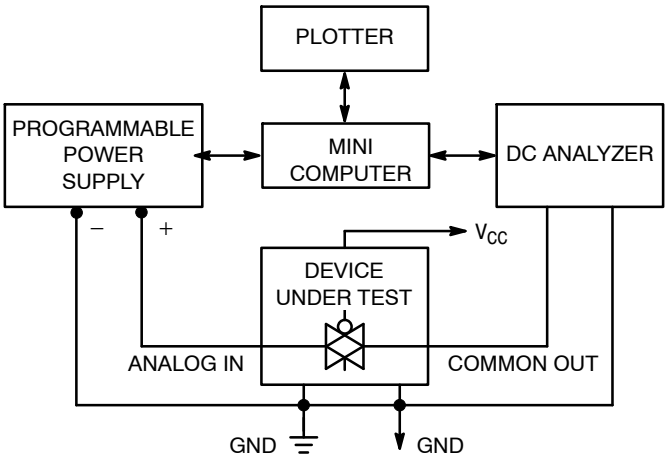



**Figure 4. On Resistance, Test Set–Up**

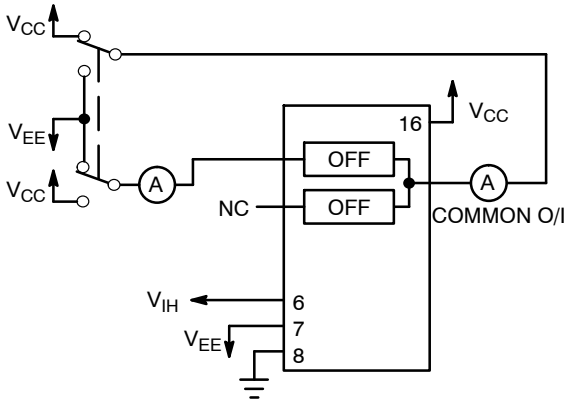



**Figure 5. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up**

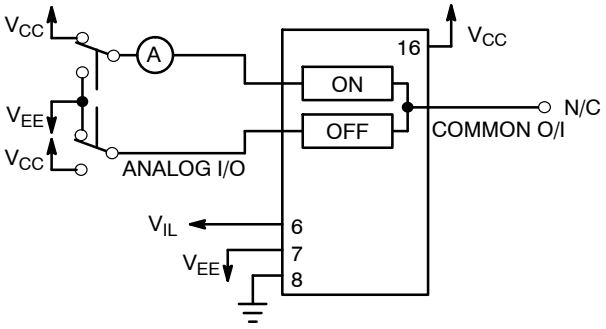



**Figure 6. Maximum On Channel Leakage Current, Channel to Channel, Test Set–Up**

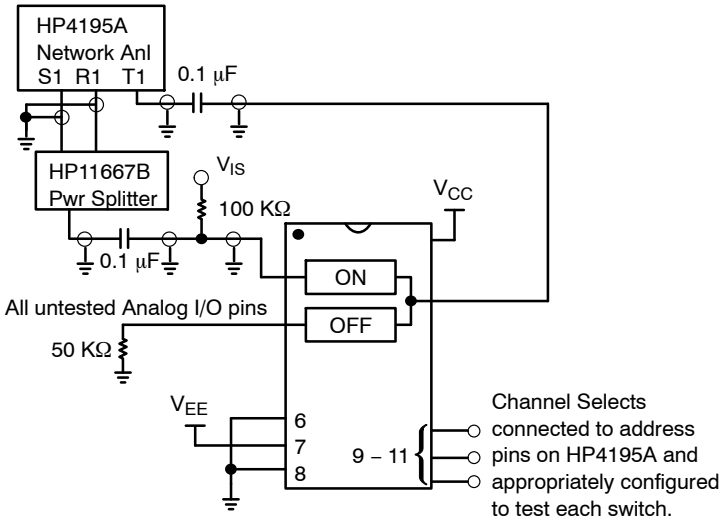
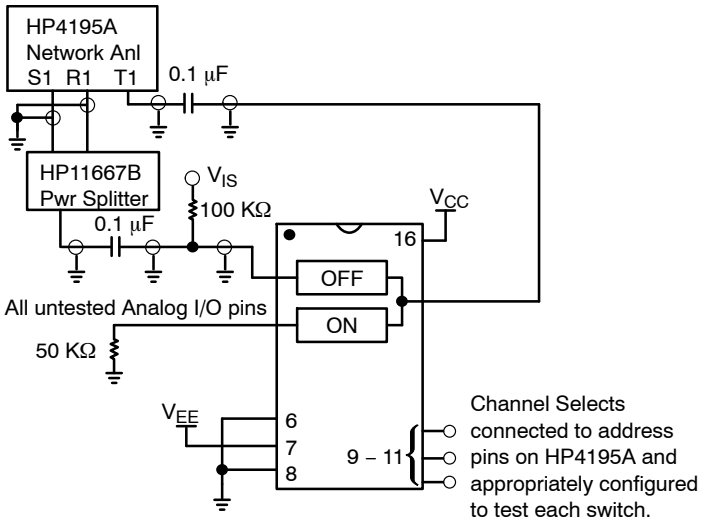


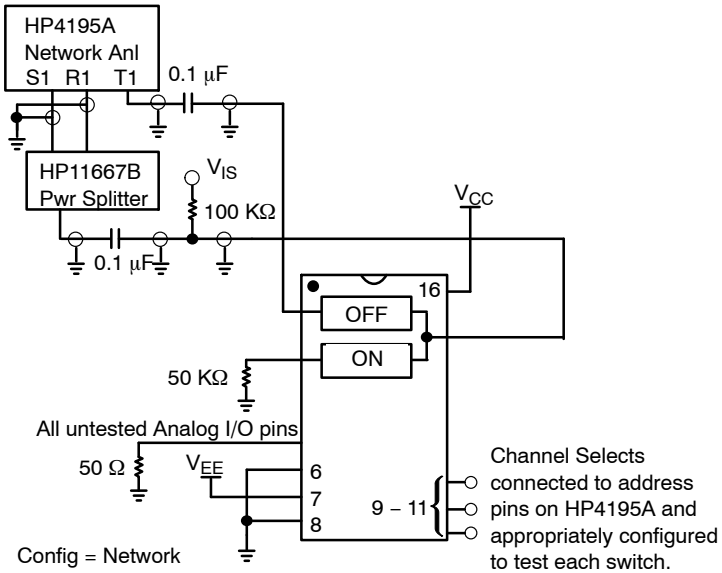

**Figure 7. Maximum On Channel Bandwidth, Test Set–Up**




Config = Network
Format = T/R (dB)
CAL = Trans Cal
Display = Rectan X − A + B
Scale Ref = Auto Scale
View = Off, Off, Off
Trig = Cont Mode
Source Amplitude = + 13 dB
Reference Attenuation = 20 dB
Test Attenuation = 0 dB

$V_{ISO}(dB) = 20 \log (V_{T1}/V_{R1})$

**Figure 8. Maximum Off Channel Feedthrough Isolation, Test Set−Up**




Config = Network
Format = T/R (dB)
CAL = Trans Cal
Display = Rectan X − A + B
Scale Ref = Auto Scale
View = Off, Off, Off
Trig = Cont Mode
Source Amplitude = + 13 dB
Reference Attenuation = 20 dB
Test Attenuation = 0 dB

$V_{ISOC}(dB) = 20 \log (V_{T1}/V_{R1})$

**Figure 9. Maximum Common−Channel Feedthrough Isolation, Test Set−Up**

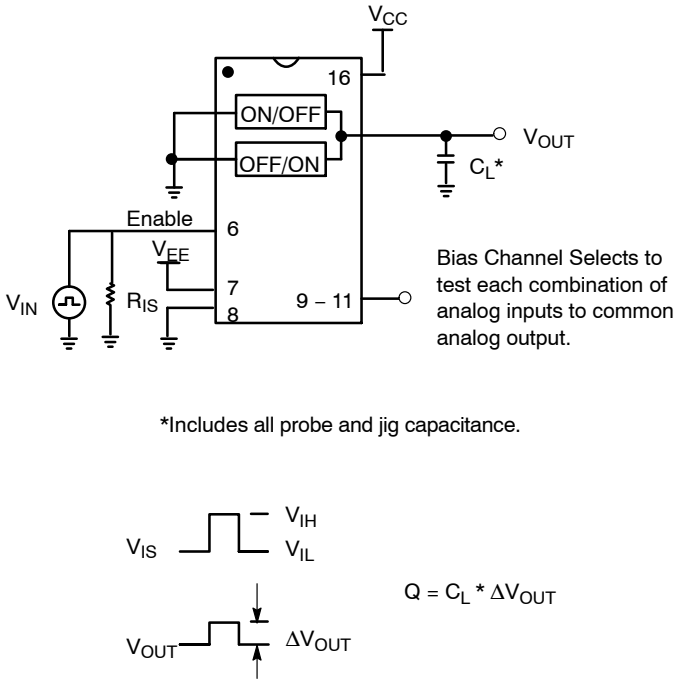



**Figure 10. Charge Injection, Test Set−Up**

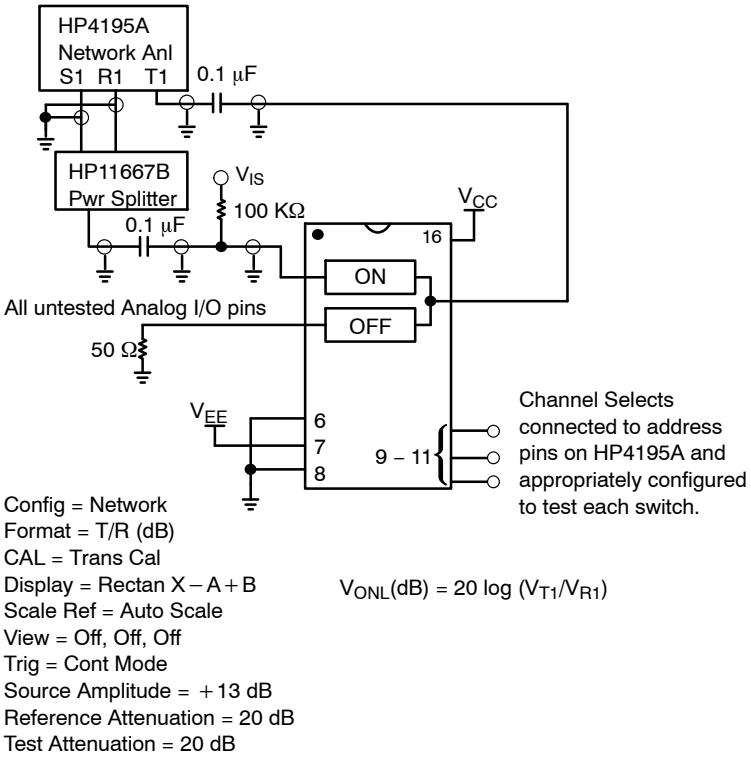



**Figure 11. Maximum On Channel Feedthrough On Loss, Test Set−Up**

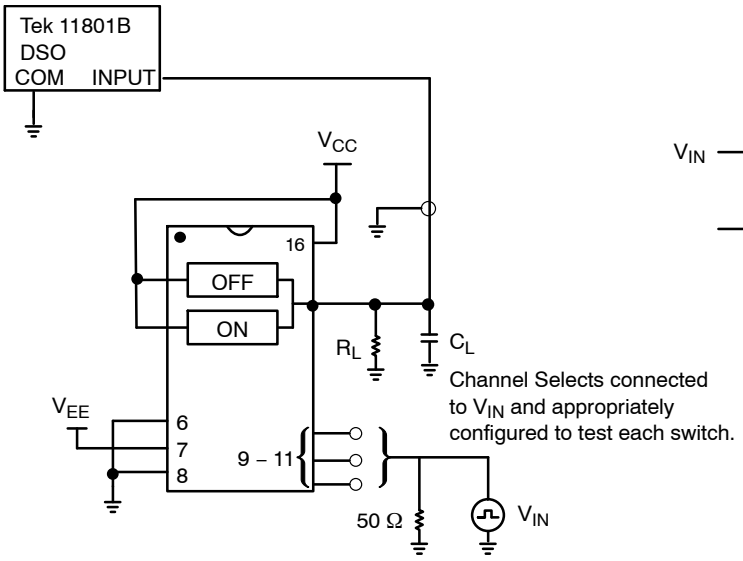



**Figure 12. Break–Before–Make, Test Set–Up**

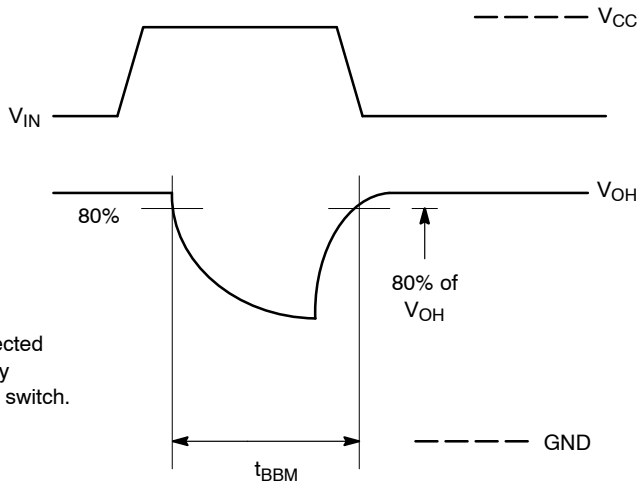



**Figure 13. Break–Before–Make Time**

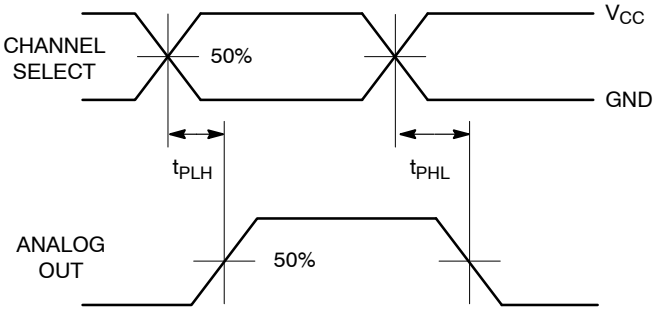
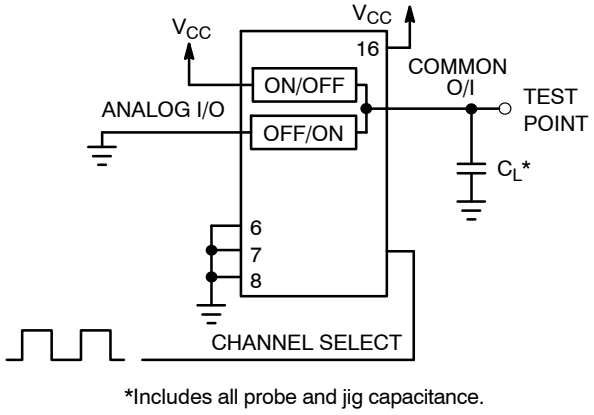



**Figure 14. Propagation Delays, Channel Select to Analog Out**




*Includes all probe and jig capacitance.

**Figure 15. Propagation Delay, Test Set–Up Channel Select to Analog Out**

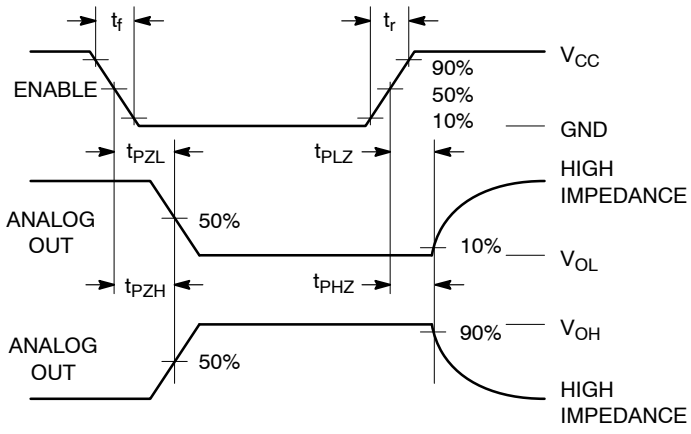



**Figure 16. Propagation Delays, Enable to Analog Out**

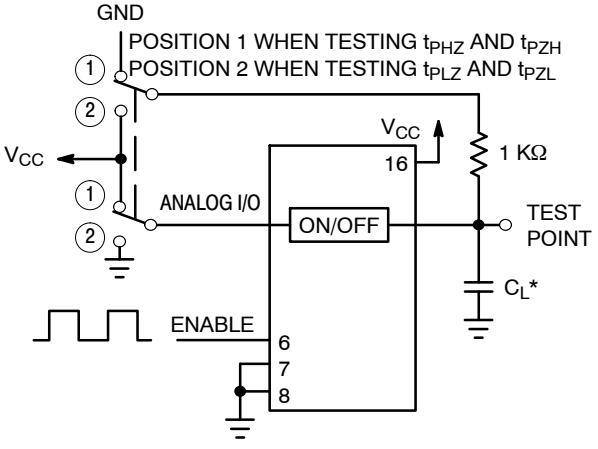



**Figure 17. Propagation Delay, Test Set–Up Enable to Analog Out**

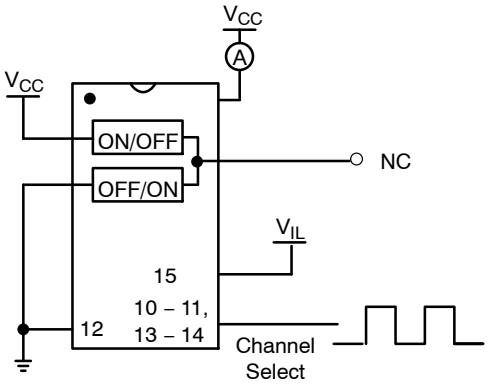



**Figure 18. Power Dissipation Capacitance, Test Set−Up**

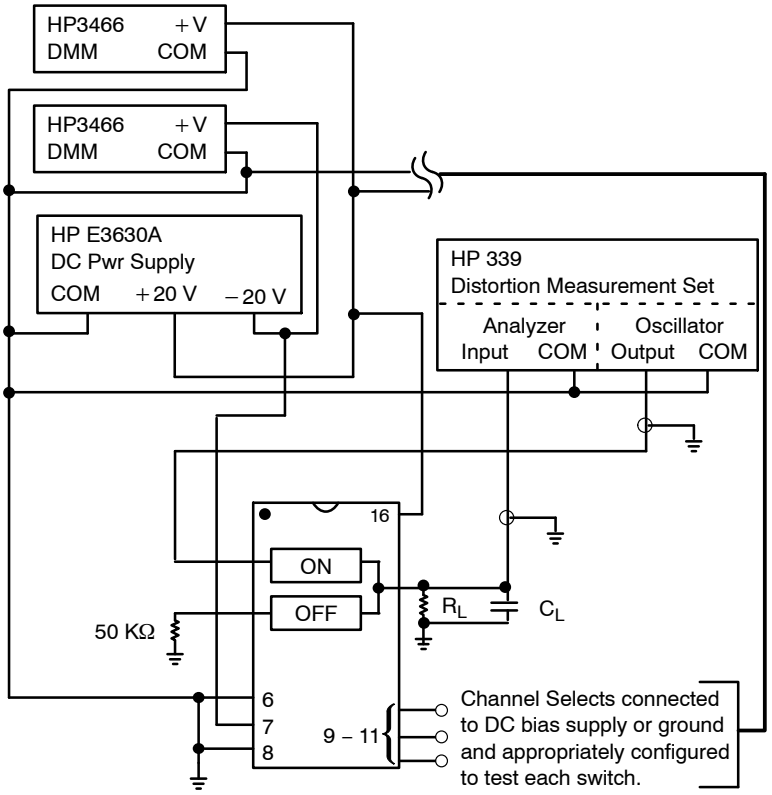



**Figure 19. Total Harmonic Distortion, Test Set−Up**

## APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at $V_{CC}$ or GND logic levels. $V_{CC}$ being recognized as a logic high and GND being recognized as a logic low. In this example:

$$V_{CC} = +5\ V = \text{logic high}$$
$$GND = 0\ V = \text{logic low}$$

The maximum analog voltage swing is determined by the supply voltages $V_{CC}$ and $V_{EE}$. The positive peak analog voltage should not exceed $V_{CC}$. Similarly, the negative peak analog voltage should not go below $V_{EE}$. In this example, the difference between $V_{CC}$ and $V_{EE}$ is 5.0 volts. Therefore, using the configuration of Figure 21, a maximum analog signal of 5.0 volts peak−to−peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to $V_{CC}$ or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$$V_{EE} - GND = 0 \text{ to } -6 \text{ volts}$$
$$V_{CC} - GND = 2.5 \text{ to } 6 \text{ volts}$$
$$V_{CC} - V_{EE} = 2.5 \text{ to } 6 \text{ volts}$$
$$\text{and } V_{EE} \leq GND$$

When voltage transients above $V_{CC}$ and/or below $V_{EE}$ are anticipated on the analog channels, external Germanium or Schottky diodes ($D_x$) are recommended as shown in Figure 22. These diodes should be able to absorb the maximum anticipated current surges during clipping.

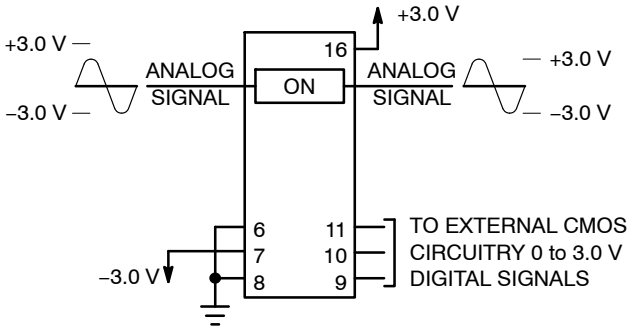



**Figure 20. Application Example**

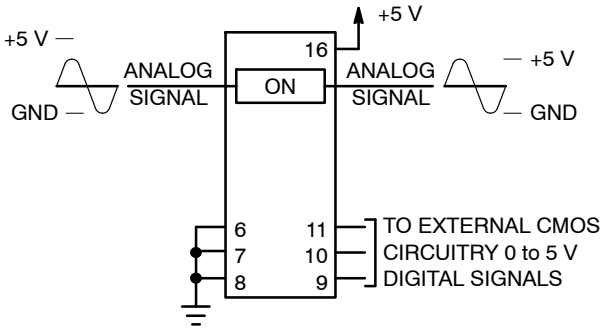



**Figure 21. Application Example**

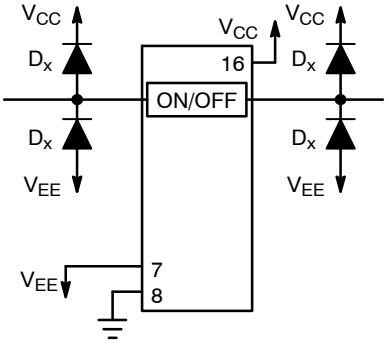



**Figure 22. External Germanium or Schottky Clipping Diodes**

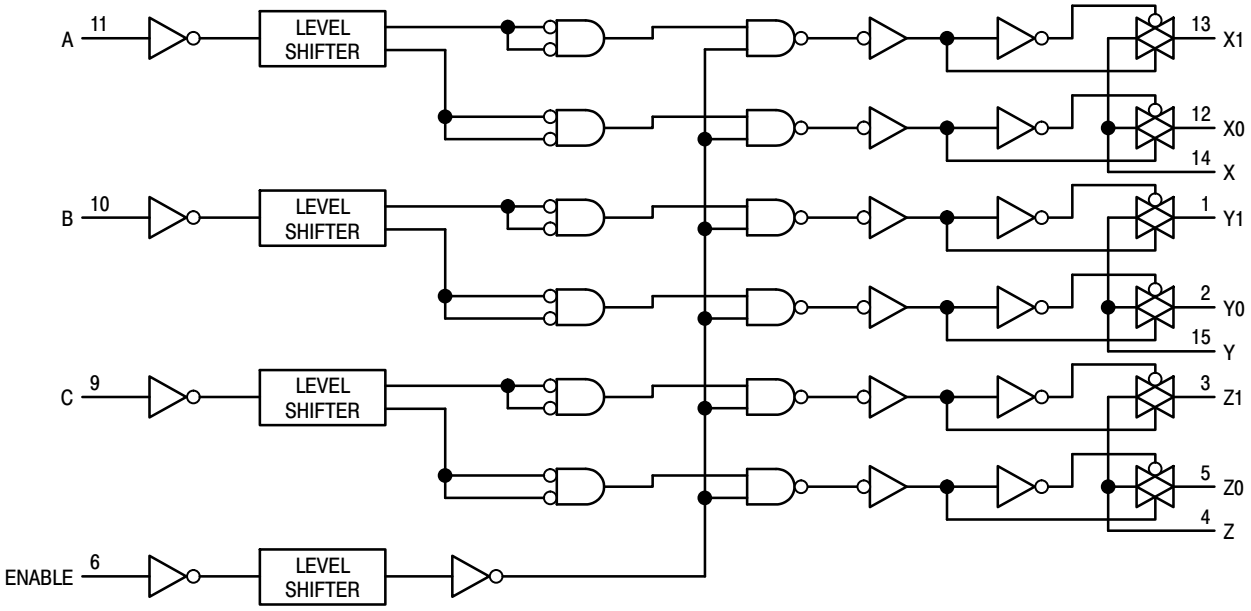
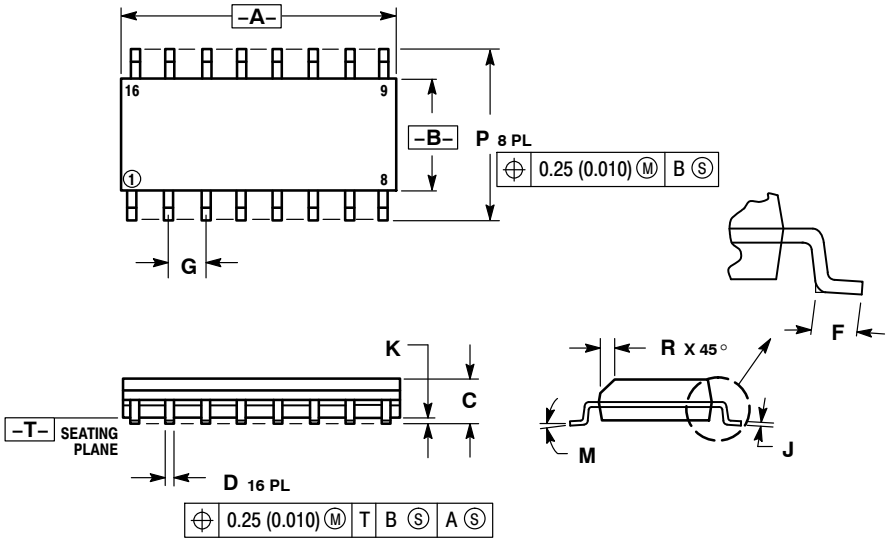



**Figure 23. Function Diagram, LVX4053**

## PACKAGE DIMENSIONS

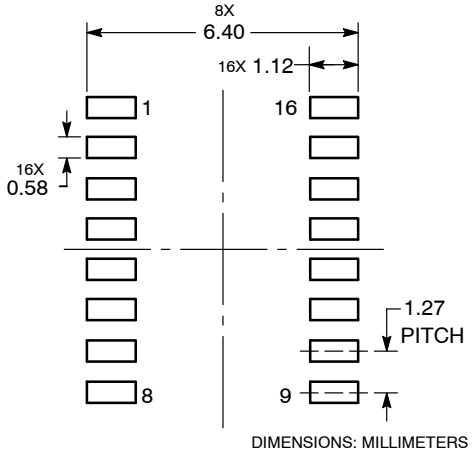
**SOIC−16**
**D SUFFIX**
CASE 751B−05
ISSUE K




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

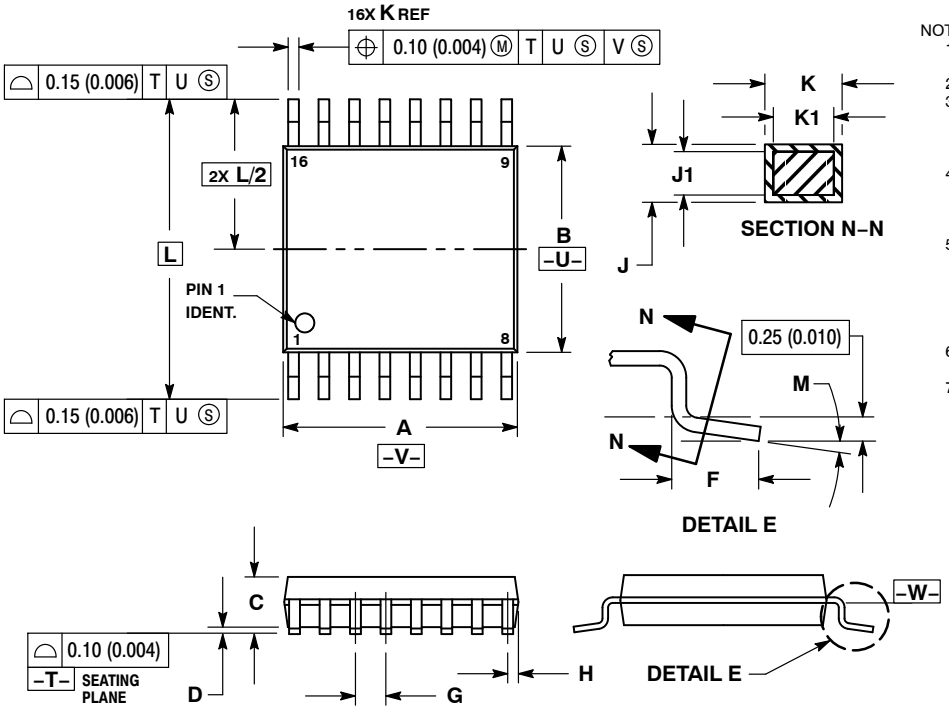
## SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

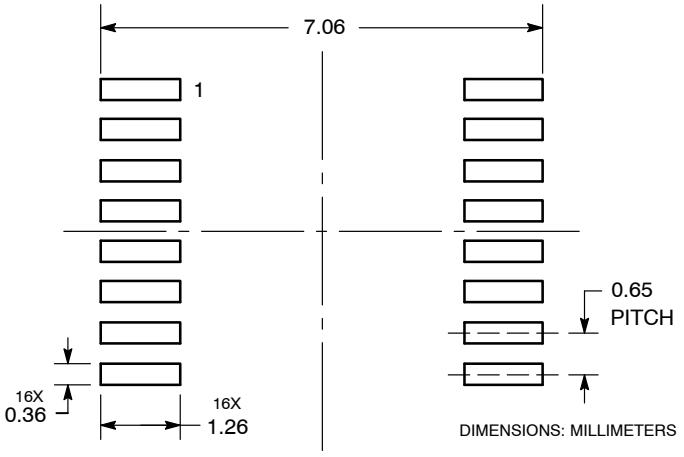
**TSSOP−16**
**DT SUFFIX**
CASE 948F−01
ISSUE B




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

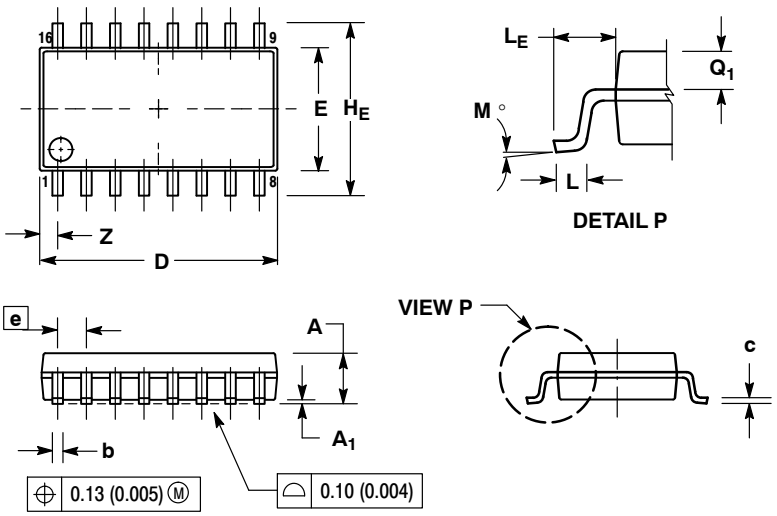
### SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

**SOEIAJ−16**
**M SUFFIX**
CASE 966−01
ISSUE A




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| $A_1$ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.10 | 0.20 | 0.007 | 0.011 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| $H_E$ | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| $L_E$ | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| $Q_1$ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.78 | --- | 0.031 |

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