

PH4530L

N-channel TrenchMOS™ logic level FET

Rev. 02 — 26 January 2005

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode field effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Low thermal resistance
- Logic level gate drive
- SO8 equivalent area footprint
- Low on-state resistance.

1.3 Applications

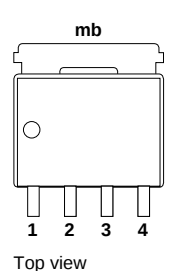
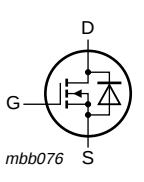
- DC-to-DC converters
- Portable appliances
- Switched-mode power supplies
- Notebook computers.

1.4 Quick reference data

- $V_{DS} \leq 30 \text{ V}$
- $I_D \leq 80 \text{ A}$
- $P_{tot} \leq 62.5 \text{ W}$
- $R_{DS(on)} \leq 5.7 \text{ m}\Omega$.

2. Pinning information

Table 1: Discrete pinning

Pin	Description	Simplified outline	Symbol
1,2,3	source	 Top view SOT669 (LFPACK)	
4	gate		
mb	mounting base; connected to drain		

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3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PH4530L	LFAK	plastic single-ended surface mounted package (LFAK); 4 leads	SOT669

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

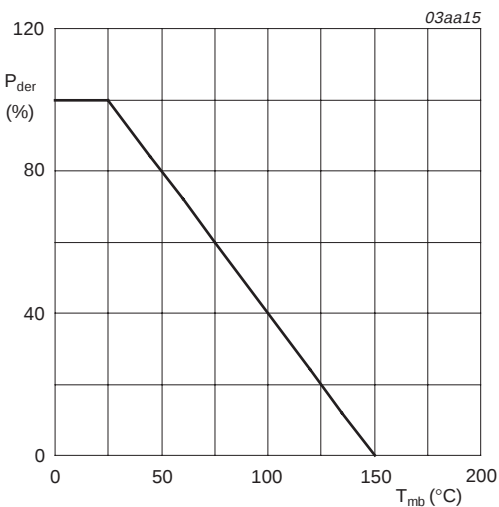
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2 and 3	-	80	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2	-	240	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	50.7	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Figure 1	-	62.5	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C

Source-drain diode

I_S	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	52	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	150	A

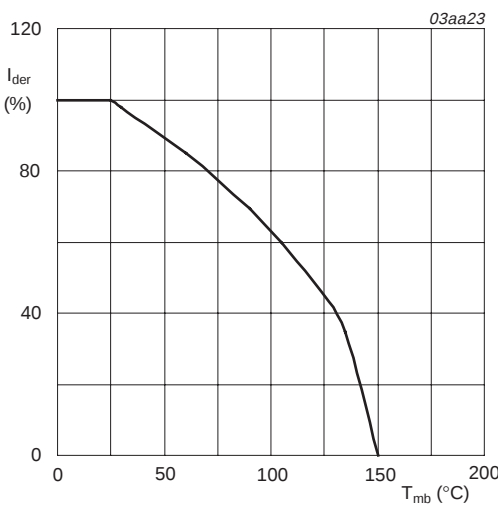
Avalanche ruggedness

$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 36.2\text{ A}$; $t_p = 0.24\text{ ms}$; $V_{DD} \leq 30\text{ V}$; $V_{GS} = 10\text{ V}$; starting $T_j = 25\text{ °C}$	-	130	mJ
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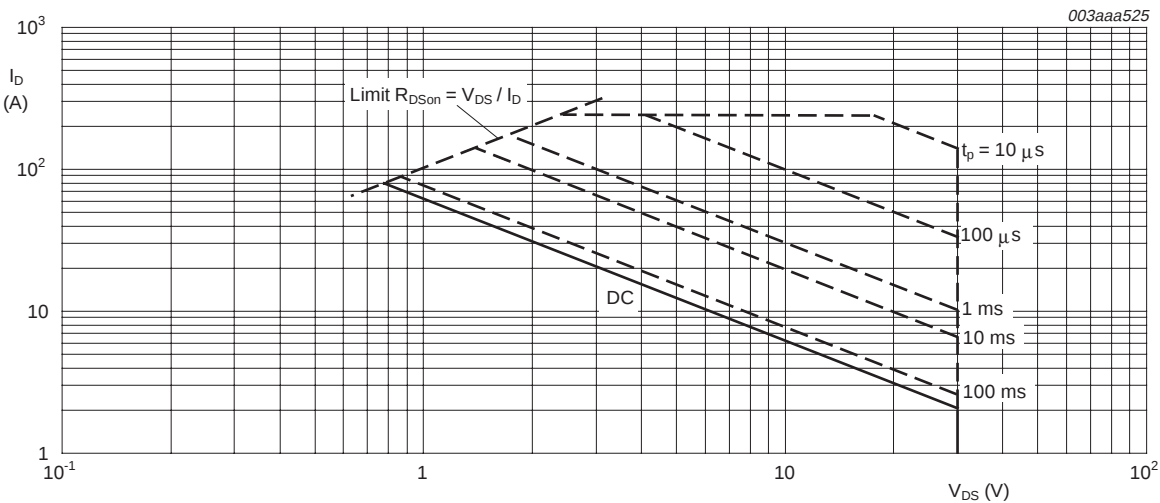
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse

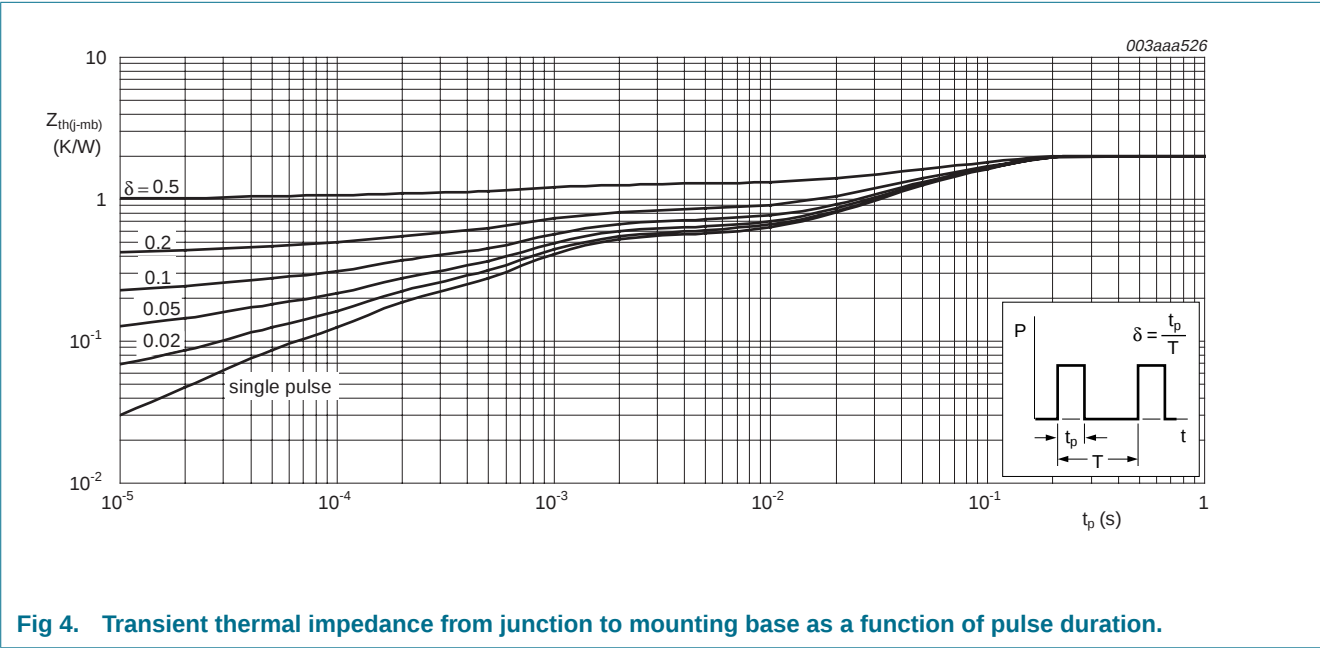
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	2	K/W

5.1 Transient thermal impedance

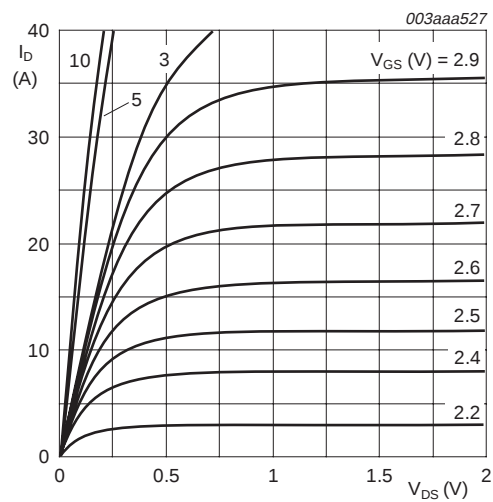


6. Characteristics

Table 5: Characteristics

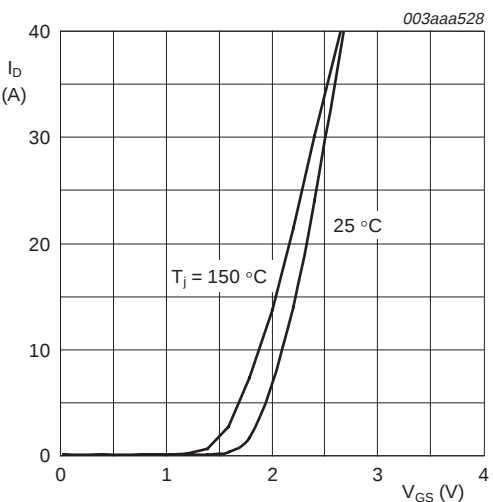
$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V	30	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; Figure 9	1	1.5	2	V
I _{DSS}	drain-source leakage current	V _{DS} = 30 V; V _{GS} = 0 V				
		T _j = 25 °C	-	0.06	1	μA
		T _j = 150 °C	-	-	500	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±15 V; V _{DS} = 0 V	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 15 A; Figure 7 and 8				
		T _j = 25 °C	-	4.8	5.7	mΩ
		T _j = 150 °C	-	8.2	9.7	mΩ
		V _{GS} = 5 V; I _D = 15 A; Figure 7 and 8	-	5.8	7.2	mΩ
Dynamic characteristics						
Q _{g(tot)}	total gate charge	I _D = 25 A; V _{DS} = 10 V; V _{GS} = 5 V; Figure 13	-	23.5	-	nC
Q _{gs}	gate-source charge		-	5.8	-	nC
Q _{gd}	gate-drain (Miller) charge		-	6.5	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 10 V; f = 1 MHz; Figure 11	-	1972	-	pF
C _{oss}	output capacitance		-	769	-	pF
C _{rss}	reverse transfer capacitance		-	304	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 10 V; I _D = 25 A;	-	22	-	ns
t _r	rise time	V _{GS} = 5 V; R _G = 4.7 Ω	-	40	-	ns
t _{d(off)}	turn-off delay time		-	48	-	ns
t _f	fall time		-	18	-	ns
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 15 A; V _{GS} = 0 V; Figure 12	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = −100 A/μs; V _{GS} = 0 V	-	38	-	ns



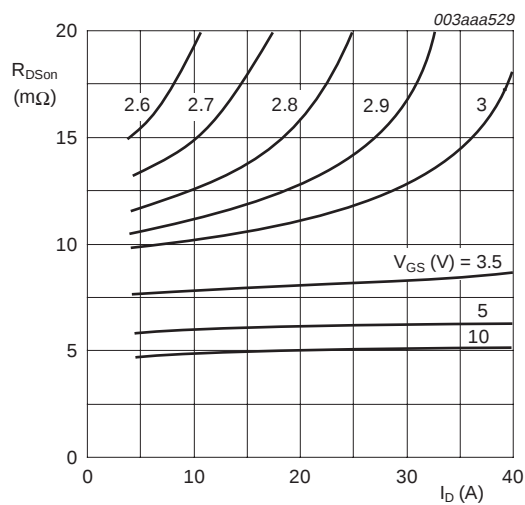
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



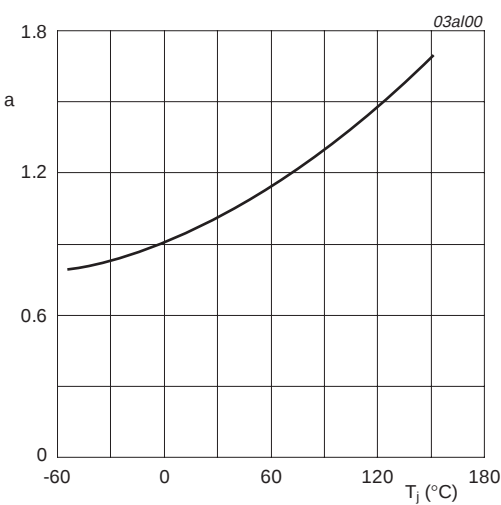
$T_j = 25^\circ\text{C}$ and 150°C ; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



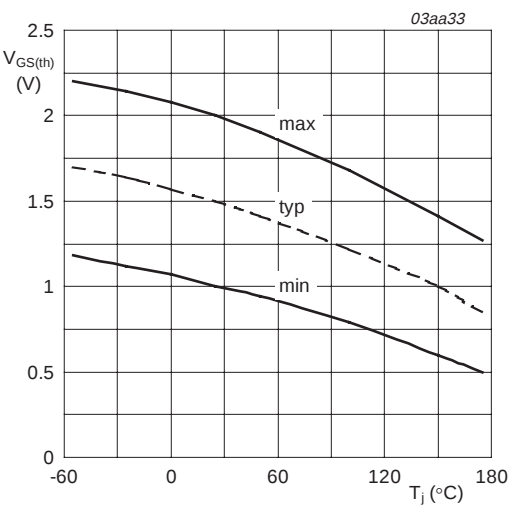
$T_j = 25^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



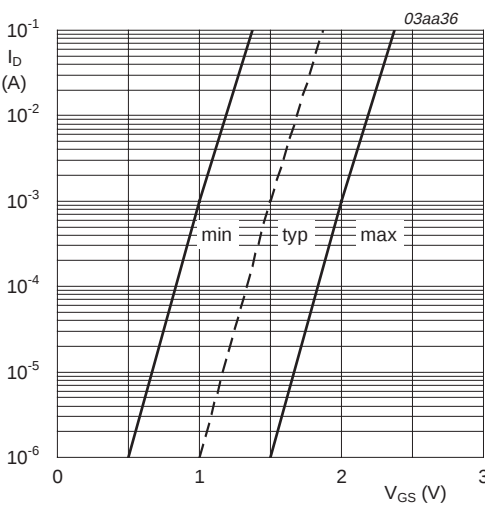
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



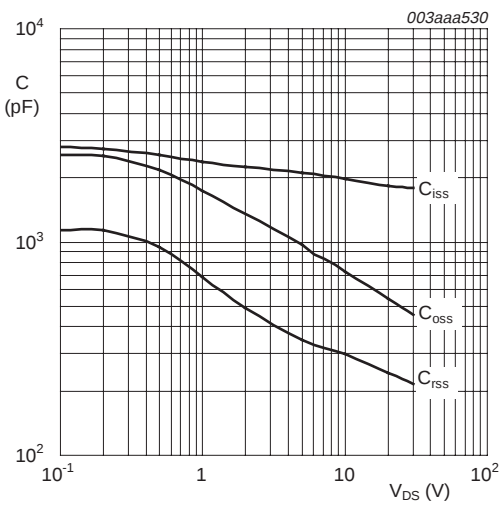
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



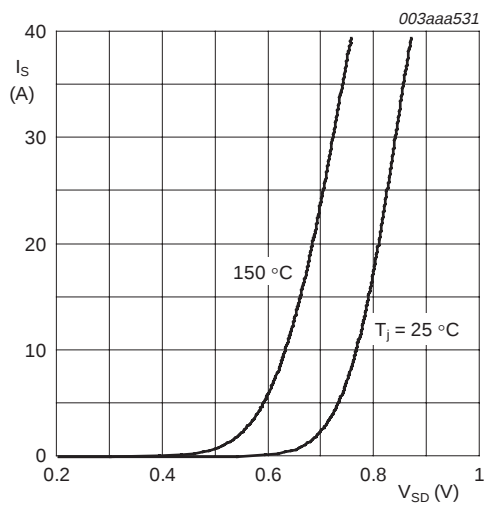
$T_j = 25\text{ °C}; V_{DS} = 5\text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



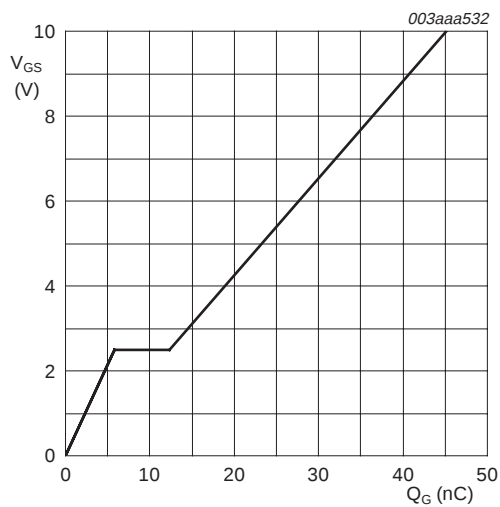
$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



Tj = 25 °C and 150 °C; VGS = 0 V

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



ID = 25 A; VDD = 10 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

Plastic single-ended surface mounted package (LPAK); 4 leads

SOT669

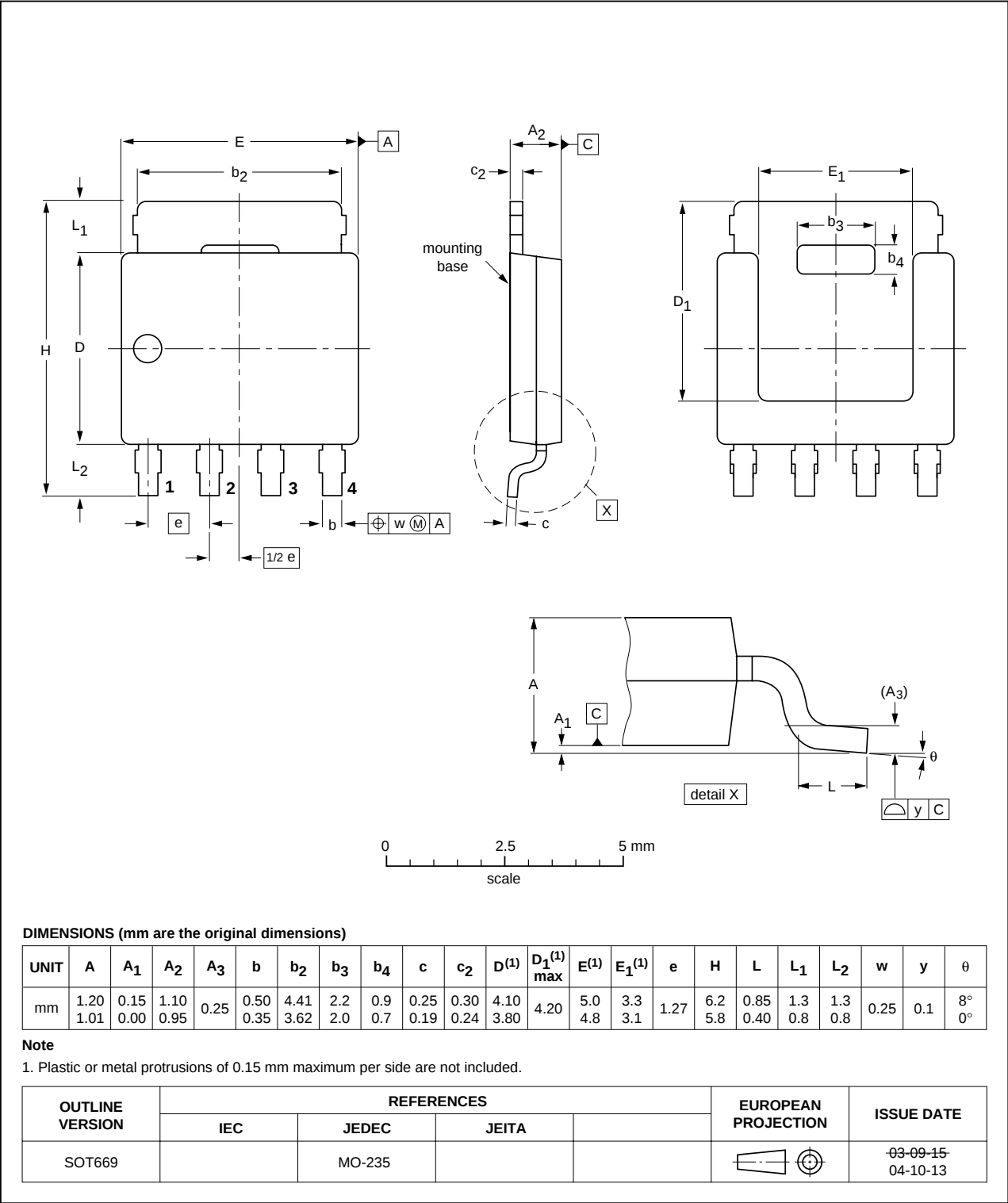


Fig 14. SOT669 (LPAK) package outline.

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PH4530L_2	20050126	Product data sheet	-	9397 750 14031	PH4530L_1
Modifications:		• Section 1.4 "Quick reference data" I_D and R_{DSon} values updated • Table 3 "Limiting values" I_D and I_{DM} values updated • Figure 3, Figure 6, Figure 11 and Figure 13 updated • Table 5 "Characteristics" R_{DSon}, $Q_{g(tot)}$, Q_{gs}, Q_{gd}, C_{iss}, C_{oss} and C_{rss} values updated.			
PH4530L_1	20040304	Preliminary data sheet	-	9397 750 12813	-

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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