8 W auxiliary SMPS for air-conditioner using ICE5AR4770BZS

REF_5AR4770BZS_8W1

About this document

Scope and purpose

This document is a reference design for an 8 W auxiliary SMPS for air-conditioner with the latest Infineon fifth-generation fixed-frequency CoolSET™ ICE5AR4770BZS. The power supply is designed with a universal input compatible with most geographic regions and isolated output (+12 V/1.25 A and +5 V/0.50 A) as typically employed in most home appliances.

Highlights of the auxiliary power supply for an air-conditioner:

- High efficiency under light-load conditions to meet ENERGY STAR requirements
- Simplified circuitry with good integration of power and protection features
- Auto-restart protection scheme to minimize interruption to enhance end-user experience

Intended audience

This document is intended for power supply design or application engineers, etc. who want to design auxiliary power supplies for air-conditioners that are efficient under light-load conditions, reliable and easy to design.

Table of contents

About this document 1
Table of contents 1
1 System introduction 3
1.1 High efficiency under light-load conditions to meet ENERGY STAR requirements 3
1.2 Simplified circuitry with good integration of power and protection features 4
1.3 Auto-restart protection scheme to minimize interruption and enhance end-user experience 4
2 Reference design board 5
3 Power supply specifications 6
4 Circuit diagram 7
5 Circuit description 8
5.1 EMI filtering and line rectification 8
5.2 Flyback converter power stage 8
5.3 Control of flyback converter through fifth-generation fixed-frequency CoolSET™ ICE5AR4770BZS 8
5.3.1 Integrated HV power MOSFET 8
5.3.2 Current Sensing (CS) 8
5.3.3 Feedback (FB) and compensation network 9
5.4 Unique features of the fifth generation fixed-frequency CoolSET™ ICE5AR4770BZS 9
5.4.1 Fast self-start-up and sustaining of V_{CC} 9
5.4.2 CCM, DCM operation with frequency reduction 9
5.4.3 Frequency jittering with modulated gate drive 10
5.4.4 System robustness and reliability through protection features 10

5.5 Clamper circuit ... 10
5.6 PCB design tips ... 10
5.7 EMI reduction tips ... 11
6 PCB layout ... 12
6.1 Top side ... 12
6.2 Bottom side ... 12
7 BOM ... 13
8 Transformer specification ... 14
9 Measurement data and graphs ... 15
9.1 Efficiency ... 16
9.2 Standby power ... 17
9.3 Line regulation ... 17
9.4 Load regulation ... 18
9.5 Maximum input power ... 18
9.6 Frequency reduction ... 19
9.7 ESD immunity (EN 61000-4-2) ... 19
9.8 Surge immunity (EN 61000-4-5) ... 19
9.9 Conducted emissions (EN 55022 class B) ... 20
9.10 Thermal measurement ... 22
10 Waveforms and oscilloscope plots ... 23
10.1 Start-up at full load ... 23
10.2 Soft-start at full load ... 23
10.3 Drain and CS voltage at full load ... 24
10.4 Frequency jittering at full load ... 24
10.5 Load transient response (dynamic load from 10 percent to 100 percent) ... 25
10.6 Output ripple voltage at full load ... 25
10.7 Output ripple voltage at ABM (0.1 W load) ... 26
10.8 Entering ABM ... 26
10.9 During ABM ... 27
10.10 Leaving ABM ... 27
10.11 V_{CC} OVP/UVP ... 28
10.12 Over-load protection ... 28
10.13 V_{CC} short-to-GND ... 29
11 Appendix A: Transformer design and spreadsheet [3] ... 30
12 Appendix B: WE transformer specification ... 38
13 References ... 39
Revision history ... 40

1 System introduction

With the growing household trend for internet-connected devices, the new generation of home appliances such as air-conditioners are equipped with advanced features such as wireless control and monitoring capability, smart sensors and touch screen display. These will transform a static product into an interactive and intelligent home appliance, capable of adapting to the smart-home theme. To support this trend, Infineon has introduced the latest fifth-generation fixed-frequency CoolSET™ to address this need in an efficient and cost-effective manner.

An auxiliary SMPS is needed to power the various modules and sensors, which typically operate from a stable DC voltage source. The Infineon fifth-generation fixed-frequency CoolSET™ (as shown in Figure 1) forms the heart of the system, providing the necessary protection and AC-DC conversion from the mains to multiple regulated DC voltages to power the various blocks.

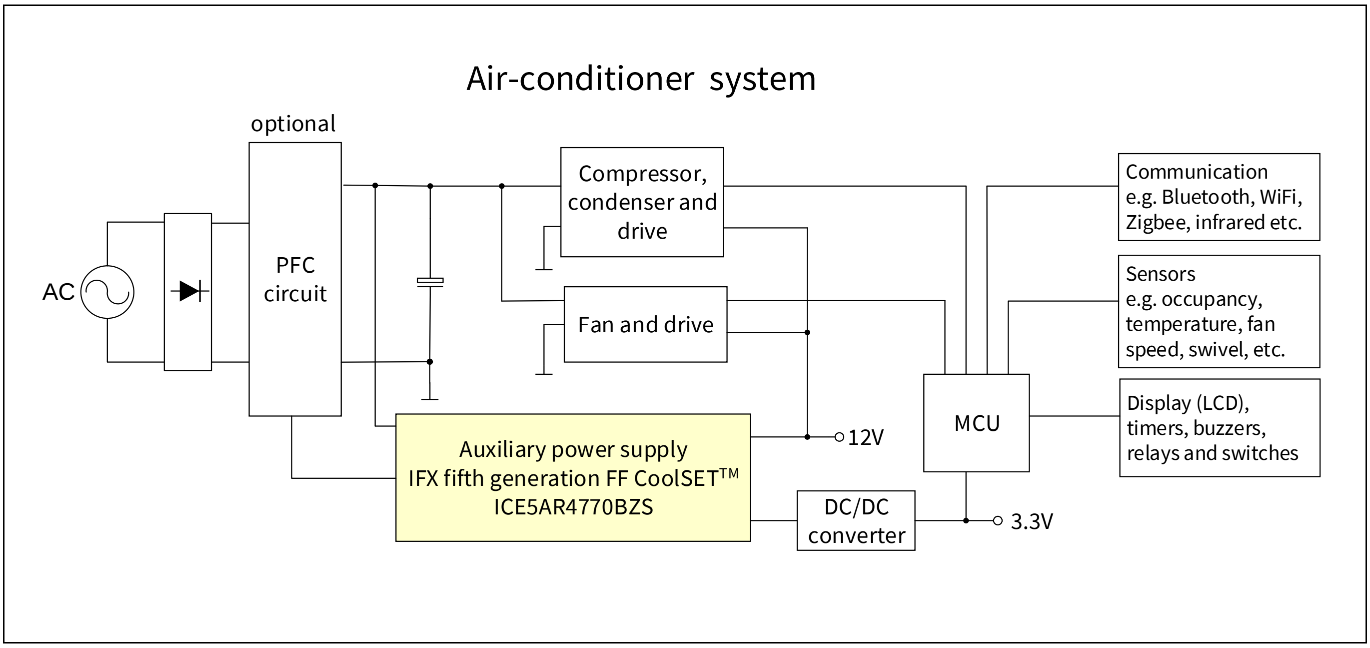


Figure 1 Simplified air-conditioner system block diagram

Table 1 lists the system requirements for an air-conditioner, and the corresponding Infineon solution is shown in the right-hand column.

Table 1 System requirements and Infineon solutions

	System requirement for air-conditioner	Infineon solution – ICE5AR4770BZS
1	High efficiency under light-load conditions to meet ENERGY STAR requirements	New fixed-frequency control and Active Burst Mode (ABM)
2	Simplified circuitry with good integration of power and protection features	Embedded 700 V MOSFET and controller in DIP-7 package
3	Auto-restart protection scheme to minimize interruption to enhance end-user experience	All abnormal protections are in auto-restart mode

1.1 High efficiency under light-load conditions to meet ENERGY STAR requirements

During typical air-conditioner operation, the power requirement fluctuates according to various use cases. However, in most cases where room temperature is already stabilized, the air-conditioner will reside in an idle state in which the loading toward the auxiliary power supply is low. It is crucial that the auxiliary power supply operates as efficiently as possible, because it will be in this particular state for most of the period. Under light-load conditions, losses incurred with the power switch are usually dominated by the switching operation. The choice of switching scheme and frequency plays a crucial role in ensuring high conversion efficiency.

In this reference design, ICE5AR4770BZS was primarily chosen due to its frequency reduction switching scheme. Compared with a traditional fixed-frequency flyback, the CoolSET™ reduces its switching frequency from medium to light load, thereby minimizing switching losses. Therefore, an efficiency of more than 80 percent is achievable under 25 percent loading conditions.

1.2 Simplified circuitry with good integration of power and protection features

To relieve the designer of the complexity of PCB layout and circuit design, CoolSET™ is a highly integrated device with both a controller and HV MOSFET integrated in a single, space-saving DIP-7 package. These certainly help the designer to reduce component count as well as simplifying the layout into a single-layer PCB design for ease of manufacturing, using the traditional cost-effective wave-soldering process.

1.3 Auto-restart protection scheme to minimize interruption and enhance end-user experience

For an air-conditioner, it would be annoying to both the end user and the manufacturer if the system were to halt and latch after protection. To minimize interruption, the CoolSET™ implements auto-restart mode for all abnormal protections.

2 Reference design board

This document provides complete design details including specifications, schematics, Bill of Materials (BOM), PCB layout, and transformer design and construction information. Performance results pertaining to line/load regulation, efficiency, transient load, thermal conditions, conducted EMI scans and so on are also included.

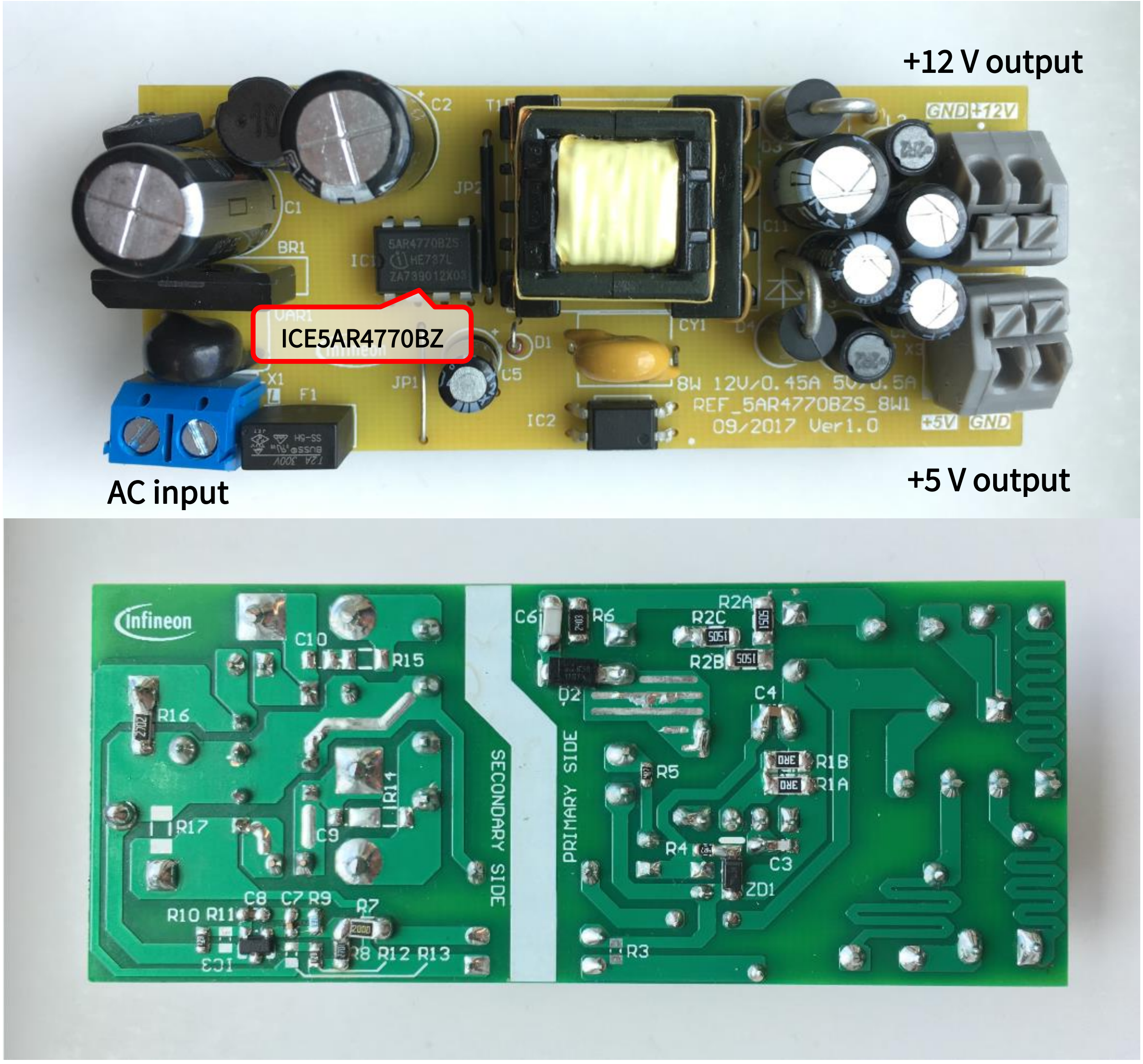


Figure 2 REF_5AR4770BZS_8W1

3 Power supply specifications

The table below represents the minimum acceptance performance of the design. Actual performance is listed in the measurements section.

Table 2 Specifications of REF_5AR4770BZS_8W1

Description	Symbol	Min.	Typ.	Max.	Units	Comments
Input						
Voltage	V_{IN}	85	–	265	V AC	Two wires (no P.E.)
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load input power	P_{stby_NL}	–	–	40	mW	
Output						
Output voltage 1	V_{OUT1}	–	12	–	V	± 15 percent
Output current 1	I_{OUT1}	60	–	450	mA	
Output voltage ripple 1	$V_{RIPPLE1}$	–	–	100	mV	20 MHz BW
Output voltage 2	V_{OUT2}	–	5	–	V	± 1 percent
Output current 2	I_{OUT2}	10	–	500	mA	
Output voltage ripple 2	$V_{RIPPLE2}$	–	–	100	mV	20 MHz BW
Max. power output	P_{OUT_Max}	–	–	7.9	W	
Efficiency						
Max. load	η	–	83	–	Percent	115 V AC/230 V AC
Average efficiency at 25 percent, 50 percent, 75 percent and 100 percent of P_{OUT_Max}	η_{avg}	82	–	–	Percent	115 V AC/230 V AC
Environmental						
Conducted EMI		6	–	–	dB	Margin, CISPR 22 class B
ESD		10	–	–	kV	EN 61000-4-2
Surge immunity						EN 61000-4-5
Differential mode		2	–	–	kV	
Common mode		4	–	–	kV	
Ambient temperature	T_{amb}	0	–	50	°C	Free convection, sea level
Form factor		85 × 35 × 25			mm^3	L × W × H

4 Circuit diagram

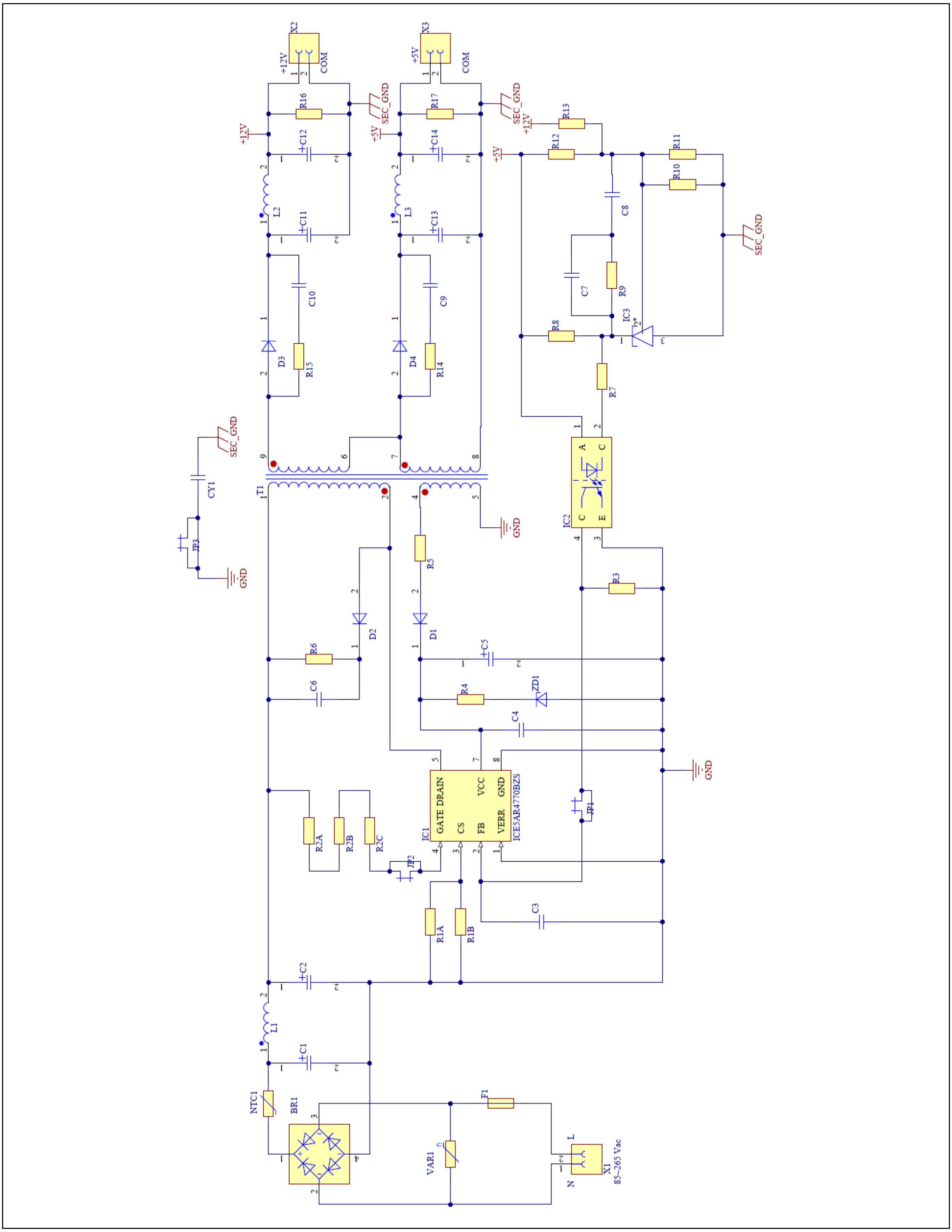


Figure 3 Schematic of REF_5AR4770BZS_8W1

5 Circuit description

In this section, the design circuit for the SMPS unit will be briefly described by the different functional blocks. For details of the design procedure and component selection for the flyback circuitry please refer to the IC design guide [2] and calculation tool [3].

5.1 EMI filtering and line rectification

The input of power supply unit is taken from the AC power grid, which is in the range of 85 V AC ~ 265 V AC. The fuse F1 is directly connected to the input line to protect the system in case of excess current entering the system circuit due to any fault. Following is the varistor VAR1, which is connected across the input to absorb excessive energy during line surge transient. The bridge rectifier BR1 rectifies the AC input into DC voltage, filtered by the bulk capacitors C1 and C2. Resistor NTC1 not only reduces the inrush current during start-up but it also helps reduce the voltage increase on the bulk capacitors C1 and C2 during line surge transients. Inductor L1 and capacitors C1 and C2 form a π filter to attenuate EMI noise.

5.2 Flyback converter power stage

The flyback converter power stage consists of transformer T1, a primary HV MOSFET (integrated into ICE5AR4770BZS), secondary rectification diodes D3 and D4, secondary output capacitors C11, C12, C13 and C14 and output filter inductors L2 and L3.

When the primary HV MOSFET turns on, energy is stored in the transformer. When it turns off, the stored energy is discharged to the output capacitors and into the output load.

Primary winding has two layers placed back to back for higher winding capacitance. This can reduce EMI by slowing the MOSFET switching. However, this can reduce efficiency. Winding capacitance can be tuned by adding a number of isolation tapes between the layers, depending on the EMI or efficiency need. If efficiency is a priority, interlacing primary and secondary winding is recommended, as it has lower leakage inductance. As a result, the clamper circuit can be relaxed to reduce its power losses.

For the output rectification, lower forward voltage and ultra-fast recovery diodes can improve efficiency. Capacitors C11 and C13 store the energy needed during output load jumps. LC filters L2/C12 and L3/C14 reduce the HF ripple voltage.

5.3 Control of flyback converter through fifth-generation fixed-frequency CoolSET™ ICE5AR4770BZS

5.3.1 Integrated HV power MOSFET

The ICE5AR4770BZS CoolSET™ is a seven-pin device in a DIP-7 package. It has been integrated with the new fixed-frequency PWM controller and all necessary features and protections, and most importantly the 700 V power MOSFET, Infineon Superjunction (SJ) CoolMOS™. Hence, the schematic is much simplified and the circuit design is made much easier.

5.3.2 Current Sensing (CS)

The ICE5AR4770BZS is a current mode controller. The primary peak current is controlled cycle-by-cycle through the CS resistors R1A and R1B in the CS pin (pin 3). Transformer saturation can be avoided through Peak Current Limitation (PCL); therefore, the system is more protected and reliable.

5.3.3 Feedback (FB) and compensation network

V_{OUT} is sensed by resistor dividers R10, R11, R12 and R13 connected to the input of error amplifier TL431 (IC3). A type 2 compensation network (C7, C8 and R9) is connected to the input and output of IC3. The output of IC3 is coupled to the FB pin via optocoupler IC2.

The FB pin of ICE5AR4770BZS is a multi-function pin, which is used to select the entry/exit burst power level through the resistor at the FB pin (R3) and also the burst-on/burst-off sense input during ABM.

5.4 Unique features of the fifth generation fixed-frequency CoolSET™ ICE5AR4770BZS

5.4.1 Fast self-start-up and sustaining of V_{CC}

The IC uses a cascode structure to fast charge the V_{CC} capacitor. Pull-up resistors R2A, R2B and R2C connected to the GATE pin (pin 4) is used to initiate the start-up phase. At first, 0.2 mA is used to charge the V_{CC} capacitor from 0 V to 1.1 V. This is a protection which reduces the power dissipation of the IC during V_{CC} short-to-GND condition. Thereafter, a much higher charging current of 3.2 mA will charge the V_{CC} capacitor until the V_{CC_ON} is reached. Start-up time of less than 200 ms is achievable with V_{CC} capacitor of 22 µF.

After start-up, the IC V_{CC} supply is sustained by the auxiliary winding of transformer TR1, which needs to support the V_{CC} to be above Under Voltage Lockout (UVLO) voltage (10 V typ.) through the rectifier circuit D12, R12, R12A and C16.

5.4.2 CCM, DCM operation with frequency reduction

ICE5AR4770BZS can be operated in either Discontinuous Conduction Mode (DCM) or Continuous Conduction Mode (CCM) with frequency-reduction feature. This reference board is designed to operate in DCM. When the system is operating at high output load, the controller will switch at 100 kHz fixed frequency. In order to achieve a better efficiency between light load and medium load, frequency reduction is implemented as a function of V_{FB}, as shown in Figure 4. Switching frequency will not reduce further once the minimum switching frequency f_{OSC2_MIN} (43 kHz) is reached.

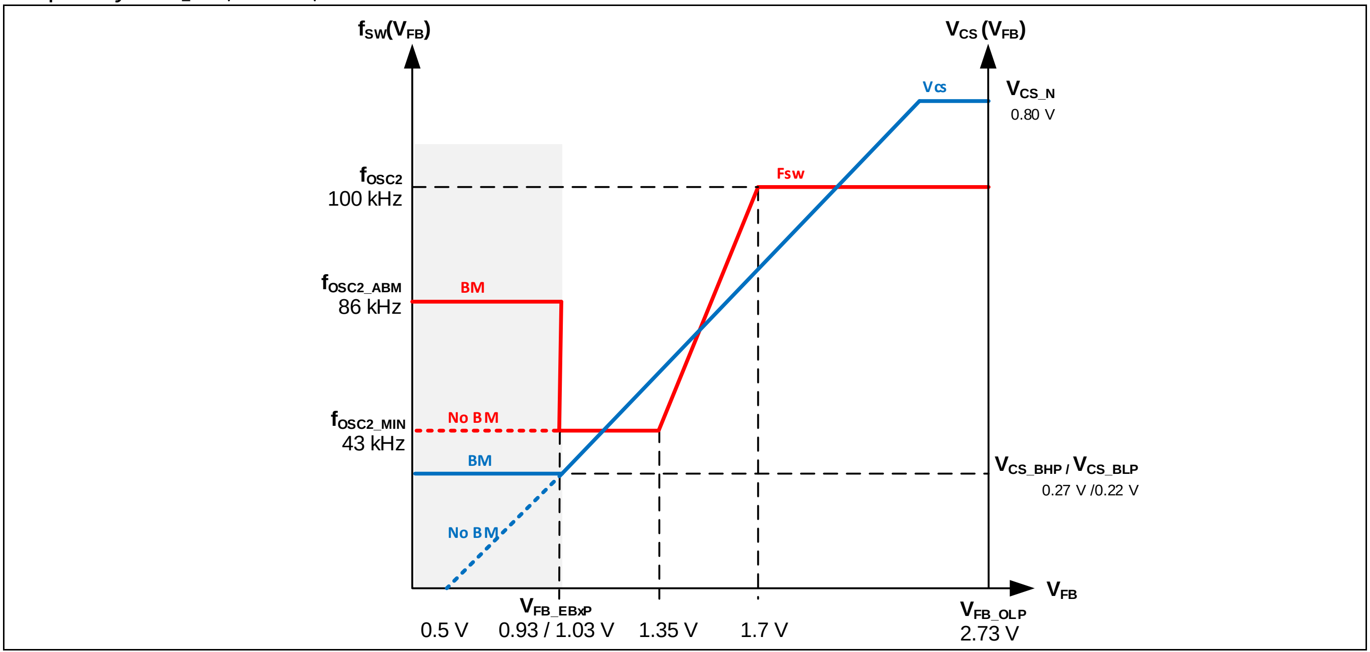


Figure 4 Frequency-reduction curve

5.4.3 Frequency jittering with modulated gate drive

The ICE5AR4770BZS has a frequency jittering feature with modulated gate drive to reduce the EMI noise. The jitter frequency is internally set at 100 kHz (±4 kHz), and the jitter period is 4 ms.

5.4.4 System robustness and reliability through protection features

Protection is one of the major factors in determining whether the system is safe and robust – therefore sufficient protection is necessary. ICE5AR4770BZS provides comprehensive protection to ensure the system is operating safely. This includes V_{CC} OV and UV, over-load, over-temperature (controller junction), CS short-to-GND and V_{CC} short-to-GND. When those faults are found, the system will enter into protection mode. Once the fault is removed, the system resumes normal operation. A list of protections and the failure conditions is shown in the table below.

Table 3 Protection functions of ICE5AR4770BZS

Protection function	Failure condition	Protection mode
V_{CC} OV	V_{VCC} greater than 25.5 V	Odd-skip auto restart
V_{CC} UV	V_{VCC} less than 10 V	Auto restart
Over-load	V_{FB} greater than 2.75 V and lasts for 54 ms	Odd-skip auto restart
Over-temperature (junction temperature of controller chip only)	T_J greater than 140°C	Non-switch auto restart
CS short-to-GND	V_{CS} less than 0.1 V, lasts for 0.4 µs and three consecutive pulses	Odd-skip auto restart
V_{CC} short-to-GND (V_{VCC} = 0 V, start-up = 50 MΩ and V_{DRAIN} = 90 V)	V_{VCC} less than 1.1 V, $I_{VCC\_Charge1}$ ≈ -0.2 mA	Cannot start up

5.5 Clamper circuit

A clamper network consisting of D2, C6 and R6 is used to reduce the switching voltage spikes on the DRAIN pin, which are generated by the leakage inductance of the transformer TR1. This is a dissipative circuit, therefore R6 and C6 need to be fine-tuned depending on the voltage derating factor and efficiency requirement.

5.6 PCB design tips

For a good PCB design layout, there are several points to note.

- The switching power loop needs to be as small as possible (see Figure 5). There are three power loops in the reference design; one on the primary side and two on the secondary side. The primary-side loop starts from the bulk capacitor (C2) positive terminal, goes through the primary transformer winding (pin 1 and pin 2 of T1), the DRAIN pin and CS pin of the CoolSET™ IC1, CS resistors R1A and R1B and back to the C2 negative terminal. The secondary-side loop starts at the 12 V output secondary transformer winding (pin 9 of T1), goes through output diode D3, output capacitor C11 and back to pin 8 of T1. Another loop on the secondary starts from the 5 V output secondary transformer winding (pin 6 and 7 of T1), output diode D4, output capacitor C13 and back to pin 8 of T1.
- Star-ground connection should be used to reduce HF noise coupling that can affect the functional operation. The ground of the small-signal components, e.g. C3 and C4, and the emitter of the optocoupler (pin 3 of IC2) should connect directly to the IC ground (pin 8 of IC1).

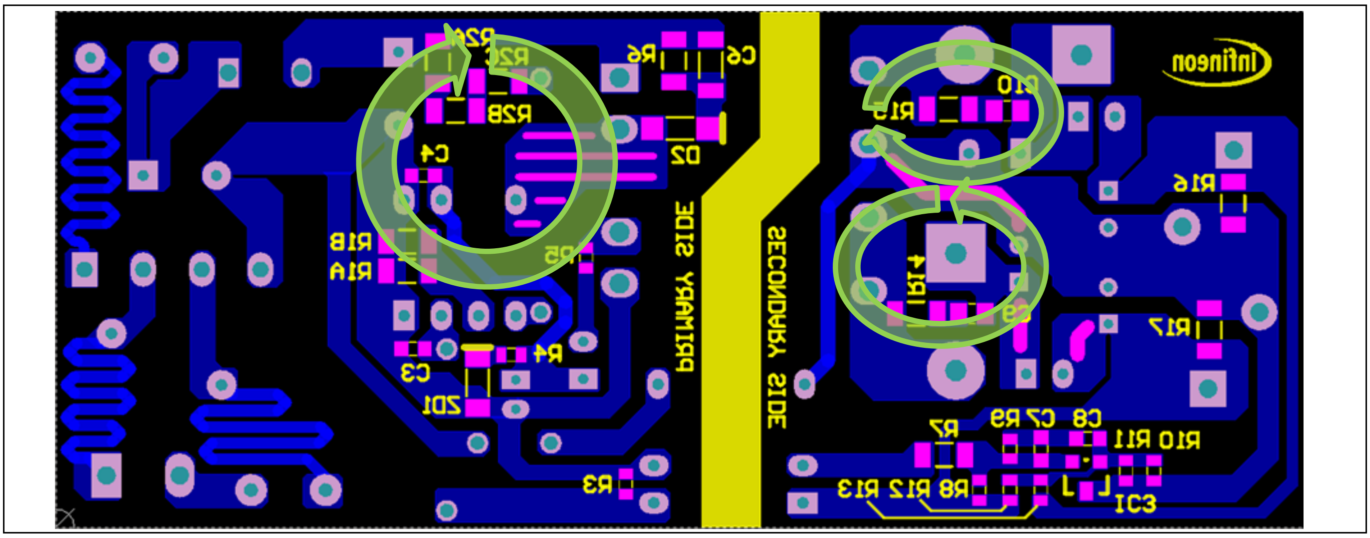


Figure 5 PCB layout tips

- Adding thin PCB track (zigzag trace) on the AC input side can increase input series resistance, which may eliminate the use of NTC1 to pass lower line surge requirements.
- Separating the HV components and LV components, e.g. clamper circuit D12, R6 and C6, at the top part of the PCB (see Figure 5) and the other LV components at the lower part of the PCB can reduce the spark-over chance of the high energy surge during ESD or a lightning surge test.
- Make the PCB copper pour area on the DRAIN pin as wide as possible to act as a heatsink for the CoolSET™.

5.7 EMI reduction tips

EMI compliance is always a challenge for the power supply designer. There are several critical points to consider in order to achieve a satisfactory EMI performance.

- A proper transformer design can significantly reduce EMI. Low leakage inductance can incur a low switching spike and HF noise. Interlaced winding technique is the most common practice to reduce leakage inductance. Winding shield, core shield and whole transformer shield are also some of the techniques used to reduce EMI.
- An input CMC and X-capacitor greatly reduce EMI but are costly and impractical, especially for low-power applications.
- Short-switching power-loop design in the PCB (as described in section 5.6) can reduce radiated EMI due to the antenna effect.
- The Y-capacitor CY1 dampens the HF noise generated between the primary and secondary, reducing the EMI noise.
- A secondary diode snubber circuit (R14/C9 and R15/C10) can reduce HF noise.
- Ferrite beads can reduce HF noise especially on criticical nodes such as the DRAIN pin, clamper diode and secondary diode terminals.
- The addition of output CMC is also effective where long cable wires are used to connect the output of the power supply to the load.

6 PCB layout

6.1 Top side

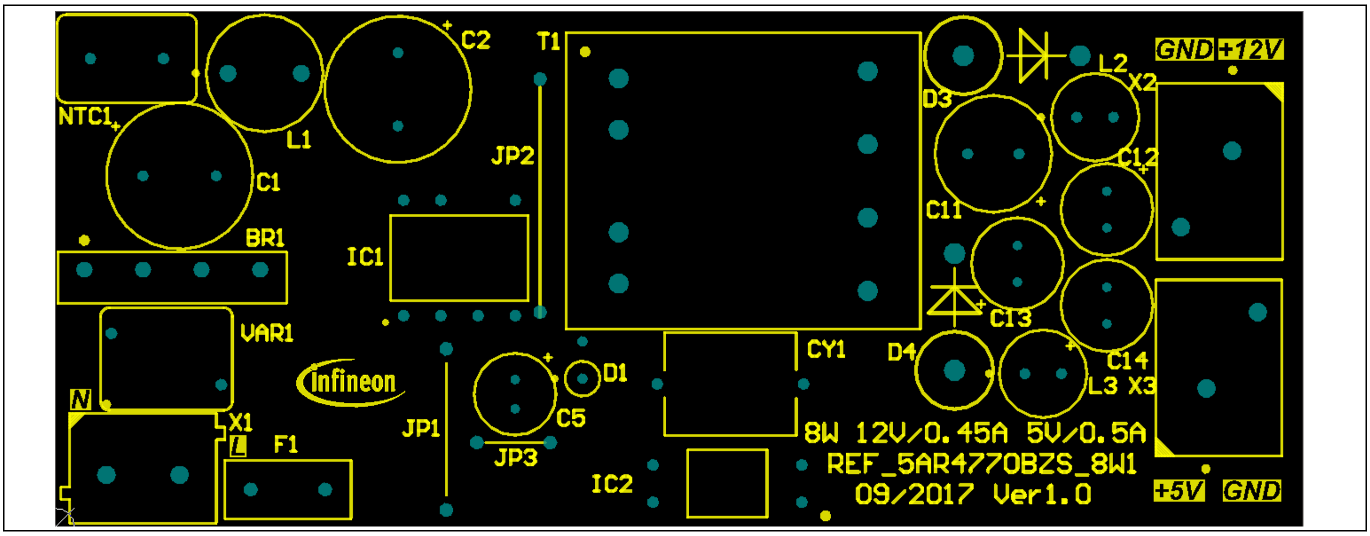


Figure 6 Top-side component legend

6.2 Bottom side

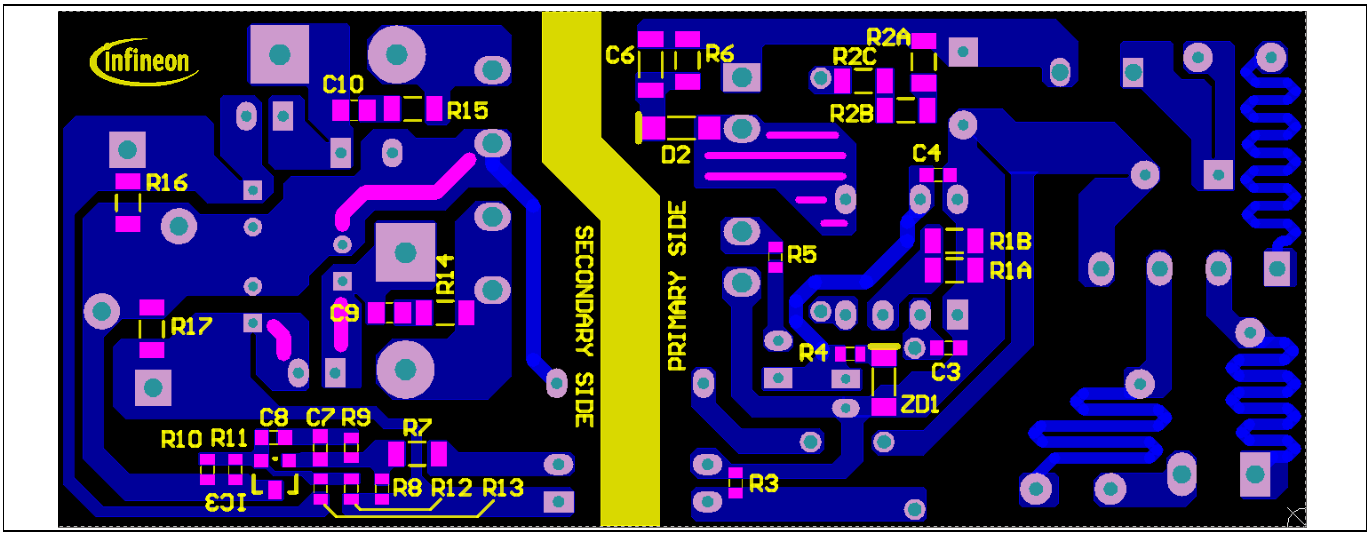


Figure 7 Bottom-side copper and component legend

7 BOM

Table 4 BOM

No.	Designator	Description	Part number	Manufacturer	Quantity
1	BR1	600 V/1 A	S1VBA60		1
2	C1, C2	10 µF/400 V	EEUEE2G100	Panasonic	2
3	C3	10 nF/50 V/0603			1
4	C4	100 nF/50 V/0603			1
5	C5	22 µF/50 V	50YXJ22MTA5X11	Rubycon	1
6	C6	470 pF/630 V/1206			1
7	C7	1 nF/50 V/0603			1
8	C8	220 nF/50 V/0603			1
9	C9, C10	Not loaded			
10	C11	470 µF/16 V	16ZLH470MEFC8X11.5	Rubycon	1
11	C12	220 µF/16 V	16ZLH220MEFC6.3X11	Rubycon	1
12	C13, C14	330 µF/10 V	10ZLJ330M6.3X11	Rubycon	2
13	CY1	1 nF/500 V	VY1102M35Y5UG63V0		1
14	D1	0.2 A/200 V	BAV20		1
15	D2	1 A/1 kV	US1K-13-F		1
16	D3	3 A/150 V	STPS3150RL		1
17	D4	3 A/60 V	MBR360G		1
18	F1	2 A/300 V	SS-5H-2A-APH	Eaton Bussmann	1
19	IC1	700 V/4.7 Ω	ICE5AR4770BZS	Infineon	1
20	IC2	Optocoupler	SFH617A-3		1
21	IC3	2.5 V ref.	TL431AQDBZRQ1		1
22	L1	1 mH/0.3 A	744 772 102	Wurth Electronics	1
23	L2, L3	2.2 µH/4.3 A	744 746 202 2	Wurth Electronics	2
24	NTC1	5 Ω/9.5 mm	B57235S0509M000	TDK	1
25	R1A, R1B	3 Ω/0.25 W/1 percent/1206	ERJ8RQF3R0V	Panasonic	2
26	R2A, R2B, R2C	15 MΩ/0.33 W/1 percent/1206			3
27	R4, R5	4.7 Ω /0.1 W/5 percent/0603			2
28	R6	240 kΩ/0.25 W/5 percent/1206	ERA8AEB244V	Panasonic	1
29	R7	330 Ω/0.25 W/5 percent/1206			1
30	R8	2.7 kΩ/0.1 W/5 percent/0603			1
31	R9	18 kΩ/0.1 W/1 percent/0603			1
32	R10, R12	12 kΩ/0.1 W/1 percent/0603			2
33	R16	27 kΩ/0.25 W/5 percent/1206			1
34	R3, R11, R13, R14, R15, R17	Not loaded			
35	T1	710 µH/EE16	750343739	Wurth Electronics	1
36	VAR1	Varistor, 0.3 W/320 V	ERZE07A511	Panasonic	1
37	ZD1	22 V/500mW	MMSZ5251BT1G		1
38	X1	Connector	691102710002	Wurth Electronics	1
39	X2, X3	Connector	691412120002B	Wurth Electronics	2
40	JP1, JP3	Jumper			2
41	JP2	Insulated jumper			1
42	PCB	85 mm × 35 mm (L × W), single layer, 2 oz, FR-4			1

8 Transformer specification

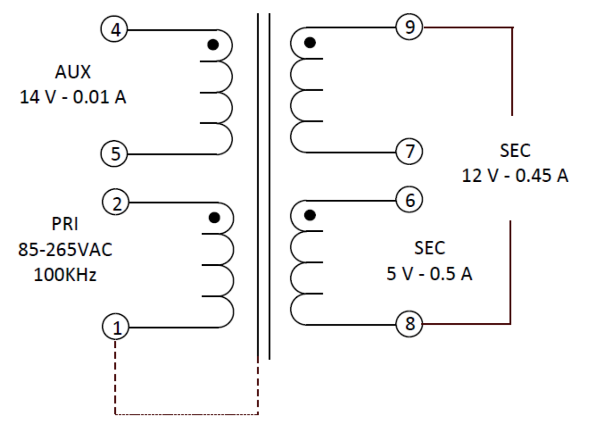
(Refer to Appendix A for transformer design and Appendix B for WE transformer specification.)

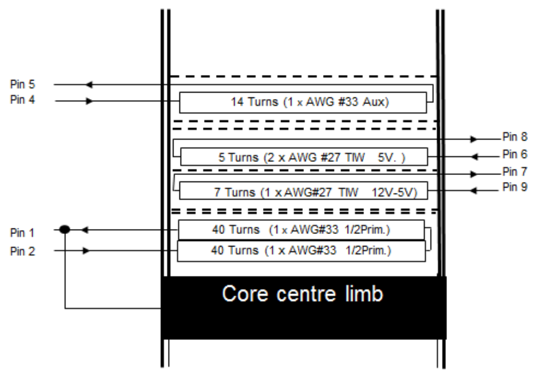
Wurth Electronics core part number: 150-2182 (EE16/8/5)

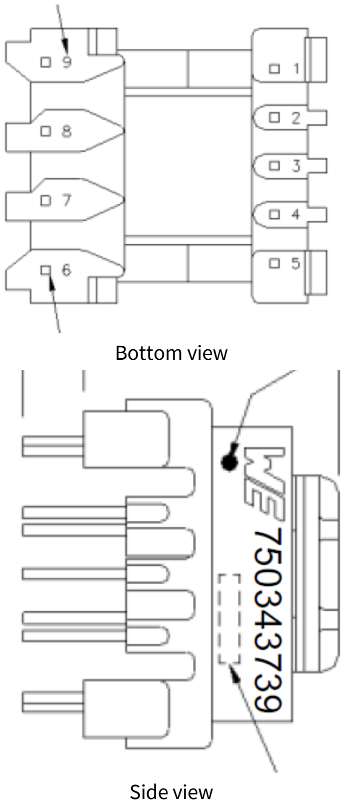
Wurth Electronics bobbin: 070-5280 (9-pin EXT, THT, horizontal version)

Primary inductance: Lp = 710 µH (±10 percent), measured between pin 1 and pin 2

Manufacturer and part number: Wurth Electronics Midcom (750343739)







Start	Stop	No. of turns	Wire size	Layer
2	-	40	1 x AWG#33	1/2 Primary
-	1	40	1 x AWG#33	1/2 Primary
9	7	7	1 x AWG#27 TIW	12V-5V
6	8	5	2 x AWG#27 TIW	5V
4	5	14	1 x AWG#33	Auxiliary

Figure 8 Transformer structure

9 Measurement data and graphs

Table 5 Electrical measurements

Input (V AC/Hz)	Pin (W)	12 V (V)	I_{out_12V} (mA)	5 V (V)	I_{out_5V} (mA)	12 V_{RPP} (mV)	5 V_{RPP} (mV)	P_{OUT} (W)	Efficiency (percent)	Average efficiency (percent)	OLP pin (W)	OLP I_{out_12V} (fixed 5 V at 0.5 A) (A)
85 V AC/ 60 Hz	0.023	12.56	0	4.99	0	17	23				13.73	0.694
	1.022	12.40	44.8	4.99	50	15	13	0.81	78.81			
	2.470	12.43	112.3	4.99	125.1	17	17	2.02	81.79	82.20		
	4.898	12.45	224.8	4.99	250.1	18	18	4.05	82.61			
	7.367	12.46	337.2	4.99	375.2	22	18	6.07	82.46			
	9.902	12.49	449.6	4.99	500.1	25	22	8.11	81.93			
115 V AC/ 60 Hz	0.024	12.56	0	4.99	0	18	25				13.57	0.706
	1.025	12.40	44.8	4.99	50	15	15	0.81	78.54			
	2.463	12.43	112.3	4.99	125.1	17	17	2.02	82.05	82.90		
	4.864	12.45	224.8	4.99	250.1	18	17	4.05	83.19			
	7.298	12.46	337.2	4.99	375.2	20	18	6.07	83.23			
	9.757	12.49	449.6	4.99	500.1	23	20	8.11	83.13			
230 V AC/ 50 Hz	0.027	12.58	0	4.99	0	18	27				13.78	0.734
	1.038	12.41	44.8	4.99	50	15	15	0.81	77.61			
	2.524	12.43	112.3	4.99	125.1	17	18	2.02	80.06	82.10		
	4.941	12.44	224.8	4.99	250.1	17	18	4.05	81.87			
	7.313	12.45	337.2	4.99	375.2	22	20	6.07	83.03			
	9.715	12.48	449.6	4.99	500.1	27	22	8.11	83.45			
265 V AC/ 50 Hz	0.029	12.58	0	4.99	0	17	27				14.12	0.756
	1.076	12.40	44.8	4.99	50	15	15	0.81	74.83			
	2.550	12.43	112.3	4.99	125.1	17	18	2.02	79.23	81.40		
	4.980	12.44	224.8	4.99	250.1	20	18	4.04	81.21			
	7.381	12.45	337.2	4.99	375.2	23	18	6.07	82.26			
	9.779	12.48	449.6	4.99	500.1	23	20	8.11	82.90			

100 percent load condition: +5 V/500 mA and +12 V/450 mA

75 percent load condition: +5 V/375 mA and +12 V/337 mA

50 percent load condition: +5 V/250 mA and +12 V/225 mA

25 percent load condition: +5 V/125 mA and +12 V/112 mA

9.1 Efficiency

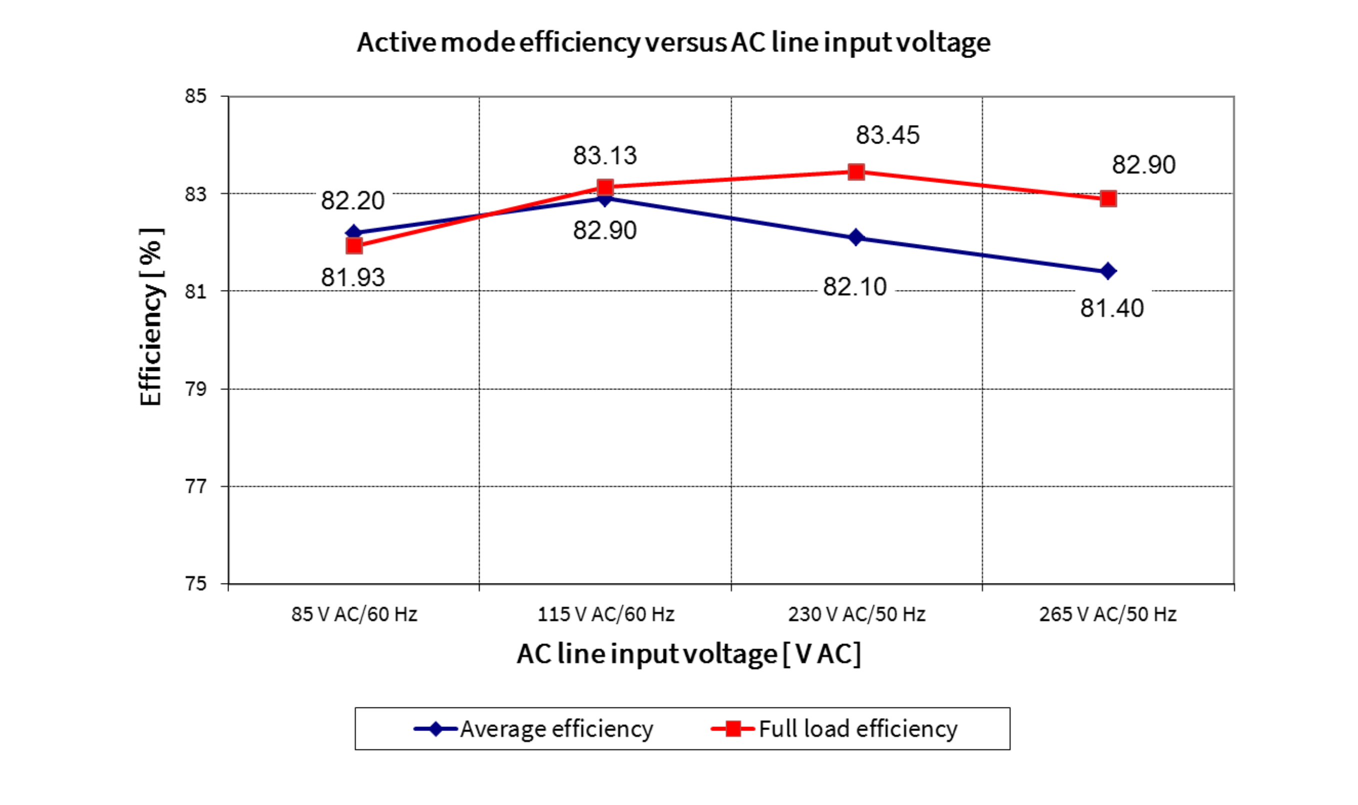


Figure 9 Efficiency vs AC-line input voltage

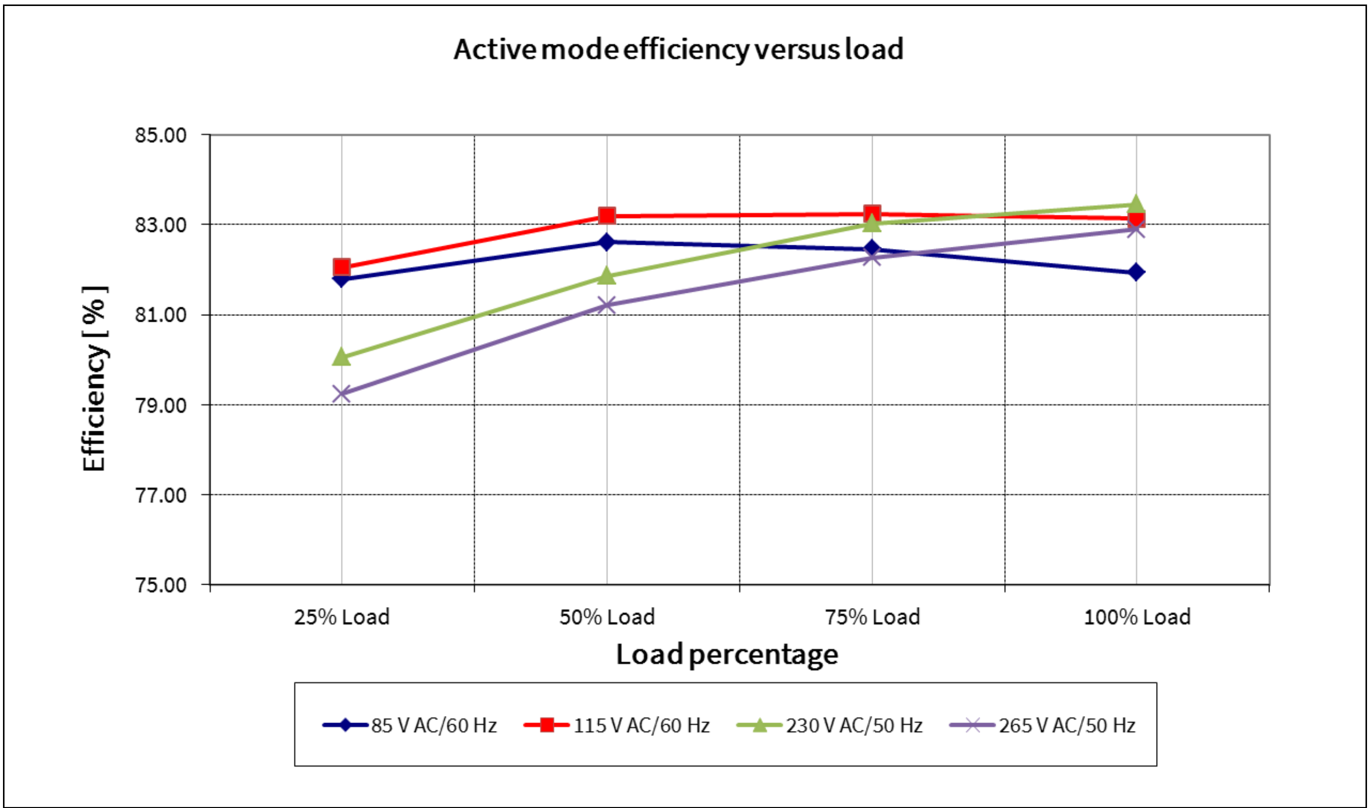


Figure 10 Efficiency vs load

9.2 Standby power

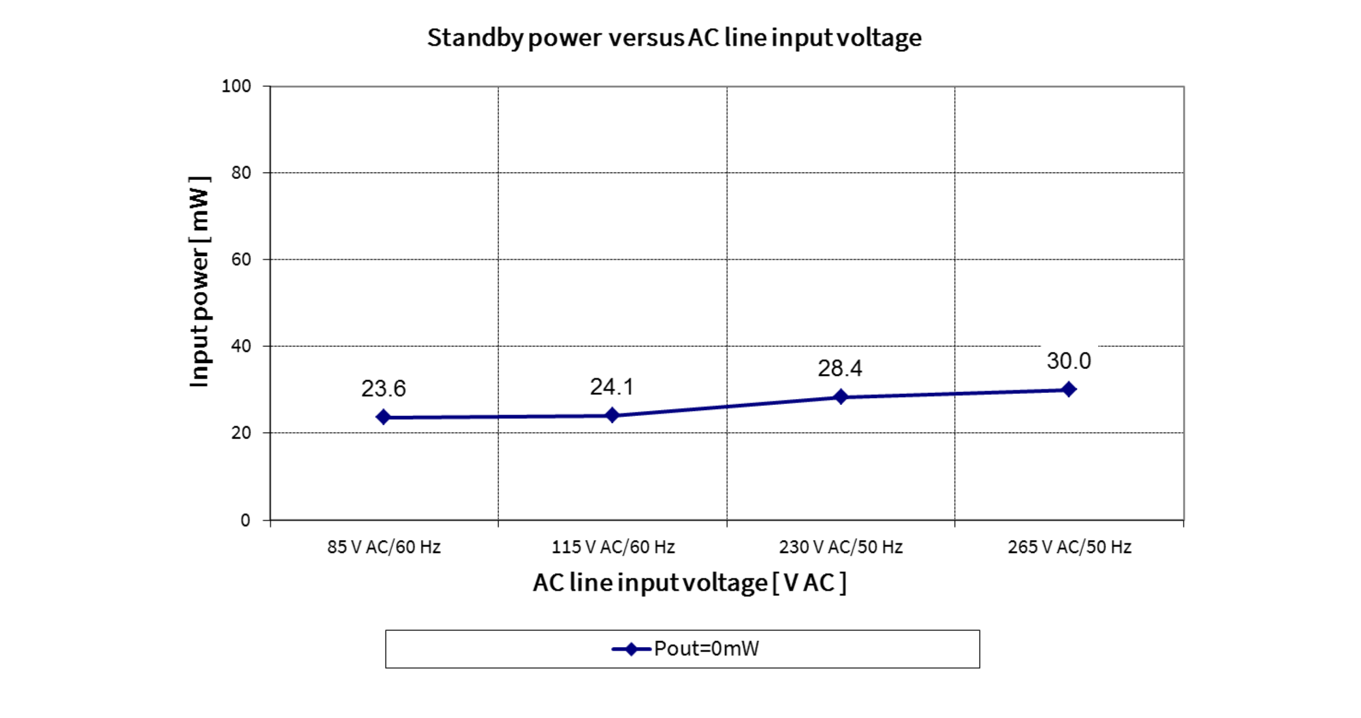


Figure 11 Standby power at no load vs AC-line input voltage (measured by Yokogawa WT210 power meter – integration mode)

9.3 Line regulation

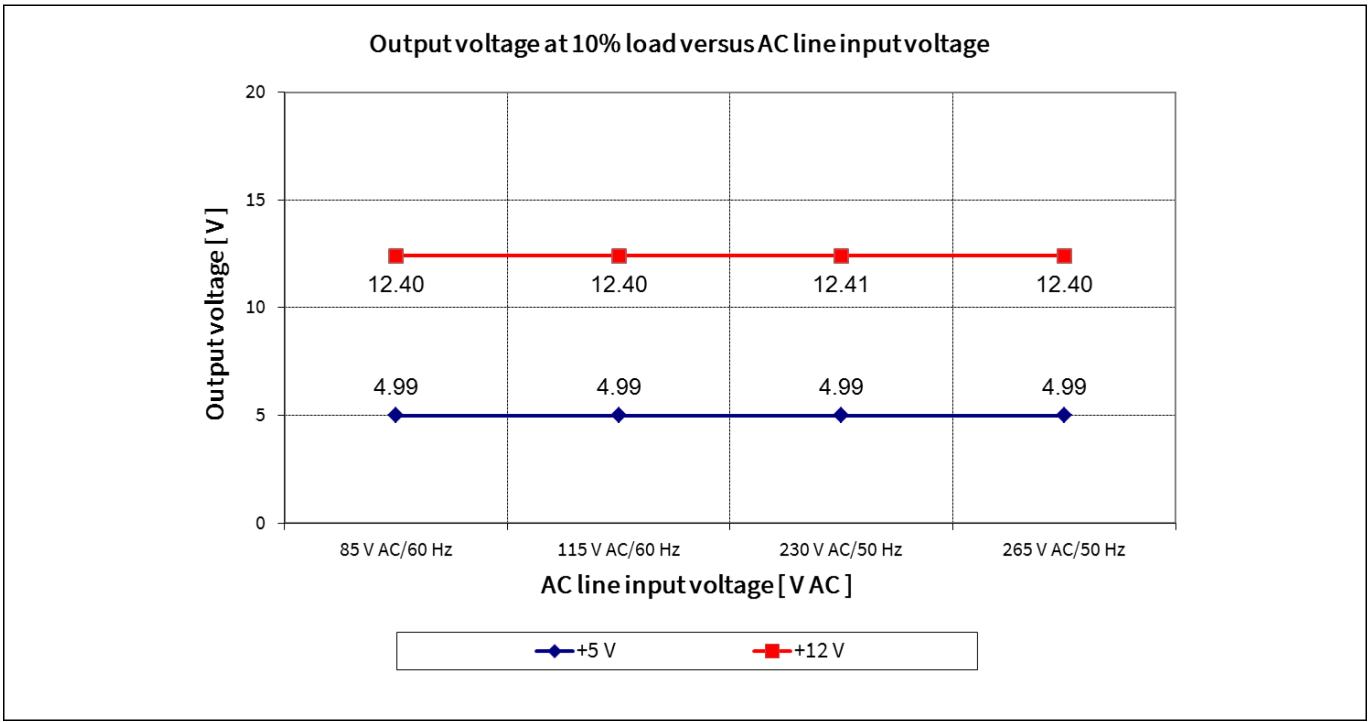


Figure 12 Output regulation at full load vs AC-line input voltage

9.4 Load regulation

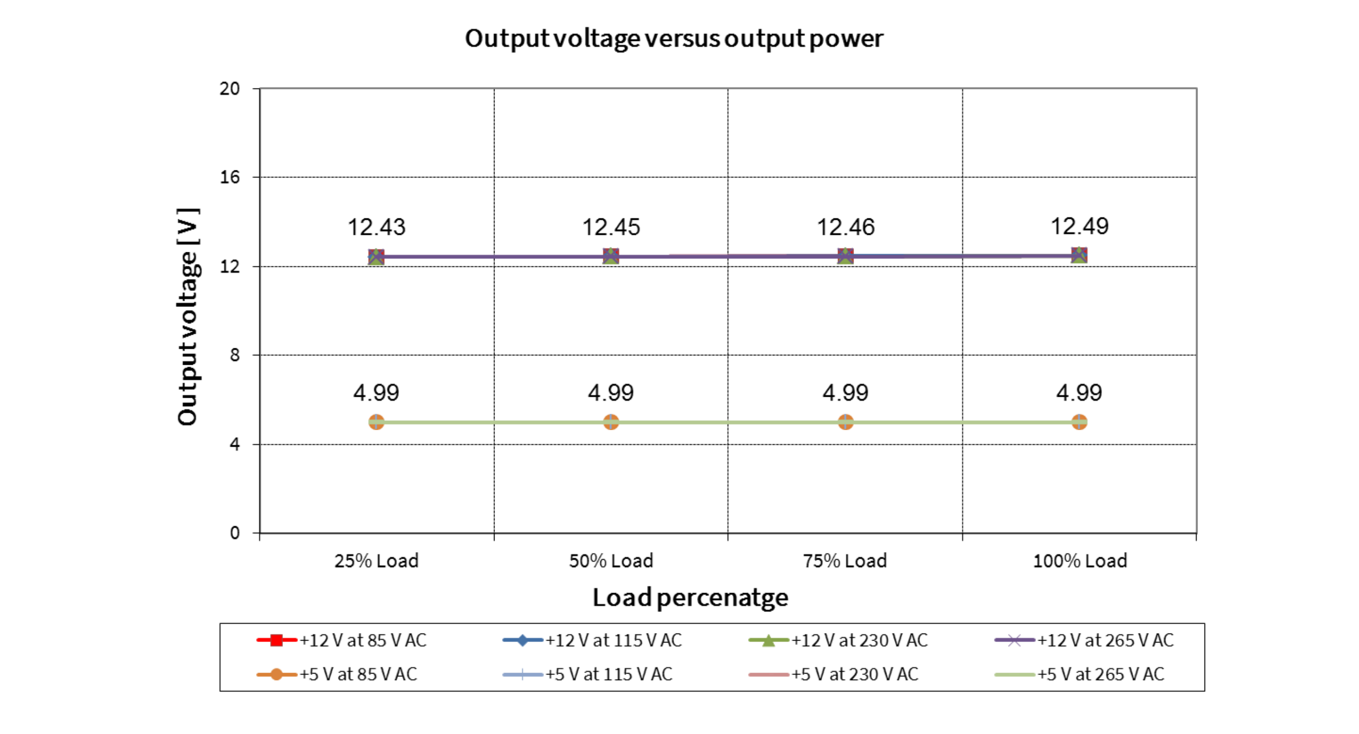


Figure 13 Output regulation vs output power

9.5 Maximum input power

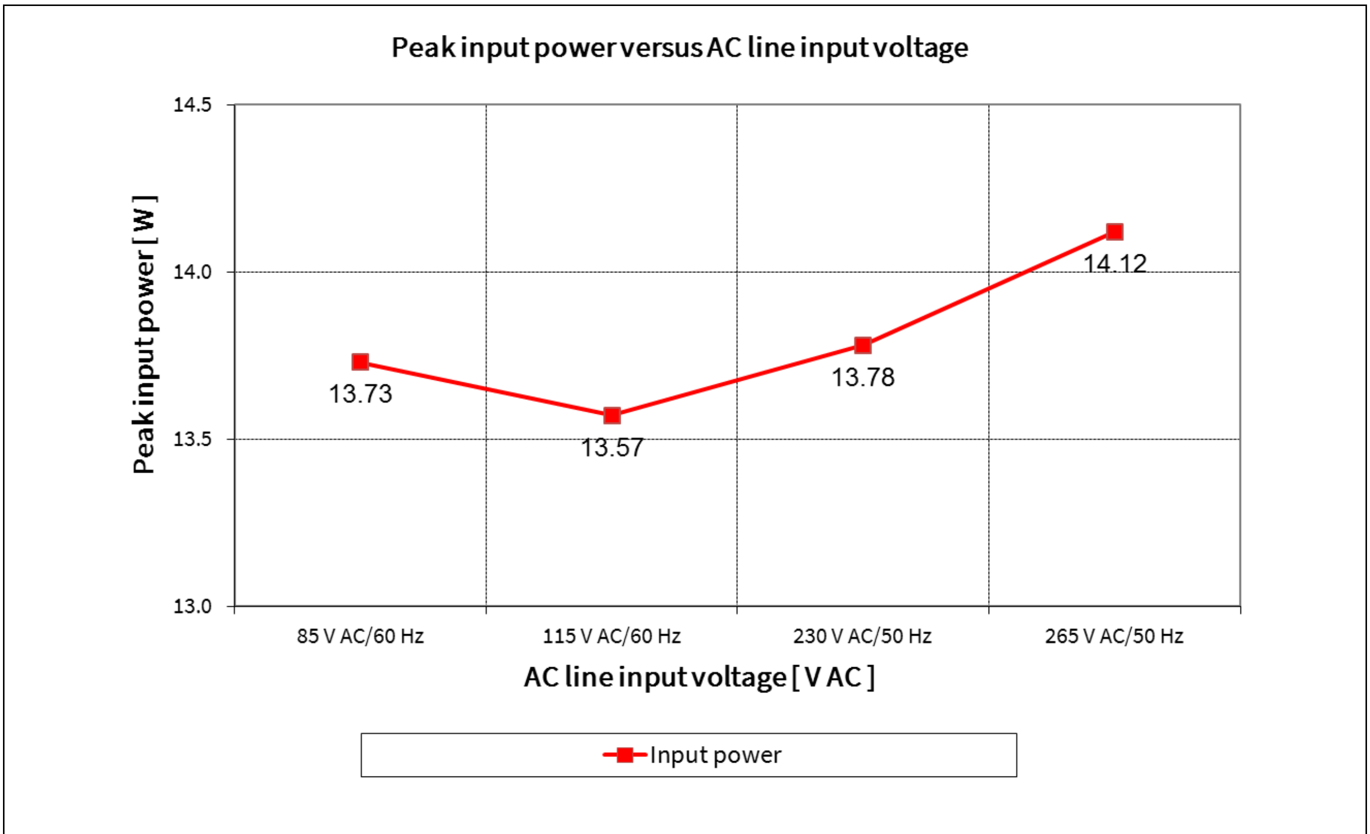


Figure 14 Maximum input power (before over-load protection) vs AC-line input voltage

9.6 Frequency reduction

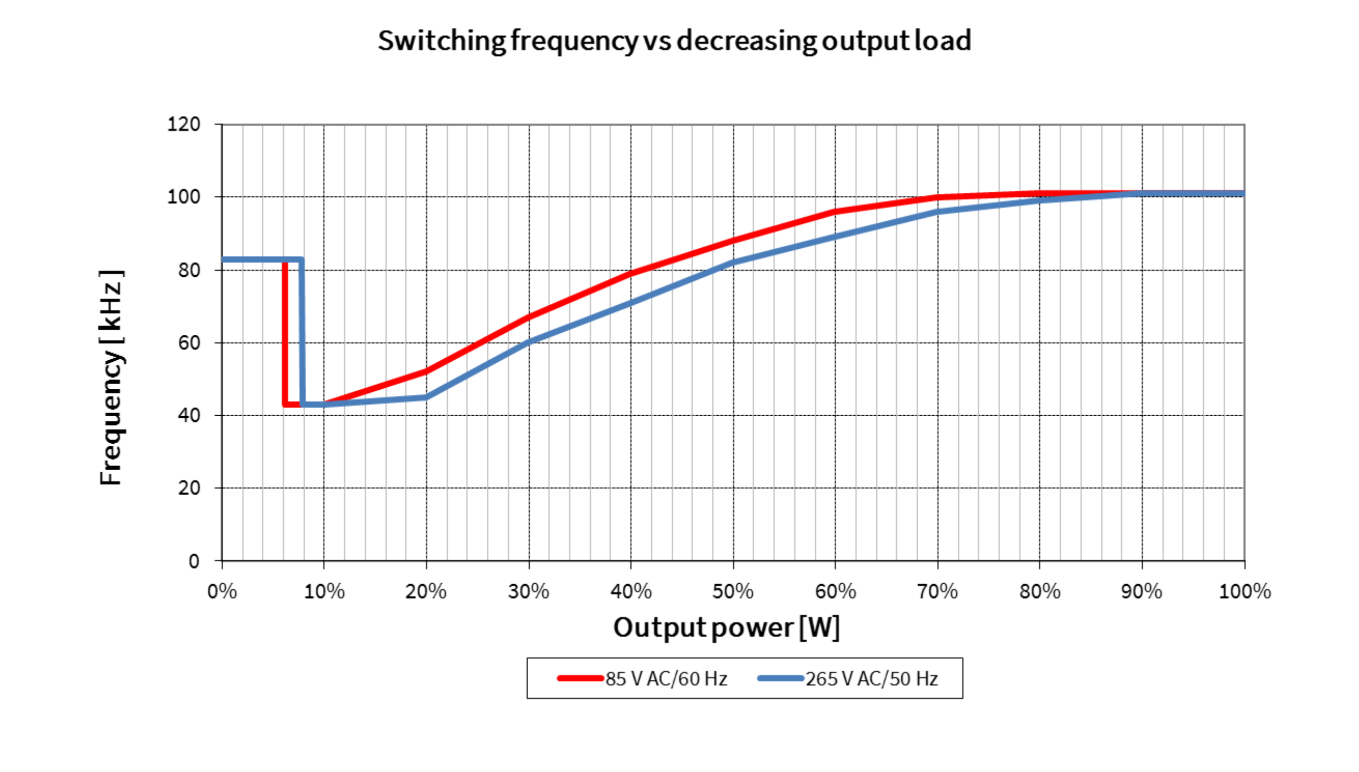


Figure 15 Frequency reduction curve vs output load

9.7 ESD immunity (EN 61000-4-2)

This system was subjected to a ±10 kV ESD test according to EN 61000-4-2 special for both contact and air discharge. A test failure was defined as non-recoverable.

- Air discharge: pass ±10 kV; contact discharge: pass ± 10 kV.

Table 6 System ESD test result

Description	ESD test	Level	Number of strikes		Test result
			$+V_{OUT}$	$-V_{OUT}$	
115 V AC, 8 W (12 V/26.7 Ω, 5 V/10 Ω)	Contact	+10 kV	10	10	PASS
		-10 kV	10	10	PASS
	Air	+10 kV	10	10	PASS
		-10 kV	10	10	PASS
230 V AC, 8 W (12 V/26.7 Ω, 5 V/10 Ω)	Contact	+10 kV	10	10	PASS
		-10 kV	10	10	PASS
	Air	+10 kV	10	10	PASS
		-10 kV	10	10	PASS

9.8 Surge immunity (EN 61000-4-5)

This system was subjected to a surge immunity test (±2 kV DM and ±4 kV CM) according to EN 61000-4-5. A test failure was defined as a non-recoverable.

- DM: pass ±2 kV; CM: pass ±4 kV.

Table 7 System surge immunity test result

Description	Test	Level		Number of strikes				Test result
				0°	90°	180°	270°	
115 V AC, 8 W (12 V/26.7 Ω, 5 V/10 Ω)	DM	+2 kV	L → N	3	3	3	3	PASS
		-2 kV	L → N	3	3	3	3	PASS
	CM	+4 kV	L → G	3	3	3	3	PASS
		+4 kV	N → G	3	3	3	3	PASS
		-4 kV	L → G	3	3	3	3	PASS
		-4 kV	N → G	3	3	3	3	PASS
230 V AC, 8 W (12 V/26.7 Ω, 5 V/10 Ω)	DM	+2 kV	L → N	3	3	3	3	PASS
		-2 kV	L → N	3	3	3	3	PASS
	CM	+4 kV	L → G	3	3	3	3	PASS
		+4 kV	N → G	3	3	3	3	PASS
		-4 kV	L → G	3	3	3	3	PASS
		-4 kV	N → G	3	3	3	3	PASS

9.9 Conducted emissions (EN 55022 class B)

The conducted EMI was measured by Schaffner (SMR4503) and followed the test standard of EN 55022 (CISPR 22) class B. The reference board is tested at full load (7.9 W) using resistive load at input voltage of 115 V AC and 230 V AC.

Pass conducted emissions EN 55022 (CISPR 22) class B with 13.6 dB margin at low-line (115 V AC) and 10.4 dB margin at high-line (230 V AC).

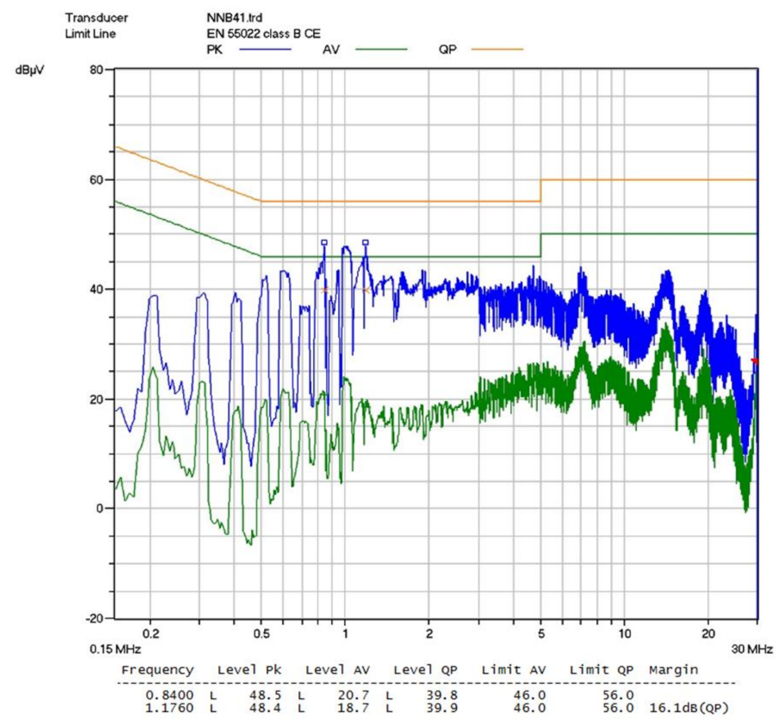
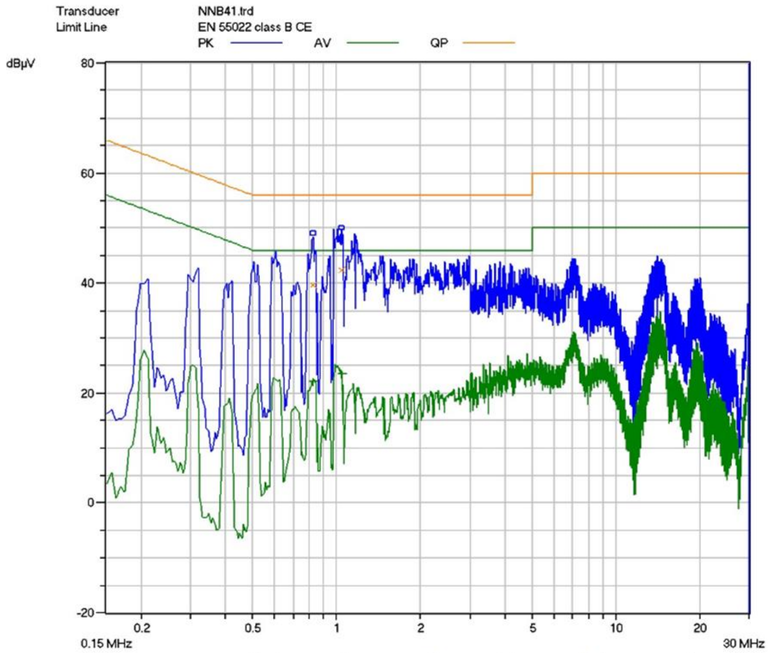
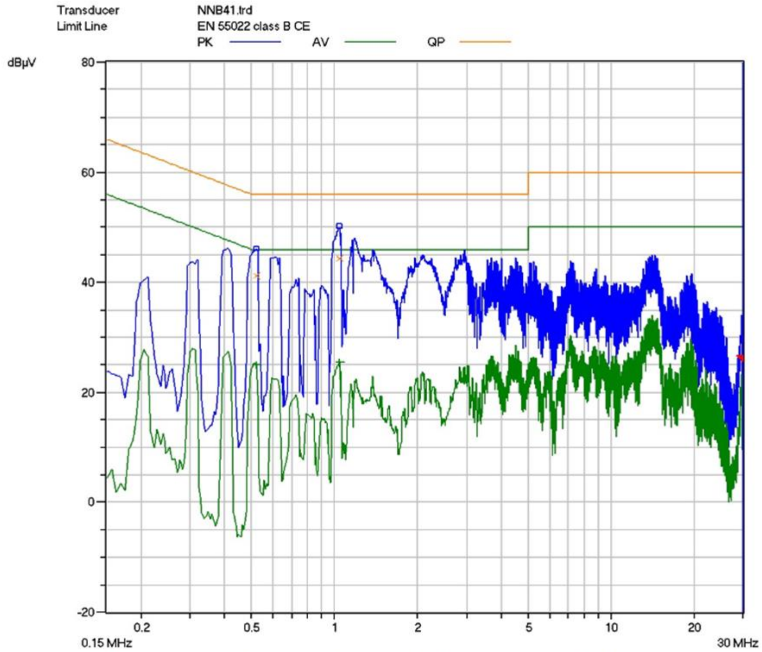


Figure 16 Conducted emissions (line) at 115 V AC and full load



Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP	Margin
0.8220	L	49.0	L	22.2	L	39.7	46.0	56.0	
1.0440	L	50.0	L	23.6	L	42.4	46.0	56.0	13.6dB(QP)

Figure 17 Conducted emissions (neutral) at 115 V AC and full load



Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP	Margin
0.5220	L	46.2	L	25.1	L	41.3	46.0	56.0	
1.0440	L	50.2	L	25.5	L	44.3	46.0	56.0	11.7dB(QP)

Figure 18 Conducted emissions (line) at 230 V AC and full load

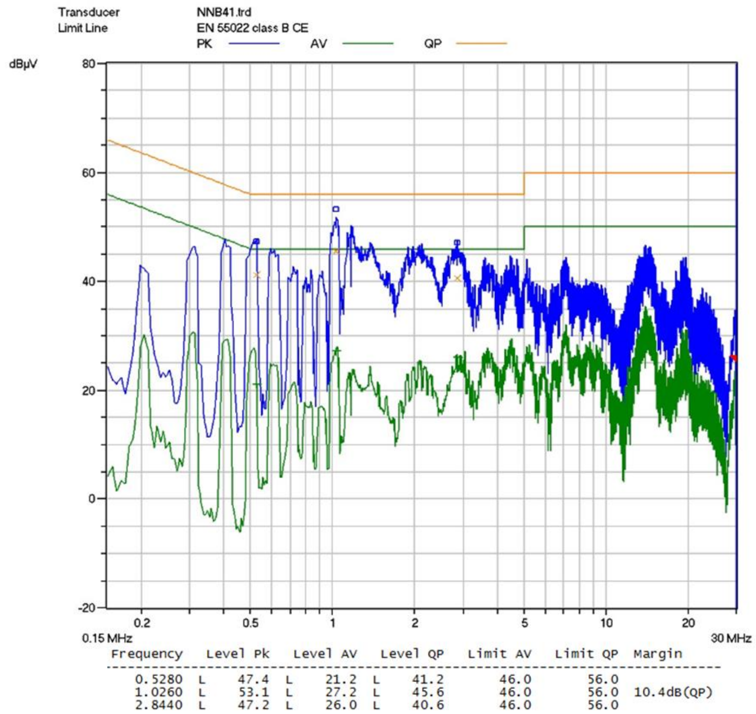


Figure 19 Conducted emissions (neutral) at 230 V AC and full load

9.10 Thermal measurement

The thermal test of the open-frame reference board was done using an infrared thermography camera (FLIR-T62101) at an ambient temperature of 25°C. The measurements were taken after one hour running at full load.

Table 8 Hottest components on the reference board

No.	Components	Temperature at 85 V AC (°C)	Temperature at 265 V AC (°C)
1	D3 (+12 V diode)	55.6	54.3
2	T1 (transformer)	56.8	62.5
3	IC1 (ICE5AR4770BZS)	54.3	52.6

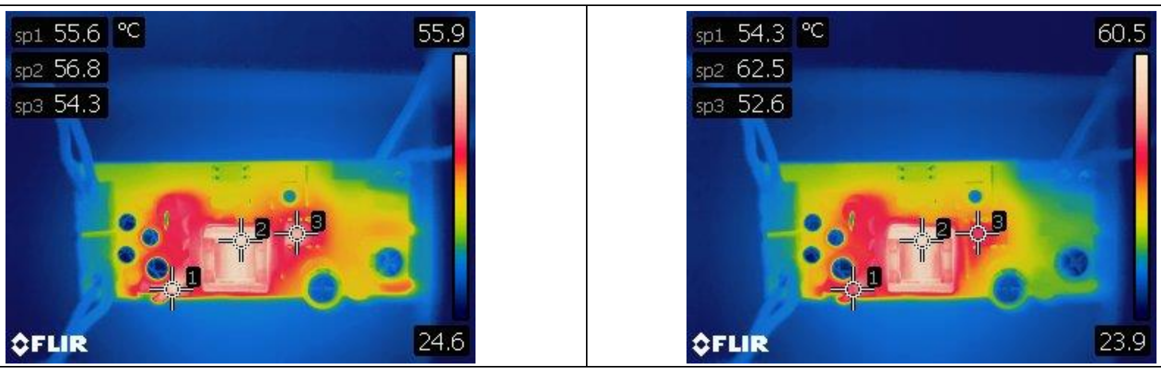


Figure 20 Top-side infrared thermal image of REF_5AR4770BZS at 85 V AC (left) and 265 V AC (right) full load

10 Waveforms and oscilloscope plots

All waveforms and scope plots were recorded with a Teledyne LeCroy 606Zi oscilloscope.

10.1 Start-up at full load

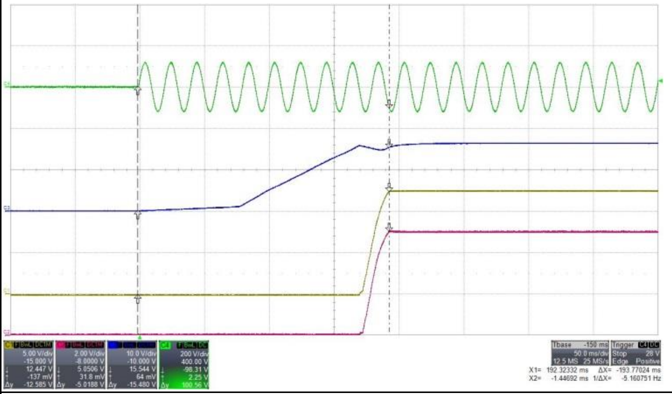
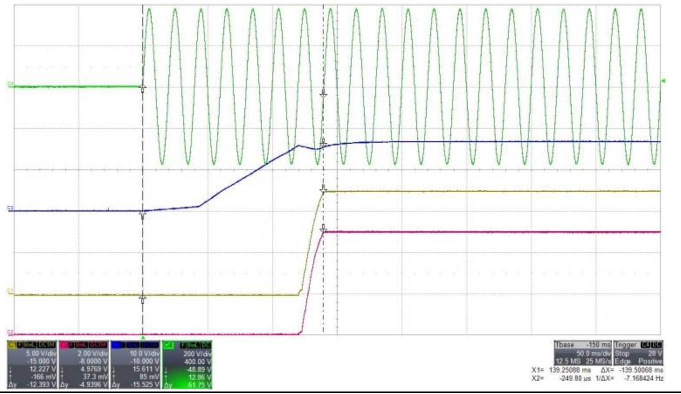
	
C1 (yellow) : +12 V output voltage C2 (purple) : +5 V output voltage C3 (blue) : V_{CC} voltage C4 (green) : AC-line voltage	C1 (yellow) : +12 V output voltage C2 (purple) : +5 V output voltage C3 (blue) : V_{CC} voltage C4 (green) : AC-line voltage
85 V AC start-up time at full load is less than 200 ms	265 V AC start-up time at full load is less than 140 ms

Figure 21 Start-up

10.2 Soft-start at full load

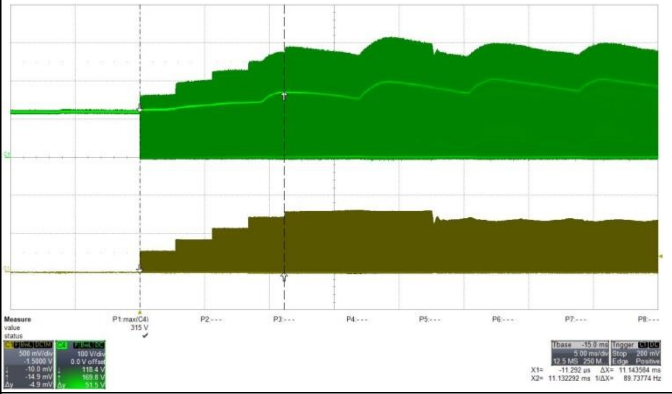
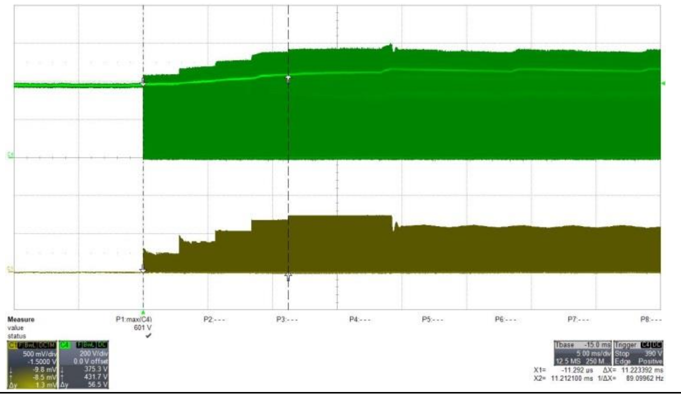
	
C1 (yellow) : CS voltage C4 (green) : Drain voltage	C1 (yellow) : CS voltage C4 (green) : Drain voltage
85 V AC soft-start time at full load is ~ 11 ms	265 V AC soft-start time at full load is ~ 11 ms

Figure 22 Soft-start

10.3 Drain and CS voltage at full load

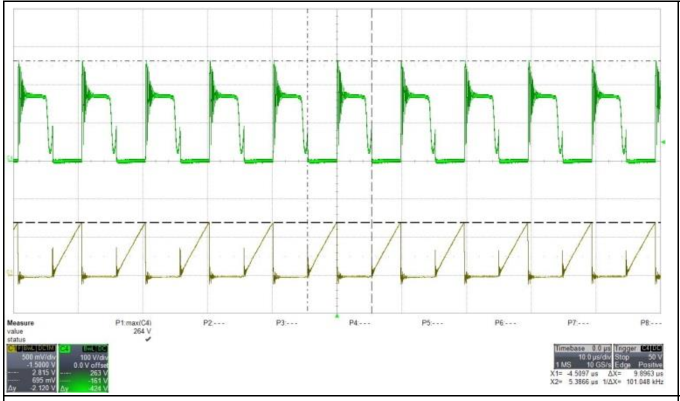
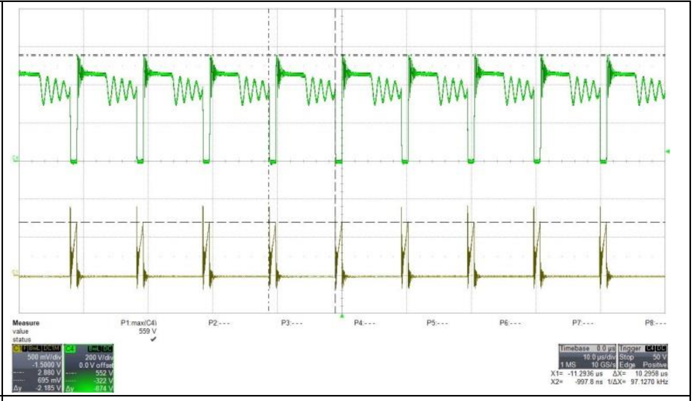
	
C1 (yellow) : CS voltage C4 (green) : Drain voltage	C1 (yellow) : CS voltage C4 (green) : Drain voltage
85 V AC maximum drain voltage at full load is ~ 264 V	265 V AC maximum drain voltage at full load is ~ 559 V

Figure 23 Drain and CS voltage

10.4 Frequency jittering at full load

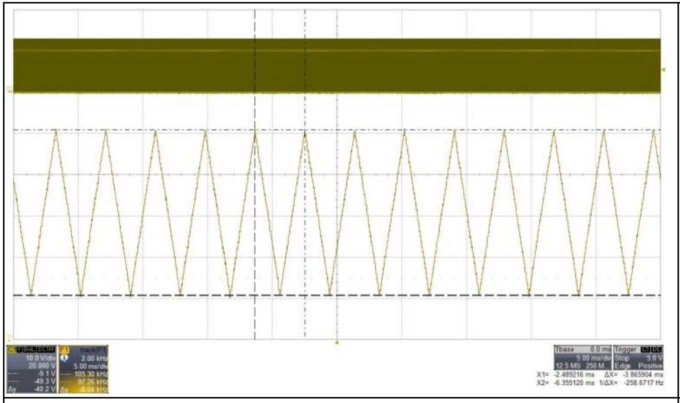
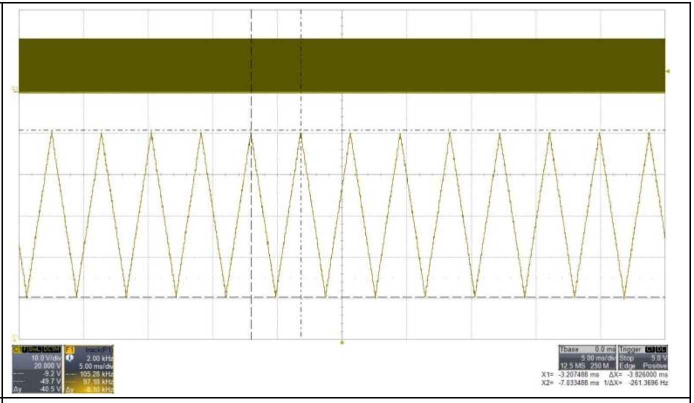
	
C1 (yellow) : Gate voltage F1 (yellow) : Frequency track of gate voltage	C1 (yellow) : Gate voltage F1 (yellow) : Frequency track of gate voltage
85 V AC frequency jittering at full load is ~ 97 kHz to ~ 105 kHz with jitter period of 3.8 ms	265 V AC frequency jittering at full load is ~ 97 kHz to ~ 105k Hz with jitter period of 3.8 ms

Figure 24 Frequency jittering

10.5 Load transient response (dynamic load from 10 percent to 100 percent)

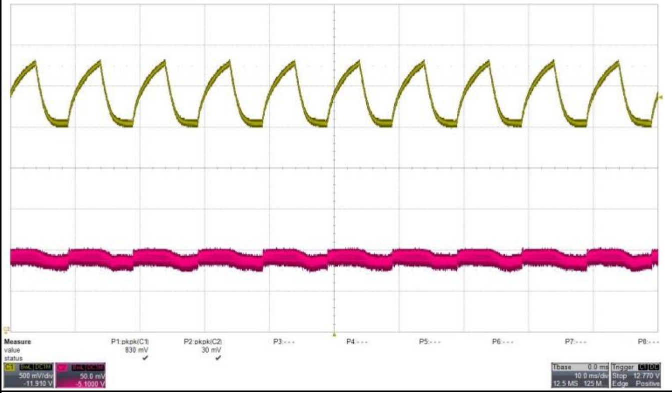
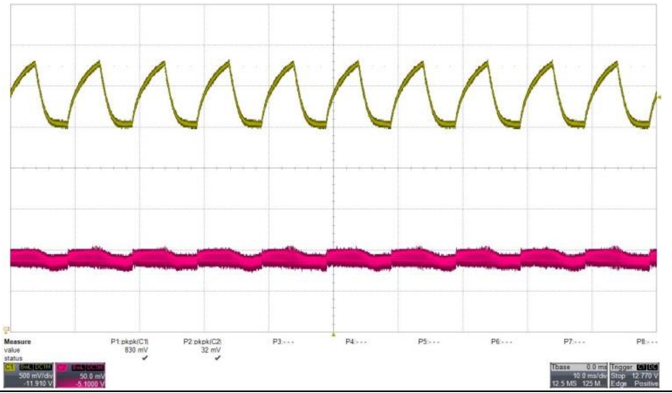
	
C1 (yellow) : +12 V output voltage C2 (purple) : +5 V output voltage	C1 (yellow) : +12 V output voltage C2 (purple) : +5 V output voltage
85 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~ 830 mV 85 V AC +5 V output voltage $V_{ripple\_pk\_pk}$ is ~ 30 mV	265 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~ 830 mV 265 V AC +5 V output voltage $V_{ripple\_pk\_pk}$ is ~ 32 mV

Figure 25 Load transient response with +12 V output load change from 10 percent to 100 percent at 0.4 A/µs slew rate, 100 Hz. +5 V output is fixed at 500 mA load. Probe terminals are decoupled with a 1 µF electrolytic capacitor and a 0.1 µF ceramic capacitor. Oscilloscope is BW filter limited to 20 MHz.

10.6 Output ripple voltage at full load

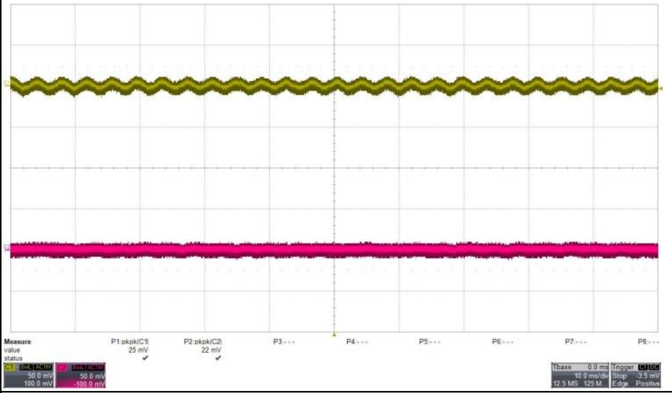
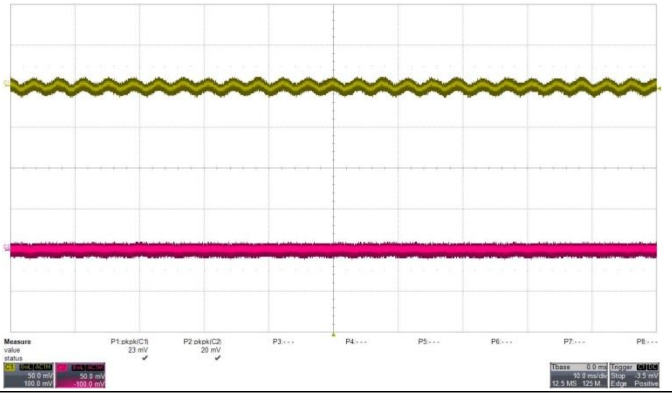
	
C1 (yellow) : +12 V output voltage C2 (purple) : +5 V output voltage	C1 (yellow) : +12 V output voltage C2 (purple) : +5 V output voltage
85 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~ 25 mV 85 V AC +5 V output voltage $V_{ripple\_pk\_pk}$ is ~ 22 mV	265 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~ 23 mV 265 V AC +5 V output voltage $V_{ripple\_pk\_pk}$ is ~ 20 mV

Figure 26 Output ripple voltage at full load. Probe terminals are decoupled with a 1 µF electrolytic capacitor and a 0.1 µF ceramic capacitor. Oscilloscope is BW filter limited to 20 MHz.

10.7 Output ripple voltage at ABM (0.1 W load)

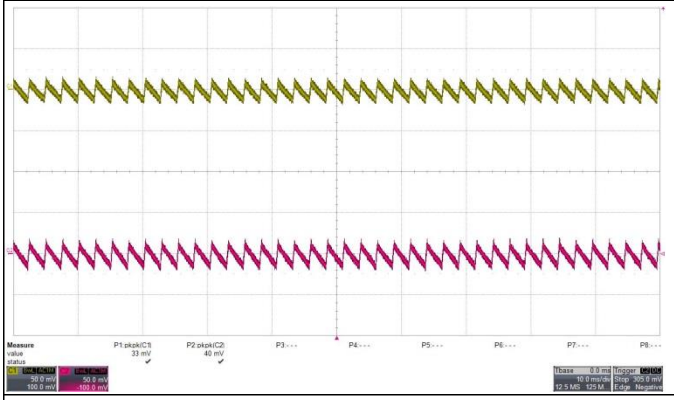
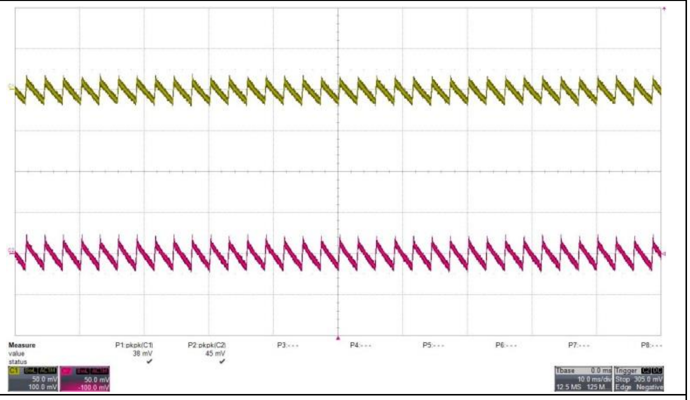
	
C1 (yellow) : +12 V output voltage C2 (purple) : +5 V output voltage	C1 (yellow) : +12 V output voltage C2 (purple) : +5 V output voltage
85 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~ 33 mV 85 V AC +5 V output voltage $V_{ripple\_pk\_pk}$ is ~ 40 mV	265 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~ 38 mV 265 V AC +5 V output voltage $V_{ripple\_pk\_pk}$ is ~ 45 mV

Figure 27 Output ripple voltage at 0.1 W load (+12 V/6 mA, +5 V/6 mA). Probe terminals are decoupled with a 1 µF electrolytic capacitor and a 0.1 µF ceramic capacitor. Oscilloscope is BW filter limited to 20 MHz.

10.8 Entering ABM

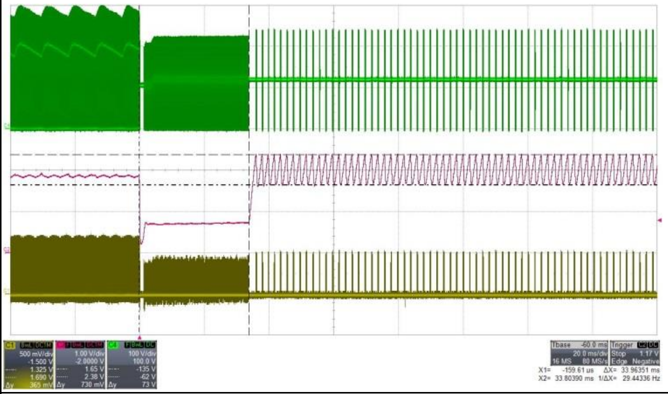
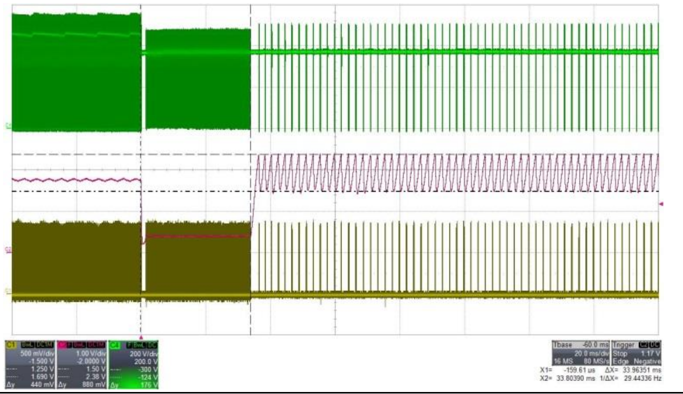
	
C1 (yellow) : CS voltage C2 (purple) : FB pin voltage C4 (green) : Drain voltage	C1 (yellow) : CS voltage C2 (purple) : FB pin voltage C4 (green) : Drain voltage
85 V AC full load to 0.1 W load. Enter ABM at FB pin voltage less than 1.03 V (V_{FB_EBHP}) for more than 36 ms (t_{FB_BEB}).	265 V AC full load to 0.1 W load. Enter ABM at FB pin voltage less than 1.03 V (V_{FB_EBHP}) for more than 36 ms (t_{FB_BEB}).

Figure 28 Entering ABM. Output at full load to 0.1 W load (+12 V/6 mA, +5 V/6 mA).

10.9 During ABM

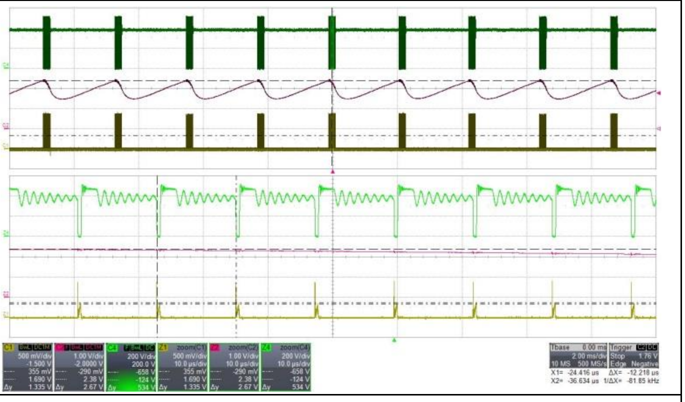
	
C1 (yellow) : CS voltage C2 (purple) : FB pin voltage C4 (green) : Drain voltage	C1 (yellow) : CS voltage C2 (purple) : FB pin voltage C4 (green) : Drain voltage
85 V AC at 0.1 W load. Burst-on at FB voltage 1.95 V ($V_{FB\_Bon\_NISO}$) and burst-off at 1.55 V ($V_{FB\_BOff\_NISO}$). CS voltage at 0.27 V (V_{CS_BHP}). Switching frequency at 86 kHz (f_{OSC4_ABM}).	265 V AC at 0.1 W load. Burst-on at FB voltage 1.95 V ($V_{FB\_Bon\_NISO}$) and burst-off at 1.55 V ($V_{FB\_BOff\_NISO}$). CS voltage at 0.27 V (V_{CS_BHP}). Switching frequency at 86 kHz (f_{OSC4_ABM}).

Figure 29 During ABM. Output at 0.1 W load (+12 V/6 mA, +5V/6 mA).

10.10 Leaving ABM

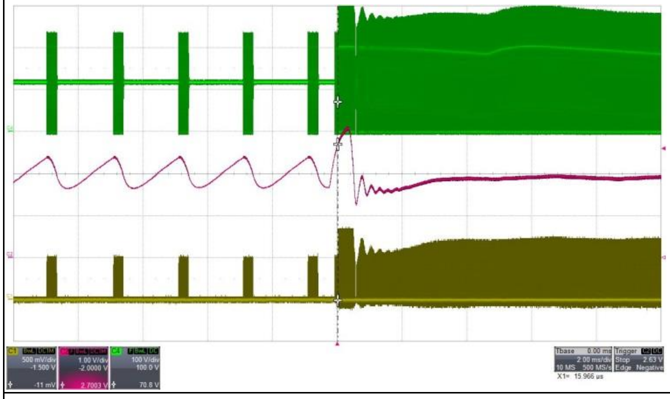
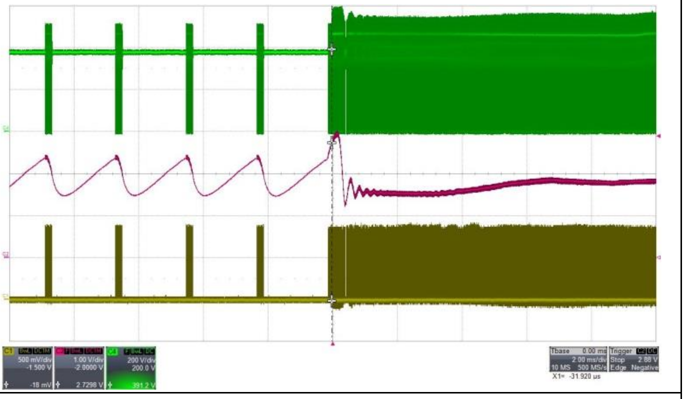
	
C1 (yellow) : CS voltage C2 (purple) : FB pin voltage C4 (green) : Drain voltage	C1 (yellow) : CS voltage C2 (purple) : FB pin voltage C4 (green) : Drain voltage
85 V AC at 0.5 W load to full load. Leave ABM at FB voltage greater than 2.73 V (V_{FB_LB}).	265 V AC at 0.5 W load to full load. Leave ABM at FB voltage greater than 2.73 V (V_{FB_LB}).

Figure 30 Leaving ABM. Output at 0.1 W load (+12 V/6 mA, +5 V/6 mA) to full load.

10.11 V_{CC} OVP/UVP

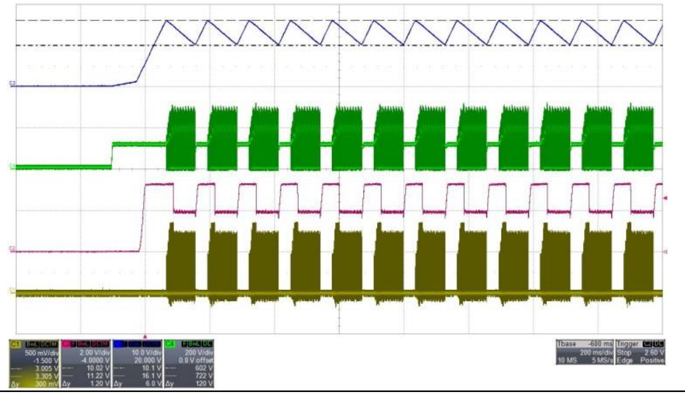
	
C1 (yellow) : CS voltage C2 (purple) : FB pin voltage C3 (blue) : V_{CC} voltage C4 (green) : Drain voltage	C1 (yellow) : CS voltage C2 (purple) : FB pin voltage C3 (blue) : V_{CC} voltage C4 (green) : Drain voltage
85 V AC at no load. Removed R4 and R12. Trigger V_{CC} OVP at V_{CC} voltage greater than 25.5 V (V_{VCC_OVP}). Odd-skip auto-restart mode.	85 V AC at full load. Removed R5. Trigger V_{CC} UVP at V_{CC} voltage less than 10 V (V_{VCC_OFF}). Auto-restart mode.

Figure 31 V_{CC} OVP/UVP

10.12 Over-load protection

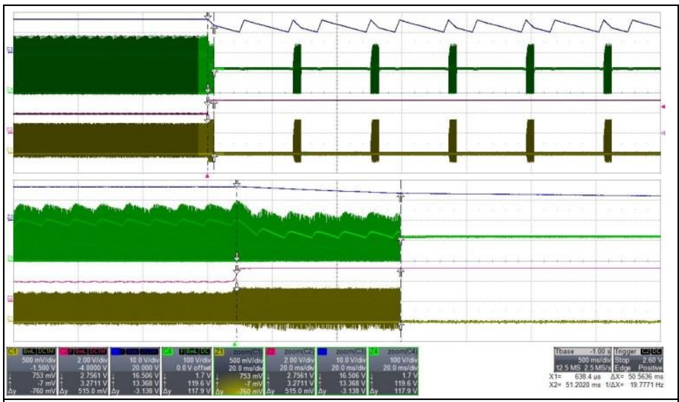
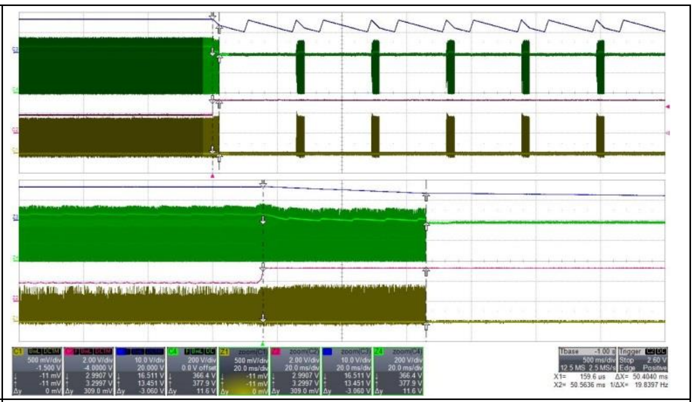
	
C1 (yellow) : CS voltage C2 (purple) : FB pin voltage C3 (blue) : V_{CC} voltage C4 (green) : Drain voltage	C1 (yellow) : CS voltage C2 (purple) : FB pin voltage C3 (blue) : V_{CC} voltage C4 (green) : Drain voltage
85 V AC at full load to over-load. Trigger protection at FB pin voltage greater than 2.73 V (V_{FB_OLP}) for more than 54 ms ($t_{FB\_OLP\_B}$). Odd-skip auto-restart mode.	265 V V AC_{AC} at full load to over-load. Trigger protection at FB pin voltage greater than 2.73 V (V_{FB_OLP}) for more than 54 ms ($t_{FB\_OLP\_B}$). Odd-skip auto-restart mode.

Figure 32 **Over-load protection. Load increased at +12 V to 2 A to trigger protection.**

10.13 V_{CC} short-to-GND

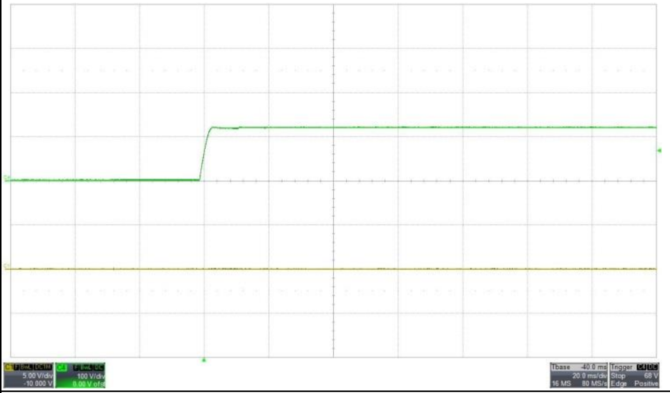
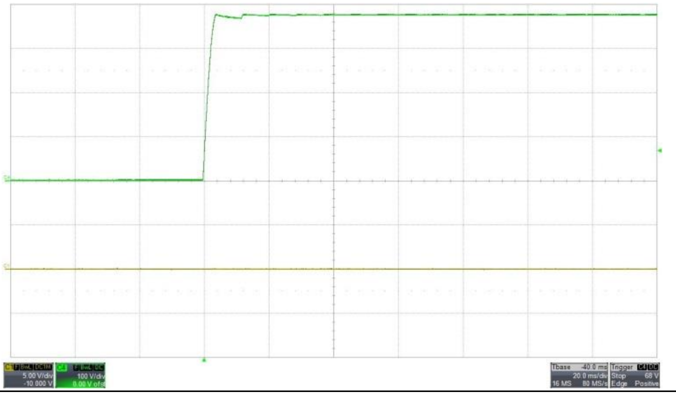
	
C1 (yellow) : V_{CC} pin voltage C4 (green) : Bus voltage	C1 (yellow) : V_{CC} pin voltage C4 (green) : Bus voltage
85 V AC. V_{CC} charging current at ~ 280 µA ($I_{VCC\_Charge1}$). IC power consumption is ~ 34 mW.	265 V AC. V_{CC} charging current at ~ 526 µA ($I_{VCC\_Charge1}$). IC power consumption is ~ 197 mW.

Figure 33 V_{CC} short-to-GND. V_{CC} charging current measured with a digital multimeter.

11 Appendix A: Transformer design and spreadsheet [3]

Calculation tool for flyback converter using fifth-generation fixed-frequency CoolSET™ (version 1.0)

Project	85 ~ 265 V AC dual-output 8 W isolated flyback power supply
Application	Auxiliary power supply for air-conditioner
CoolSET™	ICE5AR4770BZS
Date	6 Feb 18
Revision	V 1.0

Notes:
Enter design variables in orangecolored cells
Read design results in green coloured cells

	Description	Eq. #	Parameter	Unit	Value
Input, output, CoolSET™ specs					
Line input					
Input	Minimum AC input voltage		$V\ AC_{Min}$	[V]	85
Input	Maximum AC input voltage		$V\ AC_{Max}$	[V]	265
Input	Line frequency		f_{AC}	[Hz]	60
Input	Bus capacitor DC ripple voltage		$V\ DC_{Ripple}$	[V]	37
Output 1 specs					
Input	Output voltage 1		V_{Out1}	[V]	12
Input	Output current 1		I_{Out1}	[A]	0.45
Input	Forward voltage of output diode 1		V_{FOut1}	[V]	0.6
Input	Output ripple voltage 1		$V_{OutRipple1}$	[V]	100
Result	Output power 1	Eq. 001	P_{Out1}	[W]	5.4
Result	Output load weight 1	Eq. 004	K_{L1}		0.68
Output 2 specs					
Input	Output voltage 2		V_{Out2}	[V]	5
Input	Output current 2		I_{Out2}	[A]	0.5
Input	Forward voltage of output diode 2		V_{FOut2}	[V]	0.2
Input	Output ripple voltage 2		$V_{OutRipple2}$	[V]	100
Result	Output power 2	Eq. 002	P_{Out2}	[W]	2.5
Result	Output load weight 2	Eq. 005	K_{L2}		0.32
Auxiliary					
Input	V_{CC} voltage		V_{Vcc}	[V]	14
Input	Forward voltage of V_{CC} diode (D1)		$V_{F\ Vcc}$	[V]	0.6
Power					
Input	Efficency		η		0.85
Result	Nominal output power	Eq. 003	P_{OutNom}	[W]	7.90
Input	Maximum output power for over-load protection		P_{OutMax}	[W]	10
Result	Maximum input power for over-load protection	Eq. 006	P_{InMax}	[W]	12.24
Input	Minimum output power		P_{OutMin}	[W]	2
Controller/CoolSET™					
	Controller/CoolSET™				ICE5AR4770BZS
Input	Switching frequency		f_S	[Hz]	100000
Input	Targeted max. drain source voltage		V_{DSMax}	[V]	700
Input	Max. ambient temperature		T_{amax}	[°C]	50
Diode bridge and input capacitor					
Diode bridge					
Input	Power factor		$\cos\varphi$		0.6
Result	Maximum AC input current	Eq. 007	I_{ACRMS}	[A]	0.240
Result	Peak voltage at $V\ AC_{Max}$	Eq. 008	$V\ DC_{MaxPk}$	[V]	374.77

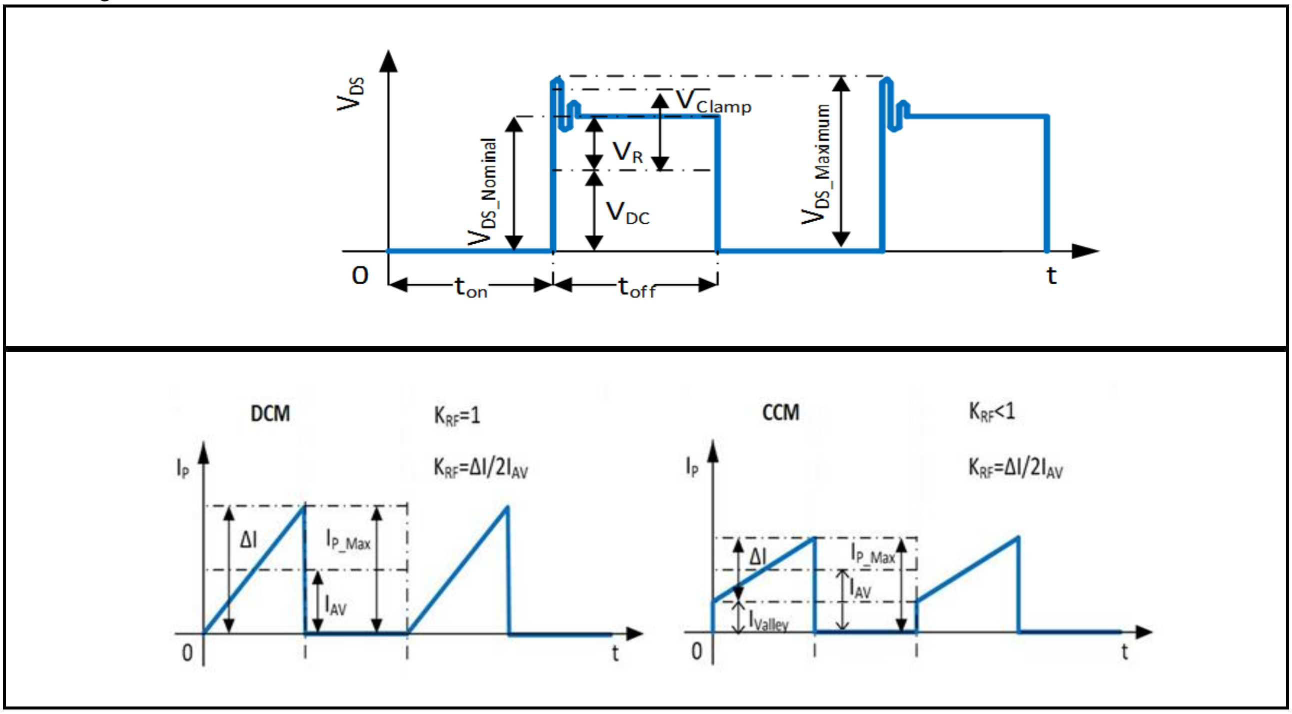
Appendix A: Transformer design and spreadsheet [3]

Input capacitor

Result	Peak voltage at V AC_{Min}	Eq. 009	V DC_{MinPk}	[V]	120.21
Result	Selected minimum DC input voltage	Eq. 010	V DC_{MinSet}	[V]	83.21
Result	Discharging time at each half-line cycle	Eq. 011	T_D	[ms]	6.19
Result	Required energy at discharging time of input capacitor	Eq. 012	W_{In}	[Ws]	0.08
Result	Calculated input capacitor	Eq. 013	C_{INCal}	[µF]	20.14
Input	Select input capacitor (C1 + C2)		C_{in}	[µF]	20
Result	Calculated minimum DC input voltage	Eq. 015	V DC_{Min}	[V]	82.89

Transformer design

Drain voltage and current waveform



Primary inductance and winding currents

Input	Reflection voltage		V_{RSET}	[V]	84
Result	Maximum duty cycle	Eq. 016	D_{Max}		0.50
Input	Select current ripple factor		K_{RF}		1
Result	Primary inductance	Eq. 017	L_P	[H]	7.11E-04
Result	Primary turn-on average current	Eq. 018	I_{AV}	[A]	0.29
Result	Primary peak-to-peak current	Eq. 019	ΔI	[A]	0.59
Result	Primary peak current	Eq. 020	I_{PMax}	[A]	0.59
Result	Primary valley current	Eq. 021	I_{Valley}	[A]	0.00
Result	Primary RMS current	Eq. 022	I_{PRMS}	[A]	0.240

Select core type

Input	Select core type				10
Result	Core type				EE16/8/5
Result	Core material				TP4A (TDG)
Result	Maximum flux density		B_{Max}	[T]	0.3
Result	Cross-sectional area		A_e	[mm²]	20.1
Result	Bobbin width		BW	[mm]	9.5
Result	Winding cross-section		A_N	[mm²]	22.3
Result	Average length of turn		l_N	[mm]	34

Winding calculation

Result	Calculated minimum number of primary turns	Eq. 023	N_{PCal}	Turns	69.19
Input	Select number of primary turns		N_P	Turns	80
Result	Calculated number of secondary 1 turns	Eq. 024	N_{S1Cal}	Turns	12.00
Input	Select number of secondary 1 turns		N_{S1}	Turns	12

Appendix A: Transformer design and spreadsheet [3]

Result	Calculated number of secondary 2 turns	Eq. 025	N_{S2Cal}	Turns	4.95
Input	Select number of secondary 2 turns		N_{S2}	Turns	5
Result	Calculated number of auxiliary turns	Eq. 026	N_{VccCal}	Turns	13.90
Input	Select number of auxiliary turns		N_{Vcc}	Turns	14
Result	Calculated V_{CC} voltage	Eq. 027	V_{VccCal}	[V]	14.10
Post calculation					
Result	Primary to secondary 1 turns ratio	Eq. 028	N_{PS1}		6.67
Result	Primary to secondary 2 turns ratio	Eq. 029	N_{PS2}		16.00
Result	Post calculated reflected voltage	Eq. 030	V_{RPost}	[V]	84.00
Result	Post calculated maximum duty cycle	Eq. 031	$D_{MaxPost}$		0.50
Result	Duty cycle prime	Eq. 032	D_{Max}'		0.50
Result	Actual flux density	Eq. 033	B_{MaxAct}	[T]	0.259
Result	Maximum DC input voltage for CCM operation	Eq. 034	$V\,DC_{maxCCM}$	[V]	82.89
Transformer winding design					
Input	Margin according to safety standard		M	[mm]	0
Input	Copper space factor		f_{Cu}		0.4
Result	Effective bobbin window	Eq. 035	BW_E	[mm]	9.5
Result	Effective winding cross-section	Eq. 036	A_{Ne}	[mm²]	22.3
Input	Primary winding area factor		AF_{NP}		0.50
Input	Secondary 1 winding area factor		AF_{NS1}		0.30
Input	Secondary 2 winding area factor		AF_{NS2}		0.15
Input	Auxiliary winding area factor		AF_{NVcc}		0.05
Primary winding					
Result	Calculated wire copper cross-sectional area	Eq. 037	A_{PCal}	[mm²]	0.0558
Result	Calculated maximum wire size	Eq. 038	AWG_{PCal}		30
Input	Select wire size		AWG_P		33
Input	Select number of parallel wire		nw_P		1
Result	Wire copper diameter	Eq. 039	d_P	[mm]	0.18
Result	Wire copper cross-sectional area	Eq. 040	A_P	[mm²]	0.0259
Result	Wire current density	Eq. 041	S_P	[A/mm²]	9.29
Input	Insulation thickness		INS_P	[mm]	0.04
Result	Turns per layer	Eq. 042	NL_P	Turns/layer	36
Result	Number of layers	Eq. 043	Ln_P	Layers	3
Secondary 1 winding					
Result	Calculated wire copper cross-sectional area	Eq. 044	A_{NS1Cal}	[mm²]	0.2230
Result	Calculated maximum wire size	Eq. 045	AWG_{S1Cal}		24
Input	Select wire size		AWG_{S1}		27
Input	Select number of parallel wire		nw_{S1}		1
Result	Wire copper diameter	Eq. 046	d_{S1}	[mm]	0.3629
Result	Wire copper cross-sectional area	Eq. 047	A_{S1}	[mm²]	0.1034
Result	Peak current	Eq. 048	I_{S1Max}	[A]	2.6728
Result	RMS current	Eq. 049	I_{S1RMS}	[A]	1.0875
Result	Wire current density	Eq. 050	S_{S1}	[A/mm²]	10.51
Input	Insulation thickness		INS_{S1}	[mm]	0.04
Result	Turns per layer	Eq. 051	NL_{S1}	Turns/layer	12
Result	Number of layers	Eq. 052	Ln_{S1}	Layers	1
Secondary 2 winding					
Result	Calculated wire copper cross-sectional area	Eq. 053	A_{NS2Cal}	[mm²]	0.2676
Result	Calculated maximum wire size	Eq. 054	AWG_{S2Cal}		23
Input	Select wire size		AWG_{S2}		27
Input	Select number of parallel wire		nw_{S2}		2
Result	Wire copper diameter	Eq. 055	d_{S2}	[mm]	0.3629
Result	Wire copper cross-sectional area	Eq. 056	A_{S2}	[mm²]	0.2069
Result	Peak current	Eq. 057	I_{S2Max}	[A]	2.9698

Appendix A: Transformer design and spreadsheet [3]

Result	RMS current	Eq. 058	I_{S2RMS}	[A]	1.2084
Result	Wire current density	Eq. 059	S_{S2}	[A/mm²]	5.84
Input	Insulation thickness		INS_{S2}	[mm]	0.04
Result	Turns per layer	Eq. 060	NL_{S2}	Turns/layer	10
Result	Number of layers	Eq. 061	Ln_{S2}	Layers	1

RCD clamper and CS resistor

RCD clamper circuit

Input	Leakage inductance percentage		$L_{LK\%}$	[Percent]	2.5
Result	Leakage inductance	Eq. 062	L_{LK}	[H]	1.78E-05
Result	Clamping voltage	Eq. 063	V_{Clamp}	[V]	241.23
Result	Calculated clamping capacitor	Eq. 064	$C_{ClampCal}$	[nF]	0.08
Input	Select clamping capacitor value (C6)		C_{clamp}	[nF]	0.47
Result	Calculated clamping resistor	Eq. 065	$R_{clampCal}$	[kΩ]	322.7
Input	Select clamping resistor value (R6)		R_{clamp}	[kΩ]	240

CS resistor

Input	CS threshold value from datasheet		V_{CS_N}	[V]	0.8
Result	Calculated CS resistor (R1A/R1B)	Eq. 066	R_{sense}	[Ω]	1.36

Ouput rectifier

Secondary 1 output rectifier

Result	Diode reverse voltage	Eq. 067	$V_{RDiode1}$	[V]	68.21
Result	Diode RMS current		I_{S1RMS}	[A]	1.09
Input	Max. voltage undershoot at output capacitor		ΔV_{Out1}	[V]	0.3
Input	Number of clock periods		n_{cp1}		20
Result	Output capacitor ripple current	Eq. 068	$I_{Ripple1}$	[A]	0.99
Result	Calculated minimum output capacitor	Eq. 069	$C_{Out1Cal}$	[µF]	300
Input	Select output capacitor value (C11)		C_{Out1}	[µF]	470
Input	ESR (Z_{max}) value from datasheet at 100 kHz		R_{ESR1}	[Ω]	0.032
Input	Number of parallel capacitors		nc_{COut1}		1
Result	Zero frequency of output capacitor	Eq. 070	f_{ZCOut1}	[Khz]	10.58
Result	First-stage ripple voltage	Eq. 071	$V_{Ripple1}$	[V]	0.085530
Input	Select LC filter inductor value (L2)		L_{out1}	[µH]	2.2
Result	Calculated LC filter capacitor	Eq. 072	C_{LCCal1}	[µF]	102.8
Input	Select LC filter capacitor value (C12)		C_{LC1}	[µF]	220
Result	LC filter frequency	Eq. 073	f_{LC1}	[Khz]	7.23
Result	Second-stage ripple voltage	Eq. 074	$V_{2ndRipple1}$	[mV]	0.45

Secondary 2 output rectifier

Result	Diode reverse voltage	Eq. 075	$V_{RDiode2}$	[V]	28.42
Result	Diode RMS current		I_{S2RMS}	[A]	1.21
Input	Max. voltage undershoot at output capacitor		ΔV_{Out1}	[V]	0.3
Input	Number of clock periods		n_{cp2}		20
Result	Output capacitor ripple current	Eq. 076	$I_{Ripple2}$	[A]	1.10
Result	Calculated minimum output capacitor	Eq. 077	$C_{Out2Cal}$	[µF]	333
Input	Select output capacitor value (C13)		C_{Out2}	[µF]	330
Input	ESR (Z_{max}) value from datasheet at 100 kHz		R_{ESR2}	[Ω]	0.032
Input	Number of parallel capacitors		nc_{COut2}		1
Result	Zero frequency of output capacitor	Eq. 078	f_{ZCOut2}	[Khz]	15.07
Result	First-stage ripple voltage	Eq. 079	$V_{Ripple2}$	[V]	0.10
Input	Select LC filter inductor value (L3)		L_{out}	[µH]	2.2
Result	Calculated LC filter capacitor	Eq. 080	C_{LCCal2}	[µF]	50.7
Input	Select LC filter capacitor value (C14)		C_{LC2}	[µF]	330
Result	LC filter frequency	Eq. 081	f_{LC2}	[Khz]	5.91
Result	Second-stage ripple voltage	Eq. 082	$V_{2ndRipple2}$	[mV]	0.33

Appendix A: Transformer design and spreadsheet [3]

V_{CC} diode and capacitor

Result	Auxiliary diode reverse voltage (D1)	Eq. 083	$V_{RDiodeVCC}$	[V]	79.68
Input	Soft-start time from datasheet		t_{ss}	[ms]	12
Input	$I_{VCC,Charge3}$ from datasheet		$I_{VCC\_Charge3}$	[mA]	3
Input	V_{CC} on-threshold		V_{VCC_ON}	[V]	16
Input	V_{CC} off-threshold		V_{VCC_OFF}	[V]	10
Result	Calculated V_{CC} capacitor	Eq. 084	C_{VCCCal}	[µF]	6.00
Input	Select V_{CC} capacitor (C3)		C_{VCC}	[µF]	22
Input	V_{CC} short threshold from datasheet		V_{VCC_SCP}	[V]	1.1
Input	$I_{VCC\_Charge1}$ from datasheet		$I_{VCC\_Charge1}$	[mA]	0.2
Result	Start-up time	Eq. 085	$t_{StartUp}$	[ms]	230.267

Calculation of losses

Input diode bridge

Input	Diode bridge forward voltage		V_{FBR}	[V]	1
Result	Diode bridge power loss	Eq. 086	P_{DIN}	[W]	0.48

Transformer copper

Result	Primary winding copper resistance	Eq. 087	R_{PCu}	[mΩ]	1808.16
Result	Secondary 1 winding copper resistance	Eq. 088	R_{S1Cu}	[mΩ]	67.85
Result	Secondary 2 winding copper resistance	Eq. 089	R_{S2Cu}	[mΩ]	14.13
Result	Primary winding copper loss	Eq. 090	P_{PCu}	[mW]	104.37
Result	Secondary 1 winding copper loss	Eq. 091	P_{S1Cu}	[mW]	80.24
Result	Secondary 2 winding copper loss	Eq. 092	P_{S2Cu}	[mW]	20.64
Result	Total transformer copper loss	Eq. 093	P_{Cu}	[W]	0.2052

Output rectifier diode

Result	Secondary 1 diode loss	Eq. 094	P_{Diode1}	[W]	0.65
Result	Secondary 2 diode loss	Eq. 095	P_{Diode2}	[W]	0.24

RCD clamper circuit

Result	RCD clamper loss	Eq. 096	$P_{Clamper}$	[W]	0.41

CS resistor

Result	CS resistor loss	Eq. 097	P_{CS}	[W]	0.08

MOSFET

Input	R_{DSON} from datasheet		R_{DSON} at T_A = 125°C	[Ω]	8.73
Input	$C_{o(er)}$ from datasheet		$C_{o(er)}$	[pF]	3.4
Input	External drain-to-source capacitance		C_{DS}	[pF]	0
Result	Switch-on loss at minimum AC input voltage	Eq. 098	$P_{SONMinAC}$	[W]	0.0047
Result	Conduction loss at minimum AC input voltage	Eq. 099	$P_{condMinAC}$	[W]	0.5039
Result	Total MOSFET loss at minimum AC input voltage	Eq. 100	$P_{MOSMinAC}$	[W]	0.5086
Result	Switch-on loss at maximum AC input voltage	Eq. 101	$P_{SONMaxAC}$	[W]	0.0358
Result	Conduction loss at maximum AC input voltage	Eq. 102	$P_{condMaxAC}$	[W]	0.1114
Result	Total MOSFET loss at maximum AC input voltage	Eq. 103	$P_{MOSMaxAC}$	[W]	0.1472
Result	Total MOSFET loss (from minimum or maximum AC)		P_{MOS}	[W]	0.5086

Controller

Input	Controller current consumption		I_{VCC_Normal}	[mA]	0.9
Result	Controller loss	Eq. 104	P_{Ctrl}	[W]	0.0127

Efficiency after losses

Result	Total power loss	Eq. 105	P_{Losses}	[W]	2.59
Result	Post calculated efficiency	Eq. 106	η_{Post}	[Percent]	80.05 percent

CoolSET™/MOSFET temperature

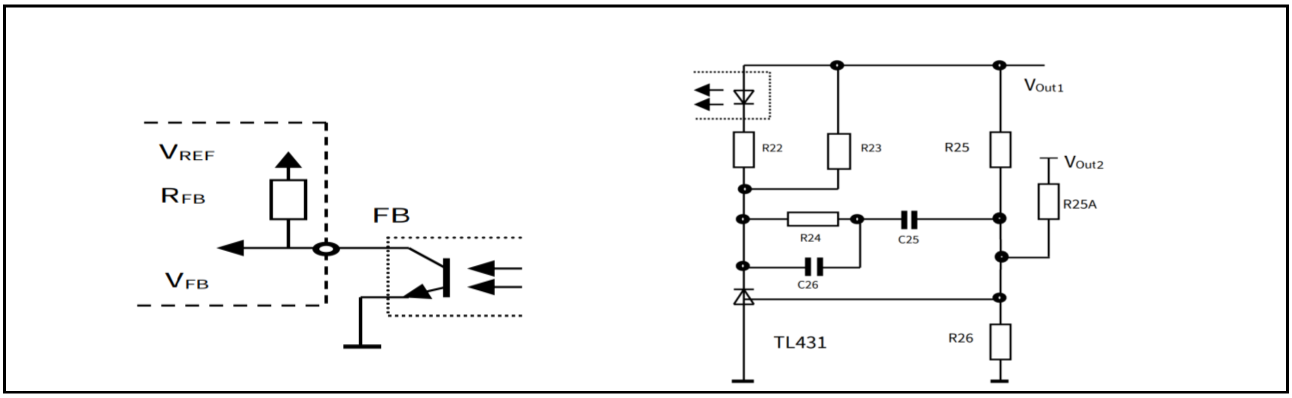
CoolSET™/MOSFET temperature

Input	Thermal resistance junction-ambient (include copper pour)		R_{thJA_As}	[°K/W]	65.0
Result	Temperature rise	Eq. 107	ΔT	[°K]	33.1
Result	Junction temperature at T_{amax}	Eq. 108	T_{jmax}	°C	83.1

Appendix A: Transformer design and spreadsheet [3]

Output regulation (isolated using TL431 and optocoupler)

Isolated FB circuit



Output regulation

Input	TL431 reference voltage		V_{REF_TL}	[V]	2.5
Input	Weighted regulation factor of V_{Out1}		W_1		0
Input	Current for voltage divider resistor R26		I_{R26}	[mA]	0.208
Result	Calculated voltage divider resistor	Eq. 111	$R26_{Cal}$	[kΩ]	12
Input	Select voltage divider resistor value		R26	[kΩ]	12
Result	Calculated voltage divider resistor	Eq. 112	$R25_{Cal}$	[kΩ]	#DIV/0!
Input	Select voltage divider resistor value		R25	[kΩ]	1.00E+30
Result	Calculated voltage divider resistor	Eq. 113	$R25A_{Cal}$	[kΩ]	12.00
Input	Select voltage divider resistor value		R25A	[kΩ]	12

Optocoupler and TL431 bias

Input	Current Transfer Ratio (CTR)		G_C	[Percent]	200 percent
Input	Optocoupler diode forward voltage		V_{FOpto}	[V]	1.25
Input	Maximum current for optocoupler diode		I_{Fmax}	[mA]	50
Input	Minimum current for TL431		I_{KAmin}	[mA]	1
Result	Calculated minimum optocoupler bias resistance (R7)	Eq. 114	$R22_{Cal}$	[kΩ]	0.0250
Input	Select optocoupler bias resistor (R7)		R22	[kΩ]	0.33
Input	FB pull-up reference voltage V_{REF} from datasheet		V_{REF}	[V]	3.3
Input	V_{FB_OLP} from datasheet		V_{FB_OLP}	[V]	2.75
Input	R_{FB} from datasheet		R_{FB}	[kΩ]	15
Result	Calculated maximum TL431 bias resistance (R8)	Eq. 115	$R23_{Cal}$	[kΩ]	1.26
Input	Selected TL431 bias resistor (R8)		R23	[kΩ]	1.2

Regulation loop

Result	FB transfer characteristic	Eq. 116	K_{FB}		90.91
Result	Gain of FB transfer characteristic	Eq. 117	G_{FB}	[dB]	39.17
Result	Voltage divider transfer characteristic	Eq. 118	K_{VD}		0.208333
Result	Gain of voltage divider transfer characteristic	Eq. 119	G_{VD}	[dB]	-13.62
Result	Resistance at maximum load pole	Eq. 120	R_{LH}	[Ω]	13.85
Result	Resistance at minimum load pole	Eq. 121	R_{LL}	[Ω]	72.00
Result	Poles of power stage at maximum load pole	Eq. 122	f_{OH}	[Hz]	48.91
Result	Poles of power stage at minimum load pole	Eq. 123	f_{OL}	[Hz]	9.41
Result	Zero frequency of the compensation network	Eq. 124	f_{OM}	[Hz]	21.45
Input	Zero dB crossover frequency		fg	[kHz]	8
Input	PWM-OP gain from datasheet		A_V		2.03
Result	Transient impedance	Eq. 117	Z_{PWM}	[V/A]	3.5
Result	Power stage at crossover frequency	Eq. 118	$\|F_{PWR}(fg)\|$		0.036
Result	Gain of power stage at crossover frequency	Eq. 119	$G_{PWR}(fg)$	[dB]	-28.84
Result	Gain of the regulation loop at fg	Eq. 120	Gs(ω)	[dB]	-3.292
Result	Separated components of the regulator	Eq. 121	Gr(ω)	[dB]	3.292
Result	Calculated resistance value of compensation network (R9)	Eq. 122	$R24_{Cal}$	[kΩ]	17.53
Input	Select resistor value of compensation network (R9)		R24	[kΩ]	18
Result	Calculated capacitance value of compensation network (C7)	Eq. 123	$C26_{Cal}$	[nF]	1.105

Appendix A: Transformer design and spreadsheet [3]

Input	Select capacitor value of compensation network (C7)		C26	[nF]	1
Result	Calculated capacitance value of compensation network (C8)	Eq. 124	$C25_{Cal}$	[nF]	411.22
Input	Select capacitor value of compensation network (C8)		C25	[nF]	220

Final design

Electrical

	Minimum AC voltage			[V]	85
	Maximum AC voltage			[V]	265
	Maximum input current			[A]	0.14
	Minimum DC voltage			[V]	83
	Maximum DC voltage			[V]	375
	Maximum output power			[W]	10.4
	Output voltage 1			[V]	12.0
	Output ripple voltage 1			[mV]	0.4
	Output voltage 2			[V]	5.0
	Output ripple voltage 2			[mV]	0.3
	Transformer peak current			[A]	0.59
	Maximum duty cycle				0.50
	Reflected voltage			[V]	84
	Copper losses			[W]	0.21
	MOSFET losses			[W]	0.51
	Sum losses			[W]	2.59
	Efficiency			[Percent]	80.05 percent

Transformer

	Core type				EE16/8/5
	Core material				TP4A (TDG)
	Effective core area			[mm²]	20.1
	Maximum flux density			[mT]	259
	Inductance			[µH]	711
	Margin			[mm]	0
	Primary turns			Turns	80
	Primary copper wire size			AWG	33
	Number of primary copper wires in parallel				1
	Primary layers			Layer	3
	Secondary 1 turns (N_{S1})			Turns	12
	Secondary 1 copper wire size			AWG	27
	Number of secondary 1 copper wires in parallel				1
	Secondary 1 layers			Layer	1
	Secondary 2 turns (N_{S2})			Turns	5
	Secondary 2 copper wire size			AWG	27
	Number of secondary 2 copper wires in parallel				2
	Secondary 2 layers			Layer	1
	Auxiliary turns			Turns	14
	Leakage inductance			[µH]	17.8

Components

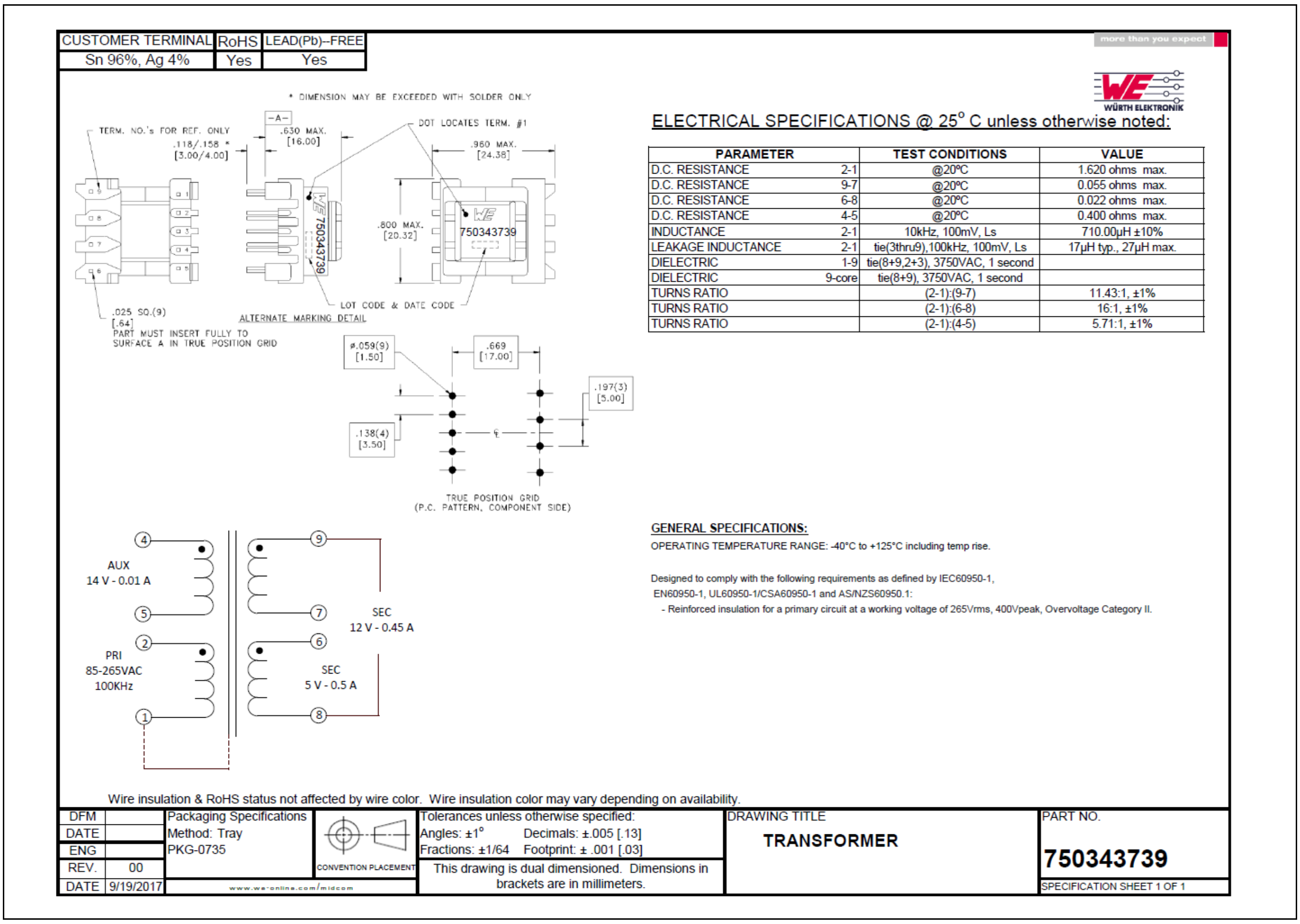
	Input capacitor (C1)			[µF]	20.0
	Secondary 1 output capacitor (C152)			[µF]	470.0
	Secondary 1 output capacitor in parallel				1.0
	Secondary 1 LC filter inductor (L151)			[µH]	2.2
	Secondary 1 LC filter capacitor (C153)			[µF]	220.0
	Secondary 2 output capacitor (C102)			[µF]	330.0
	Secondary 2 output capacitor in parallel				1.0
	Secondary 2 LC filter inductor (L101)			[µH]	2.2
	Secondary 2 LC filter capacitor (C103)			[µF]	330.0
	V_{CC} capacitor (C3)			[µF]	22.0
	Sense resistor (R8A, R8B)			[Ω]	1.36
	Clamping resistor (R4)			[kΩ]	240.0
	Clamping capacitor (C2)			[nF]	0

Appendix A: Transformer design and spreadsheet [3]

Regulation components (isolated using TL431 and optocoupler)

Voltage divider		R26	[kΩ]	12.0
Voltage divider (V_{out1} sense)		R25	[kΩ]	
Voltage divider (V_{out2} sense)		R25A	[kΩ]	12.0
Optocoupler bias resistor		R22	[kΩ]	0.33
TL431 bias resistor		R23	[kΩ]	1.2
Compensation network resistor		R24	[kΩ]	18.0
Compensation network capacitor		C26	[nF]	1.00
Compensation network capacitor		C25	[nF]	220.0

12 Appendix B: WE transformer specification



CUSTOMER TERMINAL	RoHS	LEAD(Pb)–FREE
Sn 96%, Ag 4%	Yes	Yes

ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	2-1	@20ºC	1.620 ohms max.
D.C. RESISTANCE	9-7	@20ºC	0.055 ohms max.
D.C. RESISTANCE	6-8	@20ºC	0.022 ohms max.
D.C. RESISTANCE	4-5	@20ºC	0.400 ohms max.
INDUCTANCE	2-1	10kHz, 100mV, Ls	710.00µH ±10%
LEAKAGE INDUCTANCE	2-1	tie(3thru9),100kHz, 100mV, Ls	17µH typ., 27µH max.
DIELECTRIC	1-9	tie(8+9,2+3), 3750VAC, 1 second	
DIELECTRIC	9-core	tie(8+9), 3750VAC, 1 second	
TURNS RATIO		(2-1):(9-7)	11.43:1, ±1%
TURNS RATIO		(2-1):(6-8)	16:1, ±1%
TURNS RATIO		(2-1):(4-5)	5.71:1, ±1%

GENERAL SPECIFICATIONS:

OPERATING TEMPERATURE RANGE: -40°C to +125°C including temp rise.

Designed to comply with the following requirements as defined by IEC60950-1, EN60950-1, UL60950-1/CSA60950-1 and AS/NZS60950.1:
- Reinforced insulation for a primary circuit at a working voltage of 265Vrms, 400Vpeak, Overvoltage Category II.

Figure 34 Transformer structure

13 References

[1] ICE5AR4770BZS datasheet, Infineon Technologies AG

[2] 5^{th}-Generation Fixed-Frequency Design Guide

[3] Calculation Tool Fixed-Frequency CoolSET^{TM} Generation 5

Revision history

Document version	Date of release	Description of changes
V 1.0	6 Feb 2018	First release

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