Document Number: A2T09VD250N
Rev. 0, 8/2015

RoHS

RF Power LDMOS Transistor

N–Channel Enhancement–Mode Lateral MOSFET

This 65 W RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 716 to 960 MHz.

900 MHz

- Typical Single–Carrier W–CDMA Performance: V_{DD} = 48 Vdc, $I_{DQ(A+B)}$ = 1000 mA, P_{out} = 65 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
920 MHz	22.5	34.8	7.5	–34.4	–18
940 MHz	22.7	35.4	7.4	–34.2	–19
960 MHz	22.4	35.4	7.2	–34.3	–12

800 MHz

- Typical Single–Carrier W–CDMA Performance: V_{DD} = 48 Vdc, $I_{DQ(A+B)}$ = 1000 mA, P_{out} = 65 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

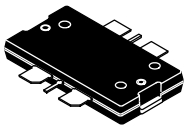
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
790 MHz	23.0	37.3	7.4	–33.0	–15
806 MHz	23.1	37.8	7.2	–33.3	–19
821 MHz	22.8	37.0	7.0	–33.8	–13

Features

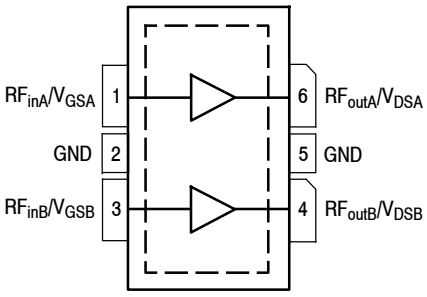
- Greater Negative Gate–Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications

A2T09VD250NR1

716–960 MHz, 65 W AVG., 48 V AIRFAST RF POWER LDMOS TRANSISTOR



TO–270WB–6A PLASTIC



(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 1. Pin Connections

freescale Airfast

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +105	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	55, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 82°C, 65 W CW, 48 Vdc, $I_{DQ(A+B)}$ = 1000 mA, 940 MHz	$R_{\theta JC}$	0.56	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	IV

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 105 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 55 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (4) (V_{DS} = 10 Vdc, I_D = 96 μAdc)	$V_{GS(th)}$	1.3	1.8	2.3	Vdc
Gate Quiescent Voltage (5) (V_{DS} = 48 Vdc, $I_{DQ(A+B)}$ = 1000 mAdc)	$V_{GS(Q)}$	—	2.5	—	Vdc
Fixture Gate Quiescent Voltage (5) (V_{DD} = 48 Vdc, $I_{DQ(A+B)}$ = 1000 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	4.0	5.0	6.0	Vdc
Drain-Source On-Voltage (4) (V_{GS} = 10 Vdc, I_D = 0.96 Adc)	$V_{DS(on)}$	0.1	0.21	0.5	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf and search for AN1955.
4. Each side of device measured separately.
5. Side A and Side B are tied together for this measurement.

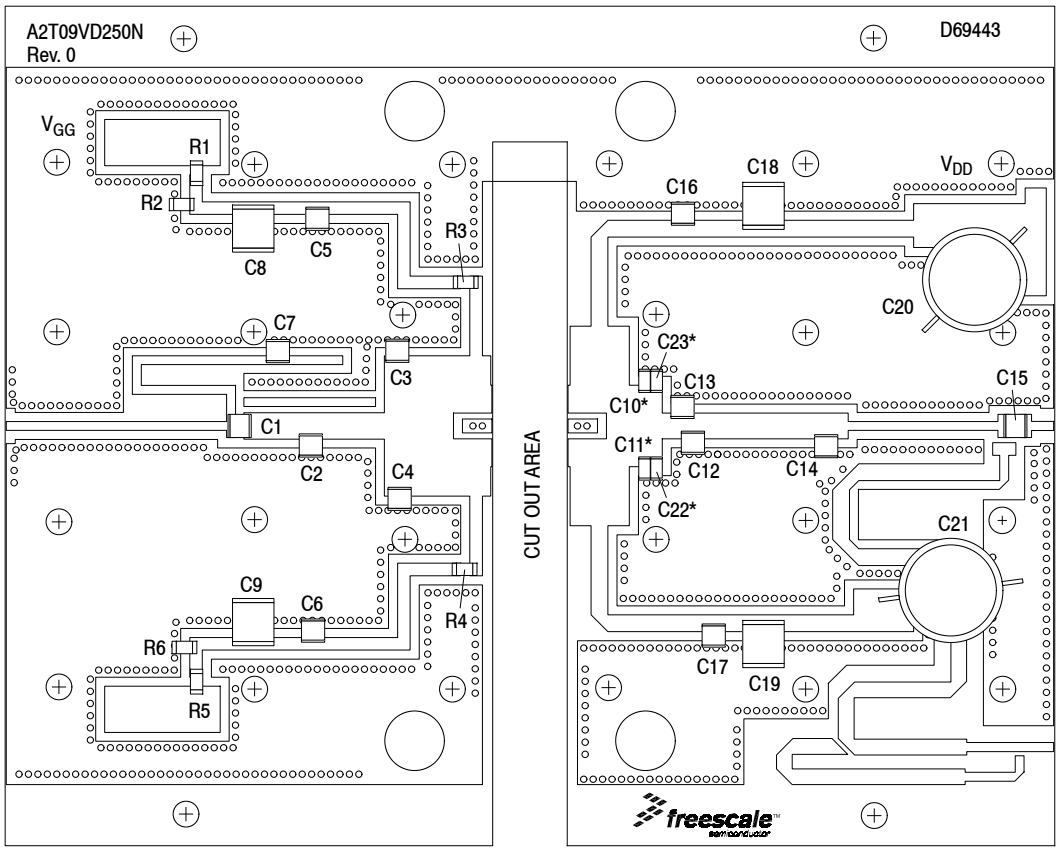
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests(1) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, $I_{DQ(A+B)}$ = 1000 mA, P_{out} = 65 W Avg., f = 920 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	21.0	22.5	24.0	dB
Drain Efficiency	η_D	31.0	34.8	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.8	7.5	—	dB
Adjacent Channel Power Ratio	ACPR	—	–34.4	–31.5	dBc
Input Return Loss	IRL	—	–18	–10	dB
Load Mismatch (In Freescale Test Fixture, 50 ohm system) $I_{DQ(A+B)}$ = 1000 mA, f = 940 MHz, 12 μsec(on), 10% Duty Cycle					
VSWR 10:1 at 52 Vdc, 363 W Pulsed CW Output Power (3 dB Input Overdrive from 308 W Pulsed CW Rated Power)	No Device Degradation				
Typical Performance (In Freescale Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, $I_{DQ(A+B)}$ = 1000 mA, 920–960 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	240	—	W
P_{out} @ 3 dB Compression Point(2)	P3dB	—	326	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 920–960 MHz frequency range)	Φ	—	19	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	90	—	MHz
Gain Flatness in 40 MHz Bandwidth @ P_{out} = 65 W Avg.	G_F	—	0.3	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.013	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.007	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2T09VD250NR1	R1 Suffix = 500 Units, 44 mm Tape Width, 13-inch Reel	TO-270WB-6A

1. Part internally input matched.
2. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.



*C10, C11, C22 and C23 are mounted vertically.

Figure 2. A2T09VD250NR1 Test Circuit Component Layout

Table 7. A2T09VD250NR1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	3.3 pF Chip Capacitor	ATC800B3R3BT500XT	ATC
C2	2.7 pF Chip Capacitor	ATC800B2R7BT500XT	ATC
C3, C4	4.3 pF Chip Capacitors	ATC800B4R3BT500XT	ATC
C5, C6, C7, C15, C16, C17	47 pF Chip Capacitors	ATC800B470JT500XT	ATC
C8, C9	1 μF Chip Capacitors	C3216X7R2A105M160AA	TDK
C10, C11	12 pF Chip Capacitors	ATC800B120JT500XT	ATC
C12	5.1 pF Chip Capacitor	ATC800B5R1BT500XT	ATC
C13	4.7 pF Chip Capacitor	ATC800B4R7BT500XT	ATC
C14	5.6 pF Chip Capacitor	ATC800B5R6BT500XT	ATC
C18, C19	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C20, C21	220 μF, 100 V Electrolytic Capacitors	EEVFK2A221M	Panasonic
C22, C23	1.7 pF Chip Capacitor	ATC800B1R7BT500XT	ATC
R1, R2, R5, R6	1 kΩ, 1/4 W Chip Resistors	WCR1206-1KF	Welwyn
R3, R4	10 Ω, 1/4 W Chip Resistors	WCR1206-10RF	Welwyn
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D69443	MTL

TYPICAL CHARACTERISTICS

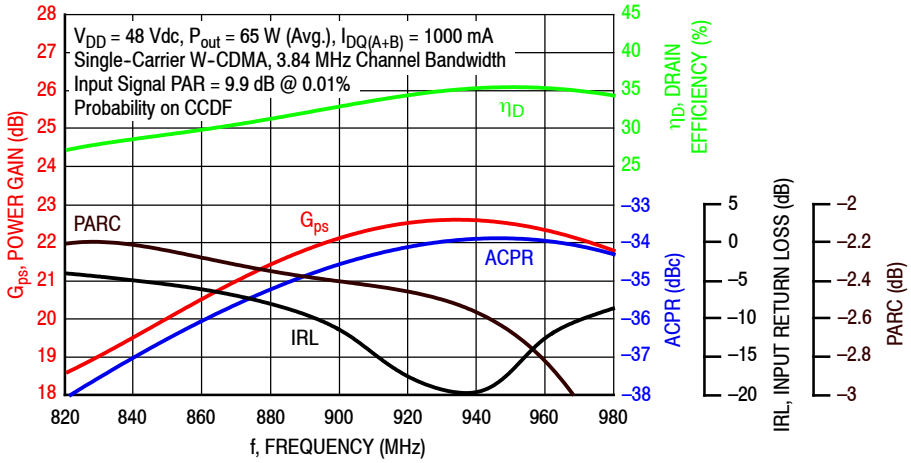


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 65 Watts Avg.

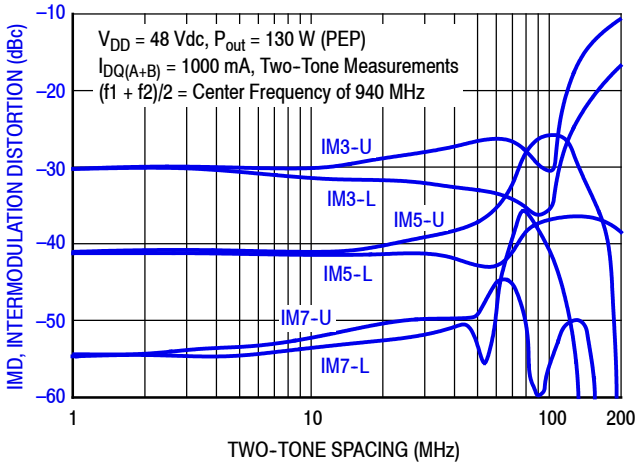


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

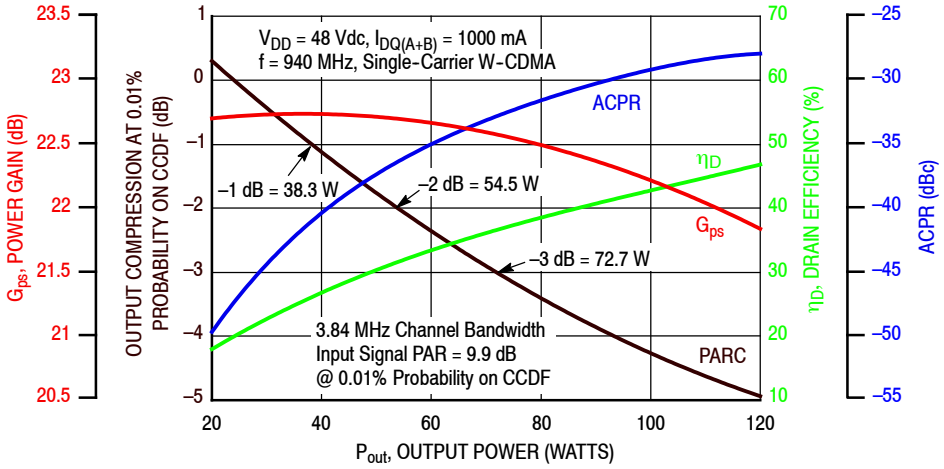


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

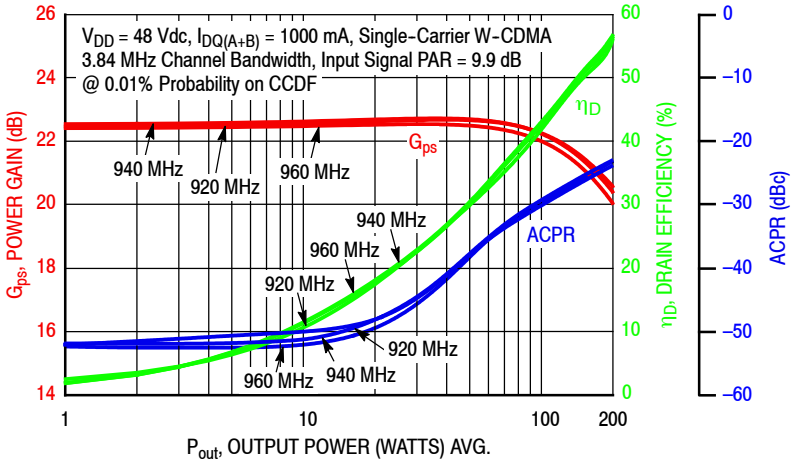


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

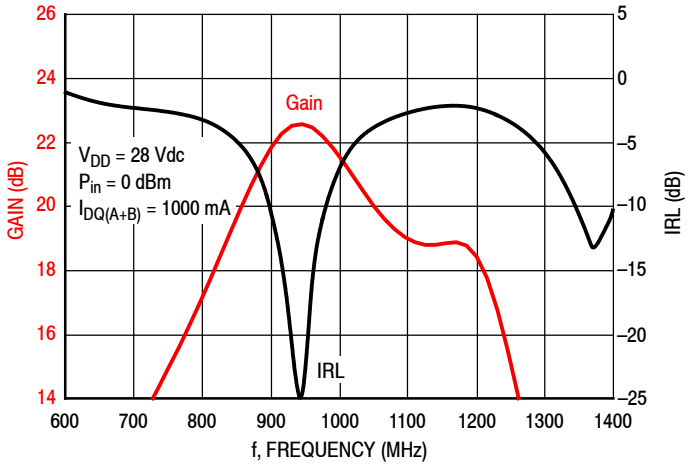


Figure 7. Broadband Frequency Response

Table 8. Single Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, I_{DQ} = 500 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.52 – j4.76	2.19 + j4.75	3.04 + j0.55	21.4	52.5	178	61.2	–14
940	2.88 – j5.34	2.22 + j5.10	2.93 + j0.37	21.4	52.5	178	61.8	–14
960	3.53 – j5.36	2.36 + j5.64	2.87 + j0.07	21.3	52.4	174	60.3	–12

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.52 – j4.76	2.01 + j5.09	3.37 + j0.34	19.4	53.2	208	62.3	–20
940	2.88 – j5.34	2.06 + j5.48	3.24 + j0.13	19.3	53.2	207	62.2	–19
960	3.53 – j5.36	2.19 + j6.04	3.19 – j0.10	19.2	53.1	204	61.5	–18

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

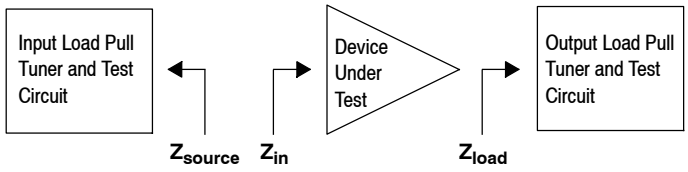
Table 9. Single Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 48 Vdc, I_{DQ} = 500 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.52 – j4.76	1.87 + j4.79	2.65 + j2.94	23.8	50.8	121	71.4	–20
940	2.88 – j5.34	1.85 + j5.18	2.40 + j2.86	24.0	50.4	111	71.9	–21
960	3.53 – j5.36	1.99 + j5.66	2.32 + j2.45	23.7	50.5	112	70.9	–19

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.52 – j4.76	1.83 + j5.10	3.13 + j2.50	21.3	52.1	162	72.0	–26
940	2.88 – j5.34	1.83 + j5.50	2.80 + j2.46	21.5	51.7	149	72.1	–26
960	3.53 – j5.36	1.95 + j6.05	2.65 + j2.16	21.4	51.7	147	71.4	–25

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL LOAD PULL CONTOURS — 940 MHz

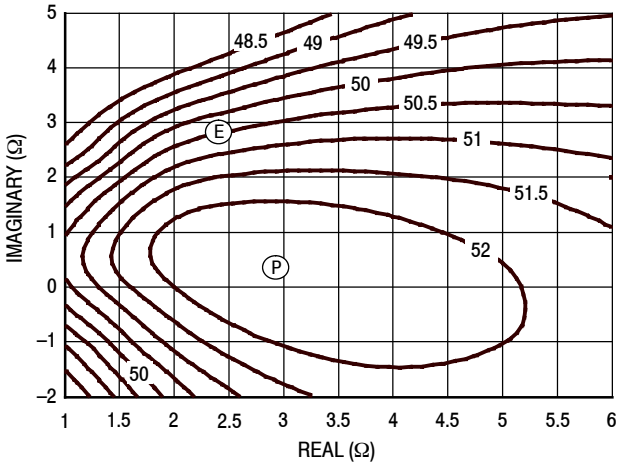


Figure 8. P1dB Load Pull Output Power Contours (dBm)

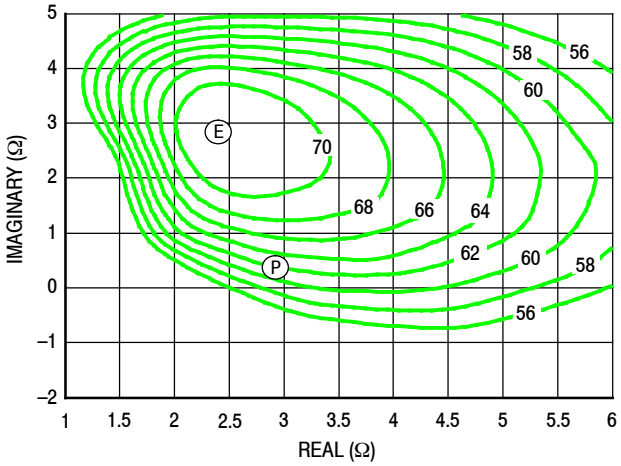


Figure 9. P1dB Load Pull Efficiency Contours (%)

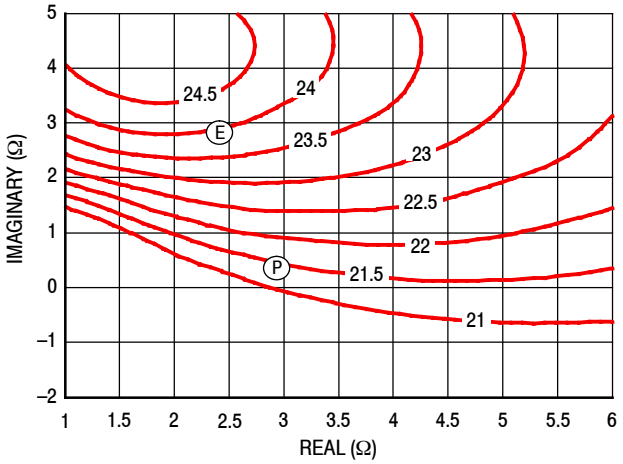


Figure 10. P1dB Load Pull Gain Contours (dB)

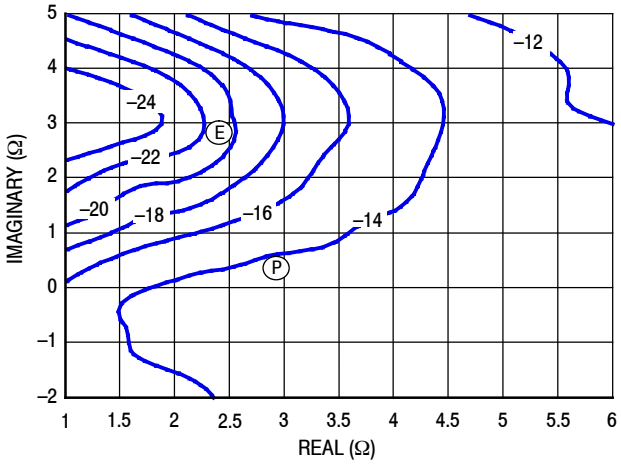


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL LOAD PULL CONTOURS — 940 MHz

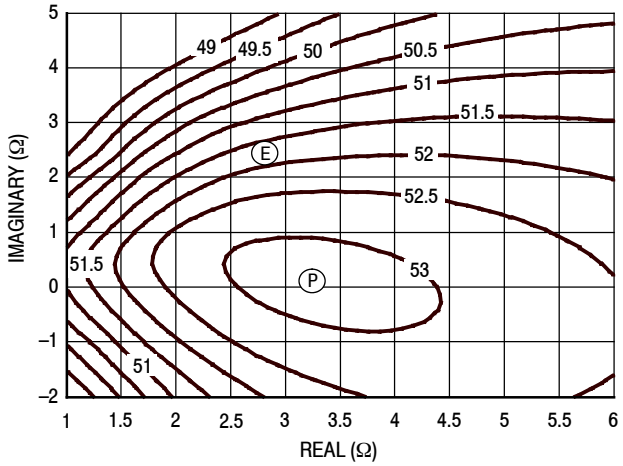


Figure 12. P3dB Load Pull Output Power Contours (dBm)

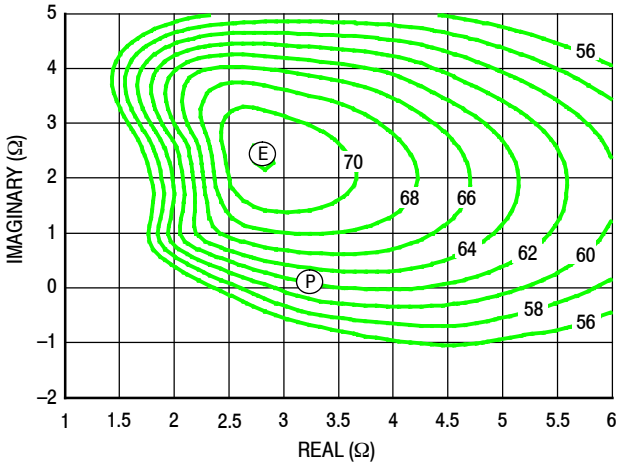


Figure 13. P3dB Load Pull Efficiency Contours (%)

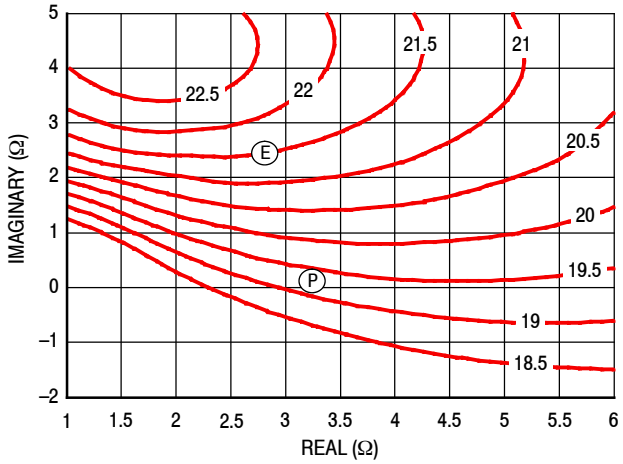


Figure 14. P3dB Load Pull Gain Contours (dB)

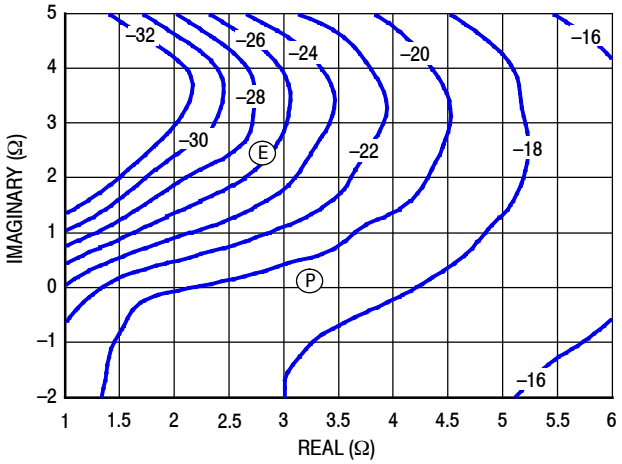


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

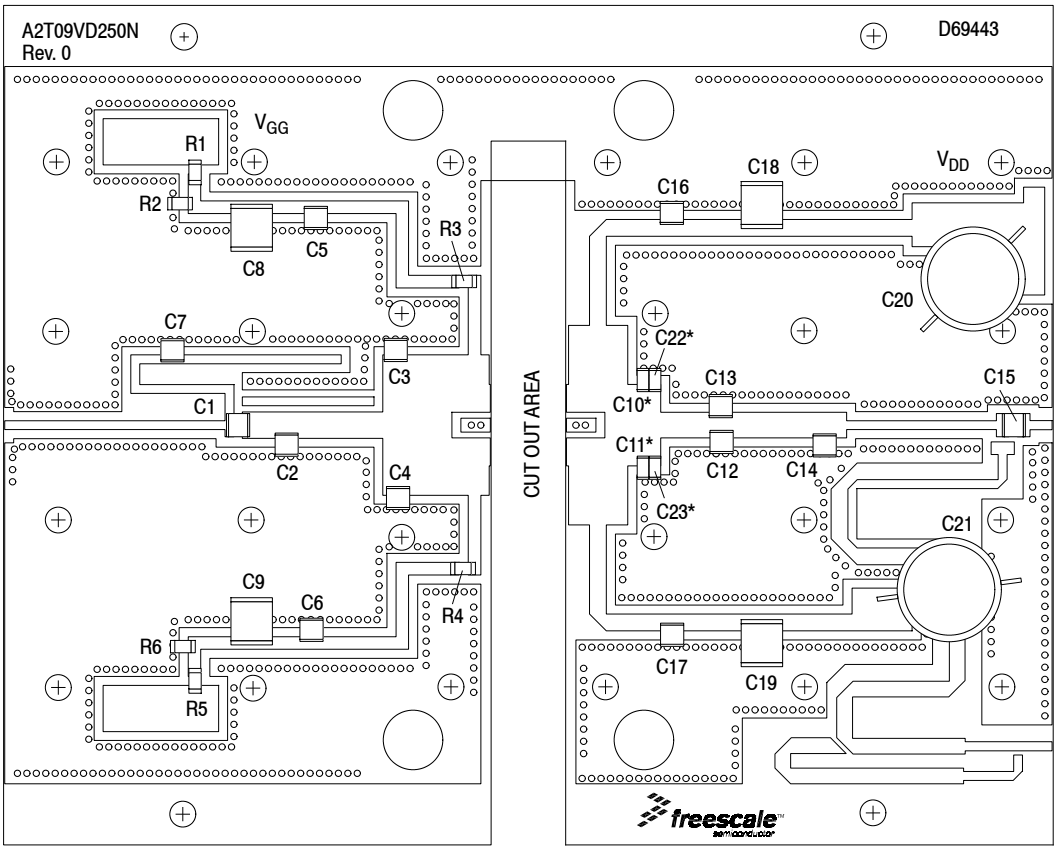
Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power



*C10, C11, C22 and C23 are mounted vertically.

Figure 16. A2T09VD250NR1 Test Circuit Component Layout — 790–821 MHz

Table 10. A2T09VD250NR1 Test Circuit Component Designations and Values — 790–821 MHz

Part	Description	Part Number	Manufacturer
C1	3.3 pF Chip Capacitor	ATC800B3R3BT500XT	ATC
C2	3.9 pF Chip Capacitor	ATC800B3R9BT500XT	ATC
C3, C4, C13, C14	6.8 pF Chip Capacitors	ATC800B6R8BT500XT	ATC
C5, C6, C7, C15, C16, C17	47 pF Chip Capacitors	ATC800B470JT500XT	ATC
C8, C9	1 μF Chip Capacitors	C3216X7R2A105M160AA	TDK
C10, C11	18 pF Chip Capacitors	ATC800B180JT500XT	ATC
C12	6.2 pF Chip Capacitor	ATC800B6R2BT500XT	ATC
C18, C19	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C20, C21	220 μF, 100 V Electrolytic Capacitors	EEVFK2A221M	Panasonic
C22, C23	0.5 pF Chip Capacitors	ATC800B0R5BT500XT	ATC
R1, R2, R5, R6	1 kΩ, 1/4 W Chip Resistors	WCR1206-1KF	Welwyn
R3, R4	10 Ω, 1/4 W Chip Resistors	WCR1206-10RF	Welwyn
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D69443	MTL

TYPICAL CHARACTERISTICS — 790–821 MHz

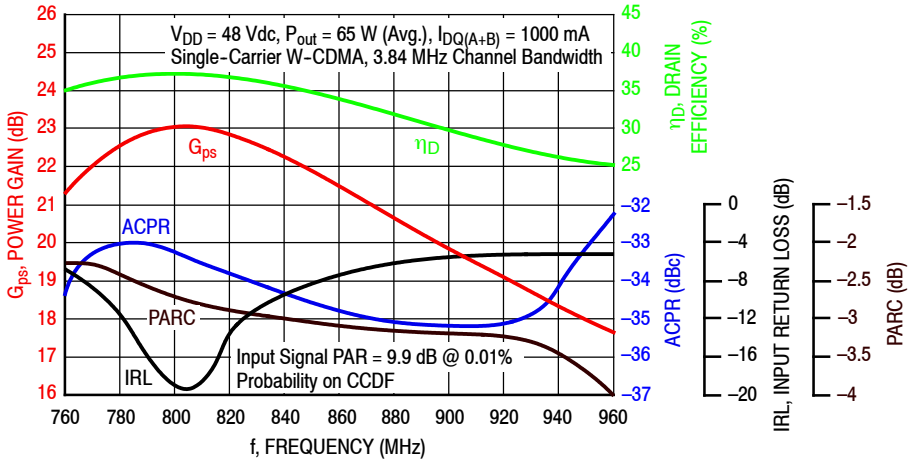


Figure 17. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 65 Watts Avg.

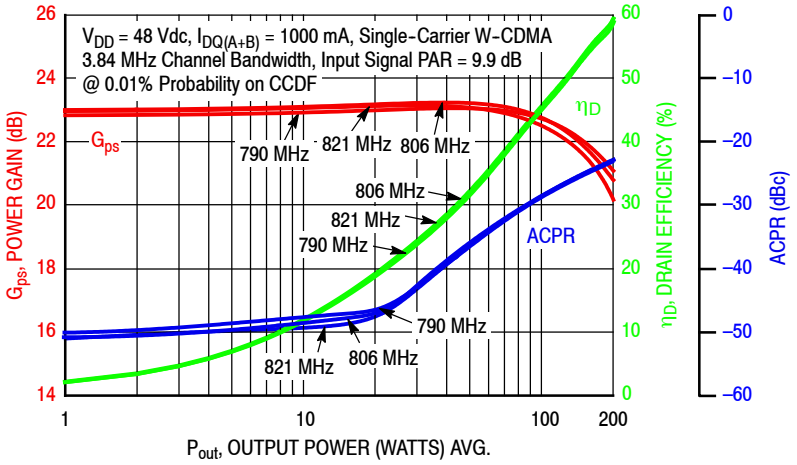


Figure 18. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

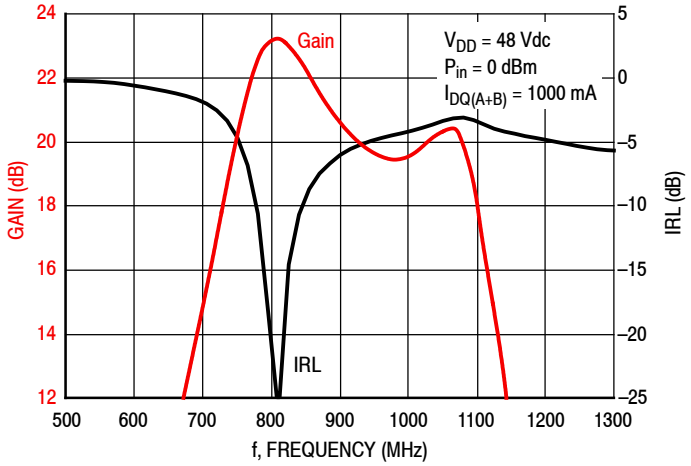


Figure 19. Broadband Frequency Response

Table 11. Single Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, I_{DQ} = 501 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
790	3.03 – j2.71	2.16 + j2.10	3.38 + j1.69	21.3	52.8	193	64.9	–12
806	3.30 – j2.82	2.16 + j2.40	3.29 + j1.70	21.3	52.7	187	63.4	–11
821	3.27 – j3.34	2.10 + j2.70	3.34 + j1.67	21.4	52.7	185	63.5	–12

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
790	3.03 – j2.71	1.99 + j2.30	3.58 + j1.49	19.2	53.4	221	65.9	–15
806	3.30 – j2.82	2.00 + j2.62	3.66 + j1.41	19.2	53.4	217	64.6	–15
821	3.27 – j3.34	1.94 + j2.93	3.67 + j1.47	19.3	53.3	215	65.7	–16

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

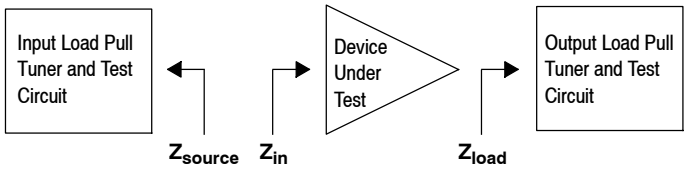
Table 12. Single Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 48 Vdc, I_{DQ} = 501 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
790	3.03 – j2.71	1.81 + j2.34	3.66 + j5.16	24.0	50.5	113	75.8	–17
806	3.30 – j2.82	1.82 + j2.60	3.53 + j4.98	24.0	50.6	114	74.9	–17
821	3.27 – j3.34	1.86 + j2.84	3.63 + j4.24	23.5	51.2	133	74.0	–15

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
790	3.03 – j2.71	1.86 + j2.40	4.26 + j3.66	21.0	52.5	177	75.2	–19
806	3.30 – j2.82	1.84 + j2.75	4.19 + j4.15	21.3	52.1	161	74.3	–20
821	3.27 – j3.34	1.81 + j3.04	4.12 + j3.87	21.2	52.2	166	73.8	–20

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL LOAD PULL CONTOURS — 806 MHz

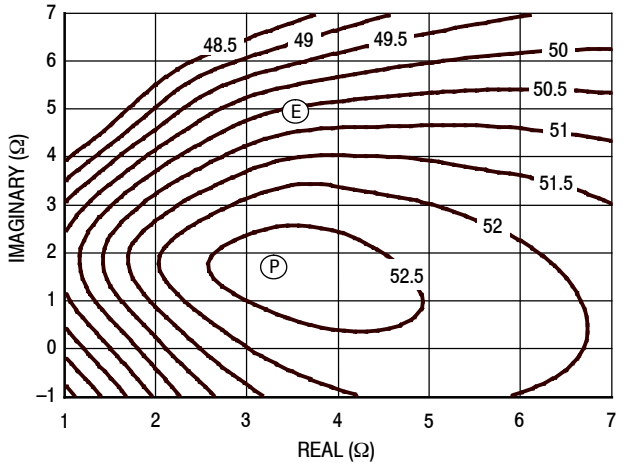


Figure 20. P1dB Load Pull Output Power Contours (dBm)

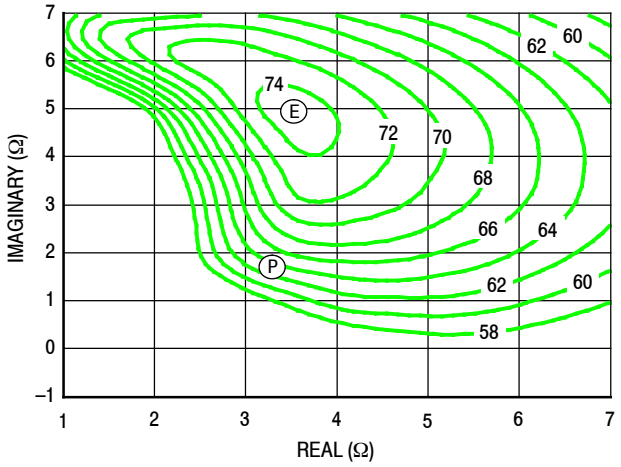


Figure 21. P1dB Load Pull Efficiency Contours (%)

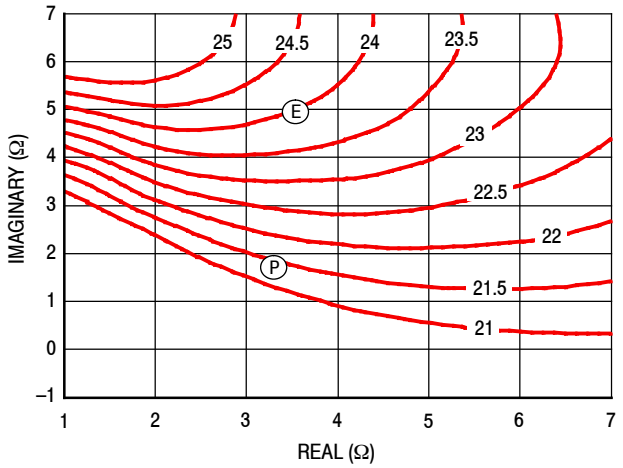


Figure 22. P1dB Load Pull Gain Contours (dB)

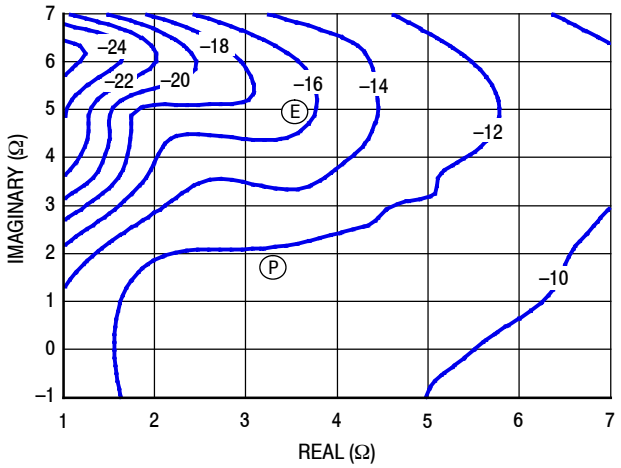


Figure 23. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL CARRIER LOAD PULL CONTOURS — 806 MHz

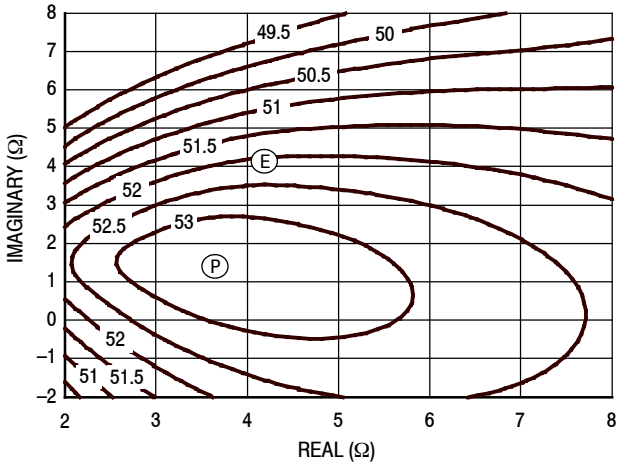


Figure 24. P3dB Load Pull Output Power Contours (dBm)

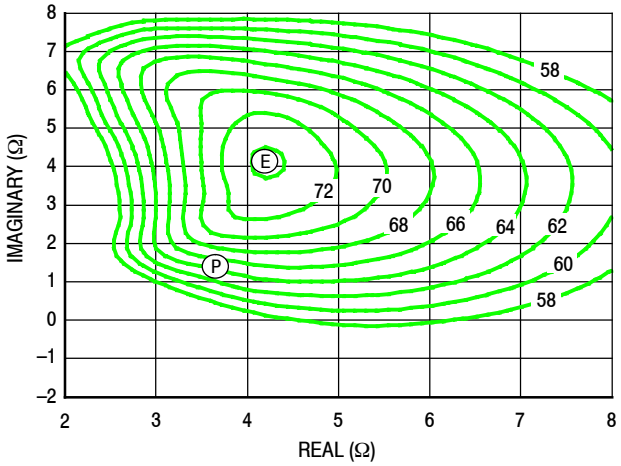


Figure 25. P3dB Load Pull Efficiency Contours (%)

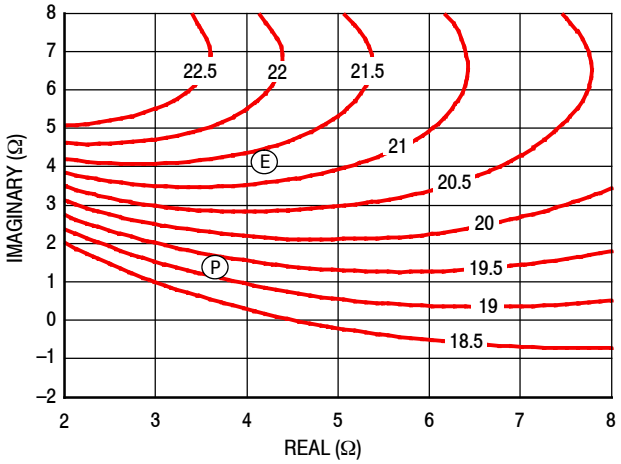


Figure 26. P3dB Load Pull Gain Contours (dB)

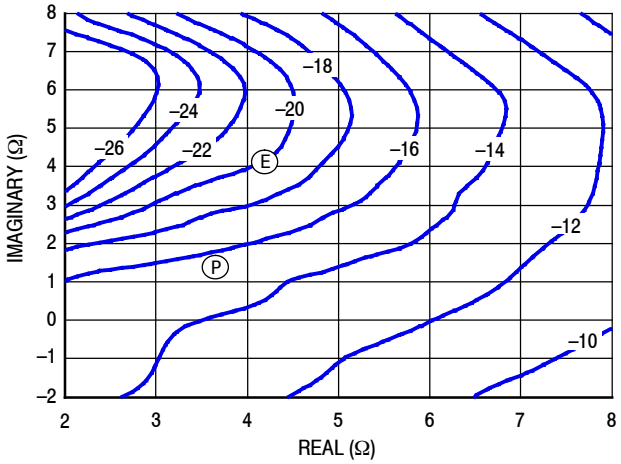


Figure 27. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

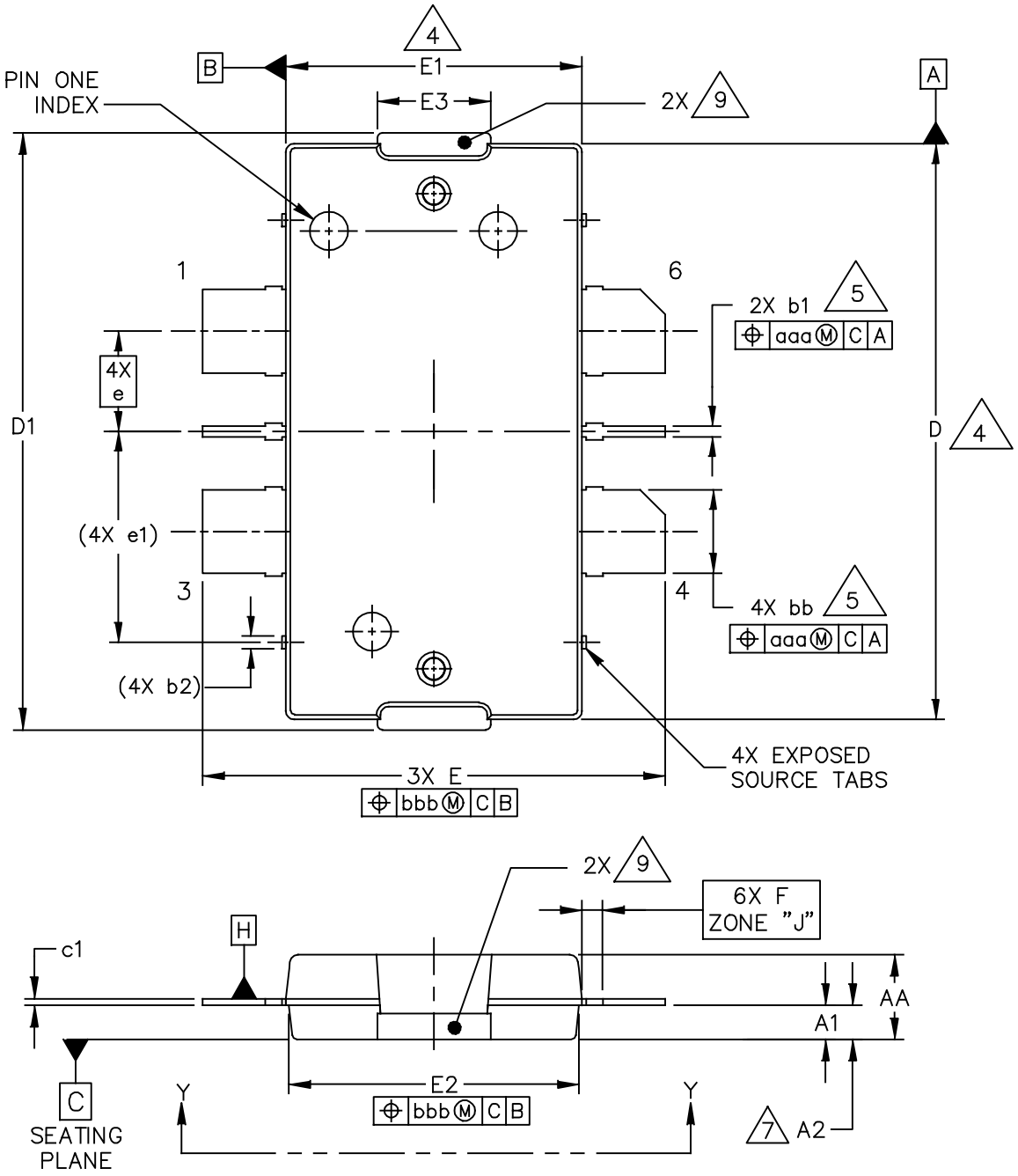
Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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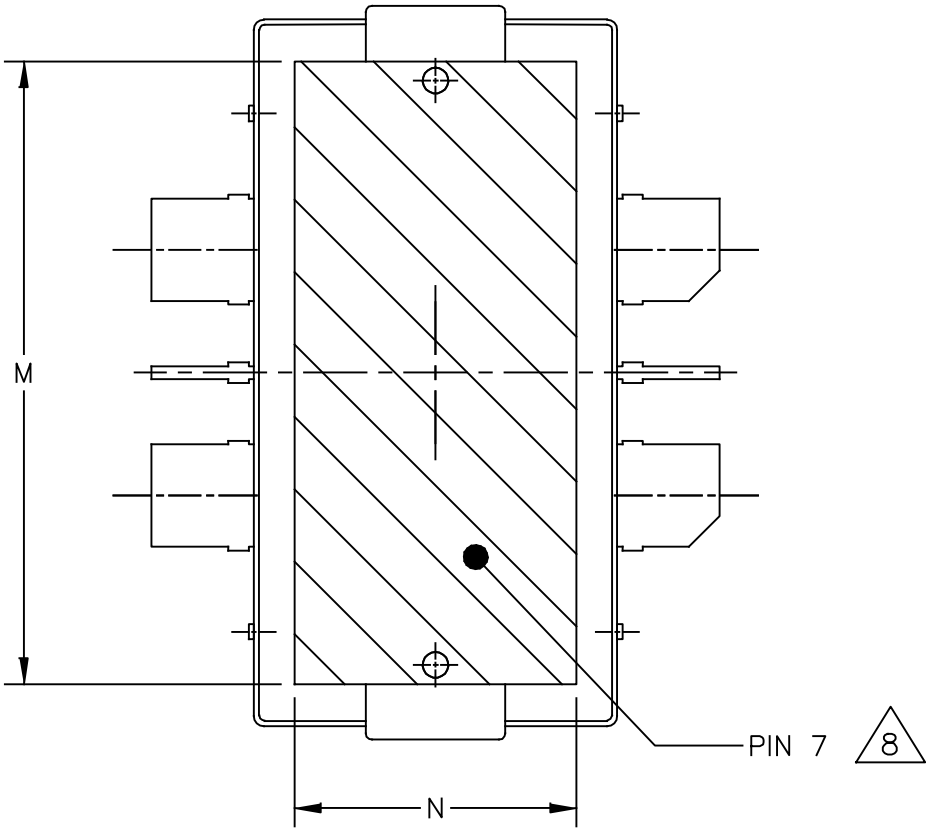
	18 JUN 2015	



VIEW Y–Y

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	STANDARD: NON–JEDEC	
	18 JUN 2015	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.

8. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.099	.105	2.51	2.67	M	.600	---	15.24	---
A1	.039	.043	0.99	1.09	N	.270	---	6.86	---
A2	.040	.042	1.02	1.07	bb	.097	.103	2.46	2.62
D	.688	.692	17.48	17.58	b1	.010	.016	0.25	0.41
D1	.712	.720	18.08	18.29	b2	---	.019	---	0.48
E	.551	.559	14.00	14.20	c1	.007	.011	0.18	0.28
E1	.353	.357	8.97	9.07	e	.120 BSC		3.05 BSC	
E2	.346	.350	8.79	8.89	e1	.253 INFO ONLY		6.43 INFO ONLY	
E3	.132	.140	3.35	3.56	aaa	.004		0.10	
F	.025 BSC		0.64 BSC		bbb	.008		0.20	

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.freescale.com/rf
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Aug. 2015	• Initial Release of Data Sheet

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Document Number: A2T09VD250N
Rev. 0, 8/2015

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