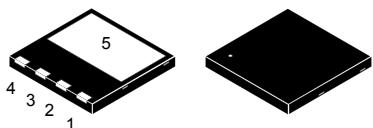
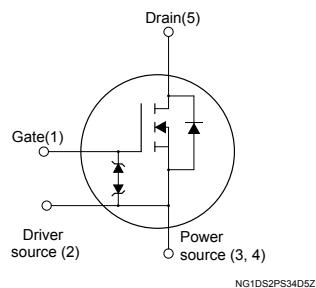


## N-channel 600 V, 175 mΩ typ., 15 A, MDmesh™ DM6 Power MOSFET in a PowerFLAT™ 8x8 HV package

### Features



**PowerFLAT™ 8x8 HV**



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STL26N60DM6	600 V	215 mΩ	15 A

- Fast-recovery body diode
- Lower R<sub>DS(on)</sub> per area vs previous generation
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

### Applications

- Switching applications

### Description

This high-voltage N-channel Power MOSFET is part of the MDmesh™ DM6 fast-recovery diode series. Compared with the previous MDmesh fast generation, DM6 combines very low recovery charge (Q<sub>rr</sub>), recovery time (t<sub>rr</sub>) and excellent improvement in R<sub>DS(on)</sub> per area with one of the most effective switching behaviors available in the market for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

#### Product status link

[STL26N60DM6](#)

#### Product summary

Order code	STL26N60DM6
Marking	26N60DM6
Package	PowerFLAT™ 8x8 HV
Packing	Tape and reel

## 1 Electrical ratings

**Table 1.** Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	15	A
	Drain current (continuous) at $T_C = 100^\circ\text{C}$	9.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	60	A
$P_{TOT}$	Total power dissipation at $T_C = 25^\circ\text{C}$	110	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	50	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	100	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 15 \text{ A}$ ,  $di/dt \leq 900 \text{ A}/\mu\text{s}$ ,  $V_{DS(\text{peak})} < V_{(BR)DSS}$ ,  $V_{DD} = 400 \text{ V}$
3.  $V_{DS} \leq 480 \text{ V}$

**Table 2.** Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.14	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	45	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of  $\text{inch}^2$ , 2oz Cu.

**Table 3.** Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	4	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50 \text{ V}$ )	360	mJ

## 2 Electrical characteristics

$T_C = 25^\circ\text{C}$  unless otherwise specified

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	600			V
$I_{\text{DSS}}$	Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V}$ $V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V},$ $T_C = 125^\circ\text{C}$ <sup>(1)</sup>			5	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$			$\pm 5$	$\mu\text{A}$
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	3.25	4	4.75	V
$R_{DS(\text{on})}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}, I_D = 7.5 \text{ A}$		175	215	$\text{m}\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance		-	940	-	pF
$C_{oss}$	Output capacitance	$V_{DS} = 100 \text{ V}, f = 1 \text{ MHz},$ $V_{GS} = 0 \text{ V}$	-	75	-	pF
$C_{rss}$	Reverse transfer capacitance		-	4	-	pF
$C_{oss \text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0 \text{ to } 480 \text{ V}, V_{GS} = 0 \text{ V}$	-	157	-	pF
$R_G$	Intrinsic gate resistance	$f = 1 \text{ MHz}, I_D = 0 \text{ A}$	-	4.8	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480 \text{ V}, I_D = 18 \text{ A},$ $V_{GS} = 0 \text{ to } 10 \text{ V}$	-	24	-	nC
$Q_{gs}$	Gate-source charge		-	6	-	nC
$Q_{gd}$	Gate-drain charge	(see Figure 14. Test circuit for gate charge behavior)	-	11.5	-	nC

1.  $C_{oss \text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300 \text{ V}, I_D = 9 \text{ A},$	-	13	-	ns
$t_r$	Rise time	$R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$	-	11	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Switching times test circuit for resistive load and Figure 18. Switching time waveform)	-	39	-	ns
$t_f$	Fall time		-	8	-	ns

**Table 7. Source drain diode**

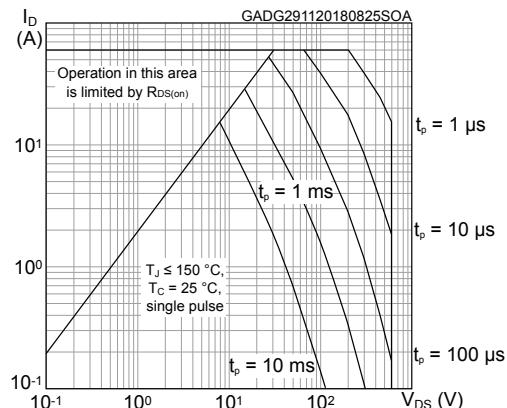
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		15	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		60	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0 \text{ V}$ , $I_{SD} = 15 \text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 18 \text{ A}$ , $dI/dt = 100 \text{ A}/\mu\text{s}$ ,	-	100		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60 \text{ V}$ (see <a href="#">Figure 15. Test circuit for inductive load switching and diode recovery times</a> )	-	0.35		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	$I_{SD} = 18 \text{ A}$ , $dI/dt = 100 \text{ A}/\mu\text{s}$ , (see <a href="#">Figure 15. Test circuit for inductive load switching and diode recovery times</a> )	-	7		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 18 \text{ A}$ , $dI/dt = 100 \text{ A}/\mu\text{s}$ ,	-	170		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 15. Test circuit for inductive load switching and diode recovery times</a> )	-	1.02		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	$I_{SD} = 18 \text{ A}$ , $dI/dt = 100 \text{ A}/\mu\text{s}$ , (see <a href="#">Figure 15. Test circuit for inductive load switching and diode recovery times</a> )	-	12		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

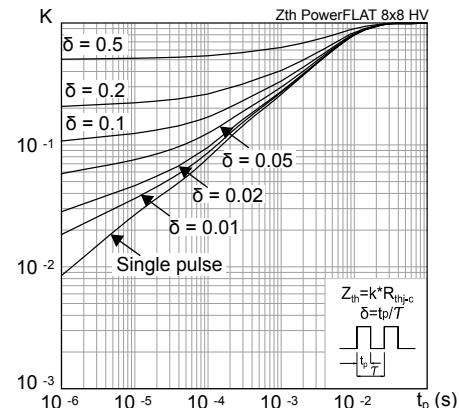
## 2.1

### Electrical characteristics (curves)

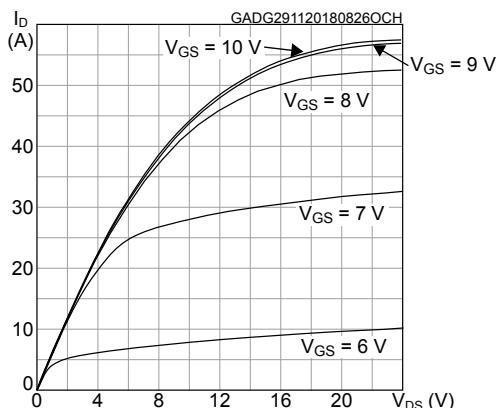
**Figure 1. Safe operating area**



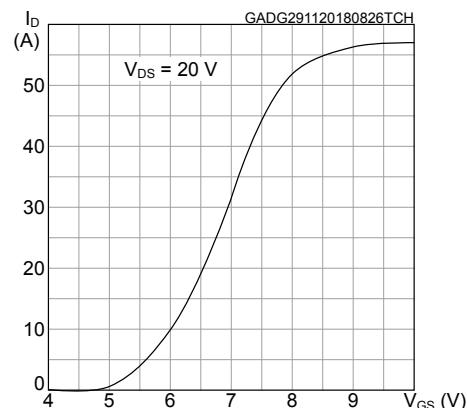
**Figure 2. Normalized thermal impedance**



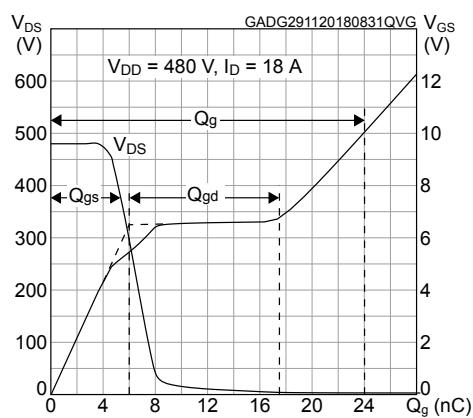
**Figure 3. Output characteristics**



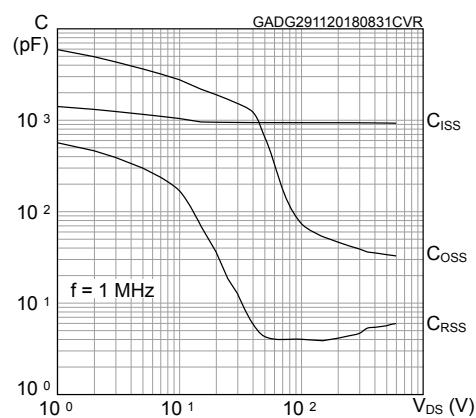
**Figure 4. Transfer characteristics**

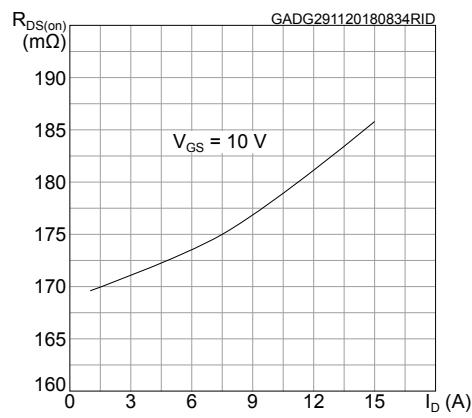
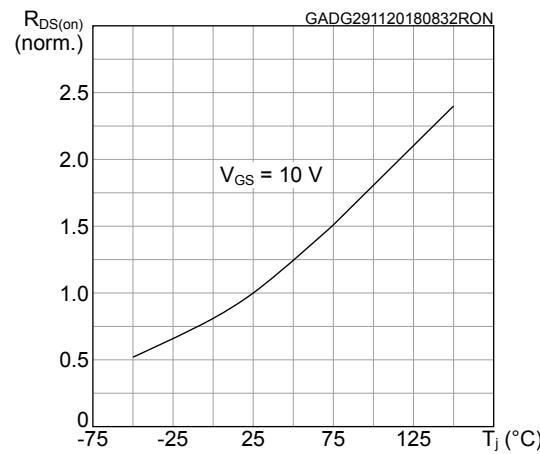
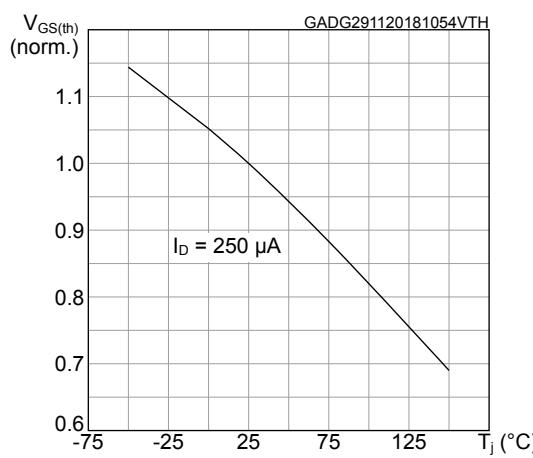
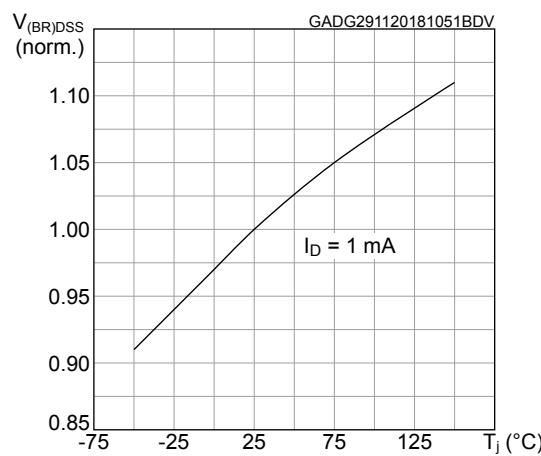
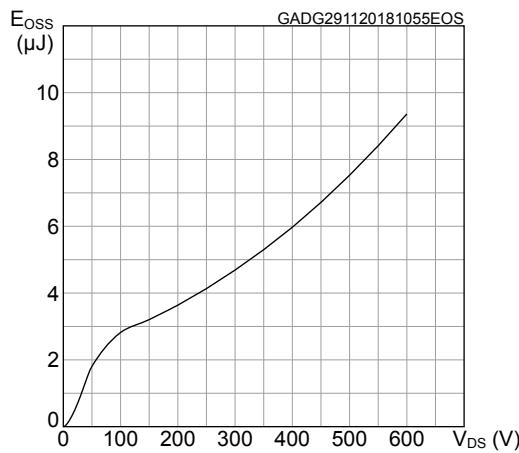
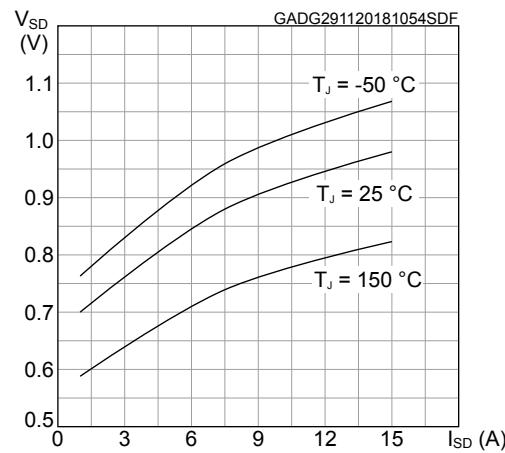


**Figure 5. Gate charge vs gate-source voltage**



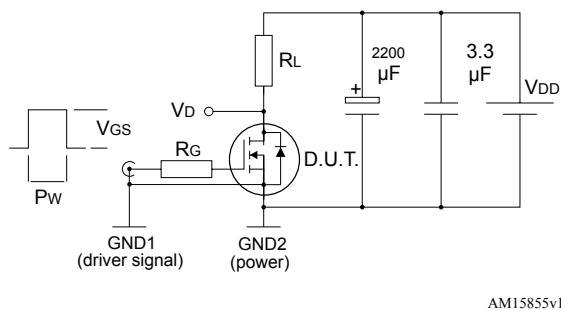
**Figure 6. Capacitance variations**



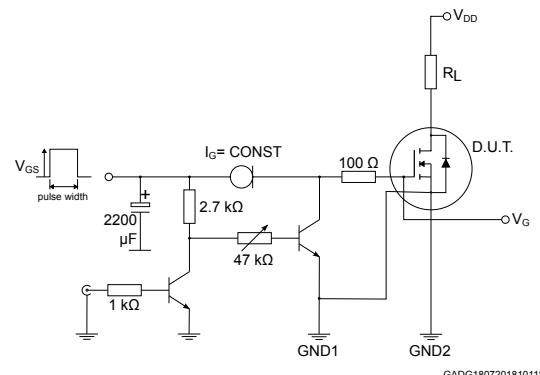
**Figure 7. Static drain-source on-resistance**

**Figure 8. Normalized on-resistance vs temperature**

**Figure 9. Normalized gate threshold voltage vs temperature**

**Figure 10. Normalized  $V_{(BR)DSS}$  vs temperature**

**Figure 11. Output capacitance stored energy**

**Figure 12. Source-drain diode forward characteristics**


### 3 Test circuits

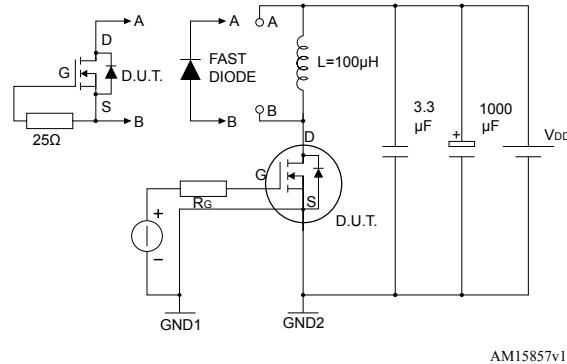
**Figure 13.** Switching times test circuit for resistive load



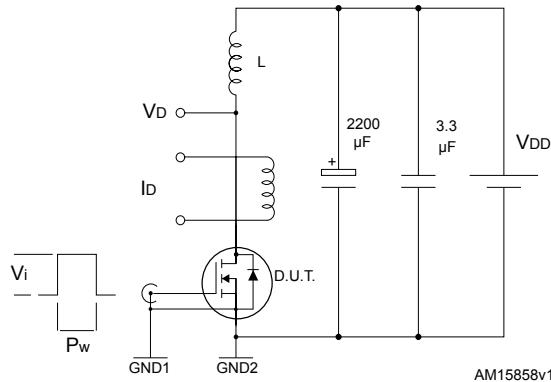
**Figure 14.** Test circuit for gate charge behavior



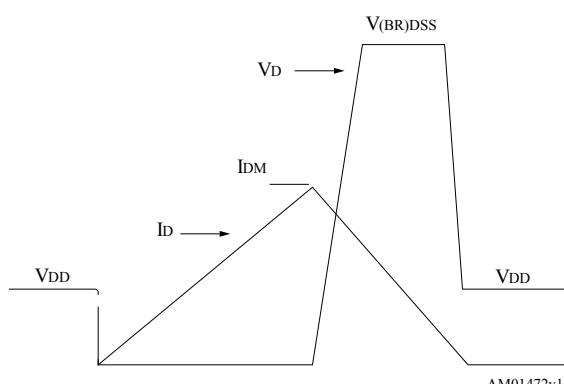
**Figure 15.** Test circuit for inductive load switching and diode recovery times



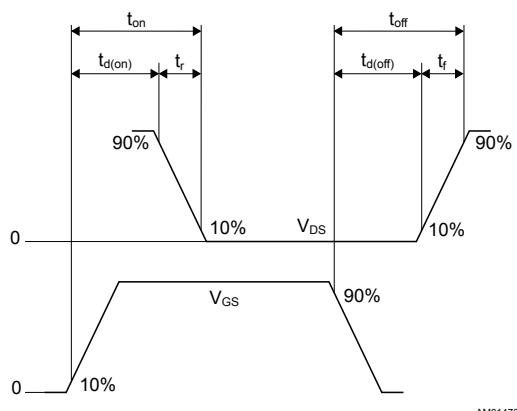
**Figure 16.** Unclamped inductive load test circuit



**Figure 17.** Unclamped inductive waveform



**Figure 18.** Switching time waveform



**4**

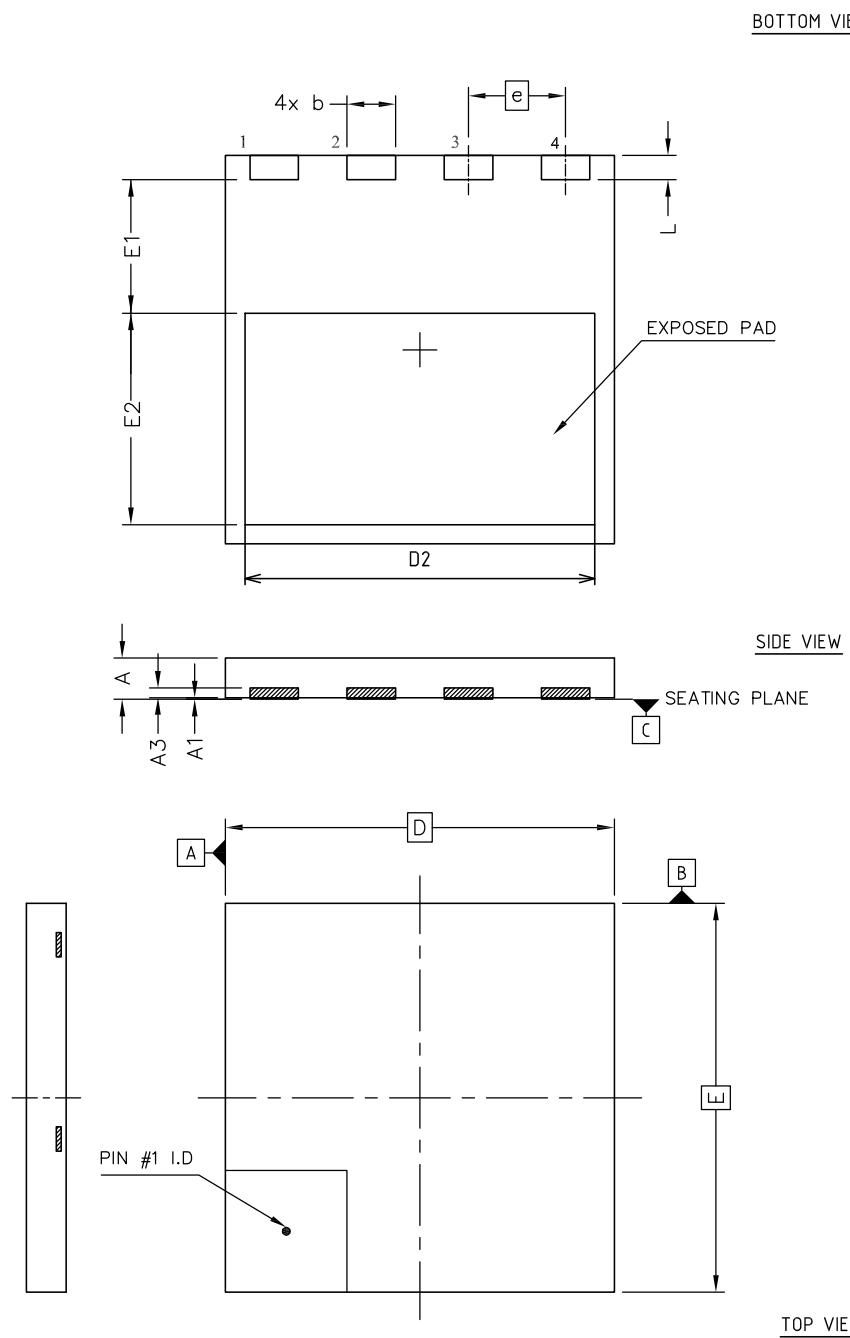
## Package information

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In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

## 4.1 PowerFLAT™ 8x8 HV package information

Figure 19. PowerFLAT™ 8x8 HV package outline

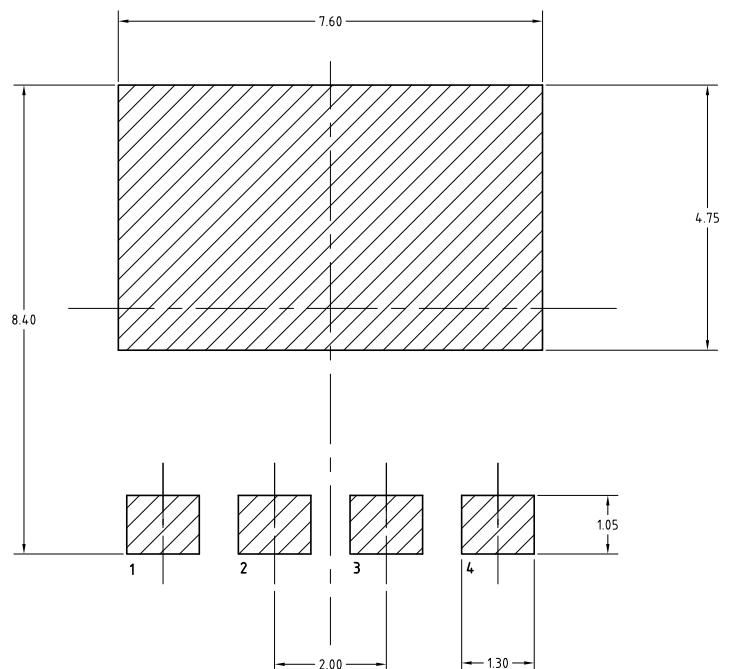


8222871\_Rev\_4

Table 8. PowerFLAT™ 8x8 HV mechanical data

Ref.	Dimensions (in mm)		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e		2.00 BSC	
L	0.40	0.50	0.60

Figure 20. PowerFLAT™ 8x8 HV footprint

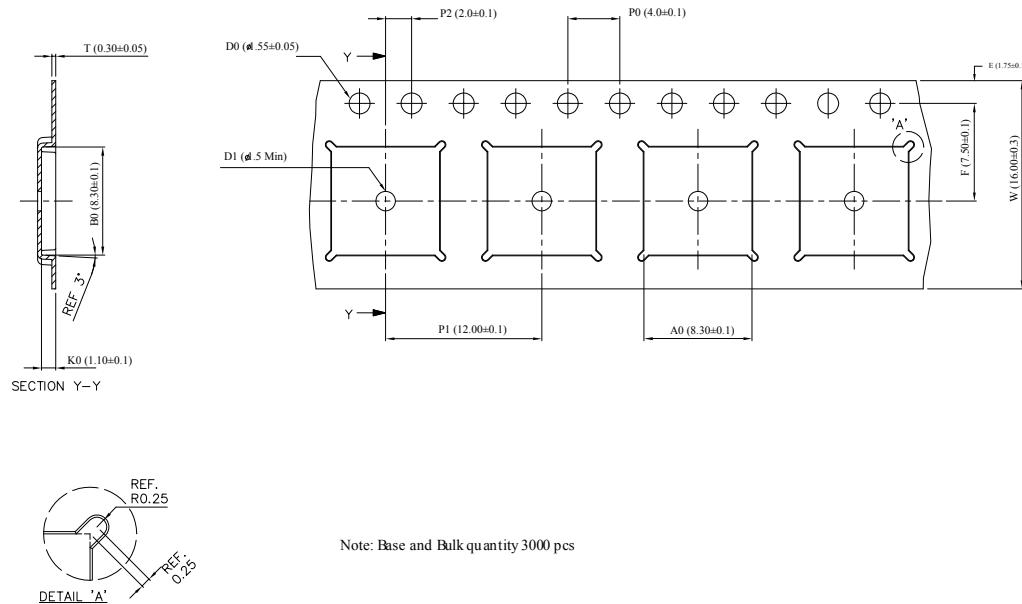


8222871\_REV\_4\_footprint

Note: All dimensions are in millimeters.

## 4.2 PowerFLAT™ 8x8 HV packing information

Figure 21. PowerFLAT™ 8x8 HV tape



8229819\_Tape\_revA

Note: All dimensions are in millimeters.

Figure 22. PowerFLAT™ 8x8 HV package orientation in carrier tape

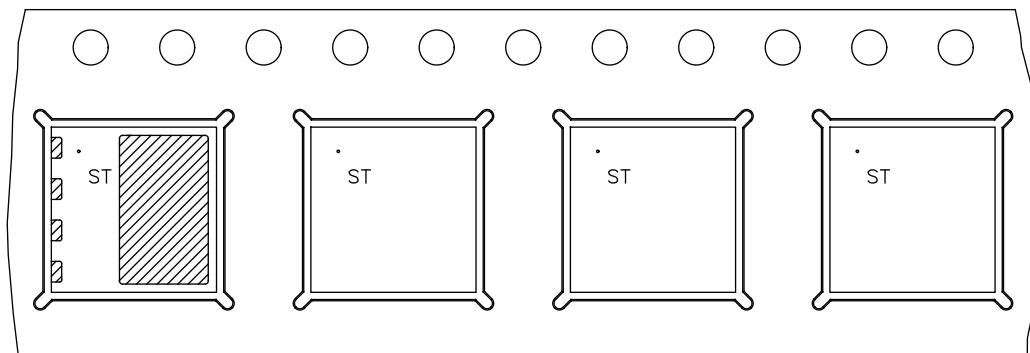
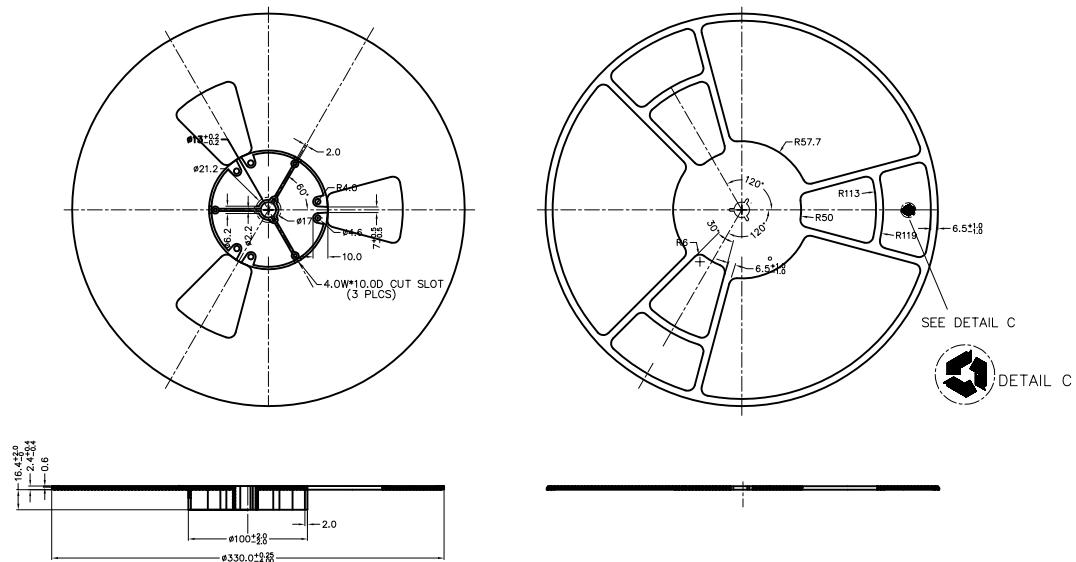


Figure 23. PowerFLAT™ 8x8 HV reel



8229819\_Reel\_revA

Note: All dimensions are in millimeters.

## Revision history

**Table 9. Document revision history**

Date	Version	Changes
29-Nov-2018	1	First release.
21-Jan-2019	2	Updated <a href="#">Table 4. On/off states</a> and <a href="#">Figure 7. Static drain-source on-resistance</a> .

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