

NTHS4166N

Power MOSFET

30 V, 8.2 A, Single N-Channel, ChipFET™ Package

Features

- Trench Technology
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Leadless ChipFET Package has 40% Smaller Footprint than TSOP-6
- Excellent Thermal Capabilities
- This is a Pb-Free Device

Applications

- Load Switching
- DC-DC Converters
- Low Side Switching

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	30	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JA}$ (Note 1)	I_D	$T_A = 25^\circ\text{C}$	6.6	A
		$T_A = 85^\circ\text{C}$	4.8	
Power Dissipation $R_{\theta JA}$ (Note 1)	P_D	$T_A = 25^\circ\text{C}$	1.5	W
		$T_A = 85^\circ\text{C}$		
Continuous Drain Current $R_{\theta JA}$ (Note 2)	I_D	$T_A = 25^\circ\text{C}$	4.9	A
		$T_A = 85^\circ\text{C}$	3.6	
Power Dissipation $R_{\theta JA}$ (Note 2)	P_D	$T_A = 25^\circ\text{C}$	0.8	W
Continuous Drain Current $R_{\theta JA}$, $t \leq 5$ s (Note 1)	I_D	$T_A = 25^\circ\text{C}$	8.2	A
		$T_A = 85^\circ\text{C}$	5.9	
Power Dissipation $R_{\theta JA}$ (Note 1)	P_D	$T_A = 25^\circ\text{C}$	2.2	W
Pulsed Drain Current	I_{DM}	32	A	
Operating Junction and Storage Temperature	T_J, T_{STG}		-55 to 150	$^\circ\text{C}$
Source Current (Body Diode) $R_{\theta JF}$	I_S	2.6	A	
Single Pulse Drain-to-Source Avalanche Energy $T_J = 25^\circ\text{C}$, $V_{DD} = 50$ V, $V_{GS} = 10$ V, $I_L = 20$ A _{pk} , $L = 0.1$ mH, $R_G = 25$ Ω	EAS	20	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

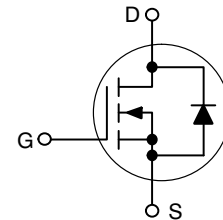
1. Surface Mounted on FR4 Board using 1 in sq. pad, 1 oz Cu.
2. Surface Mounted on FR4 Board using the minimum recommended pad size.



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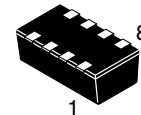
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ Max	I_D Max
30 V	22 m Ω @ 10 V	8.2 A
	27 m Ω @ 4.5 V	

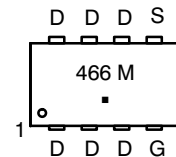


N-Channel MOSFET

MARKING DIAGRAM AND PIN ASSIGNMENT



ChipFET
CASE 1206A
STYLE 1



- 466 = Specific Device Code
- M = Month Code
- = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTHS4166NT1G	ChipFET (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	86	°C/W
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	57	
Junction-to-Ambient – $t \leq 5$ s (Note 4)	$R_{\theta JA}$	155	
Junction-to-Foot (Drain) Steady State (Note 3)	$R_{\theta JF}$	20	

3. Surface Mounted on FR4 Board using 1 in sq. pad, 1 oz Cu.
4. Surface Mounted on FR4 Board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			18.3		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 30\text{ V}$			1.0	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.1		2.3	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.5		mV/°C
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 4.9\text{ A}$		18	22	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 4.9\text{ A}$		9.0		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 15\text{ V}$		900		pF
Output Capacitance	C_{OSS}			210		
Reverse Transfer Capacitance	C_{RSS}			140		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 4.9\text{ A}$		9.2		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.85		
Gate-to-Source Charge	Q_{GS}			2.86		
Gate-to-Drain Charge	Q_{GD}			3.84		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 4.9\text{ A}$		18		nC
Gate Resistance	R_G			1.6		

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 4.9\text{ A}, R_G = 3.0\ \Omega$		12		ns
Rise Time	t_r			13		
Turn-Off Delay Time	$t_{d(off)}$			16		
Fall Time	t_f			5.0		
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 4.9\text{ A}, R_G = 3.0\ \Omega$		8.0		ns
Rise Time	t_r			11		
Turn-Off Delay Time	$t_{d(off)}$			20		
Fall Time	t_f			4.0		

5. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.
6. Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 5.2 A	T _J = 25°C	0.83	1.0	V
			T _J = 125°C	0.7		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, I _S = 5.2 A, dI _S /dt = 100 A/μs		16		ns
Charge Time	t _a			7.5		
Discharge Time	t _b			8.5		
Reverse Recovery Charge	Q _{RR}			6.0		

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

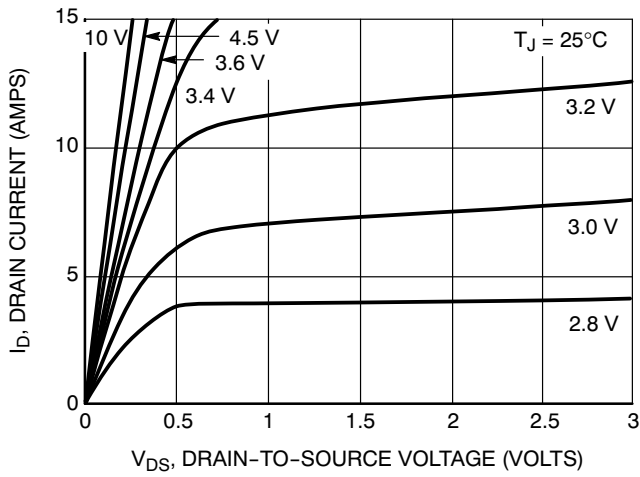


Figure 1. On-Region Characteristics

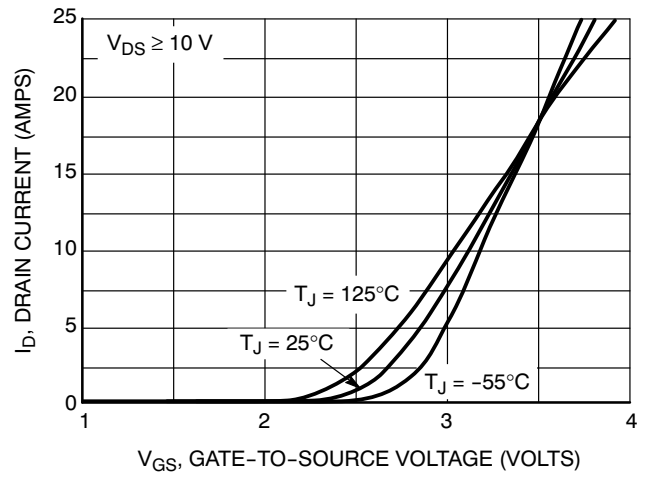


Figure 2. Transfer Characteristics

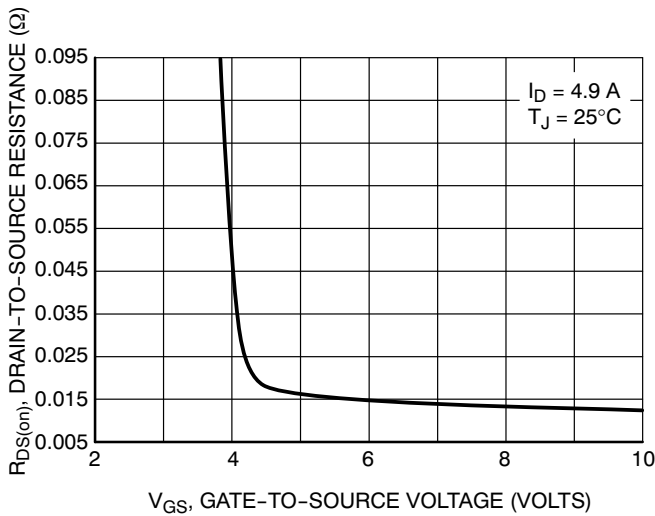


Figure 3. On-Resistance vs. Gate-to-Source Voltage

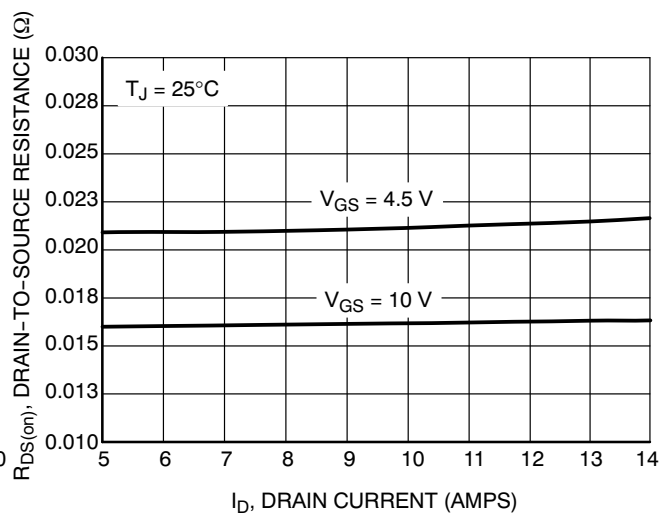


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

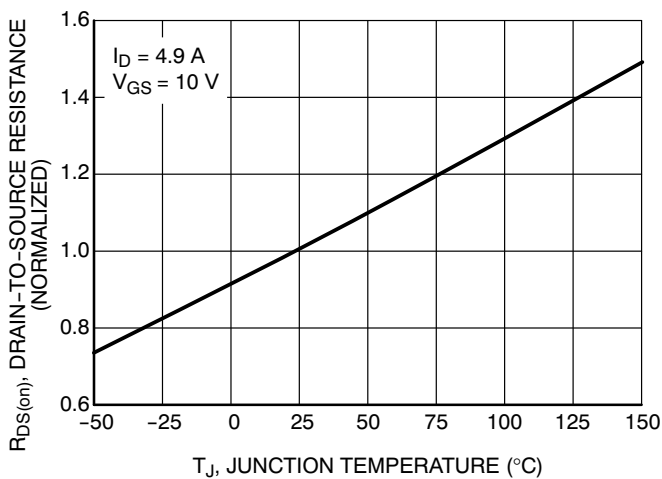


Figure 5. On-Resistance Variation with Temperature

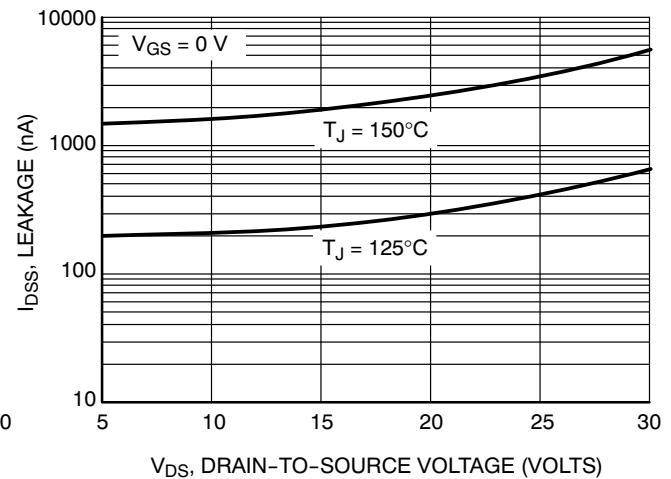


Figure 6. Drain-to-Source Leakage Current vs. Drain Voltage

TYPICAL PERFORMANCE CURVES

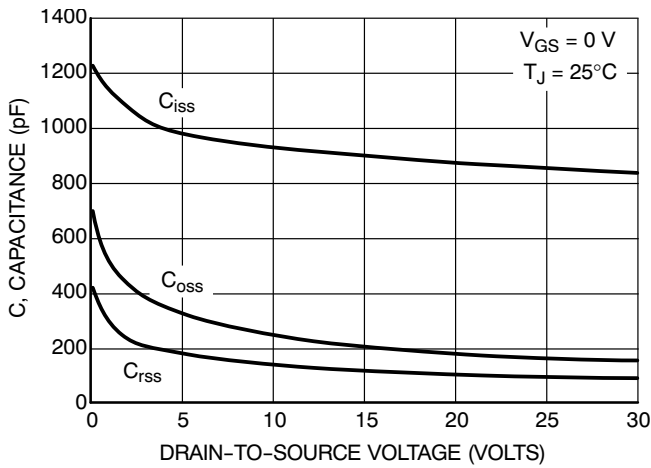


Figure 7. Capacitance Variation

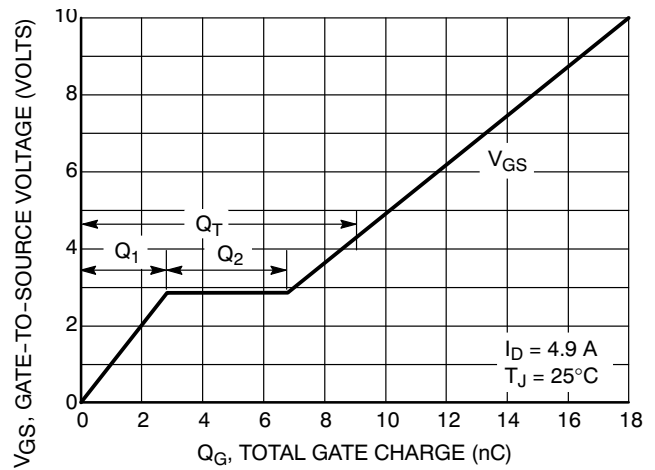


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

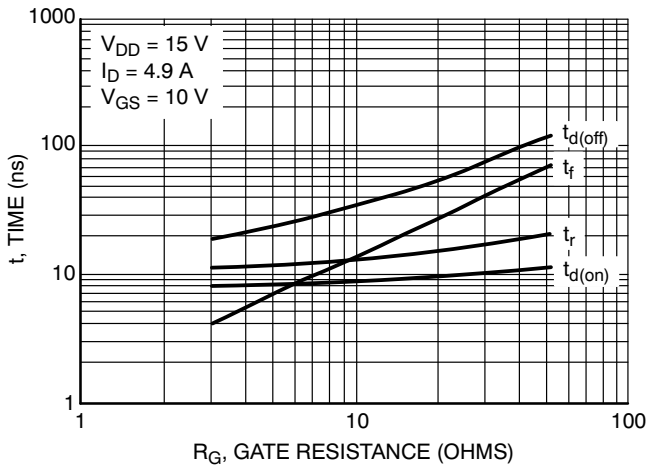


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

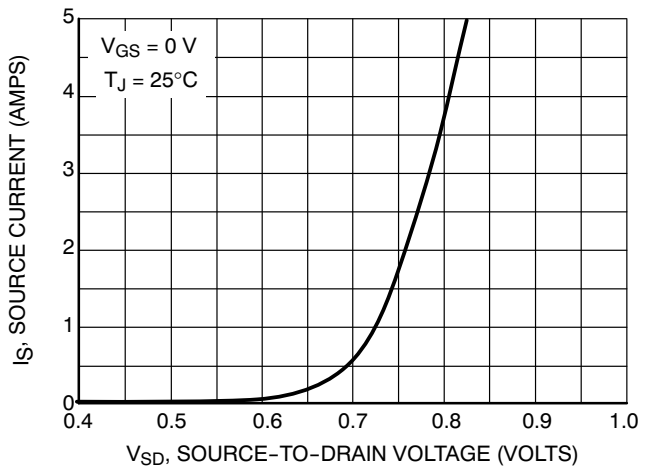


Figure 10. Diode Forward Voltage vs. Current

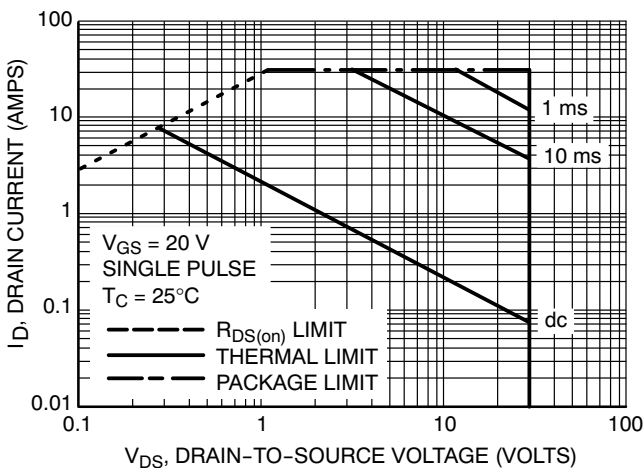


Figure 11. Maximum Rated Forward Biased Safe Operating Area

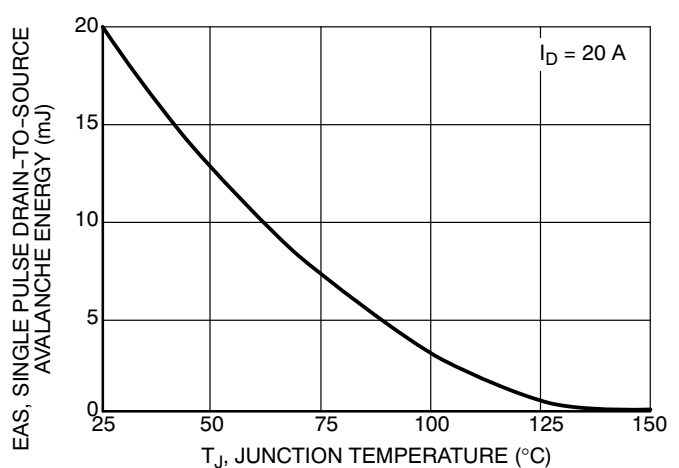
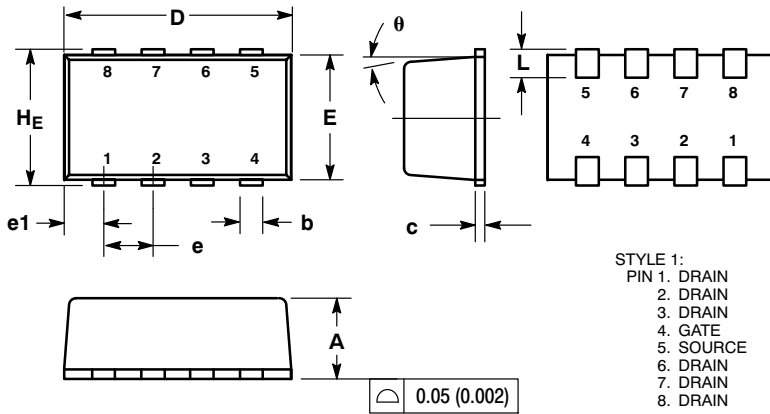


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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PACKAGE DIMENSIONS

ChipFET™ CASE 1206A-03 ISSUE H

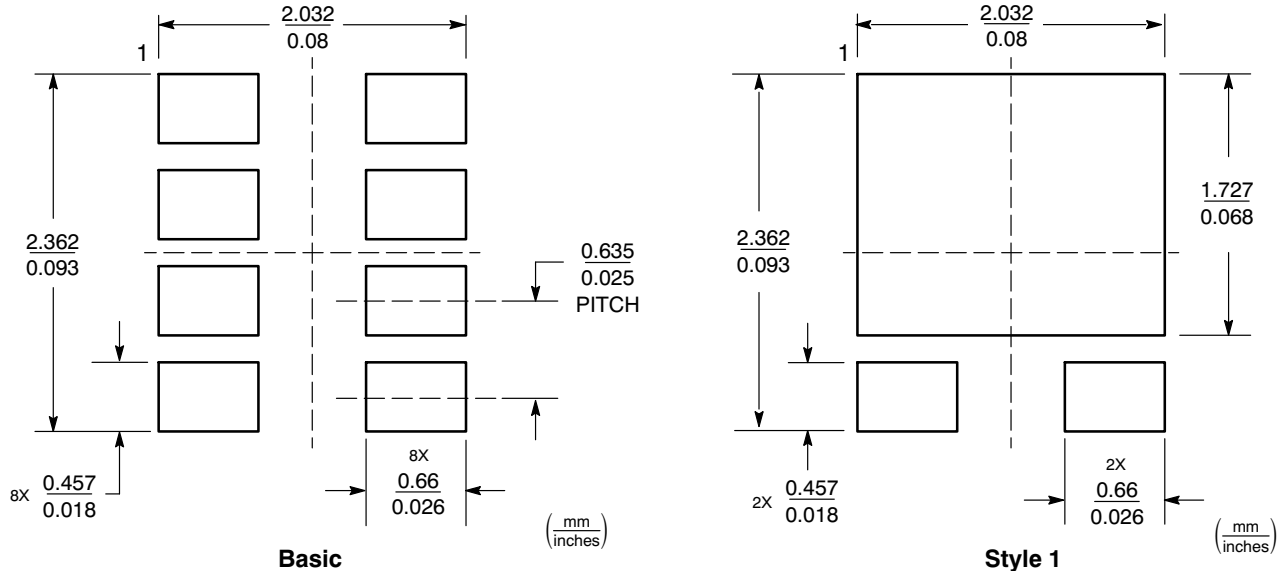


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
HE	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM			5° NOM		

SOLDERING FOOTPRINTS*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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