Dual 16-Bit SoftSpan I_{OUT} DACs

FEATURES

- **Program or Pin-Strap Six Output Ranges 0V to 5V, 0V to 10V, –2.5V to 7.5V, ±2.5V, ±5V, ±10V**
- **Maximum 16-Bit INL Error: ±1 LSB over Temperature**
- **Guaranteed Monotonic over Temperature**
- **Glitch Impulse 0.6nV•s (3V), 2.2nV•s (5V)**
- **Serial Readback of All On-Chip Registers**
- 1µA Maximum Supply Current
- 2.7V to 5.5V Single-Supply Operation
- 16-Bit Settling Time: 2µs
- Voltage-Controlled Offset and Gain Trims
- Clear and Power-On-Reset to 0V Regardless of Output Range
- 48-Pin 7mm × 7mm LQFP Package

APPLICATIONS

- High Resolution Offset and Gain Adjustment
- Process Control and Industrial Automation
- Automatic Test Equipment
- Data Acquisition Systems

DESCRIPTION

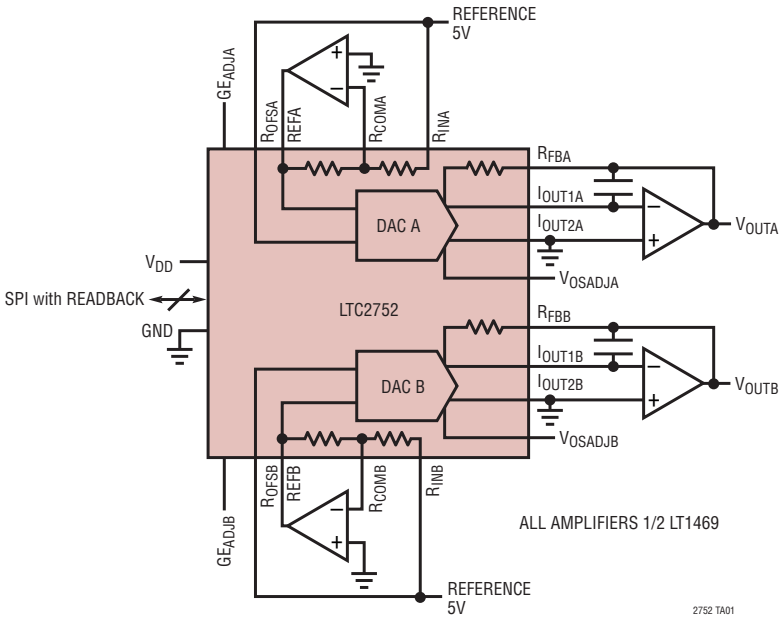
The LTC®2752 is a dual 16-bit multiplying serial-input, current-output digital-to-analog converter. It operates from a single 3V to 5V supply and is guaranteed monotonic over temperature. The LTC2752A provides full 16-bit performance (±1LSB INL and DNL, max) over temperature without any adjustments. This SoftSpan™ DAC offers six output ranges (up to ±10V) that can be programmed through the 3-wire SPI serial interface, or pinstrapped for operation in a single range.

Any on-chip register (including DAC output-range settings) can be read for verification in just one instruction cycle; and if you change register content, the altered register will be automatically read back during the next instruction cycle.

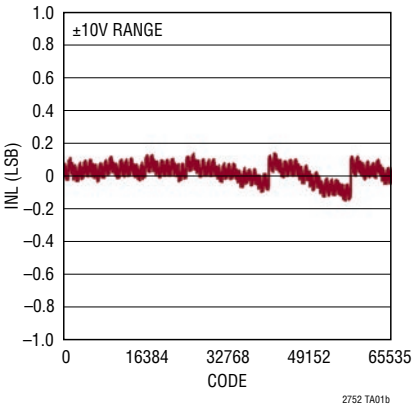
Voltage-controlled offset and gain adjustments are also provided; and the power-on reset circuit and $\overline{CLR}$ pin both reset the DAC outputs to 0V regardless of output range.

TYPICAL APPLICATION

Dual 16-Bit V_{OUT} DAC with Software-Selectable Ranges



Integral Nonlinearity (INL)

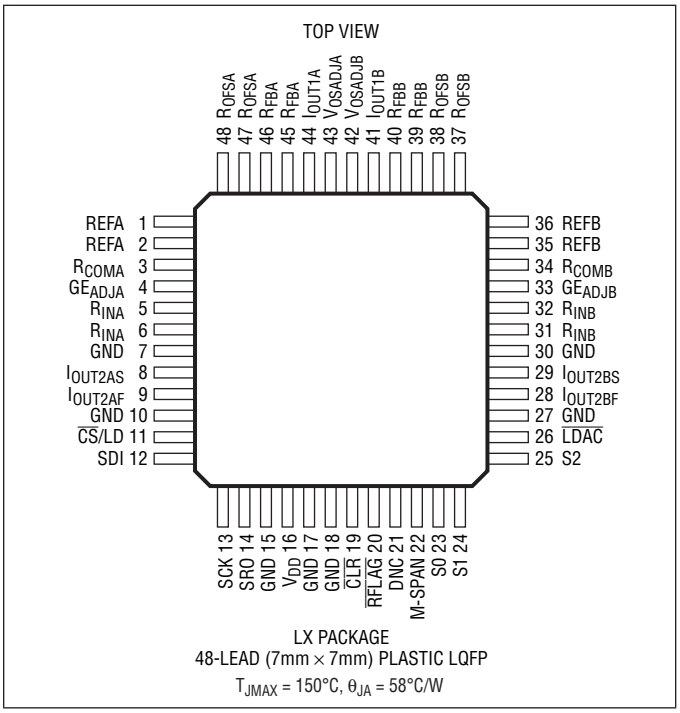


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

I_{OUT1X}, I_{OUT2X} to GND ..... ±0.3V
R_{INX}, R_{COMX}, REFX, R_{FBX}, R_{OFSX}, V_{OSADJX}, GE_{ADJX} to GND ..... ±18V
V_{DD} to GND ..... –0.3V to 7V
Digital Inputs to GND ..... –0.3V to 7V
Digital Outputs to GND ..... –0.3V to V_{DD}+0.3V (max 7V)
Operating Temperature Range
  LTC2752C ..... 0°C to 70°C
  LTC2752I ..... –40°C to 85°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PIN CONFIGURATION



LX PACKAGE
48-LEAD (7mm × 7mm) PLASTIC LQFP
T_{JMAX} = 150°C, θ_{JA} = 58°C/W

ORDER INFORMATION

LEAD FREE FINISH	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2752BCLX#PBF	LTC2752LX	48-Lead (7mm × 7mm) Plastic LQFP	0°C to 70°C
LTC2752BILX#PBF	LTC2752LX	48-Lead (7mm × 7mm) Plastic LQFP	–40°C to 85°C
LTC2752ACLX#PBF	LTC2752LX	48-Lead (7mm × 7mm) Plastic LQFP	0°C to 70°C
LTC2752AILX#PBF	LTC2752LX	48-Lead (7mm × 7mm) Plastic LQFP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, V_{RINX} = 5V unless otherwise specified. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		LTC2752B MIN	LTC2752B TYP	LTC2752B MAX	LTC2752A MIN	LTC2752A TYP	LTC2752A MAX	UNITS
Static Performance										
	Resolution		●	16			16			Bits
	Monotonicity		●	16			16			Bits
DNL	Differential Nonlinearity		●			±1		±0.2	±1	LSB
INL	Integral Nonlinearity		●			±2		±0.4	±1	LSB
GE	Gain Error	All Output Ranges	●			±20		±2	±12	LSB
	Gain Error Temperature Coefficient	ΔGain/ΔTemp			±0.25			±0.25		ppm/°C
BZE	Bipolar Zero Error	All Bipolar Ranges	●			±12		±1	±8	LSB
	Bipolar Zero Temperature Coefficient				±0.15			±0.15		ppm/°C
	Unipolar Zero-Scale Error	Unipolar Ranges (Note 3)	●		±0.01	±1		±0.01	±1	LSB
PSR	Power Supply Rejection	V_{DD} = 5V, ±10% V_{DD} = 3V, ±10%	● ●			±0.4 ±1		±0.03 ±0.1	±0.2 ±0.5	LSB/V LSB/V
I_{LKG}	I_{OUT1} Leakage Current	T_A = 25°C T_{MIN} to T_{MAX}	 ●		±0.05	±2 ±5		±0.05	±2 ±5	nA nA

V_{DD} = 5V, V_{RINX} = 5V unless otherwise specified. The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Pins							
	Reference Inverting Resistors	(Note 4)	●	16	20		kΩ
R_{REF}	DAC Input Resistance	(Notes 5, 6)	●	8	10		kΩ
R_{FB}	Feedback Resistors	(Note 6)	●	8	10		kΩ
R_{OFS}	Bipolar Offset Resistors	(Note 6)	●	16	20		kΩ
R_{VOSADJ}	Offset Adjust Resistors		●	1024	1280		kΩ
R_{GEADJ}	Gain Adjust Resistors		●	2048	2560		kΩ
C_{IOUT1}	Output Capacitance	Full-Scale Zero-Scale			90 40		pF
Dynamic Performance							
	Output Settling Time	Span Code = 0000, 10V Step. To ±0.0015% FS (Note 7)			2		µs
	Glitch Impulse	V_{DD} = 5V (Note 8) V_{DD} = 3V (Note 8)			2.2 0.6		nV•s nV•s
	Digital-to-Analog Glitch Impulse	(Note 9)			2		nV•s
	Reference Multiplying BW	0V to 5V Range, V_{REF} = $3V_{RMS}$, Code = Full Scale, –3dB BW			1		MHz
	Multiplying Feedthrough Error	0V to 5V Range, V_{REF} = ±10V, 10kHz Sine Wave			0.4		mV
	Analog Crosstalk	(Note 10)			–109		dB
THD	Total Harmonic Distortion	(Note 11) Multiplying			–108		dB
	Output Noise Voltage Density	(Note 12) at I_{OUT1}			13		nV/√Hz

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, V_{RINX} = 5V unless otherwise specified. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{DD}	Supply Voltage		●	2.7		5.5	V
I_{DD}	V_{DD} Supply Current	Digital Inputs = 0V or V_{DD}	●		0.5	1	µA
Digital Inputs							
V_{IH}	Digital Input High Voltage	3.3V ≤ V_{DD} ≤ 5.5V 2.7V ≤ V_{DD} < 3.3V	● ●	2.4 2			V V
V_{IL}	Digital Input Low Voltage	4.5V < V_{DD} ≤ 5.5V 2.7V ≤ V_{DD} ≤ 4.5V	● ●			0.8 0.6	V V
	Hysteresis Voltage				0.1		V
I_{IN}	Digital Input Current	V_{IN} = GND to V_{DD}	●			±1	µA
C_{IN}	Digital Input Capacitance	V_{IN} = 0V (Note 13)	●			6	pF
Digital Outputs							
V_{OH}	Digital Output High Voltage	I_{OH} = 200µA, 2.7V ≤ V_{DD} ≤ 5.5V	●	V_{DD} – 0.4			V
V_{OL}	Digital Output Low Voltage	I_{OL} = 200µA, 2.7V ≤ V_{DD} ≤ 5.5V	●			0.4	V

TIMING CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} = 4.5V to 5.5V							
t_1	SDI Valid to SCK Set-Up		●	7			ns
t_2	SDI Valid to SCK Hold		●	7			ns
t_3	SCK High Time		●	11			ns
t_4	SCK Low Time		●	11			ns
t_5	$\overline{CS}$/LD Pulse Width		●	9			ns
t_6	LSB SCK High to $\overline{CS}$/LD High		●	4			ns
t_7	$\overline{CS}$/LD Low to SCK Positive Edge		●	4			ns
t_8	$\overline{CS}$/LD High to SCK Positive Edge		●	4			ns
t_9	SRO Propagation Delay	C_{LOAD} = 10pF	●			18	ns
t_{10}	$\overline{CLR}$ Pulse Width Low		●	36			ns
t_{11}	$\overline{LDAC}$ Pulse Width Low		●	15			ns
t_{12}	$\overline{CLR}$ Low to $\overline{RFLAG}$ Low	C_{LOAD} = 10pF (Note 13)	●			50	ns
t_{13}	$\overline{CS}$/LD High to $\overline{RFLAG}$ High	C_{LOAD} = 10pF (Note 13)	●			40	ns
	SCK Frequency	50% Duty Cycle (Note 14)	●			40	MHz
V_{DD} = 2.7V to 3.3V							
t_1	SDI Valid to SCK Set-Up		●	9			ns
t_2	SDI Valid to SCK Hold		●	9			ns
t_3	SCK High Time		●	15			ns
t_4	SCK Low Time		●	15			ns
t_5	$\overline{CS}$/LD Pulse Width		●	12			ns
t_6	LSB SCK High to $\overline{CS}$/LD High		●	5			ns
t_7	$\overline{CS}$/LD Low to SCK Positive Edge		●	5			ns

TIMING CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_8	$\overline{CS}$/LD High to SCK Positive Edge		●	5			ns
t_9	SRO Propagation Delay	C_{LOAD} = 10pF	●			26	ns
t_{10}	$\overline{CLR}$ Pulse Width Low		●	60			ns
t_{11}	$\overline{LDAC}$ Pulse Width Low		●	20			ns
t_{12}	$\overline{CLR}$ Low to $\overline{RFLAG}$ Low	C_{LOAD} = 10pF (Note 13)	●			70	ns
t_{13}	$\overline{CS}$/LD High to $\overline{RFLAG}$ high	C_{LOAD} = 10pF (Note 13)	●			60	ns
	SCK Frequency	50% Duty Cycle (Note 14)	●			25	MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: Calculation from feedback resistance and I_{OUT1} leakage current specifications; not production tested. In most applications, unipolar zero-scale error is dominated by contributions from the output amplifier.

Note 4: Input resistors measured from R_{INX} to R_{COMX}; feedback resistors measured from R_{COMX} to REFX.

Note 5: DAC input resistance is independent of code.

Note 6: Parallel combination of the resistances from the specified pin to I_{OUT1X} and from the specified pin to I_{OUT2X}.

Note 7: Using LT1468 with $C_{FEEDBACK}$ = 27pF. A ±0.0015% settling time of 1.7µs can be achieved by optimizing the time constant on an individual basis. See Application Note 74, Component and Measurement Advances Ensure 16-Bit DAC Settling Time.

Note 8: Measured at the major carry transition, 0V to 5V range. Output amplifier: LT1468; C_{FB} = 50pF.

Note 9. Full-scale transition; REF = 0V.

Note 10. Analog Crosstalk is defined as the AC voltage ratio V_{OUTB}/V_{REFA}, expressed in dB. REFB is grounded, and DAC B is set to 0V-5V span and zero-, mid- or full- scale code. V_{REFA} is a $3V_{RMS}$, 1kHz sine wave.

Note 11. REF = $6V_{RMS}$ at 1kHz. 0V to 5V range. DAC code = FS. Output amplifier = LT1469.

Note 12. Calculation from $V_n = \sqrt{4kTRB}$, where k = 1.38E-23 J/°K (Boltzmann constant), R = resistance (Ω), T = temperature (°K), and B = bandwidth (Hz). 0V to 5V Range; zero-, mid-, or full- scale.

Note 13. Guaranteed by design, not subject to test.

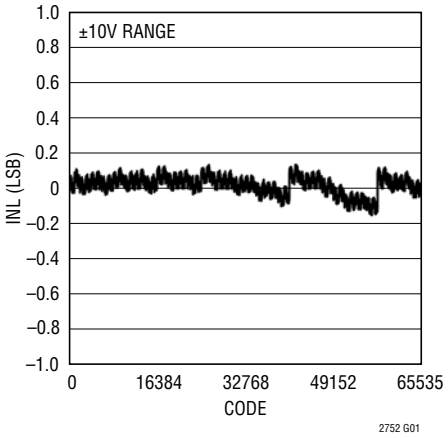
Note 14. When using SRO, maximum SCK frequency f_{MAX} is limited by SRO propagation delay t_9 as follows:

$$f_{MAX} = \left(\frac{1}{2(t_9 + t_S)}\right)$$, where t_S is the setup time of the receiving device.

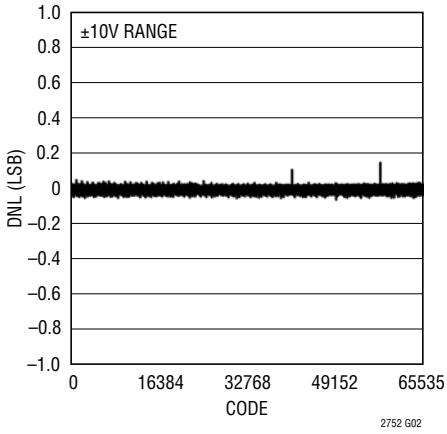
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 5V, V_{RINX} = 5V, T_A = 25°C, unless otherwise noted.

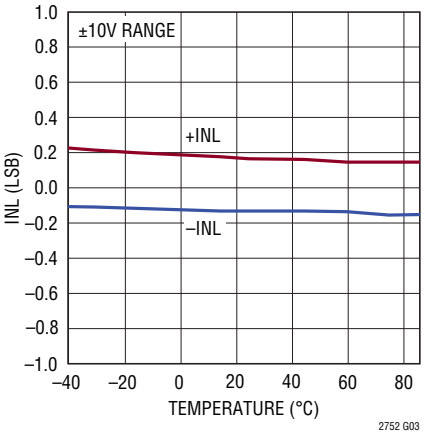
Integral Nonlinearity (INL)



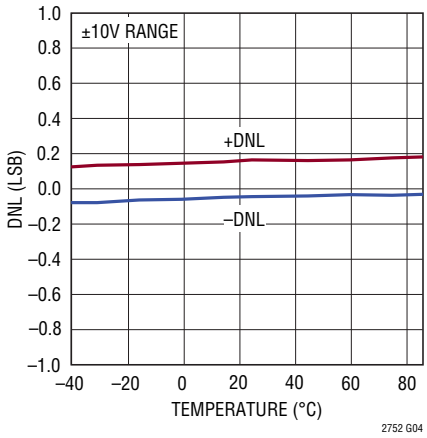
Differential Nonlinearity (DNL)



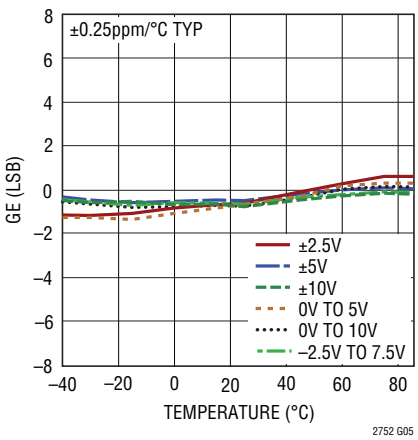
INL vs Temperature



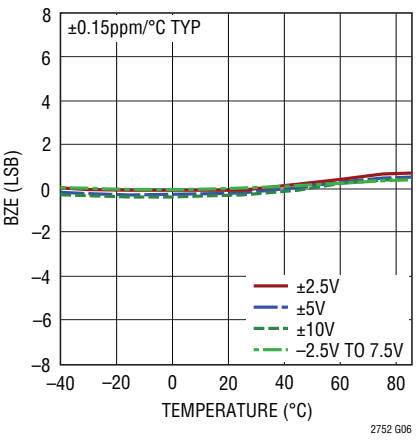
DNL vs Temperature



Gain Error vs Temperature



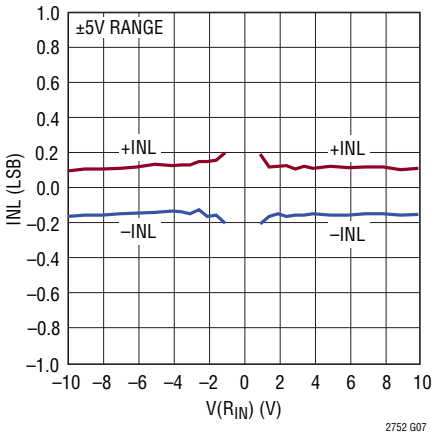
Bipolar Zero Error vs Temperature



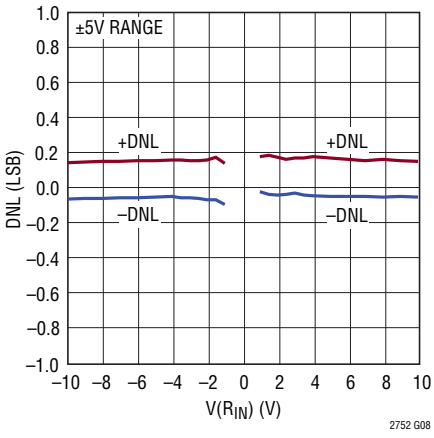
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 5V, V_{RINX} = 5V, T_A = 25°C, unless otherwise noted.

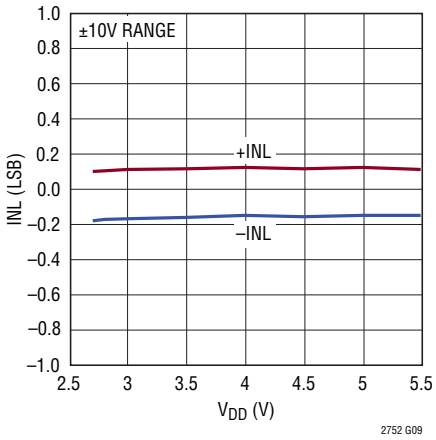
INL vs Reference Voltage



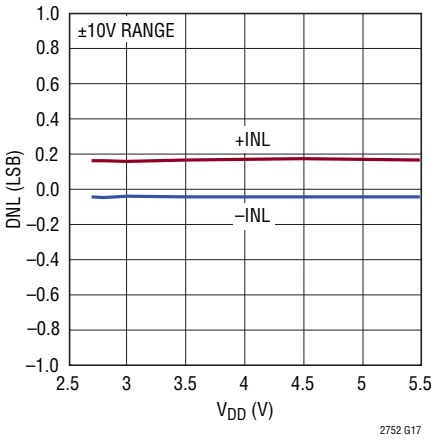
DNL vs Reference Voltage



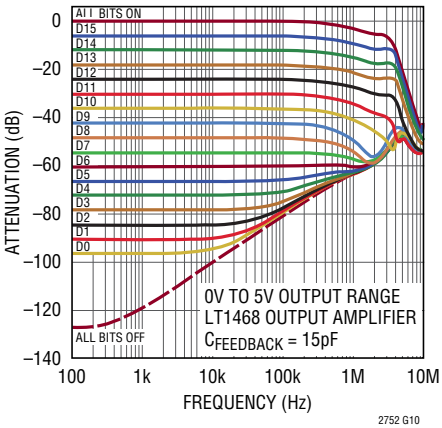
INL vs V_{DD}



DNL vs V_{DD}



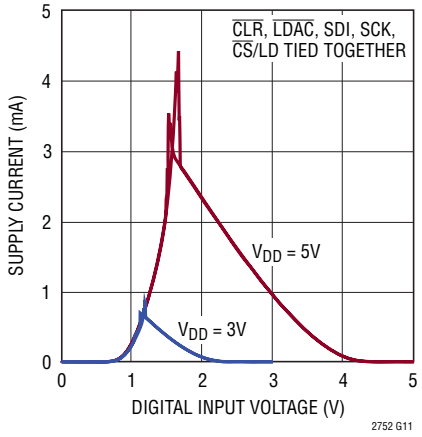
Multiplying Frequency Response vs Digital Code



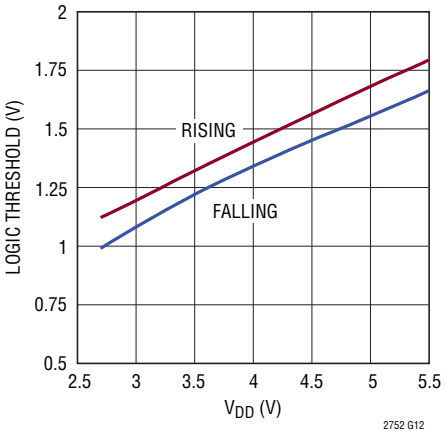
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 5V, V_{RINX} = 5V, T_A = 25°C, unless otherwise noted.

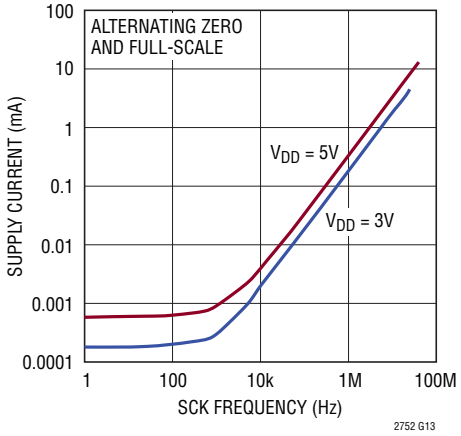
Supply Current vs Logic Input Voltage



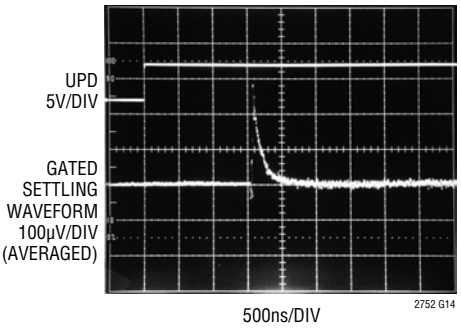
Logic Threshold vs Supply Voltage



Supply Current vs Clock Frequency

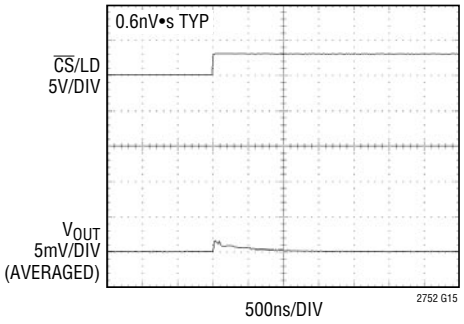


Settling Full-Scale Step



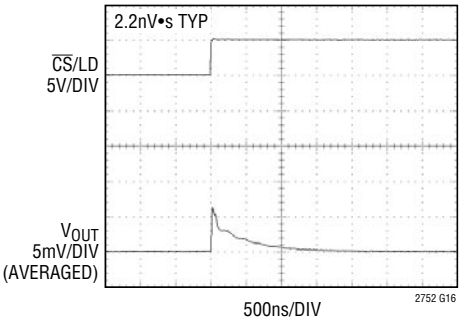
LT1468 AMP; $C_{FEEDBACK}$ = 20pF
0V TO 10V STEP
V_{REF} = –10V; SPAN CODE = 0000
t_{SETTLE} = 1.7µs to 0.0015% (16 BITS)

Midscale Glitch (V_{DD} = 3V)



0V TO 5V RANGE
LT1468 OUTPUT AMPLIFIER
$C_{FEEDBACK}$ = 50pF
FALLING MAJOR CARRY TRANSITION.
RISING TRANSITION IS SIMILAR OR BETTER.

Midscale Glitch (V_{DD} = 5V)



0V TO 5V RANGE
LT1468 OUTPUT AMPLIFIER
$C_{FEEDBACK}$ = 50pF
FALLING MAJOR CARRY TRANSITION.
RISING TRANSITION IS SIMILAR OR BETTER.

PIN FUNCTIONS

REFA (Pins 1, 2): Feedback Resistor for the DAC A Reference Inverting Amplifier, and Reference Input for DAC A. The 20k feedback resistor is connected internally from REFA to R_{COMA}. For normal operation tie this pin to the output of the DAC A reference inverting amplifier (see Typical Applications). Typically –5V; accepts up to ±15V. Pins 1 and 2 are internally shorted together.

R_{COMA} (Pin 3): Virtual Ground Point for the DAC A Reference Amplifier Inverting Resistors. The 20k reference inverting resistors are connected internally from R_{INA} to R_{COMA} and from R_{COMA} to REFA, respectively (see Block Diagram). For normal operation tie R_{COMA} to the negative input of the external reference inverting amplifier (see Typical Applications).

GE_{ADJA} (Pin 4): Gain Adjust Pin for DAC A. This control pin can be used to null gain error or to compensate for reference errors. The gain change expressed in LSB is the same for any output range. See System Offset and Gain Adjustments in the Operation section. Tie to ground if not used.

R_{INA} (Pins 5, 6): Input Resistor for External Reference Inverting Amplifier. The 20k input resistor is connected internally from R_{INA} to R_{COMA}. For normal operation tie R_{INA} to the external positive reference voltage (see Typical Applications). Either or both of these precision-matched resistor sets (each set comprising R_{INX}, R_{COMX} and R_{EFX}) may be used to invert positive references to provide the negative voltages needed by the DACs. Typically 5V; accepts up to ±15V. Pins 5 and 6 are internally shorted together.

GND (Pins 7, 10, 15, 17, 18, 27, 30): Ground; tie to ground.

I_{OUT2AS}, I_{OUT2AF} (Pins 8, 9): DAC A Current Output Complement Sense and Force Pins. Tie to ground via a clean, low-impedance path. These pins may be used with a precision ground buffer amp as a Kelvin sensing pair (see the Typical Applications section).

$\overline{CS}$/LD (Pin 11): Synchronous Chip Select and Load Input Pin.

SDI (Pin 12): Serial Data Input. Data is clocked in on the rising edge of the serial clock (SCK) when $\overline{CS}$/LD is low.

SCK (Pin 13): Serial Clock Input.

SRO (Pin 14): Serial Readback Output. Data is clocked out on the falling edge of SCK. Readback data begins clocking out after the last address bit A0 is clocked in. SRO is an active output only when the chip is selected (i.e., when $\overline{CS}$/LD is low). Otherwise SRO presents a high impedance output in order to allow other parts to control the bus.

V_{DD} (Pin 16): Positive Supply Input; $2.7V \le V_{DD} \le 5.5V$. Bypass with a 0.1µF low ESR ceramic capacitor to ground.

$\overline{CLR}$ (Pin 19): Asynchronous Clear Input. When this pin is low, all DAC registers (both code and span) are cleared to zero. All DAC outputs are cleared to zero volts.

$\overline{RFLAG}$ (Pin 20): Reset Flag Output. An active low output is asserted when there is a power-on reset or a clear event. Returns high when an Update command is executed.

DNC (Pin 21): Do not connect this pin.

M-SPAN (Pin 22): Manual Span Control Pin. M-SPAN is used in conjunction with pins S2, S1 and S0 (Pins 25, 24 and 23) to configure all DACs for operation in a single, fixed output range.

To configure the part for manual span use, tie M-SPAN directly to V_{DD}. The DAC output range is then set via hardware pin strapping of pins S2, S1 and S0 (rather than through the SPI port); and Write and Update commands have no effect on the active output span.

To configure the part for SoftSpan use, tie M-SPAN directly to GND. The output ranges are then individually controllable through the SPI port; and pins S2, S1 and S0 have no effect.

See Manual Span Configuration in the Operation section. M-SPAN must be connected either directly to GND (SoftSpan configuration) or to V_{DD} (manual span configuration).

S0 (Pin 23): Span Bit 0 Input. In Manual Span mode (M-SPAN tied to V_{DD}), pins S0, S1 and S2 are pin-strapped to select a single fixed output range for all DACs. These pins should be tied to either GND or V_{DD} even if they are unused.

S1 (Pin 24): Span Bit 1 Input. In Manual Span mode (M-SPAN tied to V_{DD}), pins S0, S1 and S2 are pin-strapped to select a single fixed output range for all DACs. These pins should be tied to either GND or V_{DD} even if they are unused.

PIN FUNCTIONS

S2 (Pin 25): Span Bit 2 Input. In Manual Span mode (M-SPAN tied to V_{DD}), pins S0, S1 and S2 are pin-strapped to select a single fixed output range for all DACs. These pins should be tied to either GND or V_{DD} even if they are unused.

$\overline{\text{LDAC}}$ (Pin 26): Asynchronous DAC Load Input. When $\overline{\text{LDAC}}$ is a logic low, all DACs are updated ($\overline{\text{CS}}$/LD must be high).

I_{OUT2BF}, I_{OUT2BS} (Pins 28, 29): DAC B Current Output Complement Force and Sense Pins. Tie to ground via a clean, low impedance path. These pins may be used with a precision ground buffer amp as a Kelvin sensing pair (see the Typical Applications section).

R_{INB} (Pins 31, 32): Input Resistor for the External Reference Inverting Amplifier. The 20k input resistor is connected internally from R_{INB} to R_{COMB}. For normal operation tie R_{INB} to the external positive reference voltage (see Typical Applications). Either or both of these precision matched resistor sets (each set comprising R_{INX}, R_{COMX} and R_{EFX}) may be used to invert positive references to provide the negative voltages needed by the DACs. Typically 5V; accepts up to ±15V. Pins 31 and 32 are internally shorted together.

GE_{ADJB} (Pin 33): Gain Adjust Pin for DAC B. This control pin can be used to null gain error or to compensate for reference errors. The gain change expressed in LSB is the same for any output range. See System Offset and Gain Adjustments in the Operation section. Tie to ground if not used.

R_{COMB} (Pin 34): Virtual Ground Point for the DAC B Reference Amplifier Inverting Resistors. The 20k reference inverting resistors are connected internally from R_{INB} to R_{COMB} and from R_{COMB} to REFB, respectively (see Block Diagram). For normal operation tie R_{COMB} to the negative input of the external reference inverting amplifier (see Typical Applications).

REFB (Pins 35, 36): Feedback Resistor for the DAC B Reference Inverting Amplifier, and Reference Input for DAC B. The 20k feedback resistor is connected internally from REFB to R_{COMB}. For normal operation tie this pin to the output of the DAC B reference inverting amplifier (see Typical Applications). Typically –5V; accepts up to ±15V. Pins 35 and 36 are internally shorted together.

R_{OFSB} (Pins 37, 38): Bipolar Offset Resistor for DAC B. These pins provide the translation of the output voltage range for bipolar spans. Accepts up to ±15V; for normal operation tie to the positive reference voltage at R_{INB} (Pins 31, 32). Pins 37 and 38 are internally shorted together.

R_{FBB} (Pins 39, 40): DAC B Feedback Resistor. For normal operation tie to the output of the I/V converter amplifier for DAC B (see Typical Applications). The DAC output current from I_{OUT1B} flows through the feedback resistor to the R_{FBB} pins. Pins 39 and 40 are internally shorted together.

I_{OUT1B} (Pin 41): DAC B Current Output. This pin is a virtual ground when the DAC is operating and should reside at 0V. For normal operation tie to the negative input of the I/V converter amplifier for DAC B (see Typical Applications).

V_{OSADJB} (Pin 42): DAC B Offset Adjust Pin. This voltage control pin can be used to null unipolar offset or bipolar zero error. The offset change expressed in LSB is the same for any output range. See System Offset and Gain Adjustments in the Operation section. Tie to ground if not used.

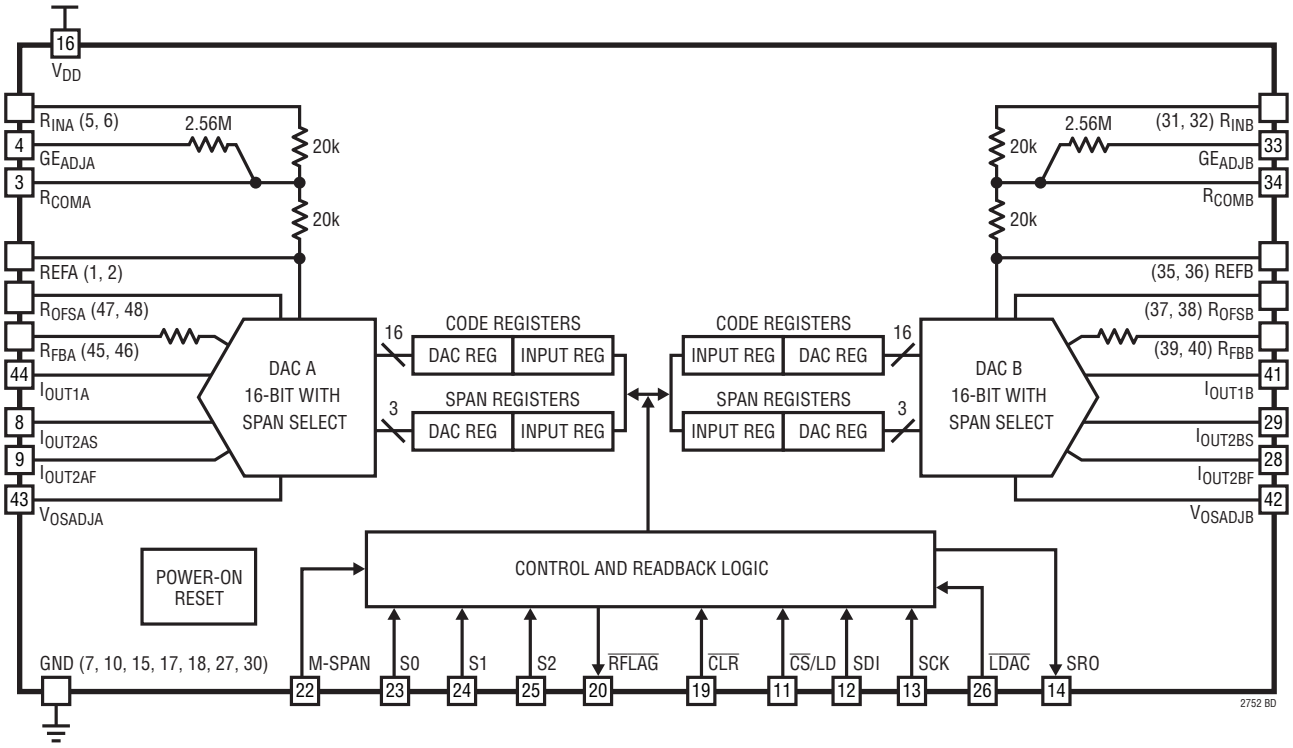
V_{OSADJA} (Pin 43): DAC A Offset Adjust Pin. This voltage control pin can be used to null unipolar offset or bipolar zero error. The offset change expressed in LSB is the same for any output range. See System Offset and Gain Adjustments in the Operation section. Tie to ground if not used.

I_{OUT1A} (Pin 44): DAC A Current Output. This pin is a virtual ground when the DAC is operating and should reside at 0V. For normal operation tie to the negative input of the I/V converter amplifier for DAC A (see Typical Applications).

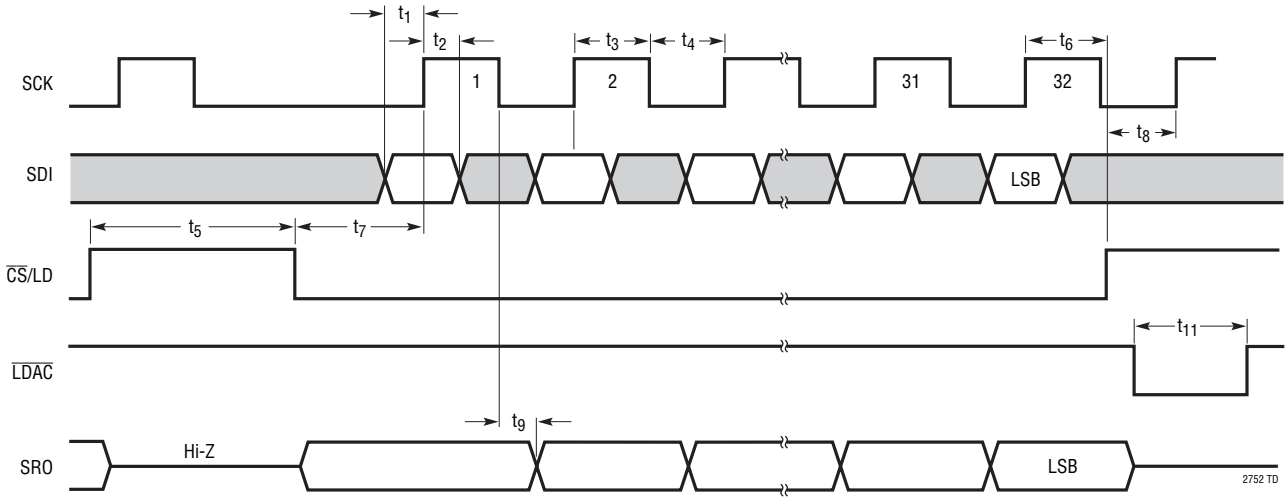
R_{FBA} (Pins 45, 46): DAC A Feedback Resistor. For normal operation tie to the output of the I/V converter amplifier for DAC A (see Typical Applications). The DAC output current from I_{OUT1A} flows through the feedback resistor to the R_{FBA} pins. Pins 45 and 46 are internally shorted together.

R_{OFSA} (Pins 47, 48): Bipolar Offset Resistor for DAC A. This pin provides the translation of the output voltage range for bipolar spans. Accepts up to ±15V; for normal operation tie to the positive reference voltage at R_{INA} (Pins 5, 6). Pins 47 and 48 are internally shorted together.

BLOCK DIAGRAM



TIMING DIAGRAM



OPERATION

Output Ranges

The LTC2752 is a dual, current-output, serial-input precision multiplying DAC with selectable output ranges. Ranges can either be programmed in software for maximum flexibility—each of the DACs can be programmed to any one of six output ranges—or hardwired through pin-strapping. Two unipolar ranges are available (0V to 5V and 0V to 10V), and four bipolar ranges (±2.5V, ±5V, ±10V and –2.5V to 7.5V). These ranges are obtained when an external precision 5V reference is used. The output ranges for other reference voltages are easy to calculate by observing that each range is a multiple of the external reference voltage. The ranges can then be expressed: 0 to 1×, 0 to 2×, ±0.5×, ±1×, ±2×, and –0.5× to 1.5×.

Manual Span Configuration

Multiple output ranges are not needed in some applications. To configure the LTC2752 to operate in a single span without additional operational overhead, tie the M-SPAN pin directly to V_{DD}. The active output range for all DACs is then set via hardware pin strapping of pins S2, S1 and S0 (rather than through the SPI port); and Write and Update commands have no effect on the active output span. See Figure 1 and Table 3.

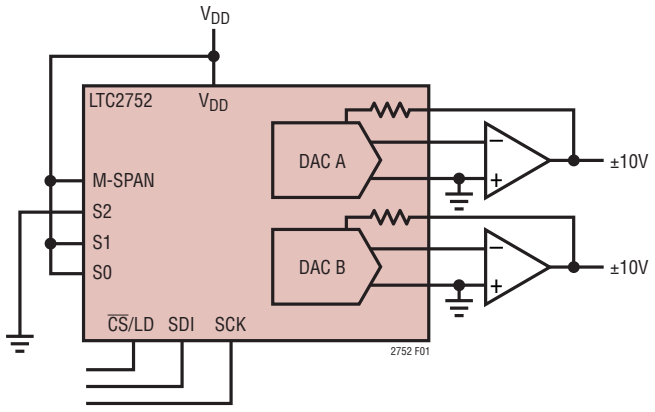


Figure 1. Using M-SPAN to Configure the LTC2752 for Single-Span Operation (±10V Range Shown)

Tie the M-SPAN pin to ground for normal SoftSpan operation.

Input and DAC Registers

The LTC2752 has 5 internal registers for each DAC, a total of 10 registers (see Block Diagram). Each DAC channel has two sets of double-buffered registers—one set for the code data, and one for the output range of the DAC—plus one readback register. Double buffering provides the capability to simultaneously update the span (output range) and code, which allows smooth voltage transitions when changing output ranges. It also permits the simultaneous updating of multiple DACs.

Each set of double-buffered registers comprises an Input register and a DAC register.

Input register: The Write operation shifts data from the SDI pin into a chosen Input register. The Input registers are holding buffers; Write operations do not affect the DAC outputs.

DAC register: The Update operation copies the contents of an Input register to its associated DAC register. The contents of a DAC register directly updates the associated DAC output voltage or output range.

Note that updates always include both Code and Span register sets; but the values held in the DAC registers will only change if the associated Input register values have previously been changed via a Write operation.

Serial Interface

When the $\overline{CS}$/LD pin is taken low, the data on the SDI pin is loaded into the shift register on the rising edge of the clock (SCK pin). The minimum (24-bit wide) loading sequence required for the LTC2752 is a 4-bit command word (C3 C2 C1 C0), followed by a 4-bit address word (A3 A2 A1 A0) and 16 data (span or code) bits, MSB first. Figure 2 shows the SDI input word syntax to use when

OPERATION

writing code or span. If a 32-bit input sequence is used, the first eight bits must be zeros, followed by the same sequence as for a 24-bit wide input. Figure 3 shows the input and readback sequences for both 24-bit and 32-bit operations.

When $\overline{CS}$/LD is low, the SRO pin (Serial Readback Output) is an active output.The readback data begins after the command (C3-C0) and address (A3-A0) words have been shifted into SDI. SRO outputs a logic low (when $\overline{CS}$/LD is low) until the readback data begins. For a 24-bit input sequence, the 16 readback bits are shifted out on the falling edges of clocks 8-23, suitable for shifting into a microprocessor on the rising edges of clocks 9-24. For a 32-bit sequence, the bits are shifted out on clocks 16-31; see Figure 3b.

When $\overline{CS}$/LD is high, the SRO pin presents a high impedance (three-state) output.

$\overline{LDAC}$ is an asynchronous update pin. When $\overline{LDAC}$ is taken low, all DACs are updated with code and span data (data in the Input buffers is copied into the DAC buffers). $\overline{CS}$/LD must be high during this operation; otherwise $\overline{LDAC}$ is locked out and will have no effect. The use of $\overline{LDAC}$ is functionally identical to the "Update All DACs" serial input command.

The codes for the command word (C3-C0) are defined in Table 1; Table 2 defines the codes for the address word (A3-A0).

Readback

In addition to the Input and DAC registers, each DAC has one Readback register associated with it. When a Read command is issued to a DAC, the contents of one of its four buffers (Input and DAC registers for each of Span and Code) is copied into its Readback register and serially shifted out through the SRO pin. Figure 3 shows the loading and readback sequences.

In the data field (D15-D0) of any non-read instruction cycle, SRO shifts out the contents of the buffer that was specified in the preceding command. This "rolling readback" default mode of operation can dramatically reduce the number of instruction cycles needed, since any command can be verified during succeeding commands with no additional overhead. See Figure 4. Table 1 shows the storage location ('readback pointer') of the data which will be output from SRO during the next instruction.

For Read commands, the data is shifted out during the Read instruction itself (on the 16 falling SCK edges immediately after the last address bit is shifted in on SDI). When checking the span of a DAC using SRO, the span bits are the last four bits shifted out, corresponding to their sequence and positions when writing a span. See Figure 3.

Span Readback in Manual Span Configuration

If a Span DAC register is chosen for readback, SRO responds by outputting the actual output span; this is true whether the LTC2752 is configured for SoftSpan (M-SPAN tied to GND) or manual span (M-SPAN tied to V_{DD}) use.

In SoftSpan configuration, SRO outputs the span code from the Span DAC register (programmed through the SPI port). In manual span configuration, the active span is controlled by pins S2, S1 and S0, so SRO outputs the logic values of these pins. The span code bits S2, S1 and S0 always appear in the same order and positions in the SRO output sequence; see Figure 3.

OPERATION

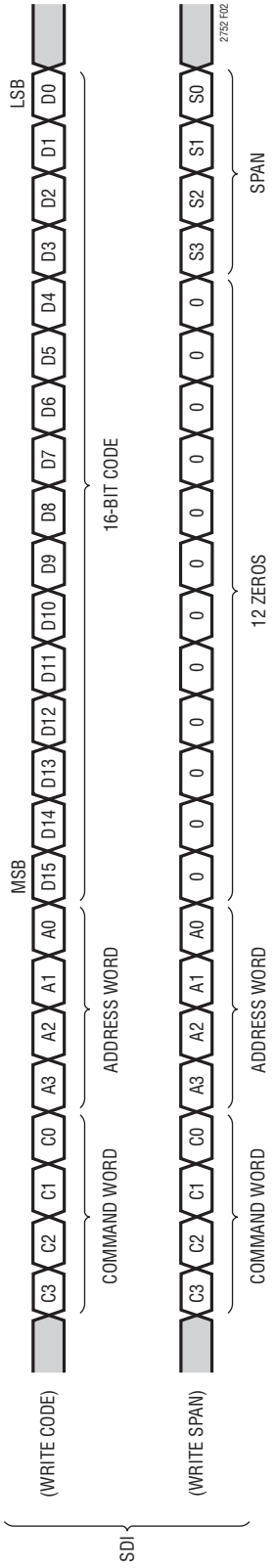


Figure 2. Serial Input Write Sequence

OPERATION

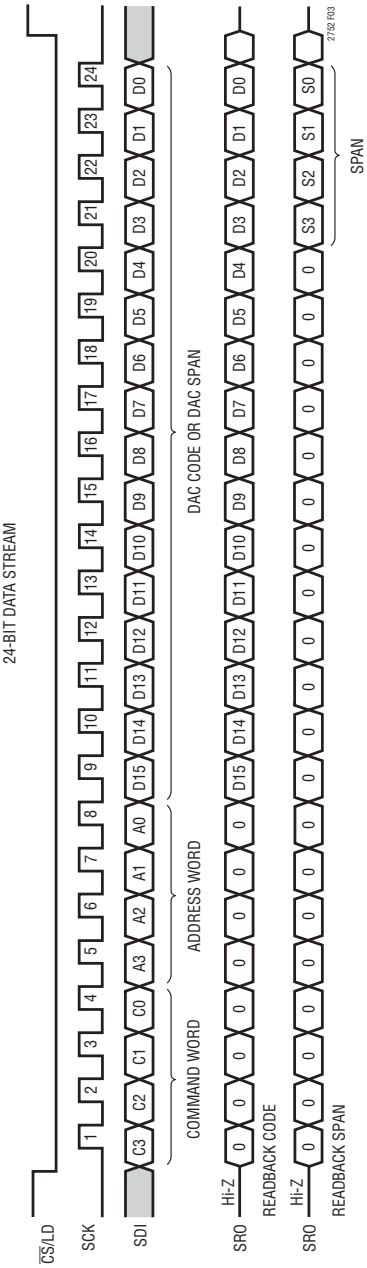


Figure 3a. 24-Bit Instruction Sequence

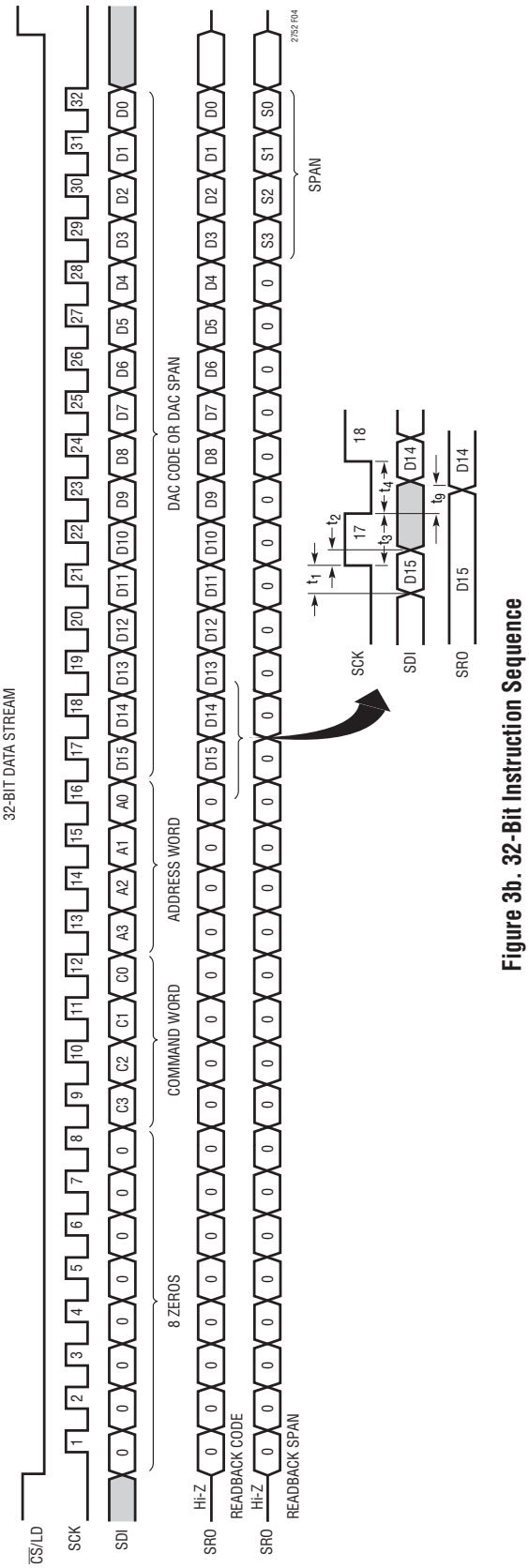


Figure 3b. 32-Bit Instruction Sequence

OPERATION

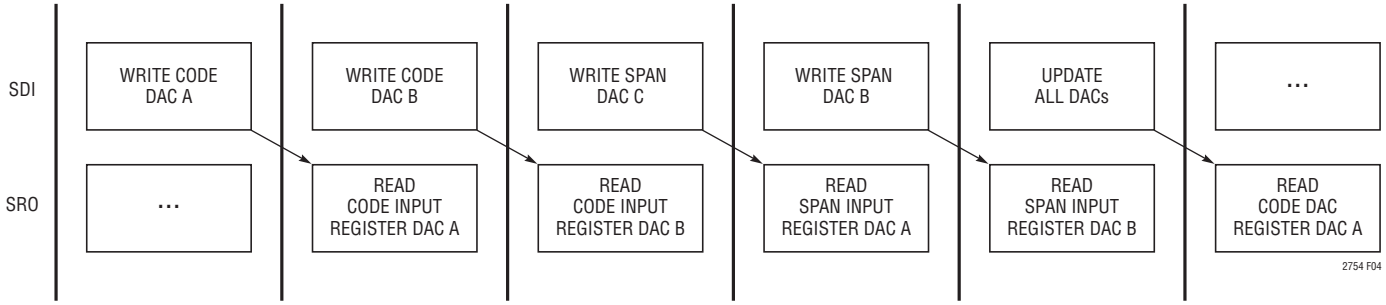


Figure 4. Rolling Readback

Table 1. Command Codes

CODE C3	C2	C1	C0	COMMAND	READBACK POINTER– CURRENT INPUT WORD W_0	READBACK POINTER– NEXT INPUT WORD W_{+1}
0	0	1	0	Write Span DAC n	Set by Previous Command	Input Span Register DAC n
0	0	1	1	Write Code DAC n	Set by Previous Command	Input Code Register DAC n
0	1	0	0	Update DAC n	Set by Previous Command	DAC Span Register DAC n
0	1	0	1	Update All DACs	Set by Previous Command	DAC Code Register DAC n
0	1	1	0	Write Span DAC n Update DAC n	Set by Previous Command	DAC Span Register DAC n
0	1	1	1	Write Code DAC n Update DAC n	Set by Previous Command	DAC Code Register DAC n
1	0	0	0	Write Span DAC n Update All DACs	Set by Previous Command	DAC Span Register DAC n
1	0	0	1	Write Code DAC n Update All DACs	Set by Previous Command	DAC Code Register DAC n
1	0	1	0	Read Input Span Register DAC n	Input Span Register DAC n	
1	0	1	1	Read Input Code Register DAC n	Input Code Register DAC n	
1	1	0	0	Read DAC Span Register DAC n	DAC Span Register DAC n	
1	1	0	1	Read DAC Code Register DAC n	DAC Code Register DAC n	
1	1	1	1	No Operation	Set by Previous Command	DAC Code Register DAC n
–				System Clear	–	DAC Span Register DAC A
–				Initial Power-Up or Power Interupt	–	DAC Span Register DAC A

Codes not shown are reserved–do not use

Table 2. Address Codes

A3	A2	A1	A0	n
0	0	0	×	DAC A
0	0	1	×	DAC B
1	1	1	×	All DACs (Note 1)

Codes not shown are reserved–do not use. × = Don't Care.

Note 1. If readback is taken using the All DACs address, the LTC2752 defaults to DAC A.

Table 3. Span Codes

S3	S2	S1	S0	SPAN
0	0	0	0	Unipolar 0V to 5V
0	0	0	1	Unipolar 0V to 10V
0	0	1	0	Bipolar –5V to 5V
0	0	1	1	Bipolar –10V to 10V
0	1	0	0	Bipolar –2.5V to 2.5V
0	1	0	1	Bipolar –2.5V to 7.5V

Codes not shown are reserved–do not use

OPERATION

Examples

1. Using a 24-bit instruction, load DAC A with the unipolar range of 0V to 10V, output at zero volts and DAC B with the bipolar range of ±10V, outputs at zero volts. Note all DAC outputs should change at the same time.

a) $\overline{CS}$/LD↓
Clock SDI = 0010 1111 0000 0000 0000 0011

b) $\overline{CS}$/LD↑
Span Input register- Range of all DACs set to bipolar ±10V.

c) $\overline{CS}$/LD↓
Clock SDI = 0010 0000 0000 0000 0000 0001

d) $\overline{CS}$/LD↑
Span Input register- Range of DAC A set to unipolar 0V to 10V.

e) $\overline{CS}$/LD↓
Clock SDI = 0011 1111 1000 0000 0000 0000

f) $\overline{CS}$/LD↑
Code Input register- Code of all DACs set to midscale.

g) $\overline{CS}$/LD↓
Clock SDI = 0011 0000 0000 0000 0000 0000

h) $\overline{CS}$/LD↑
Code Input register- Code of DAC A set to zero code.

i) $\overline{CS}$/LD↓
Clock SDI = 0100 1111 XXXX XXXX XXXX XXXX

j) $\overline{CS}$/LD↑
Update all DACs for both Code and Range.

k) Alternatively steps i and j could be replaced with $\overline{LDAC}$ ⎍.

2. Using a 32-bit load sequence, load DAC B with bipolar ±2.5V and its output at zero volts. Use readback to check Input register contents before updating the DAC output (i.e., before copying Input register contents into DAC register).

a) $\overline{CS}$/LD↓ (Note that after power-on, the code in Input register is zero)
Clock SDI =
0000 0000 0011 0010 1000 0000 0000 0000

b) $\overline{CS}$/LD↑
Code Input register- Code of DAC B set to midscale setting.

c) $\overline{CS}$/LD↓
Clock SDI =
0000 0000 0010 0010 0000 0000 0000 0100
Data out on SRO = 1000 0000 0000 0000 Verifies that Code Input register- DAC B is at midscale setting.

d) $\overline{CS}$/LD↑
Span Input register- Range of DAC B set to Bipolar ±2.5V range.

e) $\overline{CS}$/LD↓
Clock SDI =
0000 0000 1010 0010 XXXX XXXX XXXX XXXX
Data Out on SRO = 0000 0000 0000 0100
Verifies that Span Input register- range of DAC B set to Bipolar ±2.5V Range.
$\overline{CS}$/LD↑

f) $\overline{CS}$/LD↓
Clock SDI =
0000 0000 0100 0010 XXXX XXXX XXXX XXXX

g) $\overline{CS}$/LD↑
Update DAC B for both Code and Range

h) Alternatively steps f and g could be replaced with $\overline{LDAC}$ ⎍.

System Offset and Reference Adjustments

Many systems require compensation for overall system offset. This may be an order of magnitude or more greater than the offset of the LTC2752, which is so low as to be dominated by external output amplifier errors even when using the most precise op amps.

OPERATION

The offset adjust pin V_{OSADJX} can be used to null unipolar offset or bipolar zero error. The offset change expressed in LSB is the same for any output range:

$$\Delta V_{OS}[LSB] = \frac{-V_{VOSADJX}}{V_{RINX}} \bullet 512$$

A 5V control voltage applied to V_{OSADJX} produces ΔV_{OS} = –512 LSB in any output range, assuming a 5V reference voltage at R_{INX}.

In voltage terms, the offset delta is attenuated by a factor of 32, 64 or 128, depending on the output range. (These functions hold regardless of reference voltage.)

$\Delta V_{OS} = -(1/128)V_{OSADJX}$ [0V to 5V, ±2.5V spans]

$\Delta V_{OS} = -(1/64)V_{OSADJX}$ [0V to 10V, ±5V, –2.5V to 7.5V spans]

$\Delta V_{OS} = -(1/32)V_{OSADJX}$ [±10V span]

The gain error adjust pins GE_{ADJX} can be used to null gain error or to compensate for reference errors. The gain error change expressed in LSB is the same for any output range:

$$\Delta GE = \frac{V_{GEADJX}}{V_{RINX}} \bullet 512$$

The gain-error delta is non-inverting for positive reference voltages.

Note that this pin compensates the gain by altering the inverted reference voltage V_{REFX}. In voltage terms, the V_{REFX} delta is inverted and attenuated by a factor of 128.

$$\Delta V_{REFX} = -(1/128)GE_{ADJX}$$

The nominal input range of these pins is ±5V; other voltages of up to ±15V may be used if needed. However, do not use voltages divided down from power supplies; reference-quality, low-noise inputs are required to maintain the best DAC performance.

The V_{OSADJX} pins have an input impedance of 1.28MΩ. These pins should be driven with a Thevenin-equivalent impedance of 10k or less to preserve the settling performance of the LTC2752. They should be shorted to GND if not used.

The GE_{ADJX} pins have an input impedance of 2.56MΩ, and are intended for use with fixed reference voltages only. They should be shorted to GND if not used.

Power-On Reset and Clear

When power is first applied to the LTC2752, all DACs power-up in unipolar 5V mode (S3 S2 S1 S0 = 0000). All internal DAC registers are reset to 0 and the DAC outputs initialize to zero volts.

If the part is configured for manual span operation, all DACs will be set into the pin-strapped range at the first Update command. This allows the user to simultaneously update span and code for a smooth voltage transition into the chosen output range.

When the $\overline{CLR}$ pin is taken low, a system clear results. The DAC buffers are reset to 0 and the DAC outputs are all reset to zero volts. The Input buffers are left intact, so that any subsequent Update command (including the use of $\overline{LDAC}$) restores the addressed DACs to their respective previous states.

If $\overline{CLR}$ is asserted during an instruction, i.e., when $\overline{CS}$/LD is low, the instruction is aborted. Integrity of the relevant Input buffers is not guaranteed under these conditions, therefore the contents should be checked using readback or replaced.

The $\overline{RFLAG}$ pin is used as a flag to notify the system of a loss of data integrity. The $\overline{RFLAG}$ output is asserted low at power-up, system clear, or if the supply V_{DD} dips below approximately 2V; and stays asserted until any valid Update command is executed.

APPLICATIONS INFORMATION

Op Amp Selection

Because of the extremely high accuracy of the 16-bit LTC2752, careful thought should be given to op amp selection in order to achieve the exceptional performance of which the part is capable. Fortunately, the sensitivity of INL and DNL to op amp offset has been greatly reduced compared to previous generations of multiplying DACs.

Tables 4 and 5 contain equations for evaluating the effects of op amp parameters on the LTC2752's accuracy when programmed in a unipolar or bipolar output range. These are the changes the op amp can cause to the INL, DNL, unipolar offset, unipolar gain error, bipolar zero and bipolar gain error.

Table 6 contains a partial list of Linear Technology precision op amps recommended for use with the LTC2752. The easy-to-use design equations simplify the selection of op amps to meet the system's specified error budget. Select the amplifier from Table 6 and insert the specified op amp parameters in Table 5. Add up all the errors for each category to determine the effect the op amp has on the accuracy of the part. Arithmetic summation gives an (unlikely) worst-case effect. A root-sum-square (RMS) summation produces a more realistic estimate.

Table 4. Coefficients for the Equations of Table 5

OUTPUT RANGE	A1	A2	A3	A4	A5
5V	1.1	2	1		1
10V	2.2	3	0.5		1.5
±5V	2	2	1	1	1.5
±10V	4	4	0.83	1	2.5
±2.5V	1	1	1.4	1	1
–2.5V to 7.5V	1.9	3	0.7	0.5	1.5

Table 5. Easy-to-Use Equations Determine Op Amp Effects on DAC Accuracy in All Output Ranges (Circuit of Page 1). Subscript 1 Refers to Output Amp, Subscript 2 Refers to Reference Inverting Amp.

OP AMP	INL (LSB)	DNL (LSB)	UNIPOLAR OFFSET (LSB)	BIPOLAR ZERO ERROR (LSB)	UNIPOLAR GAIN ERROR (LSB)	BIPOLAR GAIN ERROR (LSB)
V_{OS1} (mV)	$V_{OS1} \cdot 3 \cdot \left(\frac{5V}{V_{REF}}\right)$	$V_{OS1} \cdot 0.78 \cdot \left(\frac{5V}{V_{REF}}\right)$	$A3 \cdot V_{OS1} \cdot 13.1 \cdot \left(\frac{5V}{V_{REF}}\right)$	$A3 \cdot V_{OS1} \cdot 19.6 \cdot \left(\frac{5V}{V_{REF}}\right)$	$V_{OS1} \cdot 13.1 \cdot \left(\frac{5V}{V_{REF}}\right)$	$V_{OS1} \cdot 13.1 \cdot \left(\frac{5V}{V_{REF}}\right)$
I_{B1} (nA)	$I_{B1} \cdot 0.0003 \cdot \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \cdot 0.00008 \cdot \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \cdot 0.13 \cdot \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \cdot 0.13 \cdot \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \cdot 0.0018 \cdot \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \cdot 0.0018 \cdot \left(\frac{5V}{V_{REF}}\right)$
A_{VOL1} (V/mV)	$A1 \cdot \left(\frac{16.5}{A_{VOL1}}\right)$	$A2 \cdot \left(\frac{1.5}{A_{VOL1}}\right)$	0	0	$A5 \cdot \left(\frac{131}{A_{VOL1}}\right)$	$A5 \cdot \left(\frac{131}{A_{VOL1}}\right)$
V_{OS2} (mV)	0	0	0	$A4 \cdot \left(V_{OS2} \cdot 13.1 \cdot \left(\frac{5V}{V_{REF}}\right)\right)$	$V_{OS2} \cdot 26.2 \cdot \left(\frac{5V}{V_{REF}}\right)$	$V_{OS2} \cdot 26.2 \cdot \left(\frac{5V}{V_{REF}}\right)$
I_{B2} (nA)	0	0	0	$A4 \cdot \left(I_{B2} \cdot 0.13 \cdot \left(\frac{5V}{V_{REF}}\right)\right)$	$I_{B2} \cdot 0.26 \cdot \left(\frac{5V}{V_{REF}}\right)$	$I_{B2} \cdot 0.26 \cdot \left(\frac{5V}{V_{REF}}\right)$
A_{VOL2} (V/mV)	0	0	0	$A4 \cdot \left(\frac{66}{A_{VOL2}}\right)$	$\left(\frac{131}{A_{VOL2}}\right)$	$\left(\frac{131}{A_{VOL2}}\right)$

Table 6. Partial List of LTC Precision Amplifiers Recommended for Use with the LTC2752 with Relevant Specifications

	AMPLIFIER SPECIFICATIONS								
AMPLIFIER	V_{OS} µV	I_B nA	A_{VOL} V/mV	VOLTAGE NOISE nV/√Hz	CURRENT NOISE pA/√Hz	SLEW RATE V/µs	GAIN BANDWIDTH PRODUCT MHz	$t_{SETTLING}$ with LTC2752 µs	POWER DISSIPATION mW
LT1001	25	2	800	10	0.12	0.25	0.8	120	46
LT1097	50	0.35	1000	14	0.008	0.2	0.7	120	11
LT1112 (Dual)	60	0.25	1500	14	0.008	0.16	0.75	115	10.5/Op Amp
LT1124 (Dual)	70	20	4000	2.7	0.3	4.5	12.5	19	69/Op Amp
LT1468	75	10	5000	5	0.6	22	90	2	117
LT1469 (Dual)	125	10	2000	5	0.6	22	90	2	123/Op Amp

APPLICATIONS INFORMATION

Op amp offset will contribute mostly to output offset and gain error, and has minimal effect on INL and DNL. For example, for the LTC2752 with a 5V reference in 5V unipolar mode, a 250µV op amp offset will cause a 3.3LSB zero-scale error and a 3.3LSB gain error; but only 0.75LSB of INL degradation and 0.2LSB of DNL degradation.

While not directly addressed by the simple equations in Tables 4 and 5, temperature effects can be handled just as easily for unipolar and bipolar applications. First, consult an op amp's data sheet to find the worst-case V_{OS} and I_B over temperature. Then, plug these numbers into the V_{OS} and I_B equations from Table 5 and calculate the temperature-induced effects.

For applications where fast settling time is important, Application Note 74, *Component and Measurement Advances Ensure 16-Bit DAC Settling Time*, offers a thorough discussion of 16-bit DAC settling time and op amp selection.

Precision Voltage Reference Considerations

Much in the same way selecting an operational amplifier for use with the LTC2752 is critical to the performance of the system, selecting a precision voltage reference also requires due diligence. The output voltage of the LTC2752 is directly affected by the voltage reference; thus, any voltage reference error will appear as a DAC output voltage error.

There are three primary error sources to consider when selecting a precision voltage reference for 16-bit applications: output voltage initial tolerance, output voltage temperature coefficient and output voltage noise.

Initial reference output voltage tolerance, if uncorrected, generates a full-scale error term. Choosing a reference with low output voltage initial tolerance, like the LT1236 (±0.05%), minimizes the gain error caused by the reference; however, a calibration sequence that corrects for system zero- and full-scale error is always recommended.

A reference's output voltage temperature coefficient affects not only the full-scale error, but can also affect the circuit's apparent INL and DNL performance. If a reference is chosen with a loose output voltage temperature coefficient, then the DAC output voltage along its transfer characteristic will be very dependent on ambient conditions. Minimizing the error due to reference temperature coefficient can be achieved by choosing a precision reference with a low output voltage temperature coefficient and/or tightly controlling the ambient temperature of the circuit to minimize temperature gradients.

As precision DAC applications move to 16-bit and higher performance, reference output voltage noise may contribute a dominant share of the system's noise floor. This in turn can degrade system dynamic range and signal-to-noise ratio. Care should be exercised in selecting a voltage reference with as low an output noise voltage as practical for the system resolution desired. Precision voltage references, like the LT1236 and LTC6655, produce low output noise in the 0.1Hz to 10Hz region, well below the 16-bit LSB level

Table 7. Partial List of LTC Precision References Recommended for Use with the LTC2752 with Relevant Specifications

REFERENCE	INITIAL TOLERANCE	TEMPERATURE DRIFT	0.1Hz to 10Hz NOISE
LT1019A-5, LT1019A-10	±0.05% Max	5ppm/°C Max	$12\mu V_{P-P}$
LT1236A-5, LT1236A-10	±0.05% Max	5ppm/°C Max	$3\mu V_{P-P}$
LT1460A-5, LT1460A-10	±0.075% Max	10ppm/°C Max	$20\mu V_{P-P}$
LT1790A-2.5	±0.05% Max	10ppm/°C Max	$12\mu V_{P-P}$
LTC6652A-2.048	±0.05% Max	5ppm/°C Max	$2.1ppm_{P-P}$
LTC6652A-2.5			$2.1ppm_{P-P}$
LTC6652A-3			$2.1ppm_{P-P}$
LTC6652A-3.3			$2.2ppm_{P-P}$
LTC6652A-4.096			$2.3ppm_{P-P}$
LTC6652A-5			$2.8ppm_{P-P}$
LT6655A-25, LT6655A-5	±0.025% Max	2ppm/°C Max	$0.25ppm_{P-P}$

APPLICATIONS INFORMATION

in 5V or 10V full-scale systems. However, as the circuit bandwidths increase, filtering the output of the reference may be required to minimize output noise.

Grounding

As with any high resolution converter, clean grounding is important. A low impedance analog ground plane is necessary, as are star grounding techniques. Keep the board layer used for star ground continuous to minimize ground resistances; that is, use the star-ground concept without using separate star traces. The I_{OUT2} pins are of particular concern; INL will be degraded by the code dependent currents carried by the I_{OUT2XF} and I_{OUT2XS} pins if voltage drops to ground are allowed to develop. The best strategy here is to tie the pins to the star ground plane by multiple vias located directly underneath the part. Alternatively, the pins may be routed to the star ground point if necessary; join the force and sense pins together at the part and route one trace for each channel of no more than 120 squares of 1oz. copper.

In the rare case in which neither of these alternatives is practicable, a force/sense amplifier should be used as a ground buffer (see Typical Applications). Note, however, that the voltage offset of the ground buffer amp directly contributes to the effects on accuracy specified in Table 5 under V_{OS1}. The combined effects of the offsets can be calculated by substituting the total offset from I_{OUT1X} to I_{OUT2XS} for V_{OS1} in the equations.

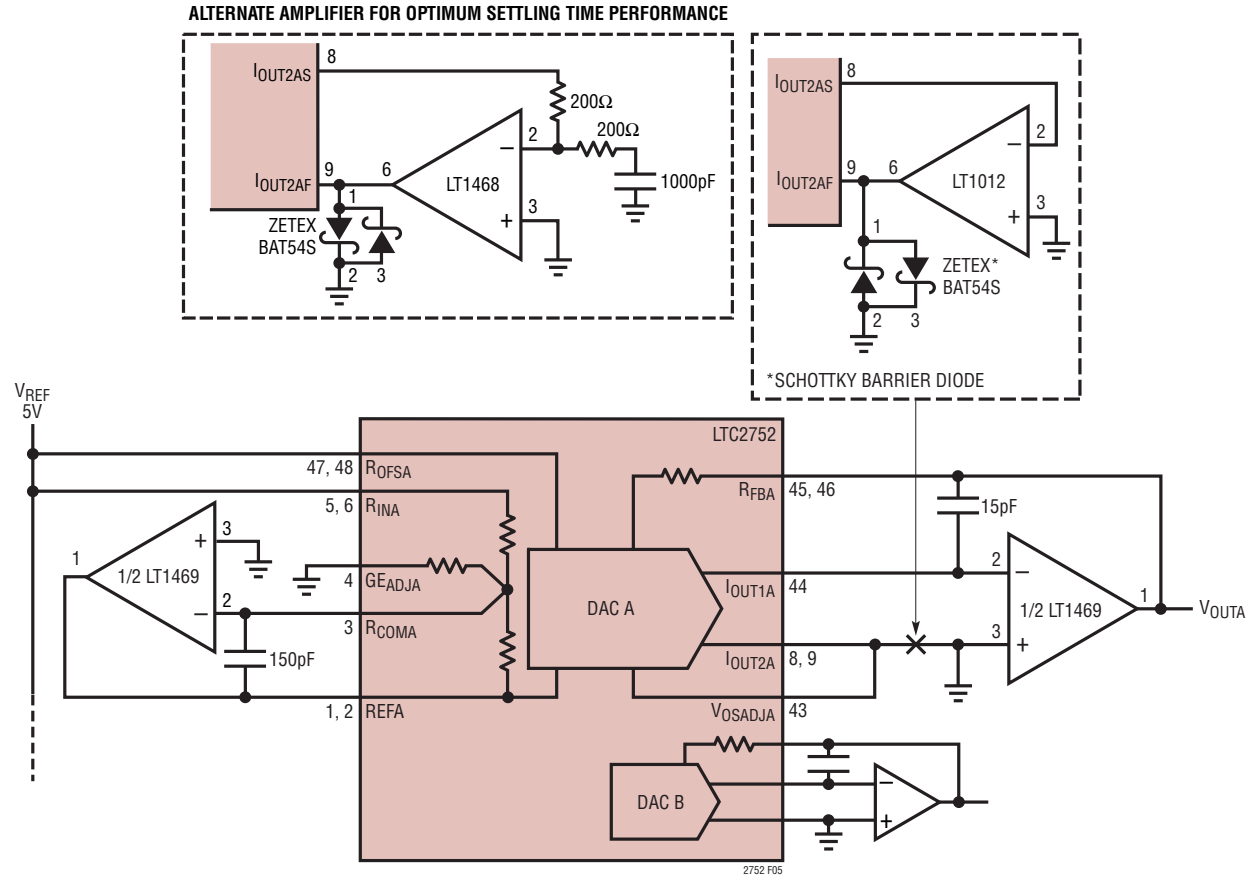
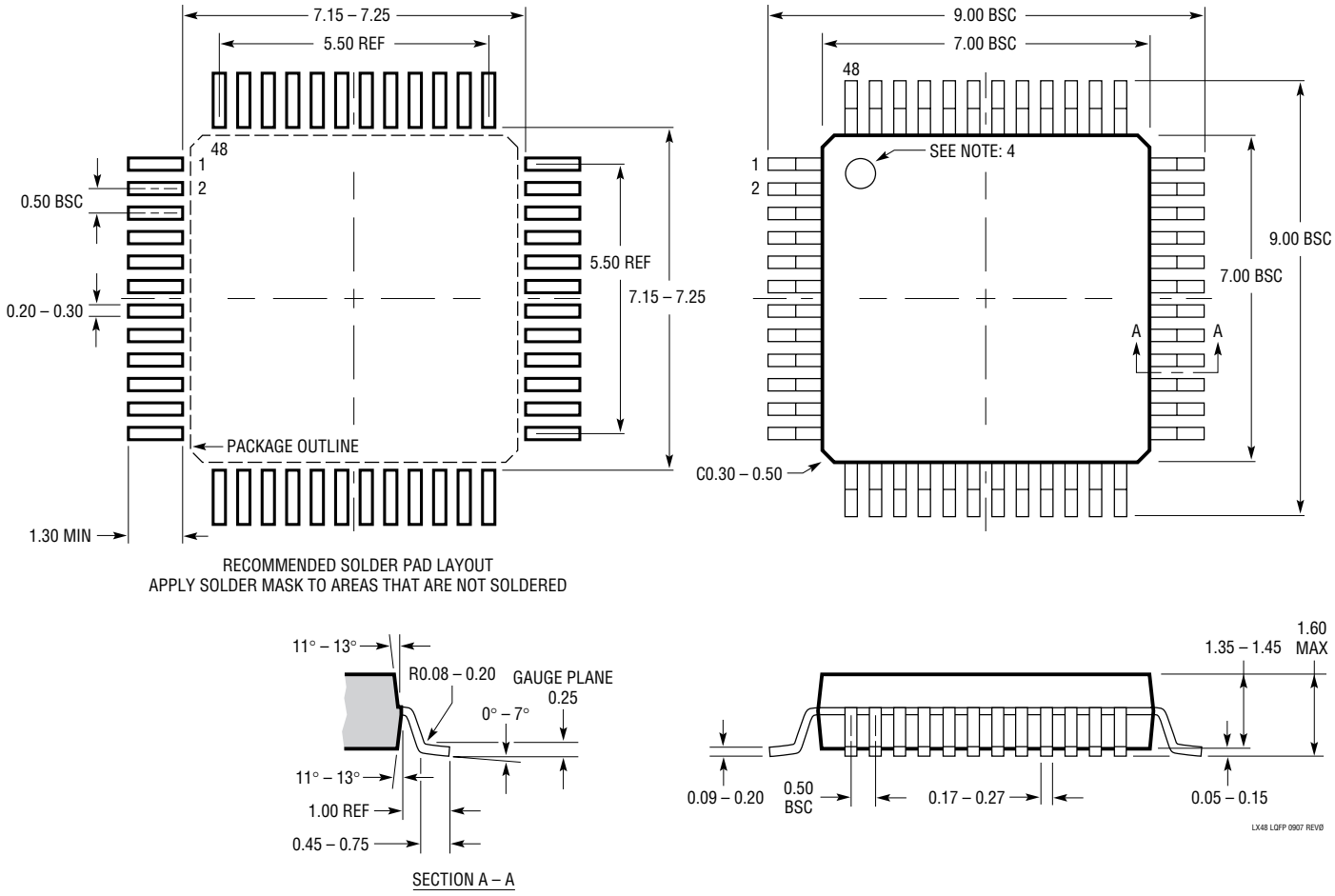


Figure 5. Optional Circuits for Driving I_{OUT2} from GND with a Force/Sense Amplifier

PACKAGE DESCRIPTION

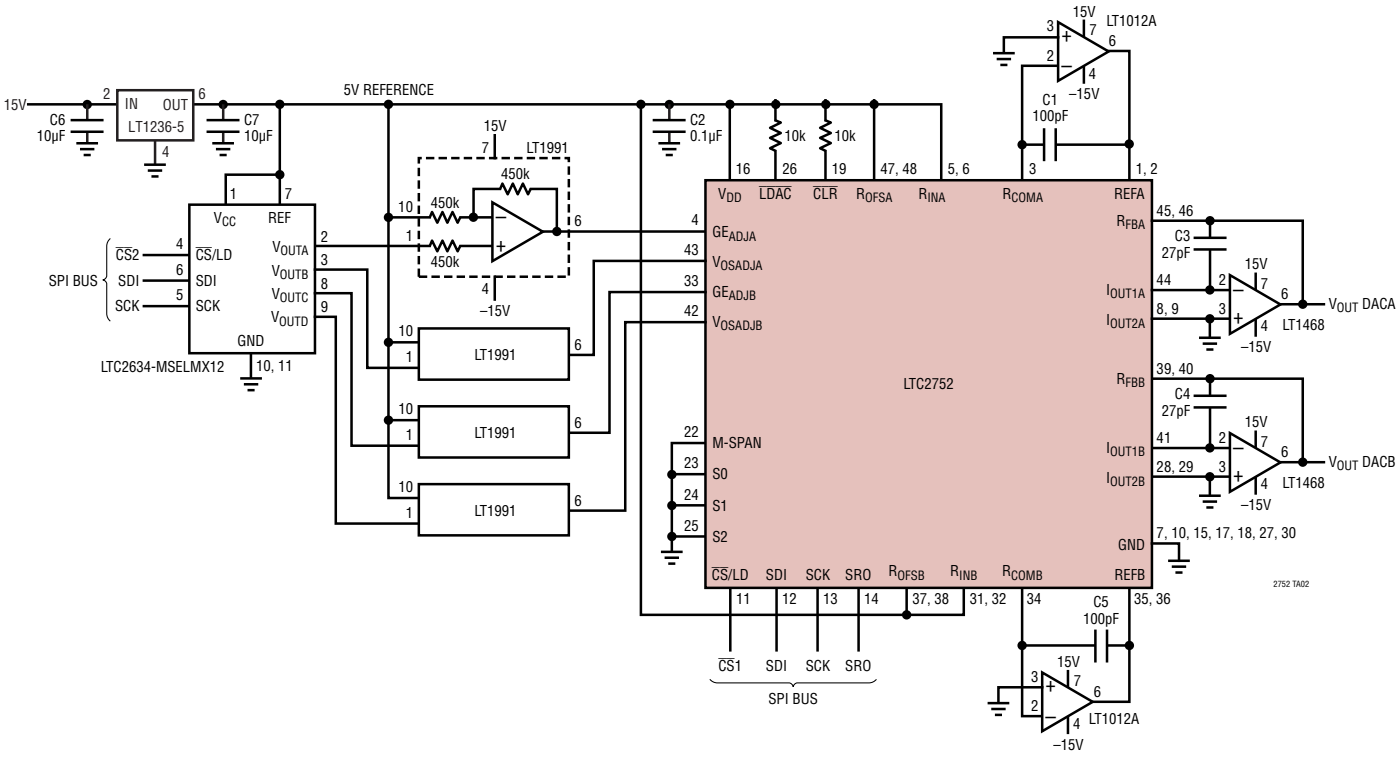
LX Package
48-Lead Plastic LQFP (7mm × 7mm)
(Reference LTC DWG # 05-08-1760 Rev Ø)



NOTE:
1. PACKAGE DIMENSIONS CONFORM TO JEDEC #MS-026 PACKAGE OUTLINE
2. DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.25mm ON ANY SIDE, IF PRESENT
4. PIN-1 INDENTIFIER IS A MOLDED INDENTATION, 0.50mm DIAMETER
5. DRAWING IS NOT TO SCALE

TYPICAL APPLICATION

Digitally Controlled Offset and Gain Trim Circuit. Powering V_{DD} from LT1236 Ensures Quiet Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2757	Single Parallel 18-Bit I_{OUT} SoftSpan DAC	±1LSB INL/DNL, Software-Selectable Ranges, 7mm × 7mm LQFP-48 Package
LTC2754	Quad Serial 16-Bit/12-Bit I_{OUT} SoftSpan DACs	±1LSB INL/DNL, Software-Selectable Ranges, 7mm × 8mm QFN-52 Package
LTC2751	Single Parallel 16-Bit/14-Bit/12-Bit I_{OUT} SoftSpan DAC	±1LSB INL/DNL, Software-Selectable Ranges, 5mm × 7mm QFN-38 Package
LTC2753	Dual Parallel 16-Bit/14-Bit/12-Bit I_{OUT} SoftSpan DACs	±1LSB INL/DNL, Software-Selectable Ranges, 7mm × 7mm QFN-48 Package
LTC2755	Quad Parallel 16-Bit/14-Bit/12-Bit I_{OUT} SoftSpan DACs	±1LSB INL/DNL, Software-Selectable Ranges, 9mm × 9mm QFN-64 Package
LTC1590	Dual Serial 12-Bit Multiplying I_{OUT} DAC	± 0.5LSB INL/DNL 2-Quadrant, 16-Pin Narrow SO and PDIP Packages
LTC1592	Single Serial 16-Bit/14-Bit/12-Bit I_{OUT} SoftSpan DAC	±1LSB INL/DNL, Software-Selectable Ranges, 16-Lead SSOP Package
LTC1591/LTC1597	Single Parallel 16-Bit/14-Bit I_{OUT} DACs	±1LSB INL/DNL, Integrated 4-Quadrant Resistors, 28-Lead SSOP Package
LTC2704	Quad Serial 16-Bit/14-Bit/12-Bit V_{OUT} SoftSpan DACs	±1LSB INL/DNL, Software-Selectable Ranges, Integrated Amplifiers
References		
LTC6655	Precision Reference	0.025% Maximum Tolerance, 0.25ppm$_{P-P}$ 0.1Hz to 10Hz Noise
LT1027	Precision Reference	2ppm/°C Maximum Drift
LT1236A-5	Precision Reference	0.05% Maximum Tolerance, 1ppm$_{P-P}$ 0.1Hz to 10Hz Noise
Amplifiers		
LT1012	Precision Operational Amplifier	25µV Max Offset, 100pA Max Bias Current, 0.5µV$_{P-P}$ Noise, 380µA Supply Current
LT1001	Precision Operational Amplifier	25µV Max Offset, 0.3µV$_{P-P}$ Noise, High Output Drive
LT1468/LT1469	Single/Dual 16-Bit Accurate Op-Amp	90MHz GBW, 22V/µs Slew Rate, 0.3µV$_{P-P}$ Noise

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