19-1432; Rev 0; 3/99

MAXIM

Single-Supply, Low-Power, Serial 8-Bit ADCs

General Description

The MAX1106/MAX1107 low-power, 8-bit, single-channel, analog-to-digital converters (ADCs) feature an internal track/hold (T/H), voltage reference, clock, and serial interface. The MAX1106 is specified from +2.7V to +3.6V and consumes only 96µA. The MAX1107 is specified from +4.5V to +5.5V and consumes only 107µA. The analog inputs are pin-configurable, allowing unipolar and single-ended or differential operation.

The full-scale analog input range is determined by the internal reference of +2.048V (MAX1106) or +4.096V (MAX1107), or by an externally applied reference ranging from 1V to V_{DD}. The MAX1106/MAX1107 also feature a pin-selectable power-down mode that reduces power consumption to 0.5µA when the device is not in use. The 3-wire serial interface directly connects to SPI™, QSPI™, and MICROWIRE™ devices without external logic. Conversions up to 25ksps are performed using the internal clock.

The MAX1106/MAX1107 are available in a 10-pin µMAX package with a footprint that is just 20% of an 8-pin plastic DIP.

Applications

Portable Data Logging

Hand-Held Measurement Devices

Medical Instruments

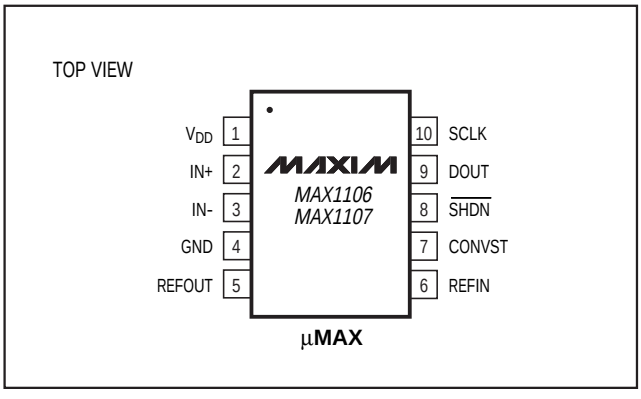
System Diagnostics

Solar-Powered Remote Systems

4–20mA-Powered Remote Systems

Receive-Signal-Strength Indicators

Pin Configuration



SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

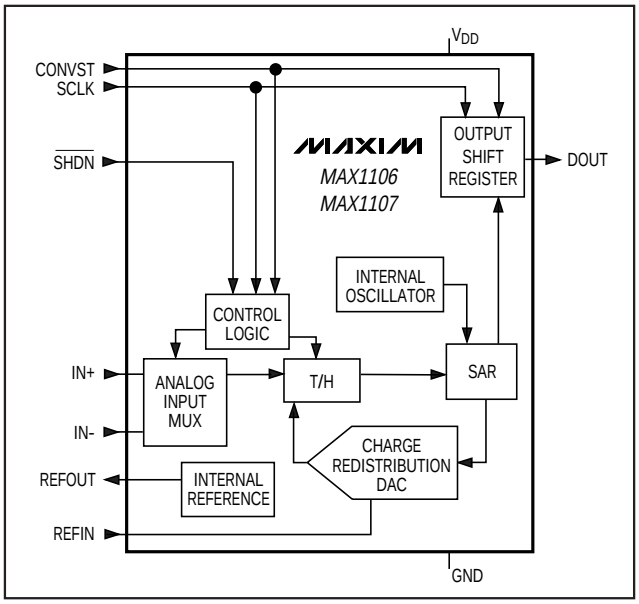
Features

- **Single Supply: +2.7V to +3.6V (MAX1106)**
  +4.5V to +5.5V (MAX1107)
- **Low Power: 96µA at +3V and 25ksps**
  0.5µA in Power-Down Mode
- **Pin-Programmable Configuration**
- **0 to V_{DD} Input Voltage Range**
- **Internal Track/Hold**
- **Internal Reference: +2.048V (MAX1106)**
  +4.096V (MAX1107)
- **1V to V_{DD} Reference Input Range**
- **SPI/QSPI/MICROWIRE-Compatible Serial Interface**
- **Small 10-Pin µMAX Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1106CUB	0°C to +70°C	10 µMAX
MAX1106EUB	-40°C to +85°C	10 µMAX
MAX1107CUB	0°C to +70°C	10 µMAX
MAX1107EUB	-40°C to +85°C	10 µMAX

Functional Diagram



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800.
For small orders, phone 1-800-835-8769.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
IN+, IN-, REFIN, REFOUT,
DOUT to GND.....-0.3V to (V_{DD} + 0.3V)
$\overline{SHDN}$, SCLK, CONVST to GND .....-0.3V to +6V
Continuous Power Dissipation (T_A = +70°C)
10-pin µMAX (derate 5.6mW/°C above +70°C) 444mW

Operating Temperature Ranges
MAX110_CUB .....0°C to +70°C
MAX110_EUB .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX1106

(V_{DD} = +2.7V to +3.6V; IN- to GND; f_{SCLK} = 2MHz; 25ksps conversion rate; 1µF capacitor at REFOUT; external +2.048V reference at REFIN; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			8			Bits
Relative Accuracy (Note 1)	INL	V_{DD} = 2.7V to 3.6V		±0.15	±0.5	LSB
		V_{DD} = 5.5V (Note 2)		±0.2		
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		V_{DD} = 2.7V to 3.6V		±0.2	±1	LSB
		V_{DD} = 5.5V (Note 2)		±0.5		
Gain Error (Note 3)					±1	LSB
Gain Temperature Coefficient				±0.8		ppm/°C
Total Unadjusted Error	TUE	T_A = +25°C			±1	LSB
		T_A = T_{MIN} to T_{MAX}		±0.5		
DYNAMIC PERFORMANCE (10kHz sine-wave input, 2.048Vp-p, 25ksps conversion rate)						
Signal-to-Noise Plus Distortion	SINAD			49		dB
Total Harmonic Distortion (up to the 5th harmonic)	THD			-70		dB
Spurious-Free Dynamic Range	SFDR			68		dB
Small-Signal Bandwidth	BW_{-3dB}	-3dB rolloff		1.5		MHz
Full-Power Bandwidth				0.8		MHz
ANALOG INPUTS						
Input Voltage Range (Note 4)	$V_{IN_}$	V_{IN+} to V_{IN-}	0		V_{REFIN}	V
Input Leakage Current		On/off-leakage current, V_{IN+} or V_{IN-} = 0 or V_{DD}		±0.01	±1	µA
Input Capacitance	C_{IN}			18		pF

ELECTRICAL CHARACTERISTICS—MAX1106 (continued)

(V_{DD} = +2.7V to +3.6V; IN- to GND; f_{SCLK} = 2MHz; 25ksps conversion rate; 1µF capacitor at REFOUT; external +2.048V reference at REFIN; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TRACK/HOLD						
Conversion Time	t_{CONV}	Figure 7			35	µs
Track/Hold Acquisition Time	t_{ACQ}		1			µs
Aperture Delay				10		ns
Aperture Jitter				<50		ps
Internal Clock Frequency				400		kHz
External Clock Frequency Range		For data transfer only			2	MHz
INTERNAL REFERENCE						
Output Voltage	V_{REFOUT}		1.968	2.048	2.128	V
REF Short-Circuit Current	I_{REFSC}	(Note 5)		150		µA
REF Tempco				±50		ppm/°C
Load Regulation		0 to 0.5mA (Note 6)		4		mV
Capacitive Bypass at REFOUT			1			µF
EXTERNAL REFERENCE						
Input Voltage Range	V_{REFIN}		1.0		V_{DD} + 0.05	V
Input Current		+2.048V at REFIN, full scale		1	20	µA
POWER REQUIREMENTS						
Supply Voltage	V_{DD}		2.7	3	5.5	V
Supply Current (Notes 2, 7)	I_{DD}	V_{DD} = 3.6V, C_L = 10pF		96	250	µA
		V_{DD} = 5.5V, C_L = 10pF		115		
		Power down, V_{DD} = 3.6V		0.5	2.5	
Power-Supply Rejection (Note 8)	PSR	Full-scale input, V_{DD} = 2.7V to 3.6V		±0.4	±4	mV
DIGITAL INPUTS ($\overline{SHDN}$, SCLK, and CONVST)						
Threshold Voltage High	V_{IH}	$V_{DD} \le 3.6V$			2	V
		V_{DD} > 3.6V			3	
Threshold Voltage Low	V_{IL}		0.8			V
Input Hysteresis	V_{HYST}			0.2		V
Input Current High	I_{IH}				±1	µA
Input Current Low	I_{IL}				±1	µA
Input Capacitance	C_{IN}			15		pF

ELECTRICAL CHARACTERISTICS—MAX1106 (continued)

(V_{DD} = +2.7V to +3.6V; IN- to GND; f_{SCLK} = 2MHz; 25ksps conversion rate; 1µF capacitor at REFOUT; external +2.048V reference at REFIN; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUT (DOUT)						
Output High Voltage	V_{OH}	I_{SOURCE} = 0.5mA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 16mA		0.8		
Three-State Leakage Current	I_L	Figure 6, DOUT High-Z		±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}	Figure 6, DOUT High-Z		15		pF
TIMING CHARACTERISTICS (Figures 6 and 7)						
Acquisition Time	t_{ACQ}		1			µs
CONVST Pulse Width High	t_{CSPW}		1			µs
CONVST Fall to Output Data Valid	t_{CONV}				35	µs
CONVST Rise to Output Enable	t_{DV}	Figure 1, C_{LOAD} = 100pF			240	ns
SCLK Fall to Output Data Valid	t_{DO}	Figure 1, C_{LOAD} = 100pF	20		200	ns
SCLK Pulse Width High	t_{CH}		200			ns
SCLK Pulse Width Low	t_{CL}		200			ns
SCLK Low to Output Disable	t_{TR}	Figure 2, C_{LOAD} = 100pF			240	ns
SCLK Low to CONVST Rise	t_{SCC}		100			ns
$\overline{SHDN}$ Fall to Output Disable	t_{SHDN}	Figure 2, C_{LOAD} = 100pF			240	ns
Wake-Up Time	t_{WAKE}	External reference		20		µs
		Internal reference (Note 9)		12		ms

ELECTRICAL CHARACTERISTICS—MAX1107

(V_{DD} = +4.5V to +5.5V; IN- = GND; f_{SCLK} = 2MHz; 25ksps conversion rate; 1µF capacitor at REFOUT; external +4.096V reference at REFIN; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			8			Bits
Relative Accuracy (Note 1)	INL			±0.15	±0.5	LSB
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error				±0.2	±1	LSB
Gain Error (Note 3)					±1	LSB
Gain Temperature Coefficient				±0.8		ppm/°C
Total Unadjusted Error	TUE	T_A = +25°C			±1	LSB
		T_A = T_{MIN} to T_{MAX}		±0.5		
DYNAMIC PERFORMANCE (10kHz sine-wave input, 4.096Vp-p, 25ksps conversion rate)						
Signal-to-Noise Plus Distortion	SINAD			49		dB
Total Harmonic Distortion (up to the 5th harmonic)	THD			-70		dB
Spurious-Free Dynamic Range	SFDR			68		dB
Small-Signal Bandwidth	BW_{-3dB}	-3dB rolloff		1.5		MHz
Full-Power Bandwidth				0.8		MHz
ANALOG INPUTS						
Input Voltage Range (Note 4)	$V_{IN_}$	V_{IN+} to V_{IN-}	0		V_{REFIN}	V
Input Leakage Current		On/off-leakage current, V_{IN+} or V_{IN-} = 0 or V_{DD}		±0.01	±1	µA
Input Capacitance	C_{IN}			18		pF
TRACK/HOLD						
Conversion Time	t_{CONV}	Figure 7			35	µs
Track/Hold Acquisition Time	t_{ACQ}		1			µs
Aperture Delay				10		ns
Aperture Jitter				<50		ps
Internal Clock Frequency				400		kHz
External Clock Frequency Range		For data transfer only			2	MHz
INTERNAL REFERENCE						
Output Voltage	V_{REFOUT}		3.936	4.096	4.256	V
REF Short-Circuit Current	I_{REFSC}			5		mA
REF Tempco				±50		ppm/°C
Load Regulation		0 to 0.5mA (Note 6)		4		mV
Capacitive Bypass at REFOUT			1			µF

ELECTRICAL CHARACTERISTICS—MAX1107 (continued)

(V_{DD} = +4.5V to +5.5V; IN- = GND; f_{SCLK} = 2MHz; 25ksps conversion rate; 1µF capacitor at REFOUT; external +4.096V reference at REFIN; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTERNAL REFERENCE						
Input Voltage Range	V_{REFIN}		1.0		V_{DD} + 0.05	V
Input Current		4.096V at REFIN, full scale		1	20	µA
POWER REQUIREMENTS						
Supply Voltage	V_{DD}		4.5	5	5.5	V
Supply Current (Notes 2, 7)	I_{DD}	V_{DD} = 5.5V, C_L = 10pF, full-scale input		115	250	µA
		Power down, V_{DD} = 4.5V to 5.5V		0.5	2.5	
Power-Supply Rejection (Note 8)	PSR	External reference = 4.096V, full-scale input, V_{DD} = 4.5V to 5.5V		±0.4	±4	mV
DIGITAL INPUTS ($\overline{SHDN}$, SCLK, and CONVST)						
Threshold Voltage High	V_{IH}				3	V
Threshold Voltage Low	V_{IL}		0.8			V
Input Hysteresis	V_{HYST}			0.2		V
Input Current High	I_{IH}				±1	µA
Input Current Low	I_{IL}				±1	µA
Input Capacitance	C_{IN}			15		pF
DIGITAL OUTPUT (DOUT)						
Output High Voltage	V_{OH}	I_{SOURCE} = 0.5mA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 16mA		0.8		
Three-State Leakage Current	I_L	Figure 6, DOUT High-Z		±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}	Figure 6, DOUT High-Z		15		pF
TIMING CHARACTERISTICS (Figures 6 and 7)						
Acquisition Time	t_{ACQ}		1			µs
CONVST Pulse Width High	t_{CSPW}		1			µs
CONVST Fall to Output Data Valid	t_{CONV}				35	µs
CONVST Rise to Output Enable	t_{DV}	Figure 1, C_{LOAD} = 100pF			240	ns
SCLK Fall to Output Data Valid	t_{DO}	Figure 1, C_{LOAD} = 100pF	20		200	ns
SCLK Pulse Width High	t_{CH}		200			ns

ELECTRICAL CHARACTERISTICS—MAX1107 (continued)

(V_{DD} = +4.5V to +5.5V; IN- = GND; f_{SCLK} = 2MHz; 25ksps conversion rate; 1µF capacitor at REFOUT; external +4.096V reference at REFIN; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

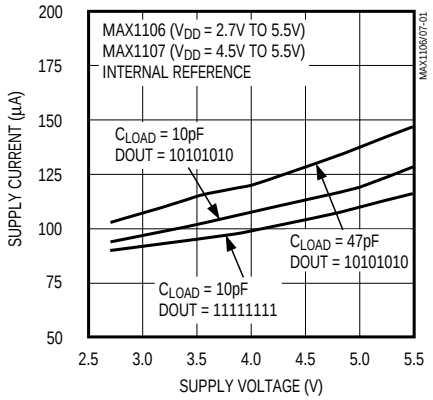
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Pulse Width Low	t_{CL}		200			ns
SCLK Low to Output Disable	t_{TR}	Figure 2, C_{LOAD} = 100pF			240	ns
SCLK Low to CONVST Rise	t_{SCC}		100			ns
$\overline{SHDN}$ Fall to Output Disable	t_{SHDN}	Figure 2, C_{LOAD} = 100pF			240	ns
Wake-Up Time	t_{WAKE}	External reference		20		µs
		Internal reference (Note 9)		12		ms

Note 1: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
Note 2: See *Typical Operating Characteristics*.
Note 3: V_{REFOUT} = +2.048V (MAX1106), V_{REFOUT} = +4.096V (MAX1107), offset nulled.
Note 4: Common-mode range (IN+, IN-) GND to V_{DD}.
Note 5: REFOUT supplies typically 2.5mA under normal operating conditions.
Note 6: External load should not change during the conversion for specified accuracy.
Note 7: Power consumption with CMOS levels.
Note 8: Measured as $|V_{FS}(2.7V) - V_{FS}(3.6V)|$ for MAX1106, and measured as $|V_{FS}(4.5V) - V_{FS}(5.5V)|$ for MAX1107.
Note 9: 1µF at REFOUT, internal reference settling to 0.5LSB.

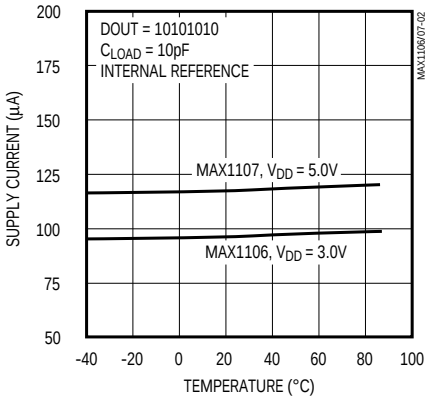
Typical Operating Characteristics

(V_{DD} = +3.0V (MAX1106), V_{DD} = +5.0V (MAX1107); f_{SCLK} = 2MHz; 25ksps conversion rate; external reference; 1µF at REFOUT; T_A = +25°C; unless otherwise noted.)

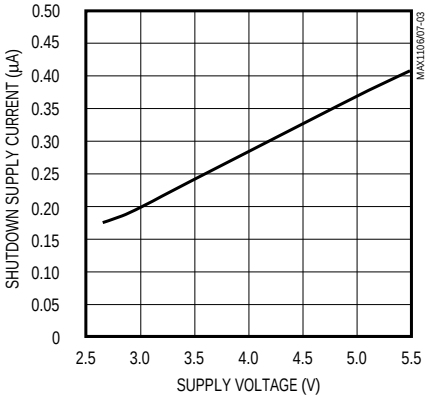
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



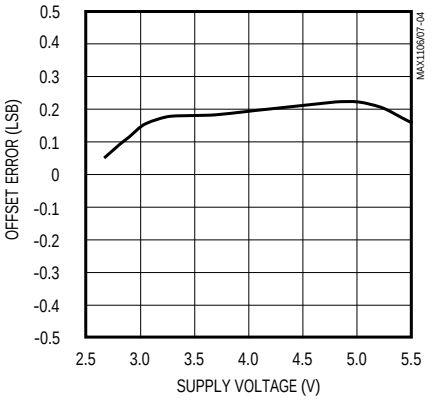
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



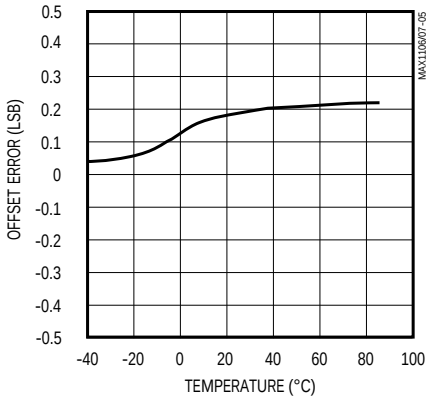
Typical Operating Characteristics (continued)

(V_{DD} = +3.0V (MAX1106), V_{DD} = +5.0V (MAX1107); f_{SCLK} = 2MHz; 25ksps conversion rate; external reference; 1µF at REFOUT; T_A = +25°C; unless otherwise noted.)

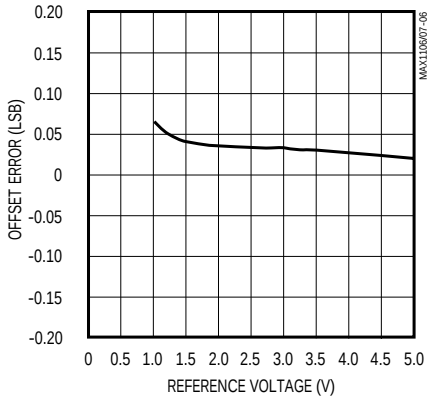
OFFSET ERROR vs. SUPPLY VOLTAGE



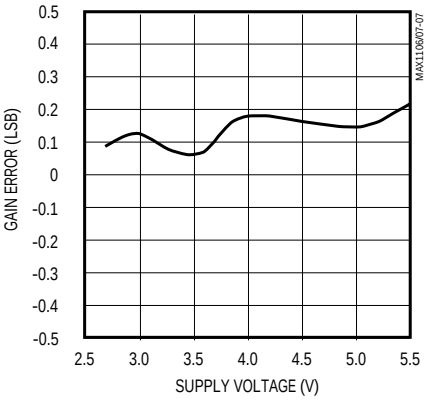
OFFSET ERROR vs. TEMPERATURE



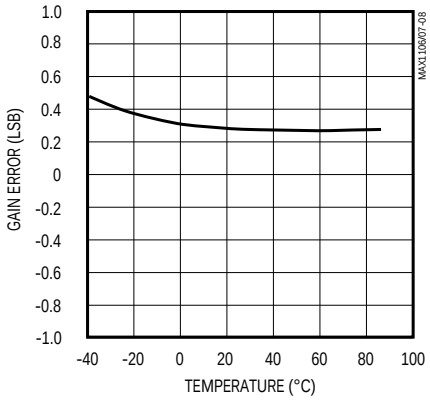
OFFSET ERROR vs. REFERENCE VOLTAGE



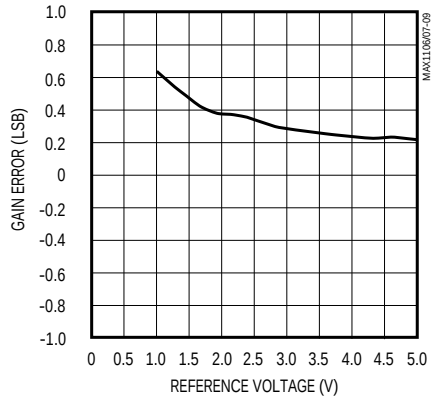
GAIN ERROR vs. SUPPLY VOLTAGE



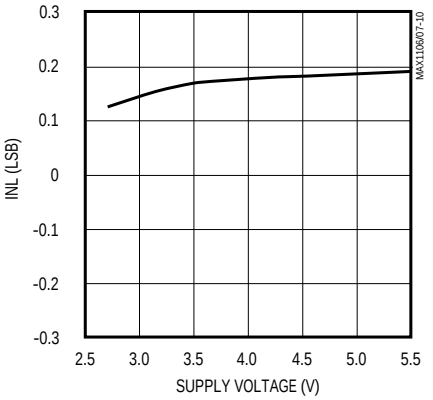
GAIN ERROR vs. TEMPERATURE



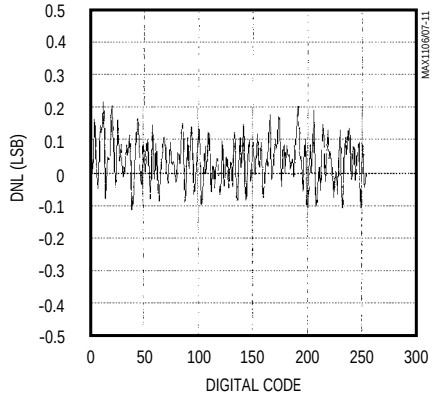
GAIN ERROR vs. REFERENCE VOLTAGE



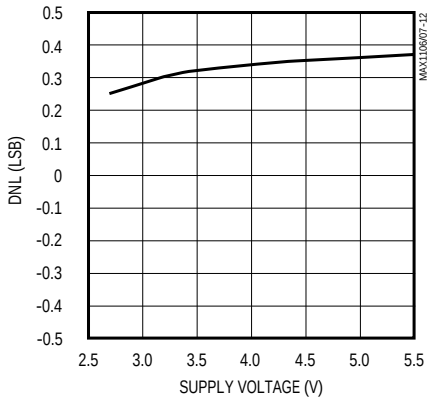
INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



DIFFERENTIAL NONLINEARITY vs. DIGITAL CODE



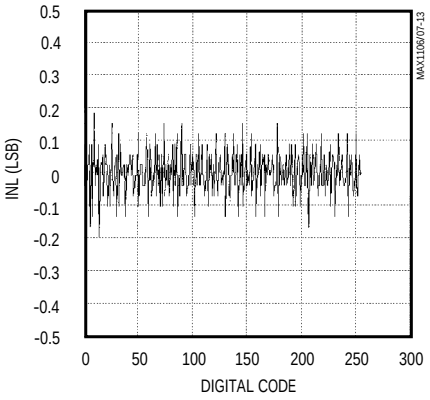
DIFFERENTIAL NONLINEARITY vs. SUPPLY VOLTAGE



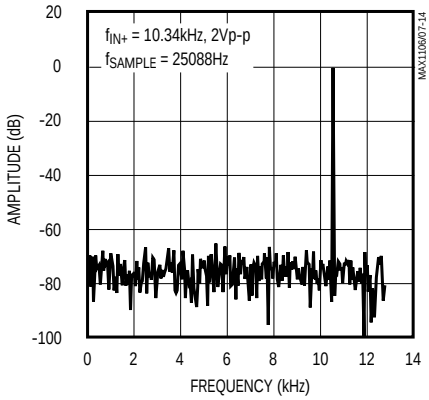
Typical Operating Characteristics (continued)

(V_{DD} = +3.0V (MAX1106), V_{DD} = +5.0V (MAX1107); f_{SCLK} = 2MHz; 25ksps conversion rate; external reference; 1µF at REFOUT; T_A = +25°C; unless otherwise noted.)

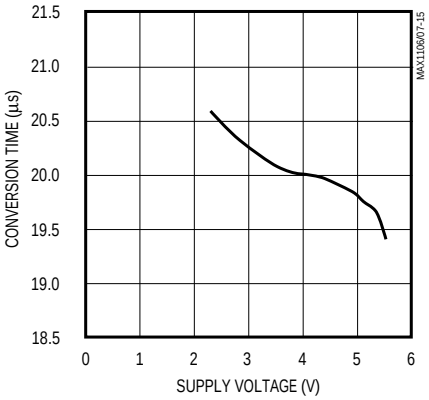
INTEGRAL NONLINEARITY vs. DIGITAL CODE



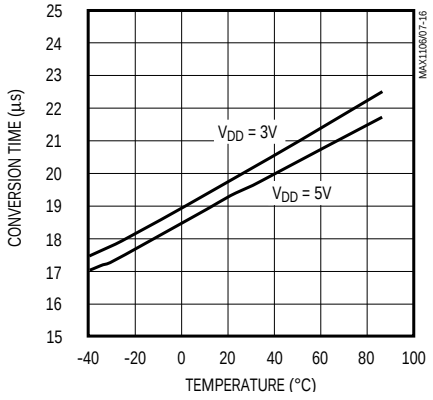
FFT PLOT



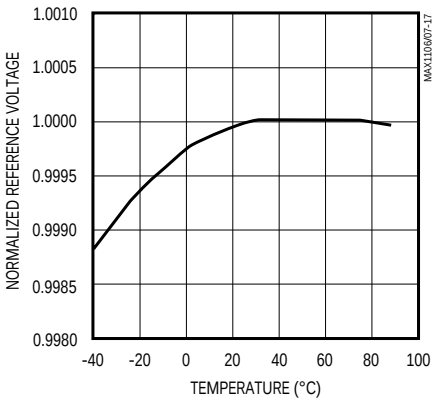
CONVERSION TIME vs. SUPPLY VOLTAGE



CONVERSION TIME vs. TEMPERATURE



NORMALIZED REFERENCE VOLTAGE vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Positive Supply Voltage
2	IN+	Positive Analog Input. Sampled. Input range from GND to V_{DD}.
3	IN-	Negative Analog Input. Input range from GND to V_{DD}.
4	GND	Ground.
5	REFOUT	Internal Reference Output. Bypass with 1µF to ground. 2.048V for MAX1106, 4.096V for MAX1107.
6	REFIN	Reference Voltage Input. Reference voltage for analog-to-digital conversion. Connect REFOUT to REFIN for internal reference. Input range from 1V to V_{DD}.
7	CONVST	Conversion Start Input. Toggle CONVST high for 1µs minimum and then low to start internal conversion. Data is not clocked out unless CONVST is low.
8	$\overline{SHDN}$	Active-Low Shutdown. Connect to V_{DD} for normal operation.
9	DOUT	Serial Data Output. Data is clocked out on the falling edge of SCLK. DOUT is high impedance in shutdown or after all data is clocked out.
10	SCLK	Serial Clock Input. Clocks data out of serial interface.

Single-Supply, Low-Power, Serial 8-Bit ADCs

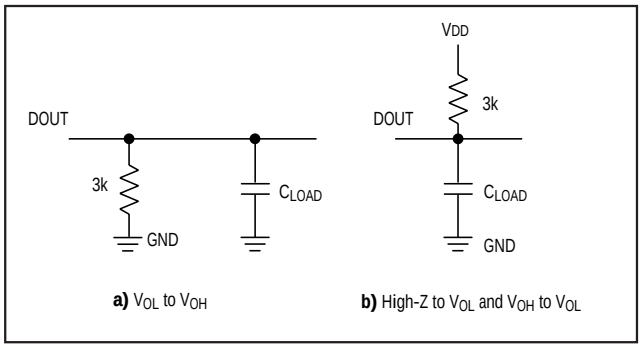


Figure 1. Load Circuits for Enable Time

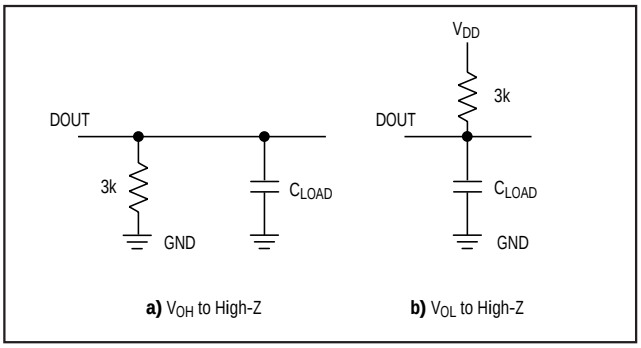


Figure 2. Load Circuits for Disable Time

Detailed Description

The MAX1106/MAX1107 analog-to-digital converters (ADCs) use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to an 8-bit digital output. A simple serial interface provides easy interface to microprocessors (µPs). No external hold capacitors are required. All of the MAX1106/MAX1107 operating modes are pin configurable: internal or external reference, single-ended or pseudo-differential unipolar conversion, and power down. Figure 3 shows the typical operating circuit.

Analog Inputs

Track/Hold

The input architecture of the ADCs is illustrated in Figure 4's equivalent-input circuit of and is composed of the T/H, the input multiplexer, the input comparator, the switched capacitor DAC, and the auto-zero rail.

The device is in acquisition mode most of the time. During the acquisition interval, the positive input (IN+) is tracked and is connected to the holding capacitor (C_{HOLD}). The acquisition interval ends with the falling edge of CONVST. At this point the T/H switch opens and C_{HOLD} is connected to the negative input (IN-), retaining charge on C_{HOLD} as a sample of the signal at IN+. Once conversion is complete the T/H returns immediately to its tracking mode.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be allowed between conversions. The acquisition time, t_{ACQ}, is the minimum time needed for the signal to be acquired. It is calculated by:

$$t_{ACQ} = 6(R_S + R_{IN})18pF$$

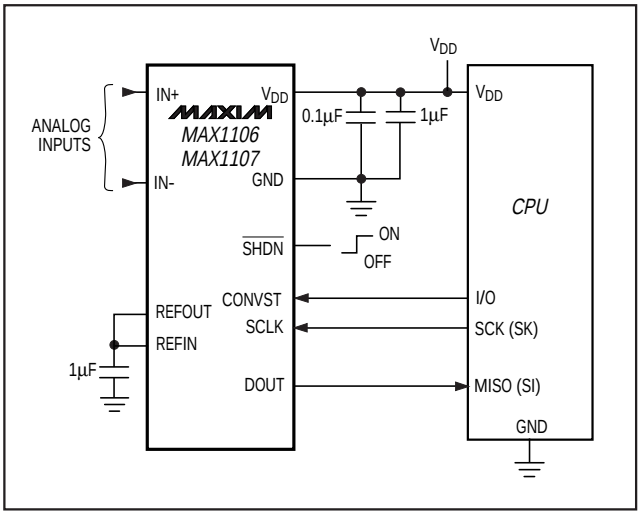


Figure 3. Typical Operating Circuit

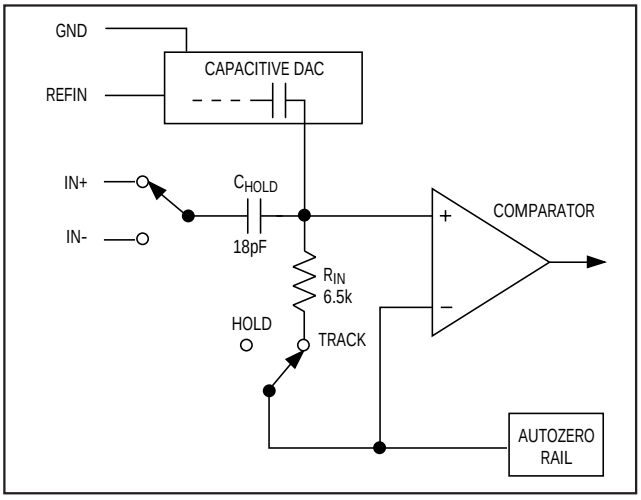


Figure 4. Equivalent Input Circuit

where R_{IN} = 6.5kΩ, R_S = the source impedance of the input signal, and t_{ACQ} must never be less than 1µs. This is easily achieved by respecting the minimum CONVST high interval required and the time required to clock the data out.

Pseudo-Differential Input

The MAX1106/MAX1107 input configuration is pseudo-differential to the extent that only the signal at the sampled input (IN+) is stored in the holding capacitor (C_{HOLD}). IN- must remain stable within ±0.5LSB (±0.1LSB for best results) in relation to GND during a conversion.

If a varying signal is applied at the IN- input, its amplitude and frequency need to be limited. The following equations determine the relationship between the maximum signal amplitude and its frequency to maintain ±0.5LSB accuracy:

Assuming a sinusoidal signal at the IN- input,

$$\upsilon_{IN-} = \left(V_{IN-}\right) \sin(2\pi ft)$$

under the maximum voltage variation is determined by

$$\max\frac{\Delta\upsilon_{IN-}}{\Delta t} = 2\pi f\left(V_{IN-}\right) \le \frac{1\ LSB}{t_{CONV}} = \frac{V_{REFIN}}{2^8 t_{CONV}}$$

a 60Hz signal at IN- with an amplitude of 1.2V will generate ±0.5LSB of error. This is with a 35µs conversion time (maximum t_{CONV}) and a reference voltage of 4.096V. When a DC reference voltage is used at IN-, connect a 0.1µF capacitor from IN_ to GND to minimize noise at the input.

The common-mode input range of IN+ and IN- is GND to +V_{DD}. Full-scale is achieved when (V_{IN-} - V_{IN+}) = V_{REFIN}. V_{IN+} must be higher than V_{IN-}.

Conversion Process

The comparator negative input is connected to the auto-zero rail. Since the device requires only a single supply, the ZERO node at the input of the comparator equals V_{DD}/2. The capacitive DAC restores node ZERO to have 0V difference at the comparator inputs within the limits of 8-bit resolution. This action is equivalent to transferring a charge of 18pF(V_{IN+} - V_{IN-}) from C_{HOLD} to the binary-weighted capacitive DAC which, in turn, forms a digital representation of the analog-input signal.

Input Voltage Range

Internal protection diodes that clamp the analog input to V_{DD} and GND allow the input pins (IN+ and IN-) to swing from (GND - 0.3V) to (V_{DD} + 0.3V) without damage. However, for accurate conversions, the inputs must not exceed (V_{DD} + 50mV) or be less than (GND - 50mV).

The MAX1106/MAX1107 input range is from GND to V_{DD}. The output code is invalid (code zero) when a negative input voltage (or a negative differential input voltage) is applied. The reference input-voltage range at REFIN is from 1V to (V_{DD} + 50mV).

Input Bandwidth

The ADC's input tracking circuitry has a 1.5MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Serial Interface

The MAX1106/MAX1107 have a 3-wire serial interface. The CONVST and SCLK inputs are used to control the device, while the three-state DOUT pin is used to access the result of conversion.

The serial interface provides easy connection to microcontrollers with SPI, QSPI, and MICROWIRE serial interfaces at clock rates up to 2MHz. For SPI and QSPI, set CPOL = CPHA = 0 in the SPI control registers of the microcontroller. Figure 5 shows the MAX1106/MAX1107 common serial-interface connections.

Digital Inputs and Outputs

The logic levels of the MAX1106/MAX1107 digital inputs are set to accept voltage levels from both 3V and 5V systems regardless of the supply voltages.

A conversion is started by toggling CONVST. CONVST idles low and needs to be set high for at least 1µs to perform the autozero adjustment. CONVST must remain low during conversion and until the result of conversion has been clocked out.

After CONVST is set low, allow 35µs for the conversion to be completed. While the internal conversion is in progress DOUT is low. Conversion is controlled by an internal 400kHz oscillator. The MSB is present at the DOUT pin immediately after conversion is completed. The conversion result is clocked out at the DOUT pin and is coded in straight binary (Figure 9). Data is clocked out at SCLK's falling edge in MSB-first format at rates up to 2MHz. Once all data bits are clocked out, DOUT goes high impedance at the falling edge of the eighth SCLK pulse.

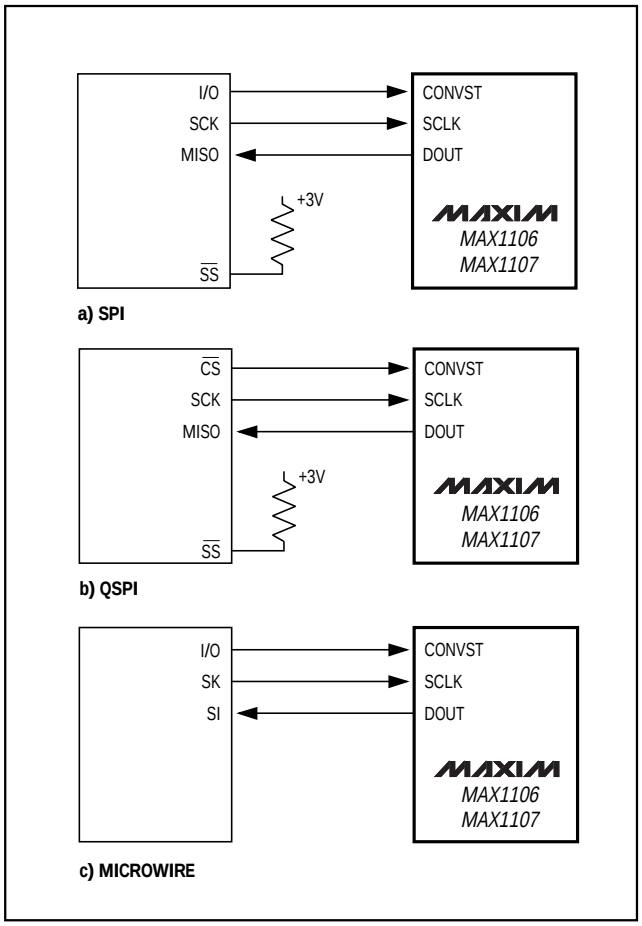


Figure 5. Common Serial-Interface Connections

Starting SCLK before conversion is complete corrupts the conversion in progress, and the data clocked out at DOUT does not represent the input signal. Bringing CONVST high at anytime during a conversion or while the data is clocked out will result in an incorrect conversion. A new conversion can be restarted only if all eight data bits of conversion have been clocked out. Toggle CONVST after all data is clocked out to restart a new conversion.

$\overline{SHDN}$ is used to place the MAX1106/MAX1107 in low-power mode (see *Power-Down* section). In this mode DOUT is high impedance and any conversion in progress is stopped immediately. If a conversion is stopped by $\overline{SHDN}$ going low, the device must be reset by waiting 35µs and clearing the output register with eight SCLKs before the next conversion.

How to Perform a Conversion

The MAX1106/MAX1107 converts an input signal using the internal clock. This frees the µP from the burden of running the SAR conversion clock, and allows the conversion results to be read back at the µP's convenience at any clock rate up to 2MHz.

Figures 6 and 7 show the serial interface timing characteristics. CONVST idles low. Toggle CONVST high for at least 1µs to perform the autozero adjustment. After CONVST goes low, conversion starts immediately. Allow 35µs for the internal conversion to complete and issue the MSB of the conversion at DOUT. CONVST needs to be held low once a conversion is started, while SCLK should remain low during conversion for best noise performance. An internal register stores data when the conversion is in progress. SCLK clocks the

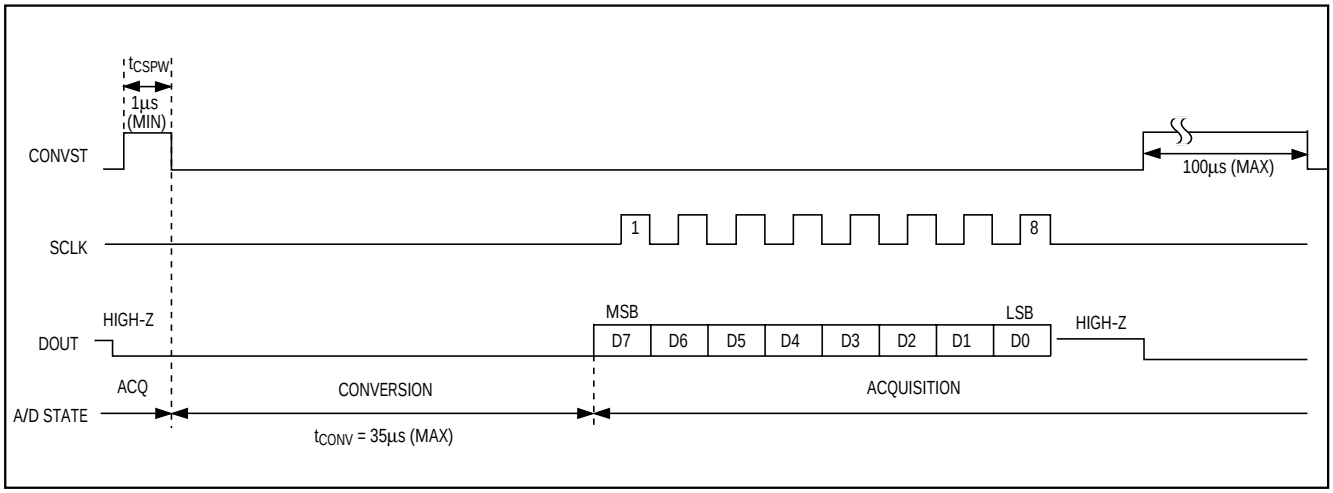


Figure 6. Conversion Timing Diagram

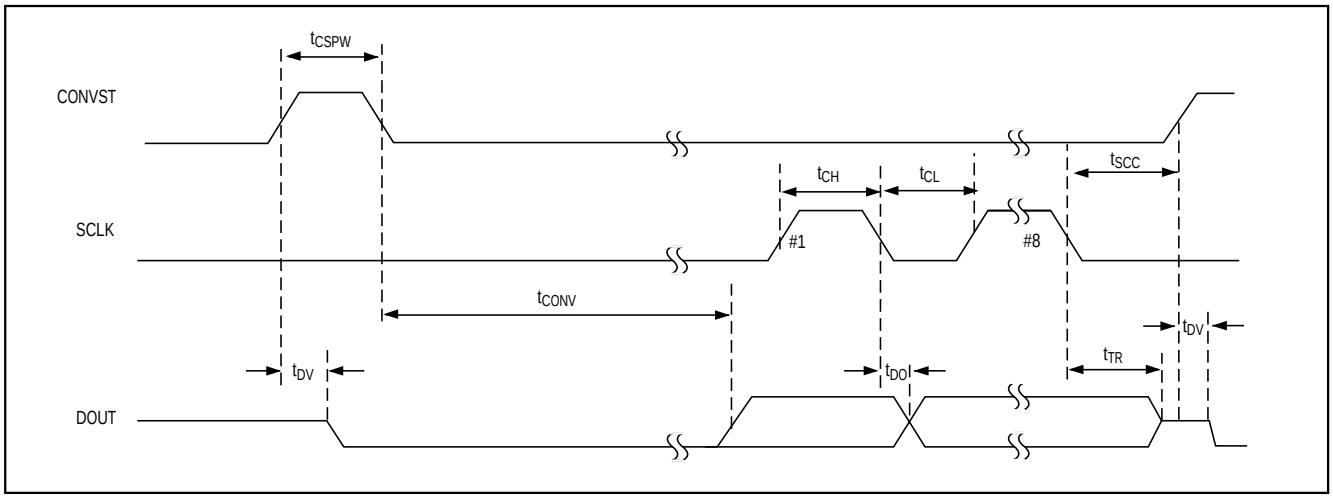


Figure 7. Detailed Serial Interface Timing

data out of this register at any time after the conversion is complete. After the eighth data-bit has clocked out, DOUT goes high impedance and remains so with additional SCLKs.

Normally leave CONVST low until a new conversion needs to be started. CONVST should be high for a maximum of 100µs to maintain the 8-bit accuracy of the Autozero Circuit.

The acquisition time, t_{ACQ}, starts immediately after the end of conversion and a new conversion can be started immediately after all data has been clocked out by toggling CONVST high. Figure 8 shows a timing diagram for a conversion at the data rate of 40ksps. Typically 20µs are necessary for the conversion to complete, 4µs for reading the eight bits of data with a serial clock of 2MHz, and 1µs to complete the zero rail adjustment and acquisition. The conversion time is guaranteed to be less than 35µs, therefore the data rate should be limited to 25ksps unless the conversion time for the specific condition is known. Conversion time can be determined by measuring the time between CONVST falling edge and DOUT rising edge with a full-scale input voltage.

Applications Information

Power-On Reset

When power is first applied with $\overline{SHDN}$ high or connected to V_{DD}, the MAX1106/MAX1107 is in track mode. Conversion can be started by toggling CONVST high to low as soon as the reference is settled when using the internal reference, or after 20µs when an external reference is used. Powering up the MAX1106/MAX1107 with

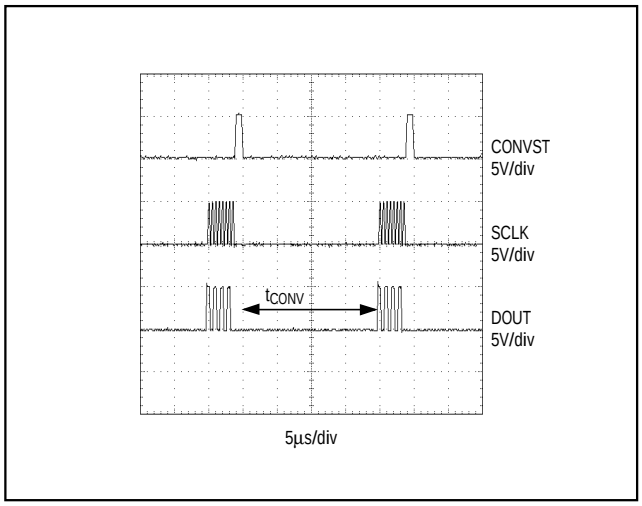


Figure 8. 40ksps Timing Diagram

CONVST low will not start a conversion. No conversions should be performed until the reference voltage (internal or external) has stabilized.

Shutdown Operation

Pulling $\overline{SHDN}$ low places the converter in low-current power-down mode. In this state the converter draws typically 0.5µA. In shutdown the analog biasing circuit and the internal bandgap reference are powered down, and DOUT goes high impedance.

The conversion stops coincidentally with $\overline{SHDN}$ going low. If shutdown occurs during a conversion, power up, wait 35µs, and clock SCLK eight times.

When operating at speeds below the maximum sampling rate, the MAX1106/MAX1107's power-down mode can save considerable power by placing the converter in a low-current shutdown state between conversions. Pull $\overline{SHDN}$ low after the conversion byte has been read to shut down the device completely.

CONVST should remain low most of the time and toggled high for 1µs (100µs max) for the autozero adjustment. An external reference is recommended for best accuracy when using the shutdown feature. This requires only 20µs for the internal biasing circuit to stabilize before starting a new conversion. Alternatively, the internal reference can be used, but additional time is required for the reference to stabilize (when bypassed by a 1µF capacitor; at data rates above 1ksps, the reference stabilizes within 1LSB in 200µs). If the reference is completely discharged it requires 12ms to settle. No conversions should be performed until the reference voltage has stabilized.

Internal or External Voltage Reference

An external reference between 1V and V_{DD} should be connected directly at the REFIN pin. To use the internal reference, connect REFOUT directly to REFIN and bypass REFOUT with a 1µF capacitor. The DC input impedance at REFIN is extremely high, consisting of leakage current only (typically 10nA). During a conversion, the reference must be able to deliver up to 20µA average load current and have an output impedance of 1kΩ or less at the conversion clock frequency. If the reference has higher output impedance or is noisy, bypass it close to the REFIN pin with a 0.1µF capacitor. The internal reference is active as long as $\overline{SHDN}$ is high and powers down when $\overline{SHDN}$ is low.

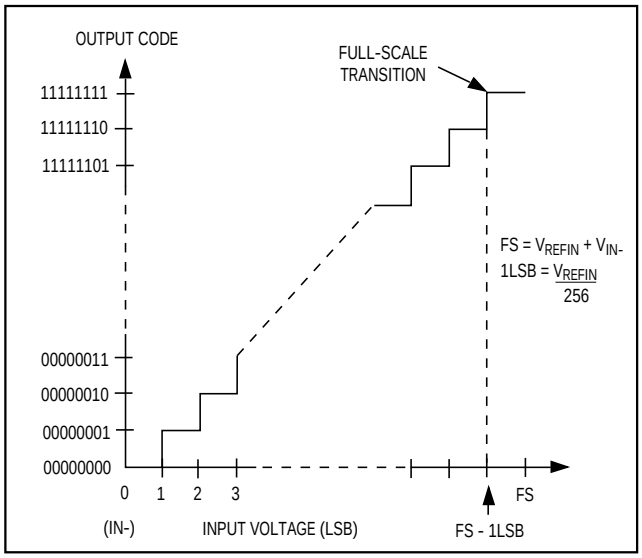


Figure 9. Input/Output Transfer Function

Transfer Function

Figure 9 depicts the input/output transfer function. Code transitions occur at integer LSB values. Output coding is binary; with a 2.048V reference 1LSB = 8mV (V_{REFIN} / 256). For single-ended operation connect IN- to GND. Full-scale is achieved at $V_{IN+} = V_{REFIN} - 1LSB$. For pseudo-differential operation the V_{IN-} voltage range is from GND to V_{DD}, where full-scale is achieved at $V_{IN+} = V_{REFIN} + V_{IN-} - 1LSB$. V_{IN+} should not be higher than V_{DD} + 50mV. Negative input voltages are invalid and give a zero output code. Voltages greater than full-scale give an all ones output code.

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another or run digital lines underneath the ADC package.

Figure 10 shows the recommended system-ground connections. A single-point analog ground (star-ground point) should be established at the A/D ground. Connect all analog grounds to the star ground. No digital-system ground should be connected to this point. The ground return to the power supply for the star ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the comparator in the ADC. Bypass the supply to the star ground with 0.1µF and 1µF capacitors close to the V_{DD} pin of the MAX1106/MAX1107. Minimize capacitor lead lengths for best supply-noise rejection. If the power supply is very noisy, a 10Ω resistor can be connected to form a lowpass filter.

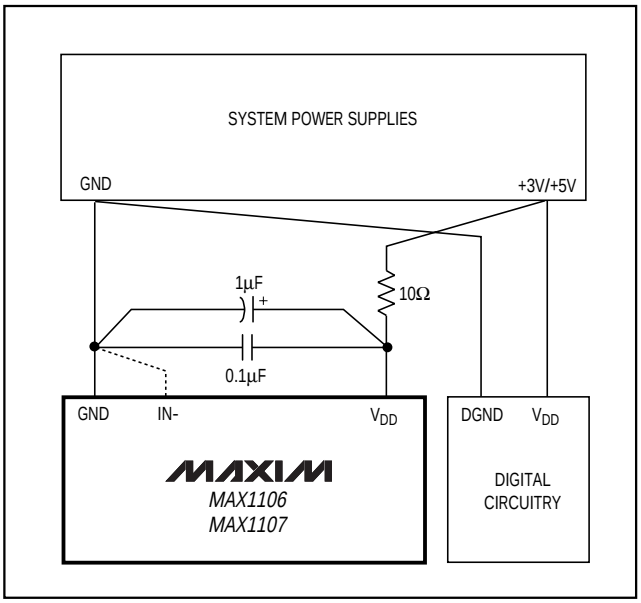


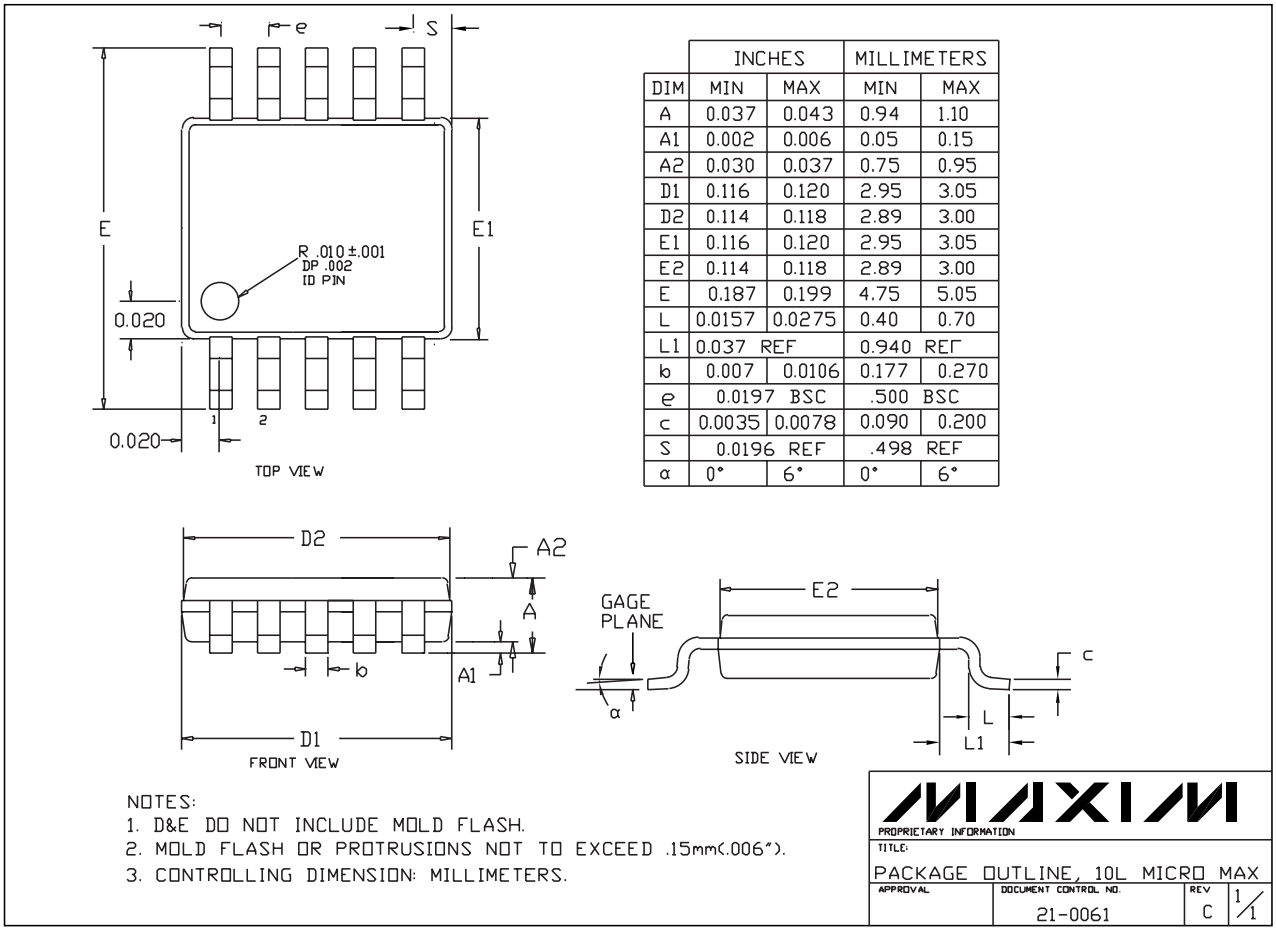
Figure 10. Power-Supply Connections

Chip Information

TRANSISTOR COUNT: 2373

Single-Supply, Low-Power, Serial 8-Bit ADCs

Package Information



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.037	0.043	0.94	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
E	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		.498 REF	
α	0°	6°	0°	6°

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