MAX120/MAX122

500ksps, 12-Bit ADCs with Track/Hold and Reference

General Description

The MAX120/MAX122 complete, BiCMOS, sampling 12-bit analog-to-digital converters (ADCs) combine an on-chip track/hold (T/H) and a low-drift voltage reference with fast conversion speeds and low-power consumption. The T/H's 350ns acquisition time combined with the MAX120's 1.6µs conversion time results in throughput rates as high as 500k samples per second (ksps). Throughput rates of 333ksps are possible with the 2.6µs conversion time of the MAX122.

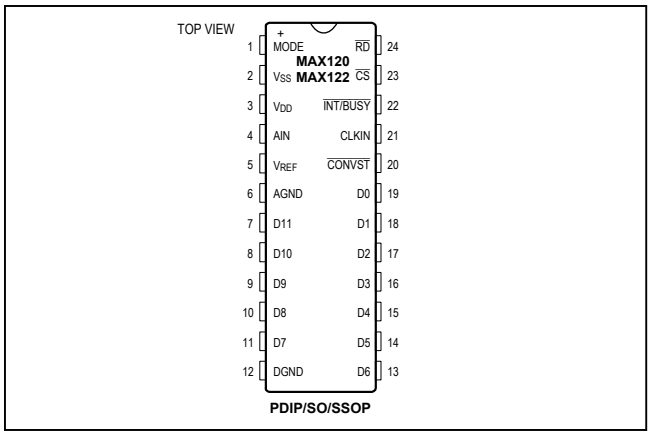
The MAX120/MAX122 accept analog input voltages from -5V to +5V. The only external components needed are decoupling capacitors for the power-supply and reference voltages. The MAX120 operates with clocks in the 0.1MHz to 8MHz frequency range. The MAX122 accepts 0.1MHz to 5MHz clock frequencies.

The MAX120/MAX122 employ a standard microprocessor (µP) interface. Three-state data outputs are configured to operate with 12-bit data buses. Data-access and bus-release timing specifications are compatible with most popular µPs without resorting to wait states. In addition, the MAX120/MAX122 can interface directly to a first-in, first-out (FIFO) buffer, virtually eliminating µP interrupt overhead. All logic inputs and outputs are TTL/CMOS compatible. For applications requiring a serial interface, refer to the MAX121.

Applications

- Digital-Signal Processing
- Audio and Telecom Processing
- Speech Recognition and Synthesis
- High-Speed Data Acquisition
- Spectrum Analysis
- Data Logging Systems

Pin Configuration



PDIP/SO/SSOP

Features

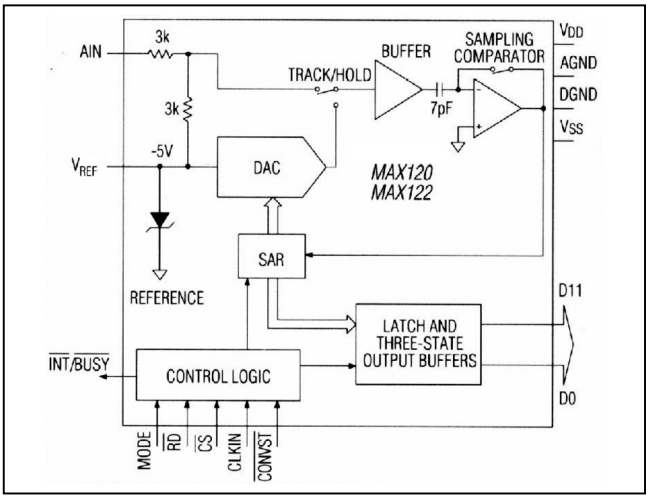
- 12-Bit Resolution
- No Missing Codes Over Temperature
- 20ppm/°C -5V Internal Reference
- 1.6µs Conversion Time/500ksps Throughput (MAX120)
- 2.6µs Conversion Time/333ksps Throughput (MAX122)
- Low Noise and Distortion:
  - 70dB (min) SINAD
  - -77dB (max) THD (MAX122)
- Low Power Dissipation: 210mW
- Separate Track/Hold Control Input
- Continuous-Conversion Mode Available
- ±5V Input Range, Overvoltage Tolerant to ±15V
- 24-Pin Narrow DIP, Wide SO, and SSOP Packages

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	INL (LSB)
MAX120CNG+	0°C to +70°C	24 PDIP	±1
MAX120CWG+	0°C to +70°C	24 Wide SO	±1
MAX120CAG+	0°C to +70°C	24 SSOP	±1
MAX120ENG+	-40°C to +85°C	24 PDIP	±1
MAX120EWG+	-40°C to +85°C	24 Wide SO	±1

+Denotes a lead(Pb)-free/RoHS-compliant package.

Functional Diagram



maxim integrated™

Absolute Maximum Ratings

V_{DD} to DGND .....-0.3V to +6V
V_{SS} to DGND .....+0.3V to -17V
AIN to AGND .....±15V
AGND to DGND .....±0.3V
Digital Inputs/Outputs to DGND .....-0.3V to (V + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Narrow PDIP (derate 13.33mW/°C above +70°C) 1067mW
SO (derate 11.76mW/°C above +70°C) 941mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
Narrow CDIP (derate 12.50mW/°C above +70°C) 1000mW
Operating Temperature Ranges
MAX12_C .....0°C to +70°C
MAX12_E_ ..... -40°C to +85°C
MAX12_MRG ..... -55°C to +125°C
Storage Temperature Range .....-65°C to+160°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{DD} = +4.75V to +5.25V, V_{SS} = -10.8V to -15.75V, f_{CLK} = 8MHz for MAX120 and 5MHz for MAX122, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution	RES			12			Bits
Differential Nonlinearity (Note 1)	DNL	12-bit no missing codes over temperature range	MAX122AC/AE			±3/4	LSB
			MAX120C/E, MAX122BC/BE			±1	
		11-bit no missing codes over temperature range	MAX120M			±2	
Integral Nonlinearity (Note 1)	INL		MAX122AC/AE			±3/4	LSB
			MAX120C/E, MAX122BC/BE			±1	
Bipolar Zero Error (Note 1)		Code 00..00 to 00..01 transition, near V_{AIN} = 0V				±3	LSB
		Temperature drift			±0.005		LSB/"C
Full-Scale Error (Notes 1, 2)		Including reference; adjusted for bipolar zero error; T_A = +25°C				±8	LSB
Full-Scale Temperature Drift		Excluding reference			±1		ppm/"C
Power-Supply Rejection Ratio (Change in FS) (Note 3)	PSRR	V_{DD} only, 5V ±5%			±1/4	±3/4	LSB
		V_{SS} only, -12V ±10%			±1/4	±1	
		V_{SS} only, -15V ±5%			±1/4	±1	
ANALOG INPUT							
Input Range				-5		+5	V
Input Current		V_{AIN} = +5V (approximately 6kΩ to REF)				2.5	mA
Input Capacitance (Note 4)						10	pF
Full-Power Input Bandwidth					1.5		MHz
REFERENCE							
Output Voltage		No external load, V_{AIN} = 5V, T_A = +25°C		-5 02		-4.98	V
External Load Regulation		0mA < I_{SINK} < 5mA, V_{AIN} = 0V				5	mV
Temperature Drift (Note 5)		MAX12_C/E				±25	ppm/°C

Electrical Characteristics (continued)

(V_{DD} = +4.75V to +5.25V, V_{SS} = -10.8V to -15.75V, f_{CLK} = 8MHz for MAX120 and 5MHz for MAX122, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (MAX120: f_S = 500kHz, V_{AIN} = ±5V_{P-P}, 100kHz: MAX122: f_S = 333kHz, V_{AIN} = ±5V_{P-P}, 50kHz							
Signal-to-Noise Plus Distortion	SINAD	T_A = +25°C	MAX120, MAX122	70	72		dB
			MAX122AC/AE	70			
			MAX122BC/BE	69			
Total Harmonic Distortion (First Five Harmonics)	THD	T_A = +25°C	MAX120		-82	-77	dB
			MAX122		-85	-78	
			MAX122AC/AE			-77	
			MAX122BC/BE			-75	
Spurious-Free Dynamic Range	SFDR	T_A = +25°C	MAX120	77	82		dB
			MAX122	78	85		
			MAX122AC/AE	77			
			MAX122BC/BE	75			
CONVERSION TIME							
Synchronous	t_{CONV}	$13t_{CLK}$	MAX120			1.63	µs
			MAX122			2.60	
Clock Frequency	f_{CLK}		MAX120	0.1		8	MHz
			MAX122	0.1		5	
DIGITAL INPUTS (CLKIN, $\overline{CONVST}$, $\overline{RD}$, $\overline{CS}$)							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Capacitance (Note 4)						10	pF
Input Current		V_{IN} = 0V or V_{DD}				±5	µA
DIGITAL OUTPUTS ($\overline{INT}$/$\overline{BUSY}$, D11–D0)							
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 1mA		V_{DD} - 0.5			V
Leakage Current	I_{LKG}	V_{IN} = 0V or V_{DD}, D11–D0				±5	µA
Output Capacitance (Note 4)						10	pF
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}	Guaranteed by supply rejection test		4.75		5.25	V
Negative Supply Voltage	V_{SS}	Guaranteed by supply rejection test		-10.80		-15.75	V
Positive Supply Current (Note 6)	I_{DD}	V_{DD} = 5.25V, V_{SS} = -15.75V, V_{AIN} = 0V			9	15	mA
Negative Supply Current (Note 6)	I_{SS}	V_{DD} = 5.25V, V_{SS} = -15.75V, V_{AIN} = 0V			14	20	mA
Power Dissipation (Note 6)		V_{DD} = 5V, V_{SS} = -12V, V_{AIN} = 0V			210	315	mW

Timing Characteristics

(V_{DD} = +5V, V_{SS} = -12V to -15V, 100% tested, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 7)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			MAX12_C/E			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{CS}		0			0			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{CH}		0			0			ns
$\overline{CONVST}$ Pulse Width	t_{CW}		30			30			ns
$\overline{RD}$ Pulse Width	t_{RW}		t_{DA}			t_{DA}			ns
Data-Access Time	t_{DA}	C_L = 100pF		40	75			100	ns
Bus-Relinquish Time	t_{DH}			30	50			65	ns
$\overline{RD}$ or $\overline{CONVST}$ to $\overline{BUSY}$	t_{B0}	C_L = 50pF		30	75			100	ns
CLKIN to $\overline{BUSY}$ or $\overline{INT}$	t_{B1}	C_L = 50pF		70	110			150	ns
CLKIN to $\overline{BUSY}$ Low	t_{B2}	In mode 5		45	90			120	ns
$\overline{RD}$ to $\overline{INT}$ High	t_{IH}	C_L = 50pF		30	50			75	ns
$\overline{BUSY}$ or $\overline{INT}$ to Data Valid	t_{BD}	C_L (Data) = 100pF, C_L ($\overline{INT}$, $\overline{BUSY}$) = 50pF			20			30	ns
Acquisition Time (Note 8)	t_{ACQ}		350			350			ns
Aperture Delay (Note 8)	t_{AP}			10					ns
Aperture Jitter (Note 8)				30					ps

Note 1: These tests are performed at V_{DD} = 5V, V_{SS} = -15V. Operation over supply is guaranteed by supply rejection tests.

Note 2: Ideal full-scale transition is at +5V - 3/2 LSB = +4.9963V, adjusted for offset error.

Note 3: Supply rejection defined as change in full-scale transition voltage with the specified change in supply voltage = (FS at nominal supply)- (FS at nominal supply ± tolerance), expressed in LSBs.

Note 4: For design guidance only, not tested.

Note 5: Temperature drift is defined as the change in output voltage from +25°C to T_{MIN} or T_{MAX}. It is calculated as $T_C = \Delta V_{REF}/V_{REF}/(\Delta T)$.

Note 6: $V_{\overline{CS}} = V_{\overline{RD}} = V_{\overline{CONVST}}$ = 0V, V_{MODE} = 5V.

Note 7: Control inputs specified with $t_r = t_f$ = 5ns (10% to 90% of +5V) and timed from a 1.6V voltage level. Output delays are measured to +0.8V if going low, or +2.4V if going high. For bus-relinquish time, a change of 0.5V is measured. See Figures 1 and 2 for load circuits.

Note 8: For design guidance only, not tested.

Pin Description

PIN	NAME	FUNCTION
1	MODE	Mode Input. Hardwire to set operational mode. V_{DD}: Single conversion, $\overline{INT}$ Output OPEN: Single conversion, $\overline{BUSY}$ Output DGND: Continuous conversions, $\overline{BUSY}$ Output
2	V_{SS}	Negative Power Supply, -12V or -15V
3	V_{DD}	Positive Power Supply, +5V
4	AIN	Sampling Analog Input, ±5V bipolar input range
5	V_{REF}	-5V Reference Output. Bypass to AGND with 22µF || 0.1µF.

Pin Description (continued)

PIN	NAME	FUNCTION
6	AGND	Analog Ground
7–11, 13–19	D11–D0	Three-State Data Outputs D11 (MSB) to D0 (LSB)
12	DGND	Digital Ground
20	$\overline{\text{CONVST}}$	Convert Start Input. Initiates conversions on its falling edge.
21	CLKIN	Clock Input. Drive with TTL-compatible clock from 0.1MHz to 8MHz (MAX120), 0.1MHz to 5MHz (MAX122)
22	$\overline{\text{INT}}$/$\overline{\text{BUSY}}$	Interrupt or Busy Output. Indicates converter status. If MODE is connected to V_{DD}, configure for an $\overline{\text{INT}}$ output. If MODE is open or connected to DGND, configure for a $\overline{\text{BUSY}}$ output. See operational diagrams.
23	$\overline{\text{CS}}$	Chip-Select Input, Active-Low. When $\overline{\text{RD}}$ is low, enables the three-state outputs. If $\overline{\text{CONVST}}$ and $\overline{\text{RD}}$ are low, a conversion is initiated on the falling edge of $\overline{\text{CS}}$.
24	$\overline{\text{RD}}$	Read Input, Active-Low. When $\overline{\text{CS}}$ is low, $\overline{\text{RD}}$ enables the three-state outputs. If $\overline{\text{CONVST}}$ and $\overline{\text{CS}}$ are low, conversion is initiated on the falling egde of $\overline{\text{RD}}$.

Detailed Description

ADC Operation

The MAX120/MAX122 use successive approximation and input T/H circuitry to convert an analog signal to a series of 12-bit digital-output codes. The control logic interfaces easily to most µPs, requiring only a few passive components tor most applications. The T/H does not require an external capacitor. Figure 3 shows the MAX120/MAX122 in the simplest operational configuration.

Analog Input Track/Hold

Figure 4 shows the equivalent input circuit, illustrating the sampling architecture of the ADC's analog comparator. An internal buffer charges the hold capacitor to minimize the required acquisition time between conversions. The analog input appears as a 6kΩ resistor in parallel with a 10pF capacitor.

Between conversions, the buffer input is connected to AIN through the input resistance. When a conversion starts, the buffer input disconnects from AIN, thus sampling the input. At the end of the conversion, the buffer input reconnects to AIN, and the hold capacitor once again charges to the input voltage.

The T/H is in tracking mode whenever a conversion is NOT in progress. Hold mode starts approximately 10ns after a conversion is initiated. Variation in this delay from one conversion to the next (aperture jitter) is typically 30ps. Figures 7 through 11 detail the T/H mode and interface timing for the various interface modes.

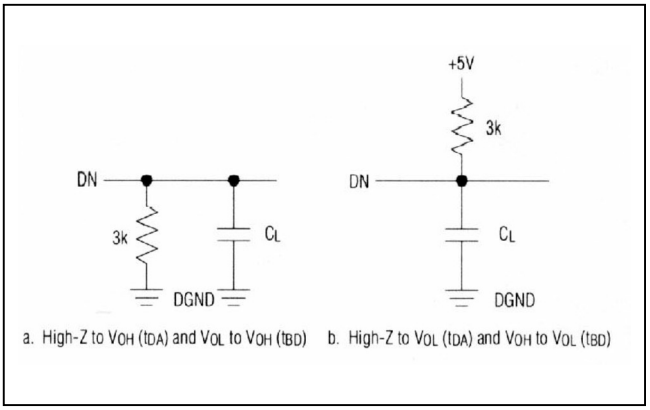


Figure 1. Load Circuits for Access Time

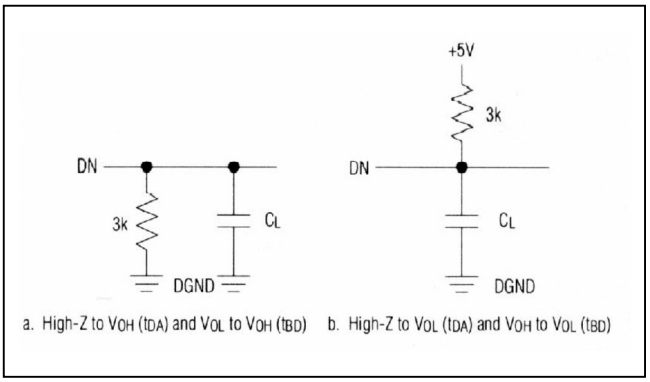


Figure 2. Load Circuits for Bus-Relinquish Time

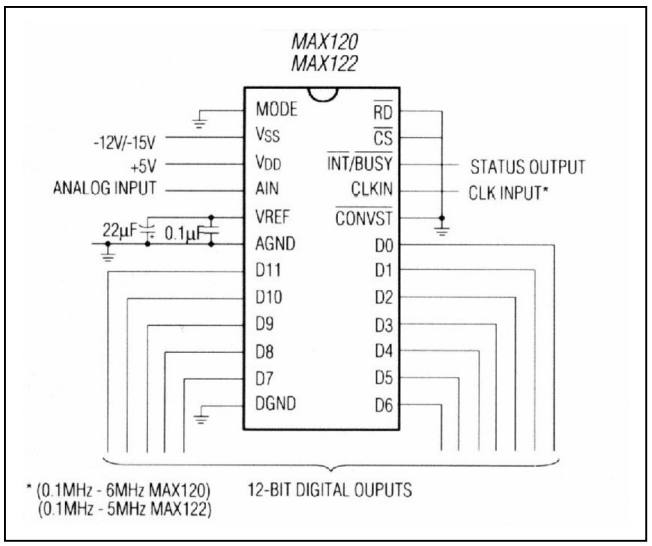


Figure 3. MAX120/MAX122 in the Simplest Operational Mode (Continuous Conversion)

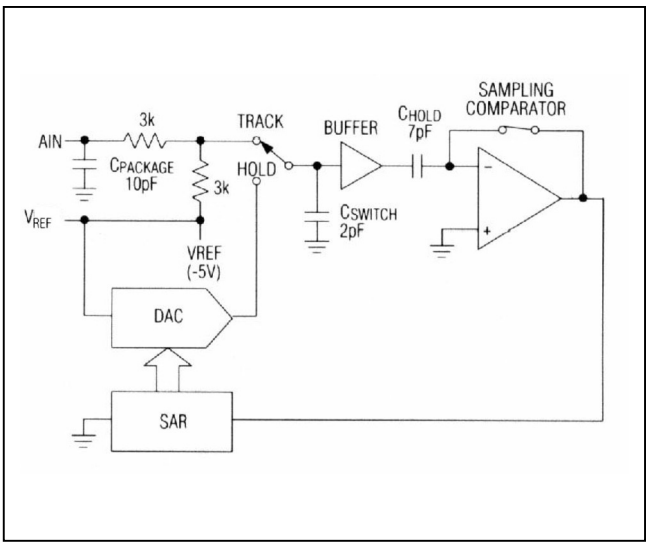


Figure 4. Equivalent Input Circuit

Internal Reference

The MAX120/MAX122 -5.00V buried-zener reference biases the internal DAC. The reference output is available at the V_{REF} pin and must be bypassed to the AGND pin with a 0.1µF ceramic capacitor in parallel with a 22µF or greater electrolytic capacitor. The electrolytic capacitor's equivalent series resistance (ESR) must be 100mΩ or less to properly compensate the reference output buffer. Sanyo's organic semiconductor works well.

Sanyo Video Components (USA)
Phone: (619) 661-6835 FAX: (619) 661-1055

Sanyo Electric Company, LTD. (Japan)
Phone: 0720-70-1005 FAX: 0720-70-1174

Sanyo Fisher Vertriebs GmbH (Germany)
Phone: 06102-27041, ext. 44 FAX: 06102-27045

Proper bypassing minimizes reference noise and maintains a low impedance at high frequencies. The internal reference output buffer can sink up to a 5mA external load.

An external reference voltage can be used to overdrive the MAX120/MAX122's internal reference if it ranges from -5.05V to -5.10V and is capable of sinking a minimum of 5mA. The external V_{REF} bypass capacitors are still required.

Digital Interlace

External Clock

The MAX120/MAX122 require a TTL-compatible clock for proper operation. The MAX120 accepts clocks in the 0.1MHz to 8MHz frequency range when operating in modes 1–4 (see the *Operating Modes* section). The maximum clock frequency is limited to 6MHz when operating in mode 5. The MAX122 requires a 0.1MHz to 5MHz clock for operation in all five modes. The minimum clock frequency for both the MAX120 and MAX122 is limited to 0.1MHz, due to the T/H's droop rate.

Clock and Control Synchronization

The clock and convert start inputs ($\overline{CONVST}$ or $\overline{RD}$ and $\overline{CS}$, see the *Operating Modes* section) are not synchronized, the conversion time can vary from 13 to 14 clock cycles. The successive approximation register (SAR) always changes state on the CLKIN input's rising edge. To ensure a fixed conversion time, see Figure 5 and the following guidelines.

For a conversion time of 13 clock cycles, the convert start input(s) should go low at least 50ns before CLKIN's next rising edge. For a conversion time of 14 clock cycles, the convert start input(s) should go low within 10ns of CLKIN's next rising edge. If the convert start input(s) go low from 10ns to 50ns before CLKIN's next rising edge, the number of clock cycles required is undefined and can be either 13 or 14. For best analog performance, synchronize the convert start inputs with the clock input.

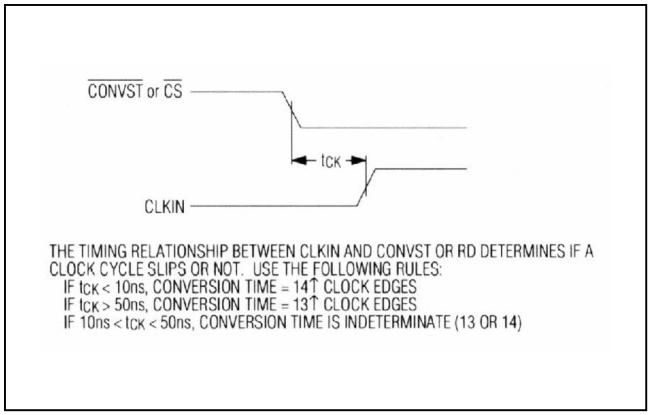


Figure 5. Clock and Control Synchronization

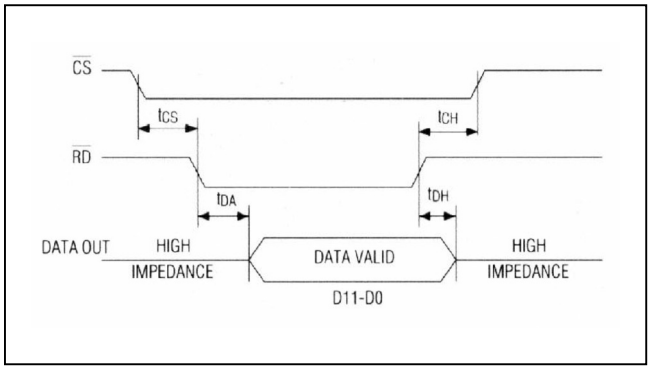


Figure 6. Data-Access and Bus-Relinquish Timing

Output Data Format

The conversion result is output on a 12-bit data bus with a 75ns data-access time. The output data format is twos-complement. Three input control signals ($\overline{CS}$, $\overline{RD}$, and $\overline{CONVST}$), the $\overline{INT}/\overline{BUSY}$ converter status output, and the 12 bits of output data can interface directly to a 16-bit data bus. See Figure 6 for data-access timing.

Timing and Control

The MAX120/MAX122 have five operational modes as outlined in Figures 7 to 11 and discussed in the *Operating Modes* section.

Full-control mode (mode 1) provides maximum control to the user for convert start and data-read operations.

Full-control mode is for µPs with or without wait-state capability. Stand-alone mode (mode 2) and continuous-conversion mode (mode 5) are for systems without µPs,

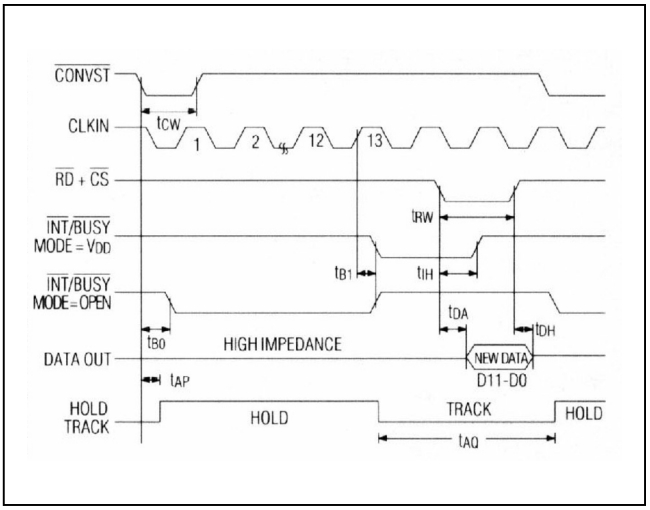


Figure 7. Full-Control Mode (Mode 1)

or for µP-based systems where the ADC and the µP are linked through first-in, first-out (FIFO) buffers or direct memory access (DMA) ports. Slow-memory mode (mode 3) is intended for µPs that can be forced into a wait state during the ADC's conversion time. ROM mode (mode 4) is for µPs that cannot be forced into a wait state.

In all five operating modes, the start of a conversion is controlled by one of three digital inputs: $\overline{CONVST}$, $\overline{RD}$, or $\overline{CS}$. Figure 12 shows the logic equivalent for the conversion circuitry. In any operating mode, $\overline{CONVST}$ must be low for a conversion to occur. Once the conversion is in progress, it cannot be restarted.

Read operations are controlled by $\overline{RD}$ and $\overline{CS}$. Both of these digital inputs must be low to read output data. The $\overline{INT}/\overline{BUSY}$ output indicates the converter's status and determines when the data from the most recent conversion is available. The MODE input configures the $\overline{INT}/\overline{BUSY}$ output as follows:

If MODE = V_{DD}, $\overline{INT}/\overline{BUSY}$ functions as an INTERRUPT output. In this configuration, $\overline{INT}/\overline{BUSY}$ goes low when the conversion is complete and returns high after the conversion data has been read.

If MODE is left open or tied to DGND, $\overline{INT}/\overline{BUSY}$ functions as a $\overline{BUSY}$ output. In this case, $\overline{INT}/\overline{BUSY}$ goes low at the start of a conversion and remains low until the conversion is complete and the data is available at D0–D11.

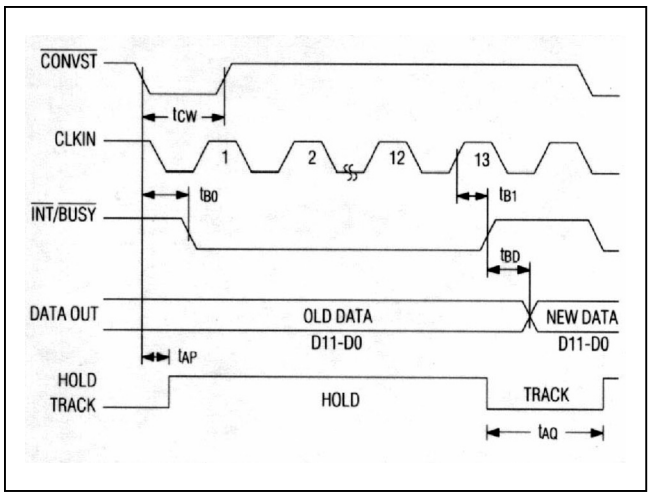


Figure 8. Stand-Alone Mode (Mode 2)

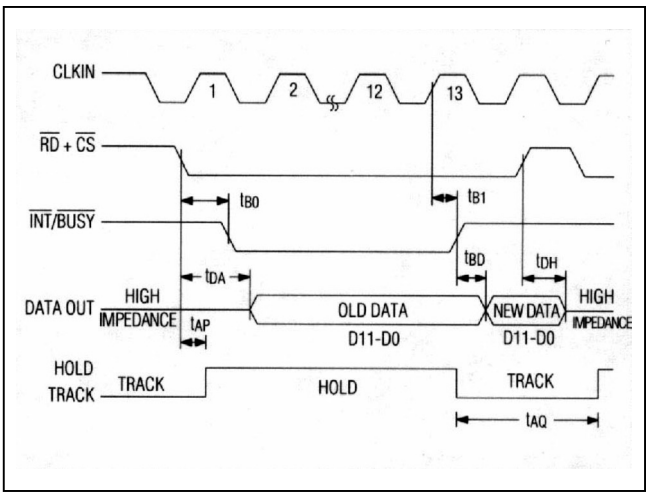


Figure 9. Slow-Memory Mode (Mode 3)

Initialization After Power-Up

On power-up, the first MAX120/MAX122 conversion is valid if the following conditions are met:

1) Allow 14 clock cycles for the internal T/H to enter the track mode, plus a minimum of 350ns in the track mode for the data-acquisition time.
2) Make sure the reference voltage has settled. Allow 0.5ms for each 1µF of reference bypass capacitance (11ms for a 22µF capacitor).

Operating Modes

Mode 1: (Full-Control Mode)

Figure 7 shows the timing diagram for full-control mode (mode 1). In this mode, the µP controls the conversion-start and data-read operations independently.

A falling edge on $\overline{CONVST}$ places the T/H into hold mode and starts a conversion in the SAR. The conversion is complete in 13 or 14 clock cycles as discussed in the *Clock and Control Synchronization* section. A change in the $\overline{INT}/\overline{BUSY}$ output state signals the end of a conversion as follows:

If **MODE = V_{DD}**, the end of conversion is signaled by the INT/BUSY output falling edge.

If MODE = OPEN or DGND, the $\overline{INT}/\overline{BUSY}$ output goes low while the conversion is in progress and returns high when the conversion is complete.

When the conversion is complete, the data can be read without initiating a new conversion by pulling $\overline{RD}$ and $\overline{CS}$ low and leaving $\overline{CONVST}$ high. To start a new conversion without reading data, $\overline{RD}$ and $\overline{CS}$ should remain high while $\overline{CONVST}$ is driven low. To simultaneous read data and initiate a new conversion, $\overline{CONVST}$, $\overline{RD}$, and $\overline{CS}$ should all be pulled low. **Note:** Allow at least 350ns for T/H acquisition time between the end of one conversion and the beginning of the next.

Mode 2: Stand-Alone Operation (MODE= OPEN, $\overline{RD}$ = $\overline{CS}$ = DGND)

For systems that do not use or require full-bus interfacing, the MAX120/MAX122 can be operated in stand-alone mode directly linked to memory through DMA ports or a FIFO buffer. In stand-alone mode, a conversion is initiated by a falling edge on $\overline{CONVST}$. The data outputs are always enabled; data changes at the end of a conversion as indicated by a rising edge on $\overline{INT}/\overline{BUSY}$. See Figure 8 for stand-alone mode timing.

Mode 3: Slow-Memory Mode (CONVST = GND, MODE= OPEN)

Taking $\overline{RD}$ and $\overline{CS}$ lo laces the T/H into hold mode and starts a conversion. $\overline{INT}/\overline{BUSY}$ remains low while the conversion is in progress and can be used as a wait input to the µP. Data from the previous conversion appears on the data bus until the conversion end is indicated by $\overline{INT}/\overline{BUSY}$. See Figure 9 for slow-memory mode timing.

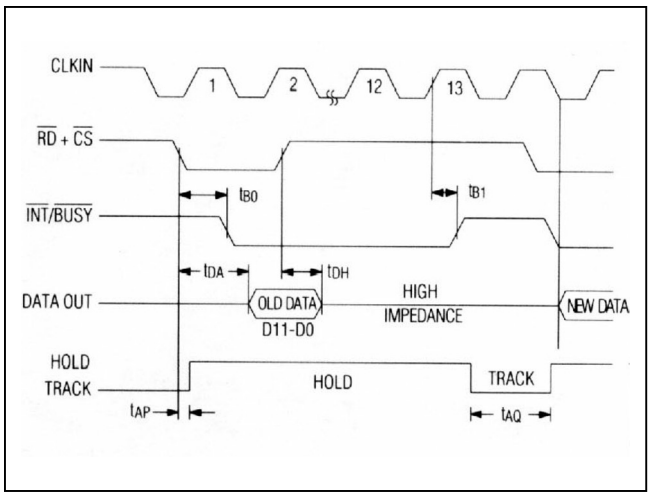


Figure 10. ROM Mode (Mode 4)

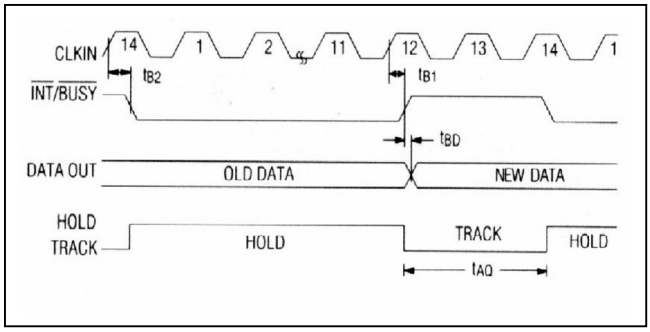


Figure 11. Continuous-Conversion Mode (Mode 5)

Mode 4: ROM Mode (MODE = OPEN, $\overline{CONVST}$ = GND)

In ROM mode, the MAX120/MAX122 behave like a fast-access memory location avoid placing the µP into a wait state. Pulling $\overline{RD}$ and $\overline{CS}$ low places the T/H in hold mode, starts a conversion, and reads data from the previous conversion. Data from the first read in a sequence is often disregarded when this interface mode is used. A second read operation accesses the first conversion's result and also starts a new conversion. The time between successive read operations must be longer than the sum of the T/H acquisition time and the MAX120/MAX122 conversion time. See Figure 10 for ROM-mode timing.

Mode 5: Continuous-Conversion Mode ($\overline{CONVST}$ = $\overline{RD}$ = $\overline{CS}$ = MODE = GND)

For systems that do not use or require full-bus interfacing, the MAX120/MAX122 can operate in continuous-conversion mode, directly linked to memory through DMA ports or a FIFO buffer. In this mode, conversions are performed

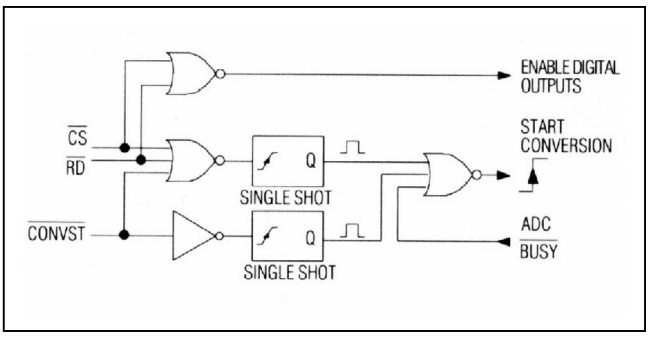


Figure 12. Conversion-Control Logic

continuously at the rate of one conversion for every 14 clock cycles, which includes 2 clock cycles for the T/H acquisition time. To satisfy the 350ns minimum acquisition time requirement within 2 clock cycles, the MAX120's maximum clock frequency is 6MHz when operating in mode 5.

The data outputs are always enabled and "new" disappears on the output bus at the end of a conversion as indicated by the $\overline{INT}/\overline{BUSY}$ output rising edge. The MODE input should be hard-wired to GND. Pulling $\overline{CS}$, $\overline{RD}$, or $\overline{CONVST}$ high stops conversions. See Figure 11 for continuous-conversion mode timing.

Applications Information

Using FIFO Buffers

Using FIFO memory to buffer blocks of data from the MAX120 reduces µP interrupt overhead time by enabling the µP to process data while the MAX120, unassisted, writes conversion results to the FIFO. To retrieve a block of data, the µP reads from the FIFO via a read-interrupt cycle. Read and write operations for the FIFO are completely asynchronous. Figure 13 shows the MAX120 operating in continuous-conversion mode (mode 5),writing data directly into the two IDT7200 256 x 9 FIFO buffers at the rate of 428ksps. The µP is interrupted to read the accumulated data by the FIFO's half-full (HF) flag approximately three times per millisecond. For operation at 500ksps, use an 8MHz clock, and pulse $\overline{CONVST}$ at 500kHz. The full flag (FF) indicates that the FIFO is full. If this flag is ignored, data may be lost. If necessary, conversions can be inhibited by pulling $\overline{CS}$, $\overline{RD}$, or $\overline{CONVST}$ high. The FIFO's read cycle times are as fast as 15ns, satisfying most system speed requirements. The $\overline{RESET}$ input resets all data in the FIFO to zero.

For synchronous operation, the $\overline{CONVST}$ pin may be used to initiate conversions, as described in the Operating Modes section (Mode 2: Stand-Alone Operation).

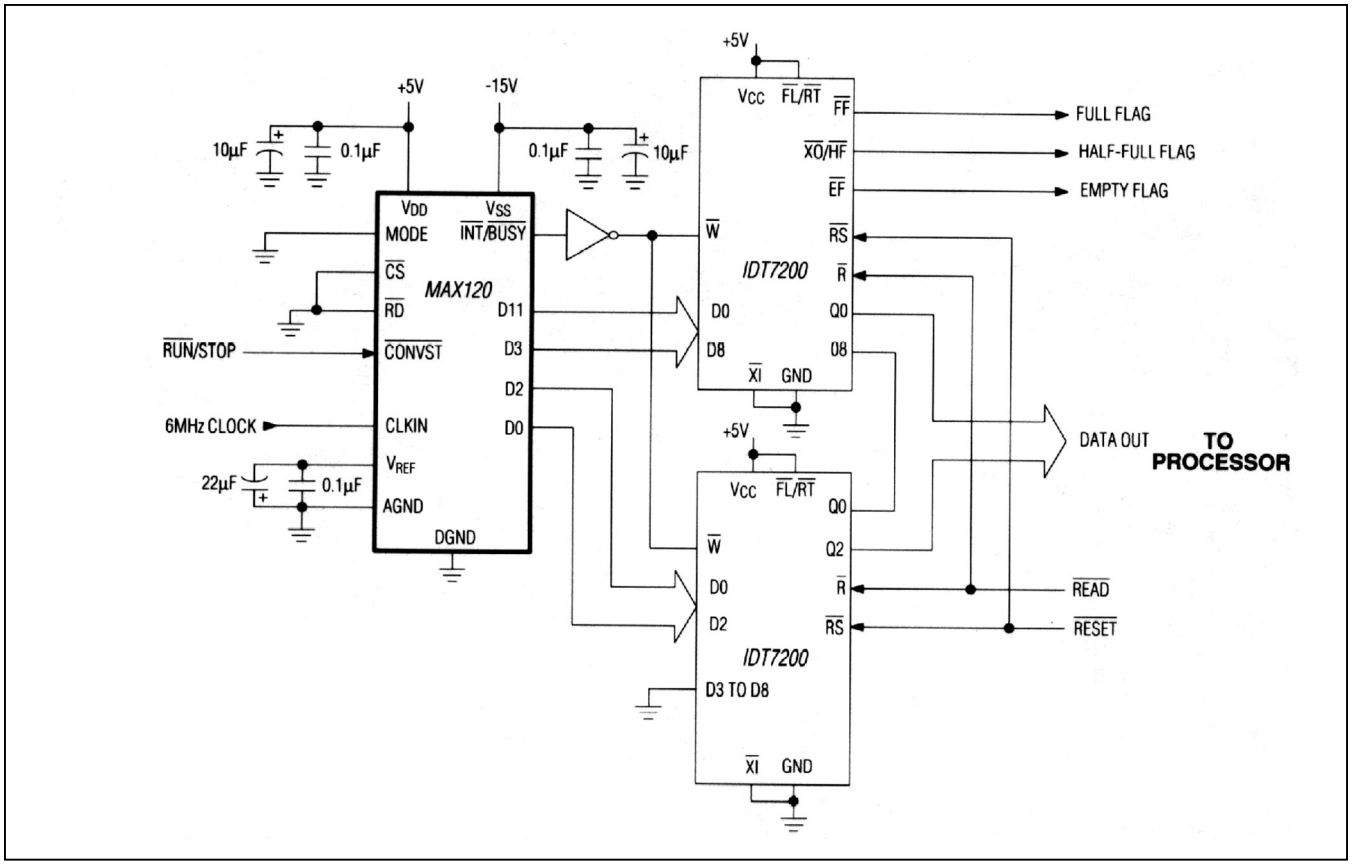


Figure 13. Using MAX120 with FIFO Memory

Digital-Bus Noise

If the ADC's data bus is active during a conversion, coupling from the data pins to the ADC comparator can cause errors. Using slow-memory mode (mode 3) avoids this problem by placing the µP in a wait state during the conversion. If the data bus is active during the conversion in either mode 1 or 4, use three-state drivers to isolate the bus from the ADC.

In ROM mode (mode 4), considerable digital noise is generated in the ADC when $\overline{RD}$ or $\overline{CS}$ go high, disabling the output buffers after a conversion is started. This noise can cause errors if it occurs at the same instant the SAR latches a comparator decision. To avoid this problem, $\overline{RD}$ and $\overline{CS}$ should be active for less than 1 clock cycle. If this is not possible, $\overline{RD}$ or $\overline{CS}$ should go high coinciding with CLKIN's falling edge, since the comparator output is always latched at CLKIN's rising edge

Layout, Grounding, and Bypassing

For best system performance, use PCBs with separate analog and digital ground planes. Wirewrap boards are not recommended. The two ground planes should be tied together at the low-impedance power-supply source, as shown in Figure 14.

The board layout should ensure that digital and analog signal lines are kept separate from each other as much as possible. Do not run analog and digital (especially clock) lines parallel to one another.

The ADC's high-speed comparator is sensitive to high-frequency noise in the V_{DD} and V_{SS} power supplies. Bypass these supplies to the analog ground plane with 0.1µF and 10µF bypass capacitors. Minimize capacitor lead lengths for best noise rejection. If the +5V power supply is very noisy, connect a 5Ω resistor, as shown in Figure 14. Figure 15 shows the negative power-supply (V_{SS}) rejection vs. frequency. Figure 16 shows the positive power-supply (V_{DD}) rejection vs. frequency, with and without the optional 5Ω resistor.

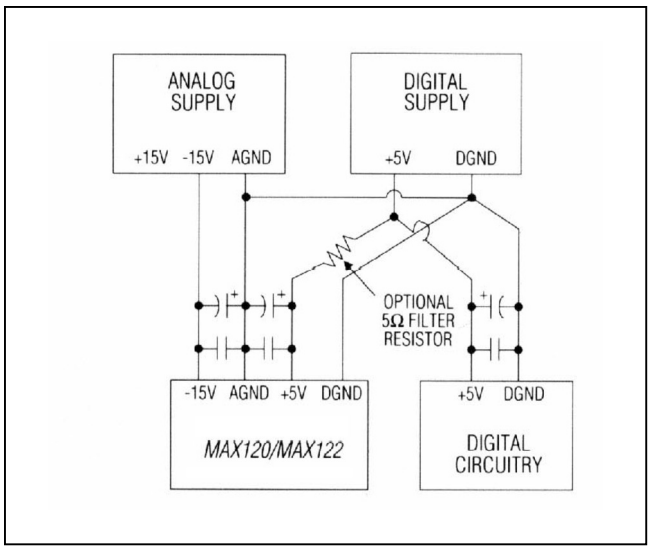


Figure 14. Power-Supply Grounding

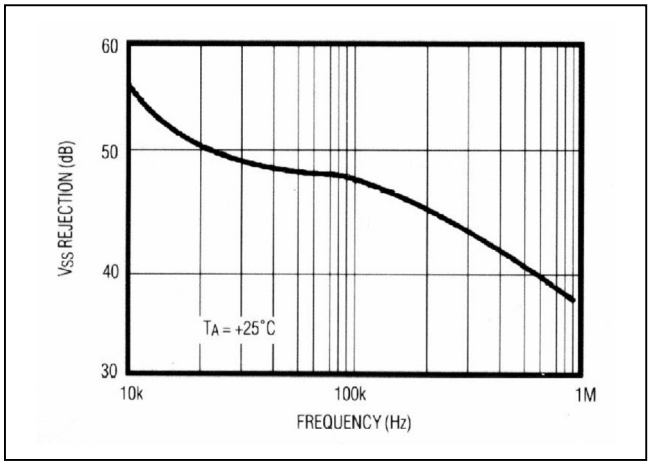


Figure 15. V_{SS} Power-Supply Rejection vs. Frequency

Gain and Offset Adjustment

Figure 17 plots the bipolar input/output transfer function for the MAX120/MAX122. Code transitions occur halfway between successive integer LSB values. Output coding is two's-complement binary with 1 LSB = 2.44mV (10V/4096).

In applications where gain (full-scale range) adjustment is required, Figure 18's circuit can be used. If both offset and gain (full-scale range) need adjustment, either of the circuits in Figures 19 and 20 can be used. Offset should be adjusted before gain for either of these circuits.

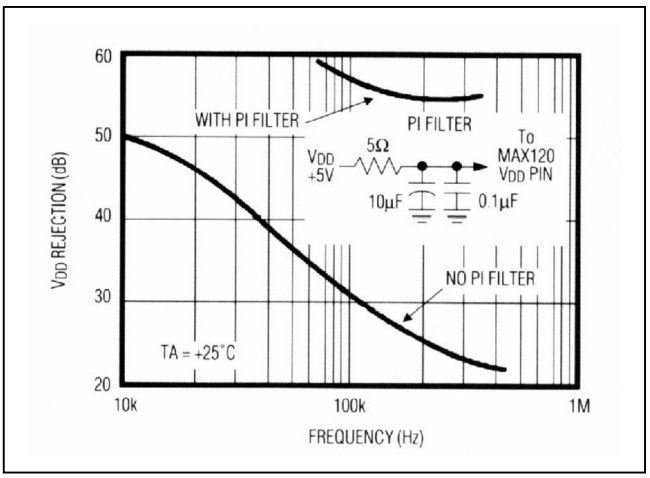


Figure 16. V_{DD} Power-Supply Rejection vs. Frequency

To adjust bipolar offset with Figure 19's circuit, apply +1/2 LSB (0.61mV) to the noninverting amplifier input and adjust R4 for output-code flicker between 0000 and 0000 0000 0001. For full scale, apply FS - the output code flickers between 0111 1111 1110 and 0111 1111 1111. There may be some interaction between these adjustments. The MAX120/MAX122 transfer function used in conjunction with Figure 19's circuit is the same as Figure 17, except the full-scale range is reduced to 2.5V.

To adjust bipolar offset with Figure 20's circuit, apply -1/2 LSB (-1.22mV) at V_{IN} and adjust R5 for output-code flicker between 0000 0000 0000 and 0000 0000 0001. For gain adjustment, apply -FS + ½ LSB (-4.9951V) at V_{IN} and adjust R1 so the output code flickers between 0111 1111 1110 and 0111 1111 1111. As with Figure 20's circuit, the offset and gain adjustments may interact. Figure 21 plots the transfer function for Figure 20's circuit.

Dynamic Performance

High-speed sampling capability and 500ksps throughput (333ksps for the MAX122) make the MAX120/MAX122 ideal for wideband-signal processing. To support these and other related applications, fast fourier transform (FFT) test techniques are used to guarantee the ADC's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low-distortion sine wave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm, which determines its spectral content.

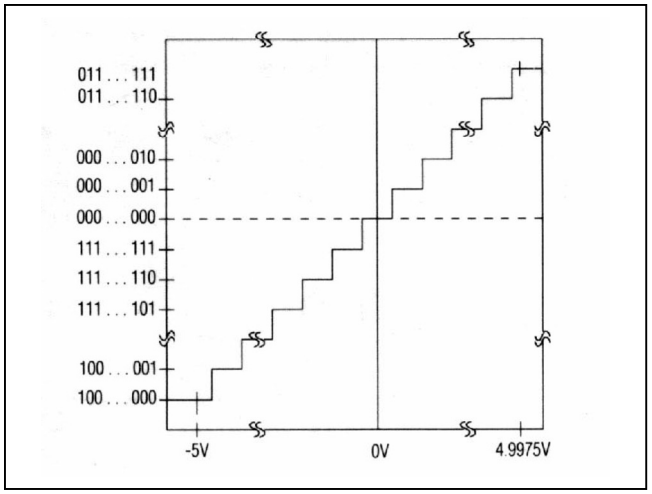


Figure 17. Bipolar Transfer Function

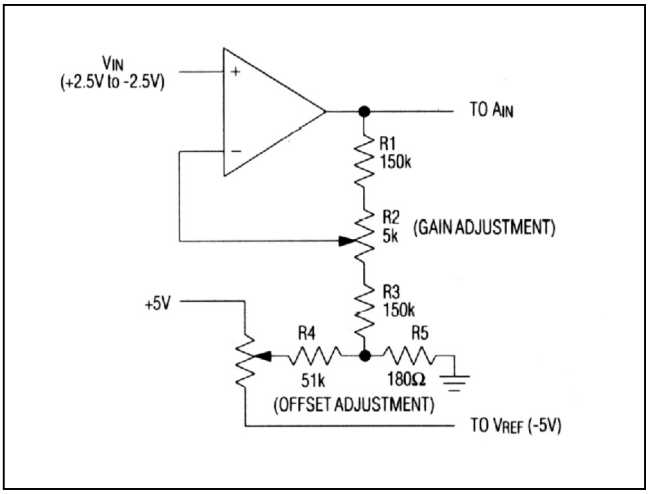


Figure 19. Offset and Gain Adjustment (Noninverting)

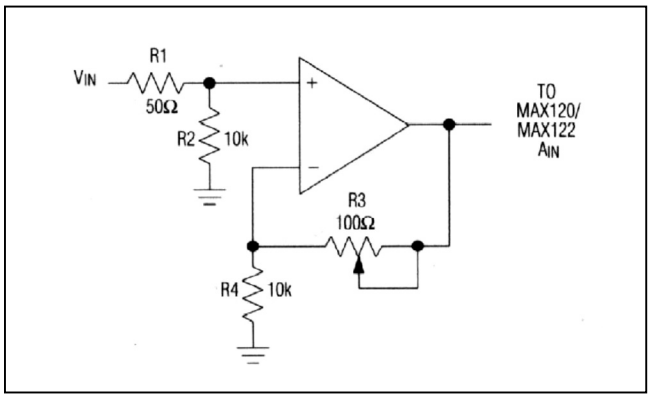


Figure 18. Trim Circuit for Gain Only

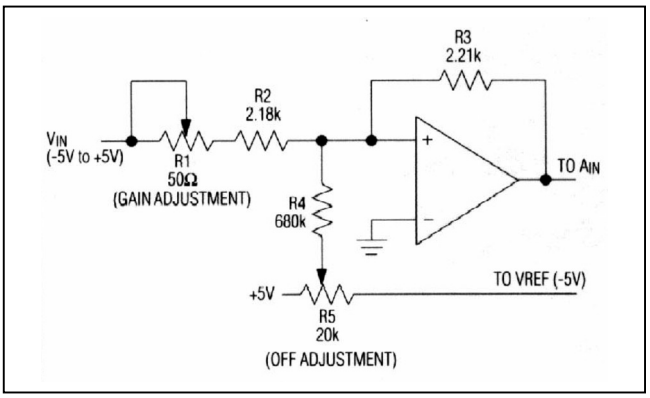


Figure 19. Offset and Gain Adjustment (Noninverting)

ADCs have traditionally been evaluated by specifications such as zero and full-scale error, integral nonlinearity (INL), and differential nonlinearity (DNL). Such parame ters are widely accepted for specifying performance with DC and slowly varying signals, but are less useful in signal processing applications where the ADC's impact on the system transfer function is the main concern. The significance of various DC errors does not translate well to the dynamic case, so different tests are required.

Signal-to-Noise Ratio and Effective Number of Bits

The signal-to-noise plus distortion ratio (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS amplitude of all other ADC output signals. The output band is limited to frequencies above DC and below one-half the ADC sample rate.

The theoretical minimum ADC noise is caused by quantization error and is a direct result of the ADC's resolution: SNR = (6.02N + 1.76)dB, where N is the number of bits of resolution. A perfect 12-bit ADC can, therefore, do no better than 74dB. An FFT plot shows the output level in various spectral bands. Figure 22 shows the result of sampling a pure 100kHz sinusoid at a 500ksps rate with the MAX120.

By transposing the equation that converts resolution to SNR, we can, from the measured SINAD, determine the effective resolution (or effective number of bits) the ADC provides: N = (SINAD - 1.76)/6.02. Figure 22 shows the effective number of bits as a function of the input frequency for the MAX120. The MAX122 performs similarly.

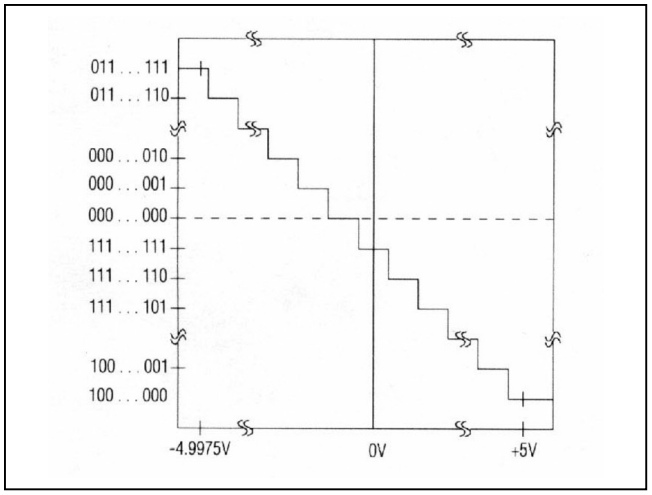


Figure 21. Inverting Bipolar Transfer Function

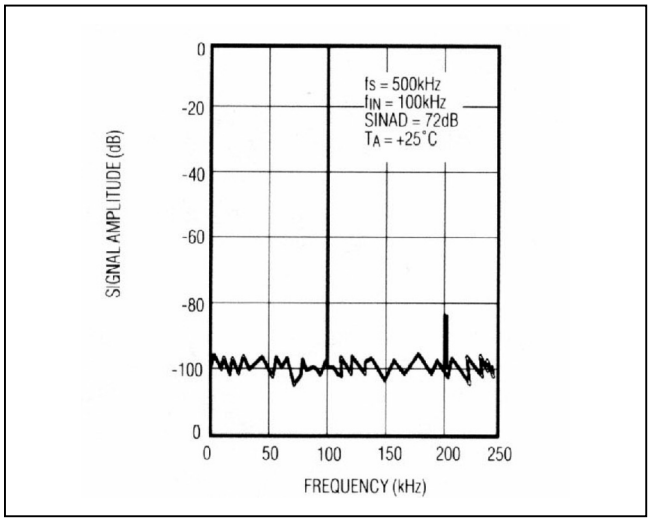


Figure 22. MAX120 FFT Plot

Total Harmonic Distortion

If a pure sine wave is sampled by an ADC at greater than the Nyquist frequency, the nonlinearities in the ADC's transfer function create harmonics of the input frequency in the sampled output data.

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics (in the frequency band above DC and below one-half the sample rate, but not including the DC component) to the RMS amplitude of the fundamental frequency. This is expressed as follows:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 ... + V_N^2}}{V_1}$$

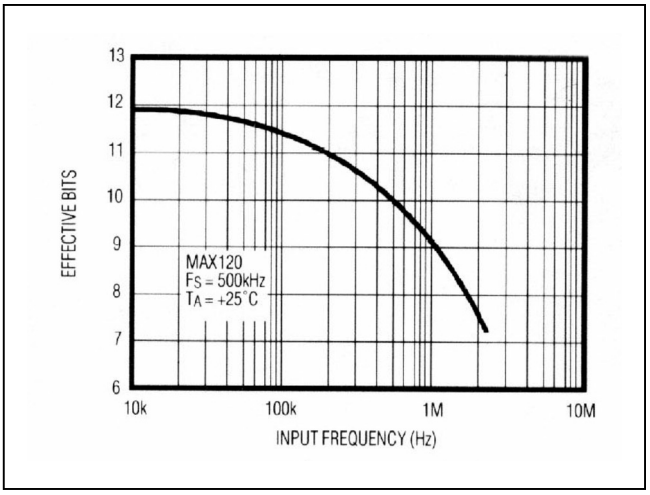


Figure 23. Effective Bits vs. Input Frequency

where V_1 is the fundamental RMS amplitude, and V_2 to V_N are the amplitudes of the 2nd through Nth harmonics. The THD specification in the *Electrical Characteristics* table includes the 2nd through 5th harmonics.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearities produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency

If two pure sine waves of frequency fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function create distortion products at sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. THD includes those distortion products with m or n equal to zero. Intermodulation distortion consists of all distortion products for which neither m nor n equal zero. For example, the 2nd-order IMD terms include (fa + fb) and (fa - fb) while the 3rd-order IMD terms include (2fa + fb), (2fa - fb) , (fa + 2fb), and (fa - 2fb).

If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd-order IMD products can be expressed by the following formula:

$$IMD\ (fa \pm fb) = 20\log\left[\frac{\text{amplitude at}\ (fa \pm fb)}{\text{amplitude at fa}}\right]$$

Spurious-Free Dynamic Range

Spurious-free dynamic range is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually the next largest spectral component occurs at some harmonic of the input frequency. However, if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 CDIP	R24-4	21-0045	—
24 PDIP	N24+3	21-0043	—
24 SO	W24+2	21-0042	90-0182
24 SSOP	A24+2	21-0056	90-0110

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	INL (LSB)
MAX120EAG+	-40°C to +85°C	24 SSOP	±1
MAX122ACNG+	0°C to +70°C	24 PDIP	±3/4
MAX122BCNG+	0°C to +70°C	24 PDIP	±1
MAX122ACWG+	0°C to +70°C	24 Wide SO	±3/4
MAX122BCWG+	0°C to +70°C	24 Wide SO	±1
MAX122ACAG+	0°C to +70°C	24 SSOP	±3/4
MAX122BCAG+	0°C to +70°C	24 SSOP	±1
MAX122AENG+	-40°C to +85°C	24 PDIP	±3/4
MAX122BENG+	-40°C to +85°C	24 PDIP	±1
MAX122AEWG+	-40°C to +85°C	24 Wide SO	±3/4
MAX122BEWG+	-40°C to +85°C	24 Wide SO	±1
MAX122AEAG+	-40°C to +85°C	24 SSOP	±3/4
MAX122BEAG+	-40°C to +85°C	24 SSOP	±1
MAX122BMRG-	-55°C to +125°C	24 CERDIP	±1
MAX120EVKIT-DIP†	0°C to +70°C	PDIP – Through Hole	

+Denotes a lead(Pb)-free/RoHS-compliant package.

†MAX120 EV kit can be used to evaluate the MAX122; when ordering the EV kit, ask for a free sample of the MAX122.

-Denotes a package containing lead(Pb).

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/92	Initial release	—
1	3/12	Removed PDIP, CERDIP packages from *Ordering Information*. Updated style throughout data sheet.	1–16

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