PCMFxUSB3S series

Common-mode EMI filter for differential channels with integrated ESD protection

Rev. 3 — 7 March 2019

Product data sheet

1. General description

Common-mode ElectroMagnetic Interference (EMI) filters with integrated ElectroStatic Discharge (ESD) protection for one, two and three differential channels. The devices are designed to provide low insertion loss for differential high-speed signals on each channel while unwanted common-mode signals are attenuated.

Each differential channel incorporates two signal lines that are coupled by integrated coils. Diodes provide protection to downstream components from ESD voltages up to ±15 kV on each signal line.

Table 1. Product overview

Type number	Number of channels	Package Name
PCMF1USB3S	1	WLCSP5
PCMF2USB3S	2	WLCSP10
PCMF3USB3S	3	WLCSP15

2. Features and benefits

- One, two and three differential channels common-mode EMI filters with integrated ESD protection
- ESD protection up to ±15 kV contact discharge according to IEC 61000-4-2
- Superior common-mode suppression over a wide frequency range
- Superior RF performance compared to other integrated filters or discrete filters with external ESD protection
- Extremely high symmetry between line pairs
- Industry-standard Wafer-Level Chip-Scale Packages: WLCSP5, 10 and 15 for smaller footprint

3. Applications

- · Smartphone, cellular and cordless phone
- Tablet PC and Mobile Internet Device (MID)
- USB 3.2, USB 2.0, HDMI 2.0, HDMI 1.4
- MIPI M-PHY and D-PHY as used in Camera Serial Interface (CSI) and Display Serial Interface (DSI)
- General-purpose EMI and Radio-Frequency Interference (RFI) filter and downstream ESD protection



4. Pinning information

Table 2. Pinning

Table 4	Table 2. Pinning					
Pin	Symbol	Description	Simplified outline	Graphic symbol		
PCMF	1USB3S (WLCSF	P5_2-1-2)				
A1	CH1_IN+	channel 1+, external	2	A1C1		
A2	CH1_IN-	channel 1-, external	2 (B1)	A2C2		
B1	GND_CH1	ground channel 1	1			
C1	CH1_OUT+	channel 1+, internal	A B C	本 本		
C2	CH1_OUT-	channel 1-, internal	Transparent top view			
			WLCSP5_2-1-2	<u> </u>		
				B1 aaa-019784		
PCMF	2USB3S (WLCSF	P10_4-2-4)	1			
A1	CH1_IN+	channel 1+, external		A1, 3 C1, 3		
A2	CH1_IN-	channel 1-, external	4 (B2)	A2, 4C2, 4		
A3	CH2_IN+	channel 2+, external	3 62			
A4	CH2_IN-	channel 2-, external		本 本		
B1	GND_CH1	ground channel 1				
B2	GND_CH2	ground channel 2	(B1)	<u>_</u>		
C1	CH1_OUT+	channel 1+, internal		B1, B2 - no internal connection aaa-019785		
C2	CH1_OUT-	channel 1-, internal	A B C Transparent top view			
C3	CH2_OUT+	channel 2+, internal	WLCSP10_4-2-4			
C4	CH2_OUT-	channel 2-, internal				
PCMF	3USB3S (WLCSF	P15_6-3-6)				
A1	CH1_IN+	channel 1+, external	6	A1, 3, 5 —C1, 3, 5		
A2	CH1_IN-	channel 1-, external	B3)	A2, 4, 6 —————————————————————————————————		
A3	CH2_IN+	channel 2+, external	5			
A4	CH2_IN-	channel 2-, external		本 本		
A5	CH3_IN+	channel 3+, external	4 0			
A6	CH3_IN-	channel 3-, external	3 (B2) (B2)			
B1	GND_CH1	ground channel 1		B1, B2, B3 - no internal connection aaa-019786		
B2	GND_CH2	ground channel 2				
В3	GND_CH3	ground channel 3	B1 O			
C1	CH1_OUT+	channel 1+, internal	1 0			
C2	CH1_OUT-	channel 1-, internal	A B C			
C3	CH2_OUT+	channel 2+, internal	Transparent top view WLCSP15_6-3-6			
C4	CH2_OUT-	channel 2-, internal	112001 10_0-0-0			
C5	CH3_OUT+	channel 3+, internal				
C6	CH3_OUT-	channel 3-, internal				

5. Ordering information

Table 3. Ordering information

Type number	Package			
	Name	Description		
PCMF1USB3S	WLCSP5	wafer level chip-size package; 5 bumps (2-1-2)		
PCMF2USB3S	WLCSP10	wafer level chip-size package; 10 bumps (4-2-4)		
PCMF3USB3S	WLCSP15	wafer level chip-size package; 15 bumps (6-3-6)		

6. Marking

Table 4. Marking codes

Type number	Marking code
PCMF1USB3S	PF1S
PCMF2USB3S	PF2S
PCMF3USB3S	PF3S

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
VI	input voltage		-0.5	5	V
V _{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4; all input pins to ground			
		contact discharge	-15	15	kV
		air discharge	-15	15	kV
		IEC 61000-4-2, level 4; all output pins to ground			
		contact discharge	-2	2	kV
		air discharge	-2	2	kV
I _{PPM}	rated peak-pulse current	t _p = 8/20 μs	-7	7	Α
T _{stg}	storage temperature		-40	125	°C
T _{amb}	ambient temperature		-40	125	°C

8. Characteristics

8.1. Channel characteristics

Table 6. Channel characteristics

 T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R _{s(ch)}	channel series resistance	single line; input to output		-	3	-	Ω
C _d	diode capacitance	f = 1 MHz; V _I = 2.5 V	[1]	-	0.25	-	pF
I _{RM}	reverse leakage current	per line; V _I = 5 V		-	-	100	nA
V_{BR}	breakdown voltage	I _R = 1 mA		6	9	-	V
V _F	forward voltage	I _F = 10 mA		-	0.8	-	V
R _{dyn}	dynamic resistance	TLP; positive transient	[2]	-	0.14	-	Ω
		TLP; negative transient	[2]	-	0.14	-	Ω
		surge; positive transient	[3]	-	0.22	-	Ω
		surge; negative transient	[3]	-	0.22	-	Ω

- [1] This parameter is guaranteed by design.
- [2] 100 ns Transmission Line Pulse (TLP); 50 Ω; pulser at 70 ns to 90 ns.
- [3] According to IEC 61000-4-5 (8/20 µs).

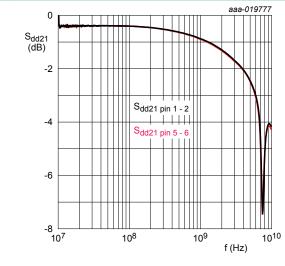
8.2. Frequency characteristics

Table 7. Frequency characteristics

 T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Commor	n mode: S _{21cc}				·		
α_{il}	insertion loss	f = 800 MHz	[1]	-	-12	-	dB
		f = 2.6 GHz	[1]	-	-38	-	dB
		f = 5 GHz	[1]	-	-18	-	dB
Different	tial mode: S _{21dd}				·	'	
α_{il}	insertion loss	f = 1 MHz	[1]	-	0.3	-	dB
f _{-3dB}	cut-off frequency		[1]	-	6	-	GHz

[1] Normalized to attenuation at 1 MHz.



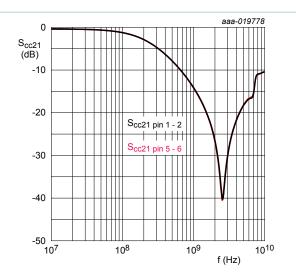
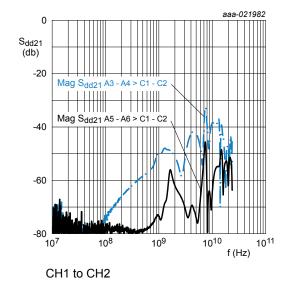


Fig. 1. Differential-mode insertion loss; typical values

Fig. 2. Common-mode insertion loss; typical values



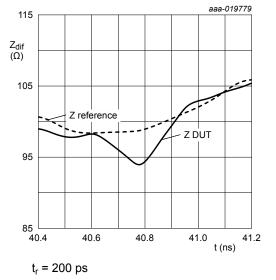
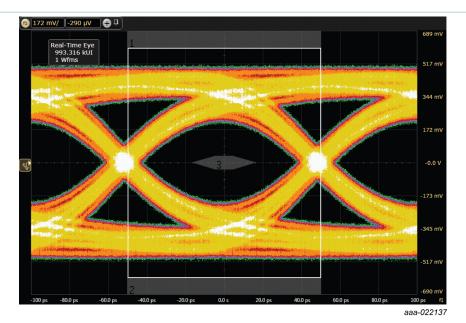


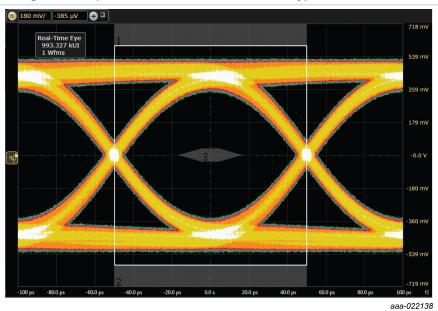
Fig. 3. Differential crosstalk; typical values

Fig. 4. Differential Time Domain Reflectometer (TDR) plot; typical values



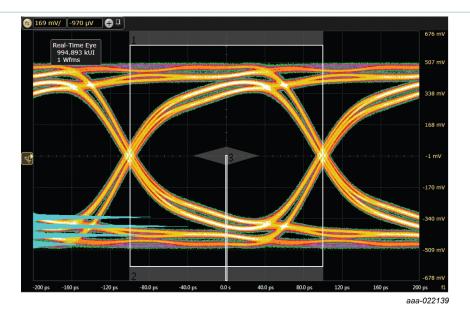
Data rate: 10 Gbit/s Vertical scale 172 mV/div Horizontal scale: 20 ps/div

Fig. 5. USB 3.2 eye diagram 10 Gbps, test board with PCMF2USB3S; typical values



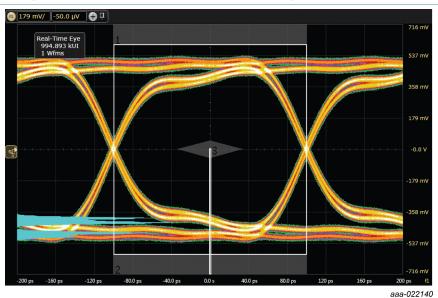
Data rate: 10 Gbit/s Vertical scale 180 mV/div Horizontal scale: 20 ps/div

Fig. 6. USB 3.2 eye diagram 10 Gbps, test board without device; typical values



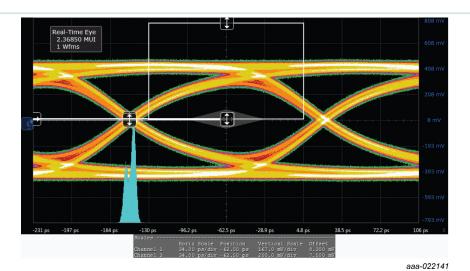
Data rate: 5 Gbit/s Vertical scale 169 mV/div Horizontal scale: 40 ps/div

Fig. 7. USB 3.2 eye diagram 5 Gbps, test board with PCMF2USB3S; typical values



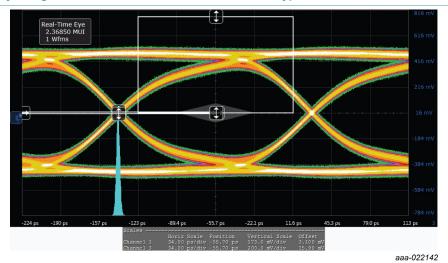
Data rate: 5 Gbit/s Vertical scale 179 mV/div Horizontal scale: 40 ps/div

Fig. 8. USB 3.2 eye diagram 5 Gbps, test board without device; typical values



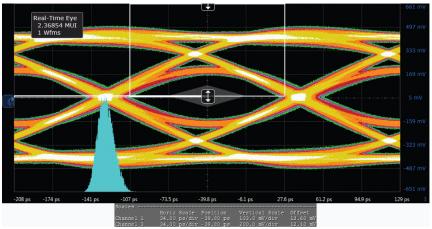
Test frequency: 148.5 MHz Differential swing voltage: 861 mV Horizontal scale: 34 ps/div

Fig. 9. HDMI 2.0 eye diagram TP1, test board with PCMF2USB3S; typical values



Test frequency: 148.5 MHz Differential swing voltage: 917 mV Horizontal scale: 34 ps/div

Fig. 10. HDMI 2.0 eye diagram TP1, test board without device; typical values



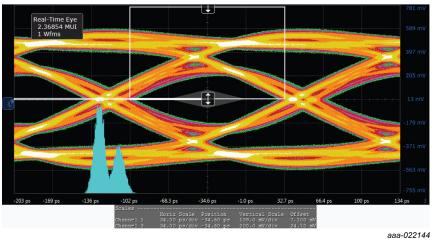
aaa-022143

Test frequency: 148.5 MHz Differential swing voltage: 849 mV Horizontal scale: 34 ps/div

Remark: Measured at Test Point 2 (TP2) worst cable emulator, reference cable equalizer and worst case positive

skew.

Fig. 11. HDMI 2.0 eye diagram TP2, test board with PCMF2USB3S; typical values

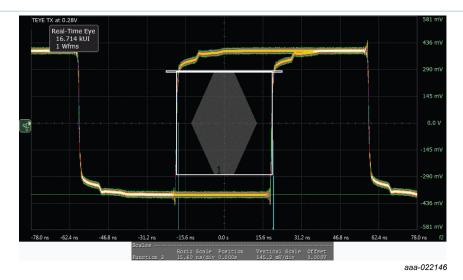


Test frequency: 148.5 MHz Differential swing voltage: 909 mV Horizontal scale: 34 ps/div

Remark: Measured at Test Point 2 (TP2) worst cable emulator, reference cable equalizer and worst case positive

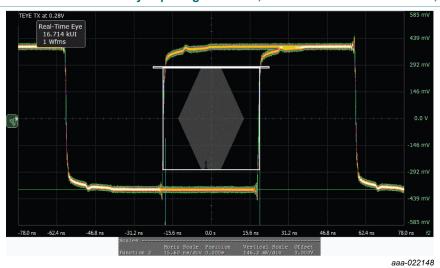
skew.

Fig. 12. HDMI 2.0 eye diagram TP2, test board without device; typical values



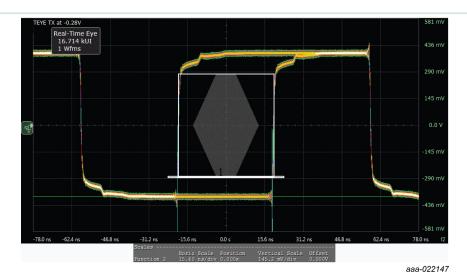
Vertical scale: 145 mV/div Horizontal scale: 15.6 ns/div

Fig. 13. MIPI M-PHY PWM-TX transmitter eye opening at 140 mV, test board with PCMF2USB3S; typical value



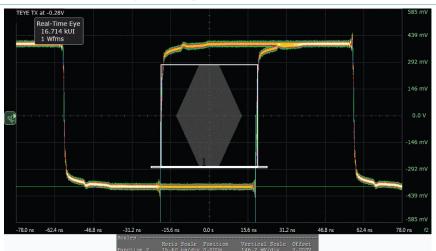
Vertical scale: 146 mV/div Horizontal scale: 15.6 ns/div

Fig. 14. MIPI M-PHY PWM-TX transmitter eye opening at 140 mV, test board without device; typical value



Vertical scale: 145 mV/div Horizontal scale: 15.6 ns/div

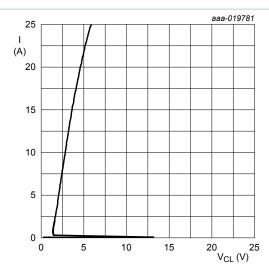
Fig. 15. MIPI M-PHY PWM-TX transmitter eye opening at -140 mV, test board with PCMF2USB3S; typical value



Vertical scale: 145 mV/div Horizontal scale: 15.6 ns/div

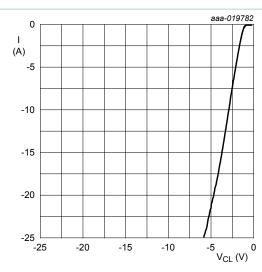
Fig. 16. MIPI M-PHY PWM-TX transmitter eye opening at -140 mV, test board without device; typical value

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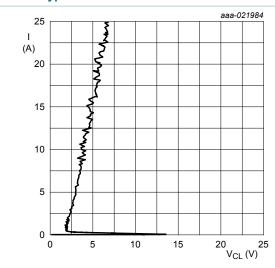
Transmission Line Pulse (TLP) = 100 ns; $t_r = 1 \text{ ns}$

Fig. 17. Dynamic resistance with positive clamping; typical values



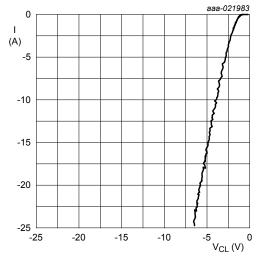
Transmission Line Pulse (TLP) = 100 ns; $t_r = 1 \text{ ns}$

Fig. 18. Dynamic resistance with negative clamping; typical values



Very-Fast Transmission Line Pulse (VF-TLP) = 5 ns; t_r = 600 ps

Fig. 19. Dynamic resistance with positive clamping; typical values



Very-Fast Transmission Line Pulse (VF-TLP) = 5 ns; $t_r = 600 \text{ ps}$

Fig. 20. Dynamic resistance with negative clamping; typical values

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

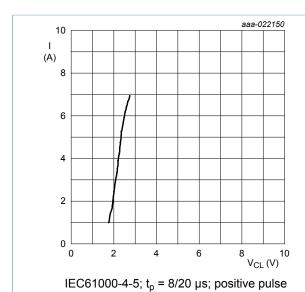


Fig. 21. Dynamic resistance with positive clamping; typical values

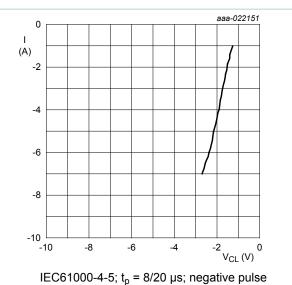


Fig. 22. Dynamic resistance with negative clamping; typical values

9. Application information

The device is designed to provide high-level ESD protection for differential high-speed data line pairs such as:

- USB 3.2
- HDMI 2.0
- Transition-Minimized Differential Signaling (TMDS)
- DisplayPort
- external Serial Advanced Technology Attachment (eSATA)
- Low Voltage Differential Signaling (LVDS)

When designing the Printed-Circuit Board (PCB), give careful consideration to impedance matching and signal coupling. Do not connect the protected signal lines to unlimited current sources like, for example, a battery.

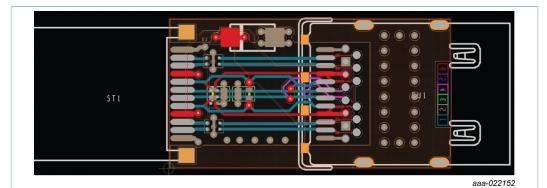


Fig. 23. Application diagram: protecting the differential data lines of a USB Type-C connector evaluation dongle with PCMF1USB3S

Since the SuperSpeed TX/RX lines are separated by GND or VBUS from the Hi-Speed lines, PCMF1USB3S makes it easy to achieve same signal lengths, straight routing, and optimal positioning for ESD protection directly at the connector.

10. Package outline

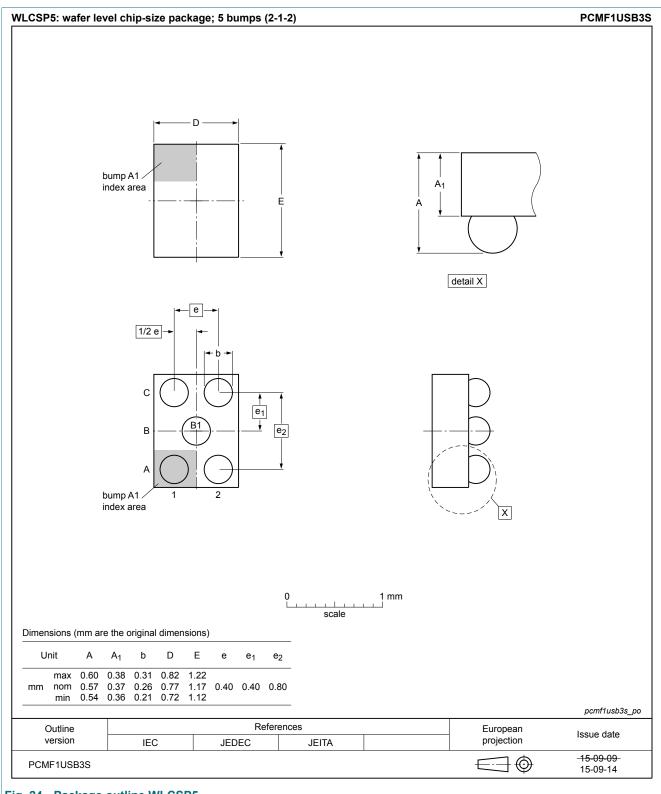


Fig. 24. Package outline WLCSP5

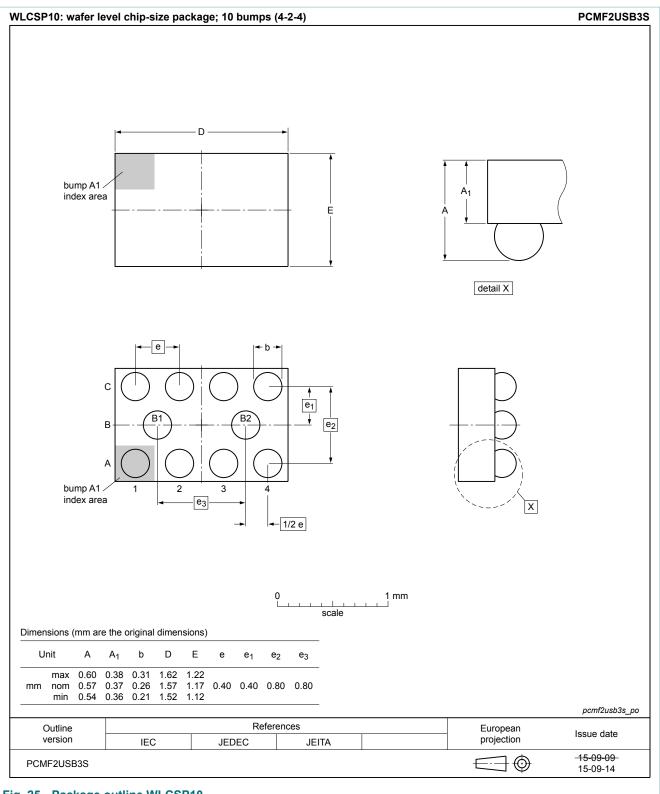


Fig. 25. Package outline WLCSP10

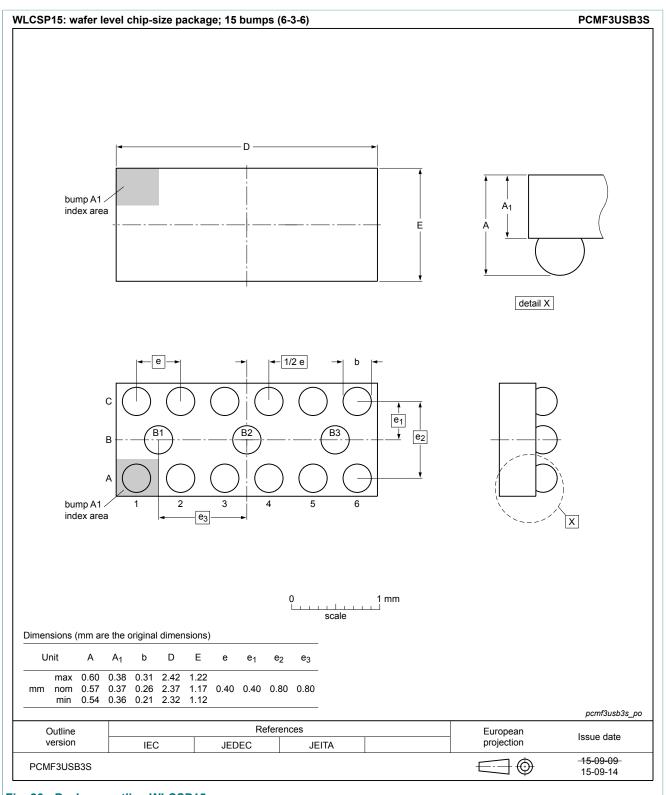
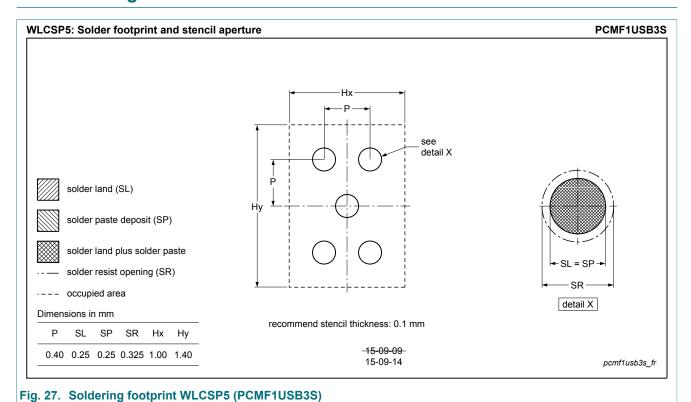
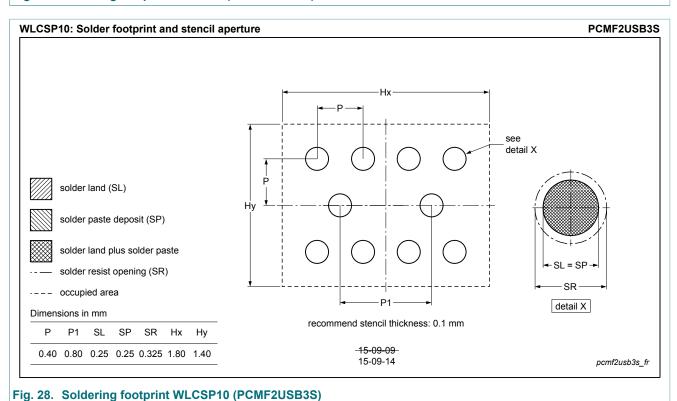
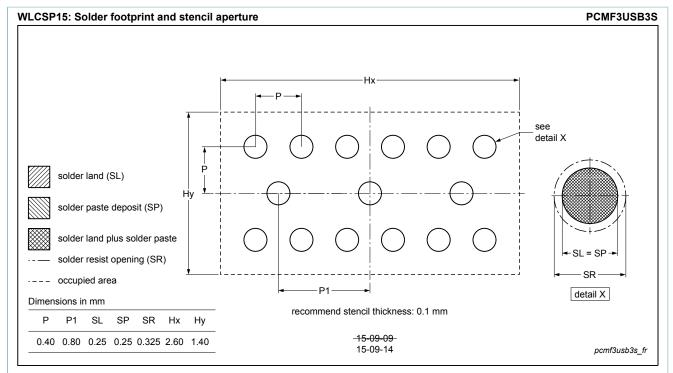


Fig. 26. Package outline WLCSP15

11. Soldering







12. Revision history

Table 8. Revision history

table of Nevicion metery							
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes			
PCMFXUSB3S_SER v.3	20190307	Product data sheet	-	PCMFXUSB3S_SER v.2			
Modifications:	 Limiting values: T_{amb} maximum values updated. Frequency characteristics: corrected typos in Figures 1, 2, 3 and 5. 						
PCMFXUSB3S_SER v.2	20160307	Product data sheet	-	PCMFXUSB3S_SER v.1			
PCMFXUSB3S_SER v.1	20151007	Preliminary data sheet	-	-			

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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For more information, please visit: http://www.nexperia.com For sales office addresses, please send an email to: salesaddresses@nexperia.com Date of release: 7 March 2019

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