

Low Noise, 8th Order, Clock Sweepable Elliptic Lowpass Filter

FEATURES

- 8th Order Filter in a 14-Pin Package
- No External Components
- 100:1 Clock to Center Ratio
- $150\mu V_{RMS}$ Total Wideband Noise
- 0.03% THD or Better
- 50kHz Maximum Corner Frequency
- Operates from $\pm 2.37V$ to $\pm 8V$ Power Supplies
- Passband Ripple Guaranteed Over Full Military Temperature Range

APPLICATIONS

- Antialiasing Filters
- Telecom PCM Filters

DESCRIPTION

The LTC[®]1064-1 is an 8th order, clock sweepable elliptic (Cauer) lowpass switched capacitor filter. The passband ripple is typically $\pm 0.15dB$, and the stopband attenuation at 1.5 times the cutoff frequency is 68dB or more.

An external TTL or CMOS clock programs the value of the filter's cutoff frequency. The clock to cutoff frequency ratio is 100:1.

No external components are needed for cutoff frequencies up to 20kHz. For cutoff frequencies over 20kHz two low value capacitors are required to maintain passband flatness. The LTC1064-1 features low wideband noise and low harmonic distortion even for input voltages up to $3V_{RMS}$. In fact the LTC1064-1 overall performance compares with equivalent multiple op amp RC active realizations.

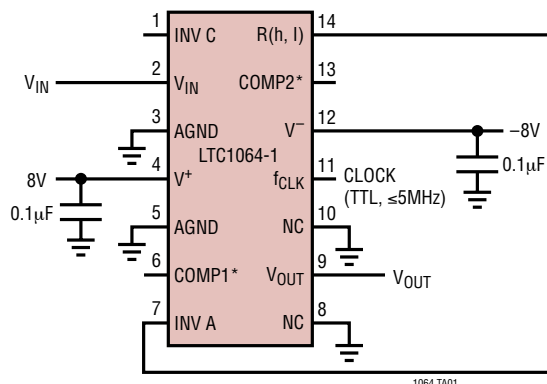
The LTC1064-1 is available in a 14-pin DIP or 16-pin surface mounted SW package.

The LTC1064-1 is pin compatible with the LTC1064-2.

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TYPICAL APPLICATION

8th Order Clock Sweepable Lowpass Elliptic Antialiasing Filter

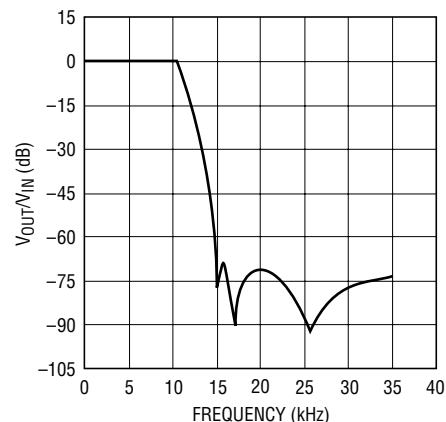


NOTE: THE POWER SUPPLIES SHOULD BE BYPASSED BY A $0.1\mu F$ CAPACITOR CLOSE TO THE PACKAGE.

FOR SERVO OFFSET NULLING APPLICATIONS, PIN 1 IS THE 2ND STAGE SUMMING JUNCTION.

*FOR CUTOFF FREQUENCY ABOVE 20kHz, USE COMPENSATION CAPACITORS ($5pF$ TO $56pF$) BETWEEN PIN 13 AND PIN 1 AND PIN 6 AND PIN 7.

Frequency Response



1064 TA02

8th ORDER CLOCK SWEEPABLE LOWPASS ELLIPTIC ANTIALIASING FILTER MAINTAINS, FOR $0.1Hz \leq f_{CUTOFF} \leq 10kHz$, A $\pm 0.15dB$ PASSBAND RIPPLE AND 72dB STOPBAND ATTENUATION AT $1.5 \times f_{CUTOFF}$. TOTAL WIDEBAND NOISE = $150\mu V_{RMS}$, THD = 0.03% FOR $V_{IN} = 1V_{RMS}$

LTC1064-1

ABSOLUTE MAXIMUM RATINGS (Note 1)

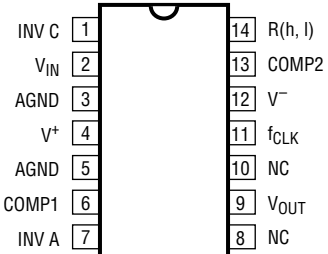
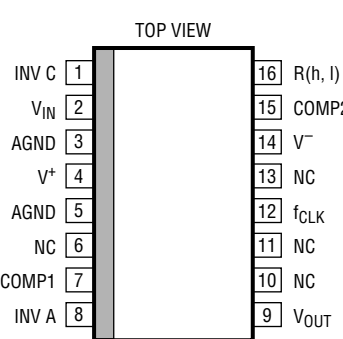
Total Supply Voltage (V^+ to V^-) 16.5V
 Power Dissipation 400mW
 Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10 sec) 300°C

Operating Temperature Range

LTC1064-1M (**OBSOLETE**) -55°C to 125°C

LTC1064-1C/AC -40°C to 85°C

PACKAGE/ORDER INFORMATION

TOP VIEW  N PACKAGE 14-LEAD PDIP $T_{JMAX} = 110^{\circ}\text{C}$, $\theta_{JA} = 70^{\circ}\text{C/W}$	ORDER PART NUMBER LTC1064-1CN LTC1064-1ACN	TOP VIEW  SW PACKAGE 16-LEAD PLASTIC (WIDE) SO $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 90^{\circ}\text{C/W}$	ORDER PART NUMBER LTC1064-1CSW
J PACKAGE 14-LEAD CERDIP OBSOLETE PACKAGE Consider the N14 Package for Alternate Source	LTC1064-1MJ LTC1064-1CJ		

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}\text{C}$. $V_S = \pm 7.5\text{V}$, $f_{CLK} = 1\text{MHz}$, $R_1 = 10\text{k}$, $C_1 = 10\text{pF}$, TTL or CMOS clock input level unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain, LTC1064-1, 1A	Referenced to 0dB, 1Hz to $0.1f_C$	●		± 0.1	± 0.35	dB
Gain TempCo				0.0002		dB/ $^{\circ}\text{C}$
Passband Edge Frequency, f_C				$10 \pm 1\%$		kHz
Gain at f_C	Referenced to Passband Gain	●	-1.25		0.85	dB
LTC1064-1		●	-0.75		0.65	dB
LTC1064-1A						
-3dB Frequency				10.7		kHz
Passband Ripple (Note 1)	$0.1f_C$ to $0.85f_C$ Referenced to Passband Gain, Measured at 6.25kHz and 8.5kHz	●		± 0.15	± 0.32	dB
LTC1064-1		●		± 0.1	± 0.19	dB
LTC1064-1A						
Ripple TempCo				0.0004		dB/ $^{\circ}\text{C}$
Stopband Attenuation	At $1.5f_C$ Referenced to 0dB					
LTC1064-1		●	66	72		dB
LTC1064-1A		●	68	72		dB
Stopband Attenuation	At $2f_C$ Referenced to 0dB					
LTC1064-1		●	67	72		dB
LTC1064-1A		●	68	72		dB

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ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = \pm 7.5\text{V}$, $f_{\text{CLK}} = 1\text{MHz}$, $R_1 = 10\text{k}\Omega$, $C_1 = 10\text{pF}$, TTL or CMOS clock input level unless otherwise specified.

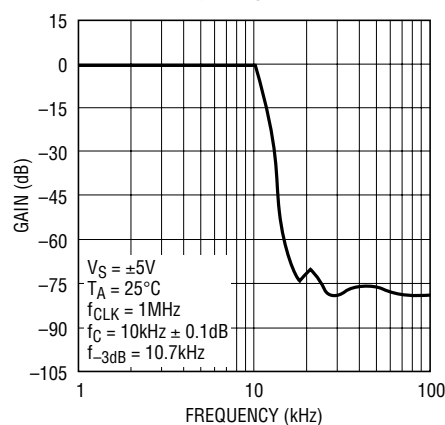
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Frequency Range		0		$f_{\text{CLK}}/2$	kHz
Output Voltage Swing and Operating Input Voltage Range	$V_S = \pm 2.37\text{V}$ $V_S = \pm 5\text{V}$ $V_S = \pm 7.5\text{V}$	● ± 1 ● ± 3 ● ± 5			V V V
Total Harmonic Distortion	$V_S = \pm 5\text{V}$, Input = $1V_{\text{RMS}}$ at 1kHz $V_S = \pm 7.5\text{V}$, Input = $3V_{\text{RMS}}$ at 1kHz		0.015 0.03		% %
Wideband Noise	$V_S = \pm 5\text{V}$, Input = GND 1Hz to 999kHz $V_S = \pm 7.5\text{V}$, Input = GND 1Hz to 999kHz		150 165		μV_{RMS} μV_{RMS}
Output DC Offset	$V_S = \pm 7.5\text{V}$, Pin 2 Grounded		50 50	175 125	mV mV
LTC1064-1 LTC1064-1A					
Output DC Offset TempCo	$V_S = \pm 5\text{V}$		-100		$\mu\text{V}/^\circ\text{C}$
Input Impedance		10	20		$\text{k}\Omega$
Output Impedance	$f_{\text{OUT}} = 10\text{kHz}$		2		Ω
Output Short-Circuit Current	Source/Sink		3/1		mA
Clock Feedthrough			200		μV_{RMS}
Maximum Clock Frequency	50% Duty Cycle, $V_S = \pm 7.5\text{V}$			5	MHz
Power Supply Current	$V_S = \pm 2.37\text{V}$	●	10	22	mA
	$V_S = \pm 5\text{V}$	●	12	23	mA
		●		26	mA
	$V_S = \pm 7.5\text{V}$, $f_{\text{CLK}} = 1\text{MHz}$	●	16	28	mA
		●		32	mA
Power Supply Voltage Range		● ± 2.37		± 8	V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: For tighter specifications please contact LTC Marketing.

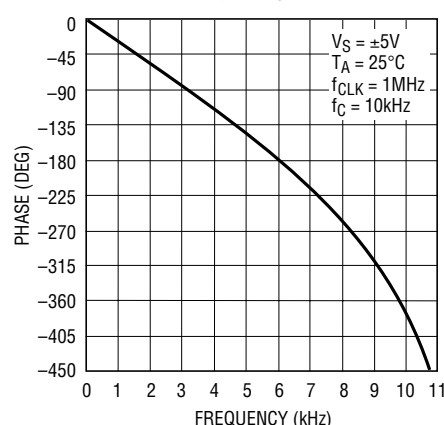
TYPICAL PERFORMANCE CHARACTERISTICS

Gain vs Frequency



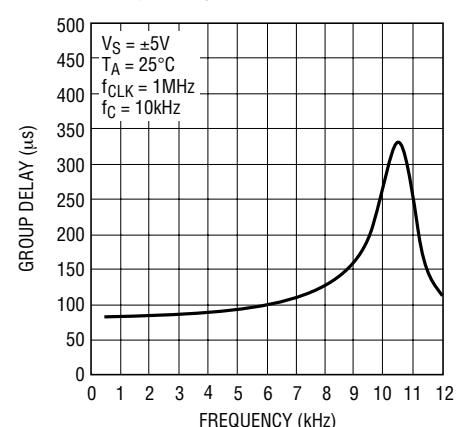
1064 G01

Phase vs Frequency



1064 G02

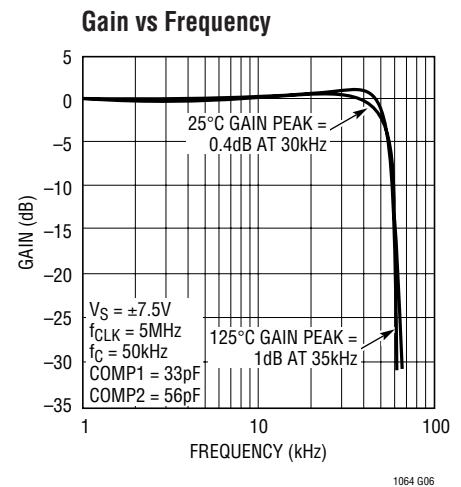
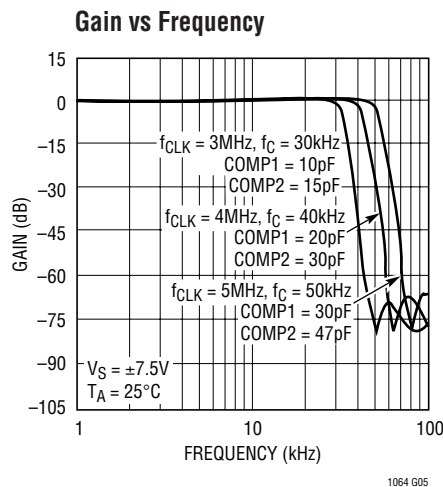
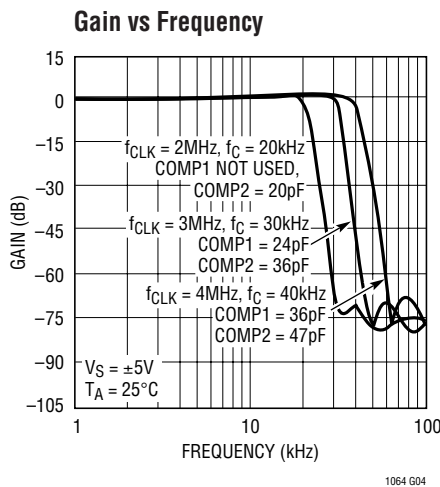
Group Delay



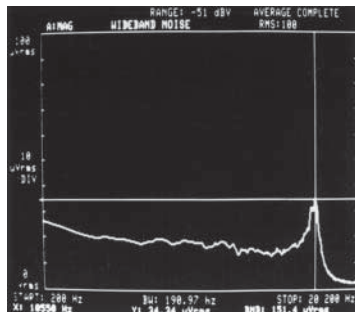
1064 G03

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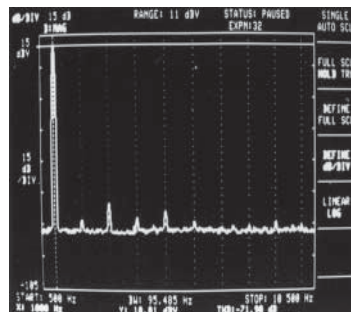
TYPICAL PERFORMANCE CHARACTERISTICS



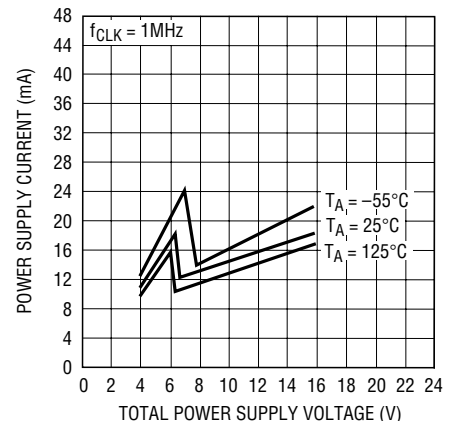
Typical Wideband Noise
(151 μ V_{RMS}) $V_S = \pm 5V$, $T_A = 25^\circ C$
 $f_{CLK} = 1MHz$, $f_C = 10kHz$ Input
Grounded



Total Harmonic Distortion
(0.025%) $V_S = \pm 7.5V$, $T_A = 25^\circ C$
 $f_{CLK} = 1MHz$, $f_C = 10kHz$
Input = 1kHz at 3V_{RMS}



Power Supply Current vs Power Supply Voltage



PIN FUNCTIONS (Pin Numbers Refer to the 14-Pin Package)

COMP1, INV A, COMP2, INV C (Pins 1, 6, 7, and 13): For filter cutoff frequencies higher than 20kHz, in order to minimize the passband ripple, compensation capacitors should be added between Pin 6 and Pin 7 (COMP1) and Pin 1 and Pin 13 (COMP2). For COMP1 (COMP2), add 1pF (1.5pF) mica capacitor for each kHz increase in cutoff frequency above 20kHz. For more detail refer to Gain vs Frequency graphs.

V_{IN}, V_{OUT} (Pins 2, 9): The input Pin 2 is connected to an 18k resistor tied to the inverting input of an op amp. Pin 2

is protected against static discharge. The device's output, Pin 9, is the output of an op amp which can typically source/sink 3mA/1mA. Although the internal op amps are unity gain stable, driving long coax cables is not recommended.

When testing the device for noise and distortion, the output, Pin 9, should be buffered (Figure 4). *The op amp power supply wire (or trace) should be connected directly to the power source.*

AGND (Pins 3, 5): For dual supply operation these pins should be connected to a ground plane. For single supply

PIN FUNCTIONS (Pin Numbers Refer to the 14-Pin Package)

operation both pins should be tied to one half supply (Figure 2). Also Pin 8 and Pin 10, although they are not internally connected should be tied to analog ground or system ground. This improves the clock feedthrough performance.

V⁺, V⁻ (Pins 4, 12): The V⁺ and V⁻ pins should be bypassed with a 0.1μF capacitor to an adequate analog ground. Low noise, nonswitching power supplies are recommended. *To avoid latchup when the power supplies exhibit high turn-on transients, a 1N5817 Schottky diode should be added from the V⁺ and V⁻ pins to ground (Figure 1).*

INV A, R(h, I) (Pins 7, 14): A very short connection between Pin 14 and Pin 7 is recommended. This connection should be preferably done under the IC package. In a

breadboard, use a one inch, or less, shielded coaxial cable; the shield should be grounded. In a PC board, use a one inch trace or less; surround the trace by a ground plane.

NC (Pins 8, 10): The “no connection” pins preferably should be grounded.

f_{CLK} (Pin 11): For ±5V supplies the logic threshold level is 1.4V. For ±8V and 0V to 5V supplies the logic threshold levels are 2.2V and 3V respectively. The logic threshold levels vary ±100mV over the full military temperature range. The recommended duty cycle of the input clock is 50% although for clock frequencies below 500kHz the clock “on” time can be as low as 200ns. The maximum clock frequency for ±5V supplies is 4MHz. For ±7V supplies and above, the maximum clock frequency is 5MHz. Do not allow the clock levels to exceed the power supplies. For clock level shifting (see Figure 3).

TYPICAL APPLICATIONS

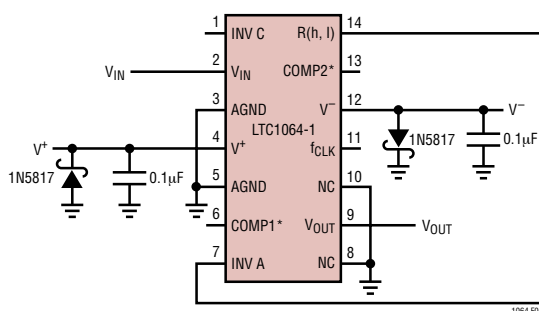


Figure 1. Using Schottky Diodes to Protect the IC from Power Supply Spikes

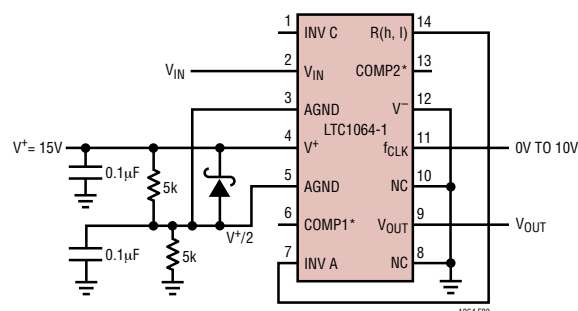


Figure 2. Single Supply Operation. If Fast Power Up or Down Transients are Expected, Use a 1N5817 Schottky Diode Between Pin 4 and Pin 5.

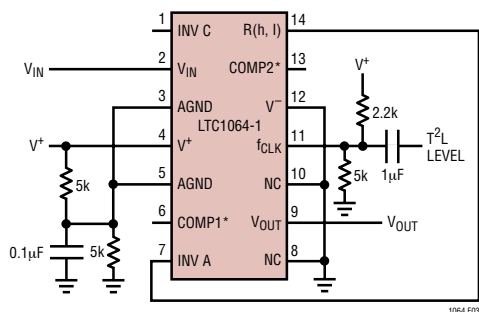


Figure 3. Level Shifting the Input T²L Clock for Single Supply Operation, V₊ > 6V.

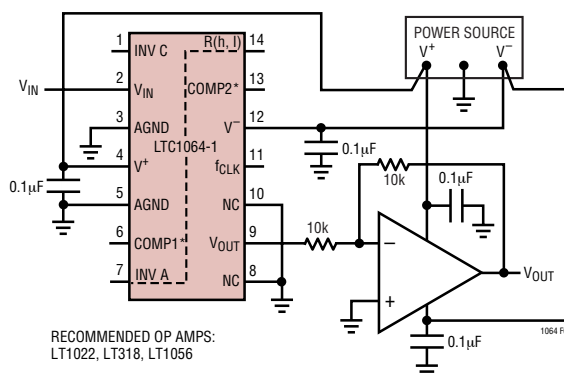
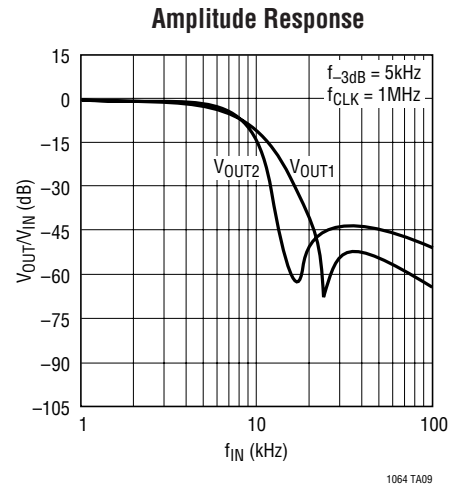
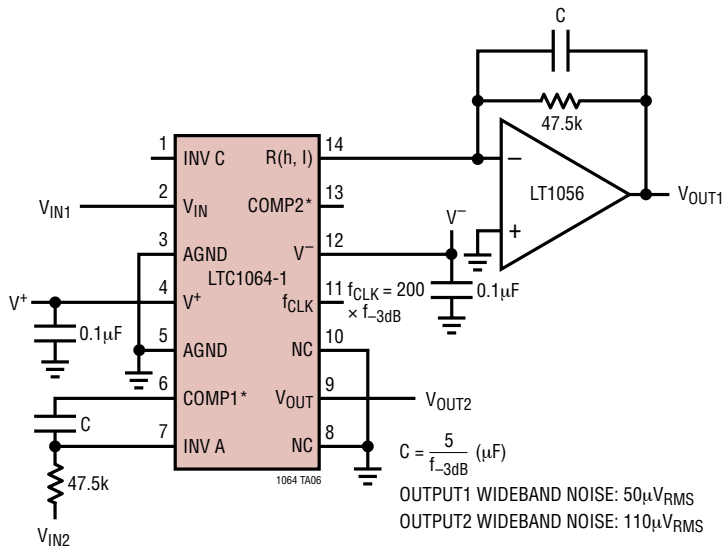


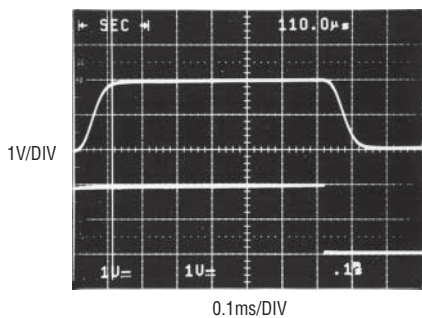
Figure 4. Buffering the Filter Output. The Buffer Op Amp Should Not Share the LTC1064-1 Power Lines.

TYPICAL APPLICATIONS

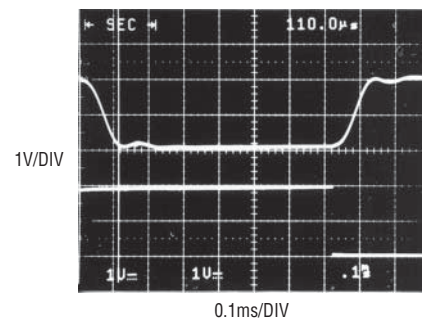
Transitional Elliptic-Bessel Dual 5th Order Lowpass Filter



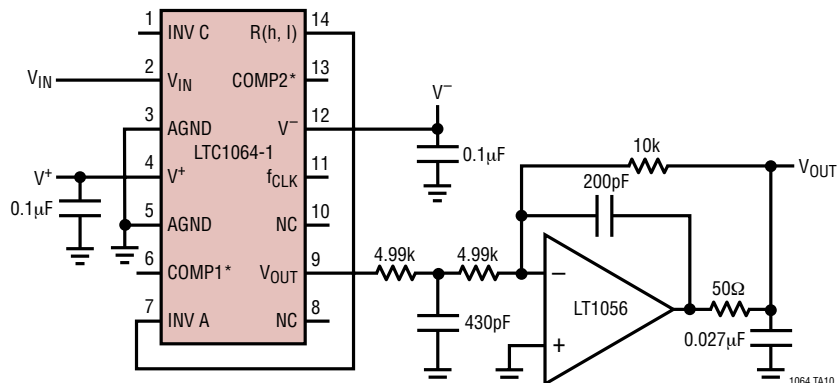
Transient Response to a 2V Step Input $V_{\text{OUT}2}$



Transient Response to a 2V Step Input $V_{\text{OUT}1}$

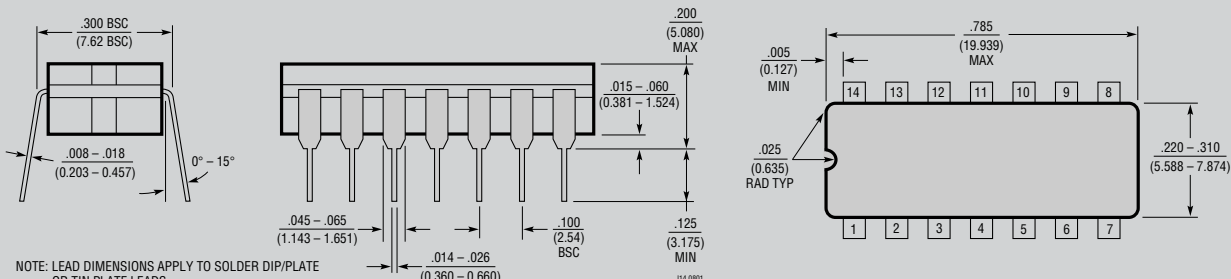


Adding an Output Buffer-Filter to Eliminate Any Clock Feedthrough Over a 10:1 Clock Range, for $f_{\text{CLK}} = 2\text{kHz}$ to 20kHz



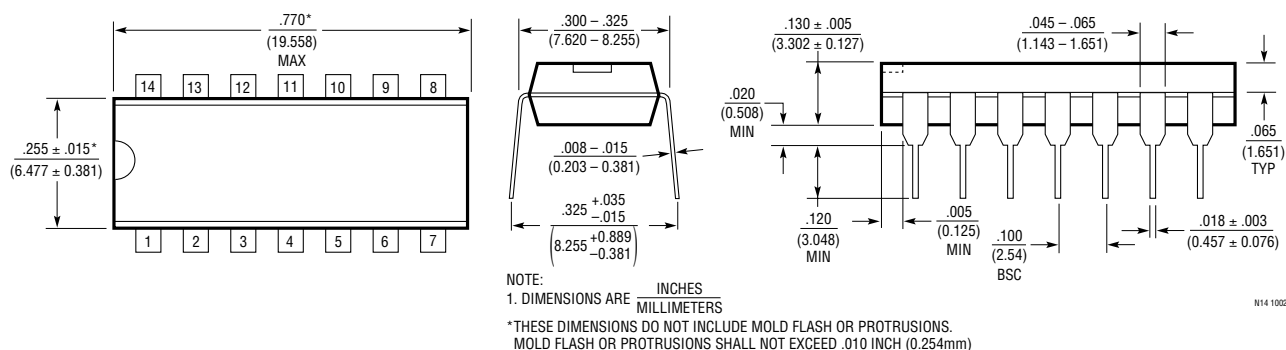
PACKAGE DESCRIPTION

J Package 14-Lead CERDIP (Narrow 0.300, Hermetic) (LTC DWG # 05-08-1110)

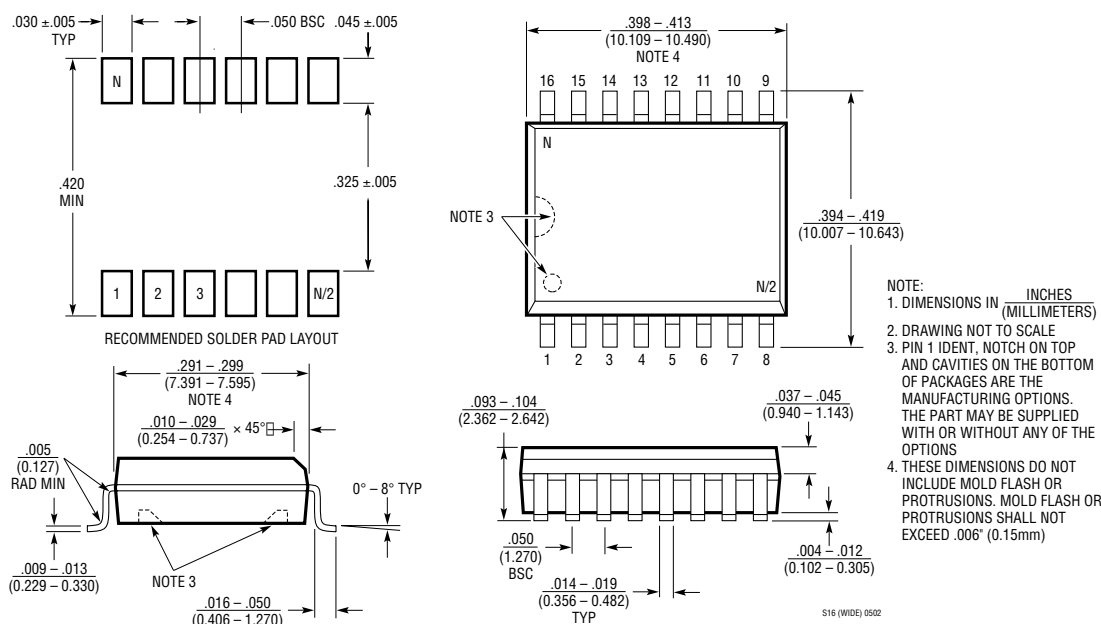


OBSOLETE PACKAGE

N Package 14-Lead PDIP (Narrow 0.300) (LTC DWG # 05-08-1510)

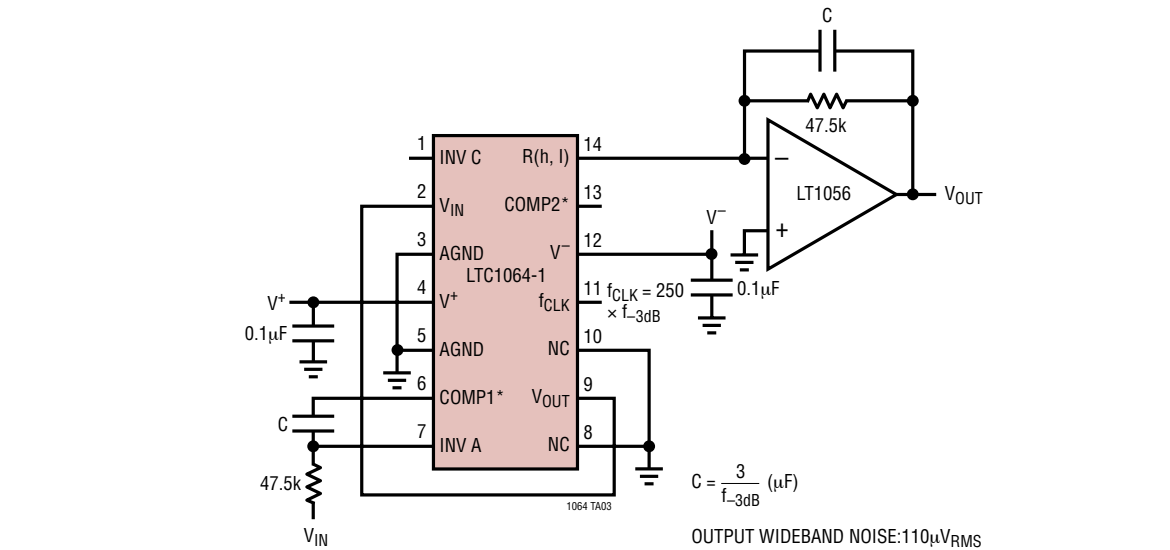


SW Package 16-Lead Plastic Small Outline (Wide .300 Inch) (Reference LTC DWG # 05-08-1620)

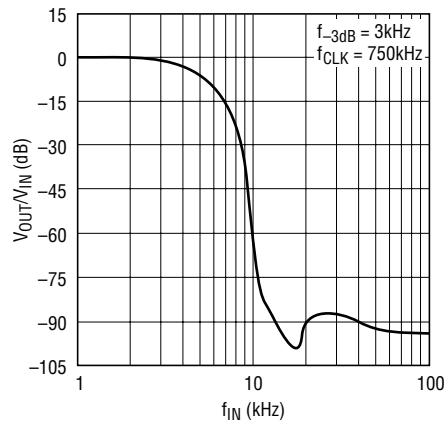


TYPICAL APPLICATION

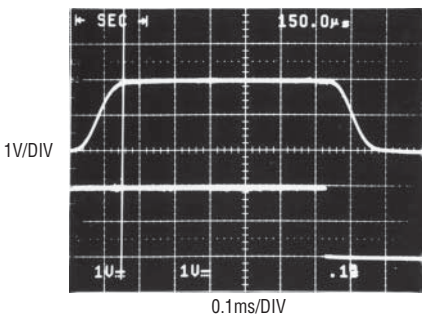
Transitional Elliptic-Bessel 10th Order Lowpass Filter



Amplitude Response



Transient Response to a 2V Step Input



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1069-1	8th Order Elliptic Lowpass	S0-8 Package, Low Power
LTC1069-6	Single Supply, 8th Order Elliptic Lowpass	S0-8 Package, Very Low Power
LTC1569-6	DC Accurate, 10th Order, Lowpass	Internal Precision Clock, Low Power
LTC1569-7	DC Accurate, 10th Order, Lowpass	Internal Precision Clock, S0-8 Package



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Электрон
Связь**

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