

**FEATURES**

- 1  $\Omega$  typical on resistance
- 0.2  $\Omega$  on resistance flatness
- $\pm 3.3$  V to  $\pm 8$  V dual-supply operation
- 3.3 V to 16 V single-supply operation
- No  $V_L$  supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- Continuous current per channel
  - LFCSP: 504 mA
  - TSSOP: 315 mA
- 14-lead TSSOP and 16-lead, 4 mm  $\times$  4 mm LFCSP

**APPLICATIONS**

- Communication systems
- Medical systems
- Audio signal routing
- Video signal routing
- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Relay replacements

**GENERAL DESCRIPTION**

The **ADG1604** is a complementary metal-oxide semiconductor (CMOS) analog multiplexer and switches one of four inputs to a common output, D, as determined by the 3-bit binary address lines, A0, A1, and EN. Logic 0 on the EN pin disables the device. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

The ultralow on resistance of these switches make them ideal solutions for data acquisition and gain switching applications where low on resistance and distortion is critical. The on resistance profile is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching audio signals.

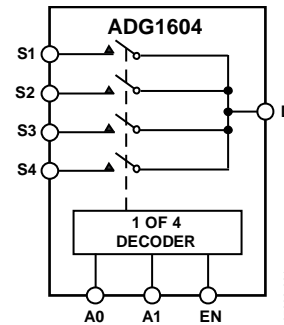
**FUNCTIONAL BLOCK DIAGRAM**

Figure 1.

The CMOS construction ensures ultralow power dissipation, making the devices ideally suited for portable and battery-powered instruments.

**PRODUCT HIGHLIGHTS**

1. 1.6  $\Omega$  maximum on resistance over temperature.
2. Minimum distortion: THD + N = 0.007%.
3. 3 V logic-compatible digital inputs:  $V_{INH} = 2.0$  V,  $V_{INL} = 0.8$  V.
4. No  $V_L$  logic power supply required.
5. Ultralow power dissipation: <16 nW.
6. 14-lead TSSOP and 16-lead, 4 mm  $\times$  4 mm LFCSP.

Rev. B

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## REVISION HISTORY

### 3/16—Rev. A to Rev. B

Changed CP-16-13 to CP-16-26 .....	Throughout
Changes to Figure 2, Figure 3, and Table 7 .....	9
Updated Outline Dimensions .....	17
Changes to Ordering Guide .....	17

### 9/09—Rev. 0 to Rev. A

Changes to On Resistance ( $R_{ON}$ ) Parameter, On Resistance Match Between Channels ( $\Delta R_{ON}$ ) Parameter, and On Resistance Flatness ( $R_{FLATON}$ ) Parameter, Table 4 .....	6
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### 1/09—Revision 0: Initial Version

## SPECIFICATIONS

## ±5 V DUAL SUPPLY

$V_{DD} = +5\text{ V} \pm 10\%$ ,  $V_{SS} = -5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

Table 1.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	
On Resistance ( $R_{ON}$ )	1			$\Omega$ typ	$V_S = \pm 4.5\text{ V}$ , $I_S = -10\text{ mA}$ ; see Figure 22
	1.2	1.4	1.6	$\Omega$ max	$V_{DD} = \pm 4.5\text{ V}$ , $V_{SS} = \pm 4.5\text{ V}$
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.04			$\Omega$ typ	$V_S = \pm 4.5\text{ V}$ , $I_S = -10\text{ mA}$
	0.08	0.09	0.1	$\Omega$ max	
On Resistance Flatness ( $R_{FLAT(ON)}$ )	0.2			$\Omega$ typ	$V_S = \pm 4.5\text{ V}$ , $I_S = -10\text{ mA}$
	0.25	0.29	0.34	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.1$			nA typ	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$
	$\pm 0.2$	$\pm 1$	$\pm 8$	nA max	$V_S = \pm 4.5\text{ V}$ , $V_D = \mp 4.5\text{ V}$ ; see Figure 23
Drain Off Leakage, $I_D$ (Off)	$\pm 0.1$			nA typ	$V_S = \pm 4.5\text{ V}$ , $V_D = \mp 4.5\text{ V}$ ; see Figure 23
	$\pm 0.2$	$\pm 2$	$\pm 16$	nA max	
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.2$			nA typ	$V_S = V_D = \pm 4.5\text{ V}$ ; see Figure 24
	$\pm 0.4$	$\pm 2$	$\pm 16$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	8			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
Transition Time, $t_{TRANSITION}$	150			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	278	336	376	ns max	$V_S = 2.5\text{ V}$ ; see Figure 29
$t_{ON}$ (EN)	116			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	146	166	177	ns max	$V_S = 2.5\text{ V}$ ; see Figure 31
$t_{OFF}$ (EN)	186			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	234	277	310	ns max	$V_S = 2.5\text{ V}$ ; see Figure 31
Break-Before-Make Time Delay, $t_D$	50			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
			28.5	ns min	$V_{S1} = V_{S2} = 2.5\text{ V}$ ; see Figure 30
Charge Injection	140			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 32
Off Isolation	70			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 25
Channel-to-Channel Crosstalk	70			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 27
Total Harmonic Distortion + Noise (THD + N)	0.007			% typ	$R_L = 110\ \Omega$ , $5\text{ V p-p}$ , $f = 20\text{ Hz}$ to $20\text{ kHz}$ ; see Figure 28
-3 dB Bandwidth	15			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 26
$C_S$ (Off)	63			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)	270			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ , $C_S$ (On)	360			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$
			1.0	$\mu\text{A}$ max	Digital inputs = $0\text{ V}$ or $V_{DD}$
$V_{DD}/V_{SS}$			$\pm 3.3/\pm 8$	V min/max	

<sup>1</sup> Guaranteed by design, not subject to production test.

**12 V SINGLE SUPPLY**

$V_{DD} = 12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 2.**

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	0.95			$\Omega$ typ	$V_S = 0\text{ V to }10\text{ V}$ , $I_S = -10\text{ mA}$ ; see Figure 22
	1.1	1.25	1.45	$\Omega$ max	$V_{DD} = 10.8\text{ V}$ , $V_{SS} = 0\text{ V}$
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.03			$\Omega$ typ	$V_S = 10\text{ V}$ , $I_S = -10\text{ mA}$
	0.06	0.07	0.08	$\Omega$ max	
On Resistance Flatness ( $R_{FLAT(ON)}$ )	0.2			$\Omega$ typ	$V_S = 0\text{ V to }10\text{ V}$ , $I_S = -10\text{ mA}$
	0.23	0.27	0.32	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.1$			nA typ	$V_{DD} = 13.2\text{ V}$ , $V_{SS} = 0\text{ V}$
	$\pm 0.2$	$\pm 1$	$\pm 8$	nA max	$V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ ; see Figure 23
Drain Off Leakage, $I_D$ (Off)	$\pm 0.1$			nA typ	$V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ ; see Figure 23
	$\pm 0.2$	$\pm 2$	$\pm 16$	nA max	
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.2$			nA typ	$V_S = V_D = 1\text{ V or }10\text{ V}$ ; see Figure 24
	$\pm 0.4$	$\pm 2$	$\pm 16$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.001			$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	8			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
Transition Time, $t_{TRANSITION}$	100			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	161	192	220	ns max	$V_S = 8\text{ V}$ ; see Figure 29
$t_{ON}$ (EN)	80			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	95	104	111	ns max	$V_S = 8\text{ V}$ ; see Figure 31
$t_{OFF}$ (EN)	144			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	173	205	234	ns max	$V_S = 8\text{ V}$ ; see Figure 31
Break-Before-Make Time Delay, $t_D$	25			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
			18	ns min	$V_{S1} = V_{S2} = 8\text{ V}$ ; see Figure 30
Charge Injection	125			pC typ	$V_S = 6\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 32
Off Isolation	70			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 25
Channel-to-Channel Crosstalk	70			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 27
Total Harmonic Distortion + Noise	0.013			% typ	$R_L = 110\ \Omega$ , $5\text{ V p-p}$ , $f = 20\text{ Hz to }20\text{ kHz}$ ; see Figure 28
-3 dB Bandwidth	19			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 26
$C_S$ (Off)	60			pF typ	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)	270			pF typ	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ , $C_S$ (On)	350			pF typ	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = 12\text{ V}$
			1	$\mu\text{A}$ max	Digital inputs = 0 V or $V_{DD}$
$I_{DD}$	230			$\mu\text{A}$ typ	Digital inputs = 5 V
			360	$\mu\text{A}$ max	
$V_{DD}$			3.3/16	V min/max	

<sup>1</sup> Guaranteed by design, not subject to production test.

**5 V SINGLE SUPPLY**

$V_{DD} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 3.**

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	1.7			$\Omega$ typ	$V_S = 0\text{ V to } 4.5\text{ V}$ , $I_S = -10\text{ mA}$ ; see Figure 22
	2.15	2.4	2.7	$\Omega$ max	$V_{DD} = 4.5\text{ V}$ , $V_{SS} = 0\text{ V}$
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.05			$\Omega$ typ	$V_S = 0\text{ V to } 4.5\text{ V}$ , $I_S = -10\text{ mA}$
	0.09	0.12	0.15	$\Omega$ max	
On Resistance Flatness ( $R_{FLAT(ON)}$ )	0.4			$\Omega$ typ	$V_S = 0\text{ V to } 4.5\text{ V}$ , $I_S = -10\text{ mA}$
	0.53	0.55	0.6	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.05$			nA typ	$V_{DD} = 5.5\text{ V}$ , $V_{SS} = 0\text{ V}$
	$\pm 0.2$	$\pm 1$	$\pm 8$	nA max	$V_S = 1\text{ V}/4.5\text{ V}$ , $V_D = 4.5\text{ V}/1\text{ V}$ ; see Figure 23
Drain Off Leakage, $I_D$ (Off)	$\pm 0.05$			nA typ	$V_S = 1\text{ V}/4.5\text{ V}$ , $V_D = 4.5\text{ V}/1\text{ V}$ ; see Figure 23
	$\pm 0.2$	$\pm 2$	$\pm 16$	nA max	
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.1$			nA typ	$V_S = V_D = 1\text{ V or } 4.5\text{ V}$ ; see Figure 24
	$\pm 0.4$	$\pm 2$	$\pm 16$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.001			$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	8			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
Transition Time, $t_{TRANSITION}$	175			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	283	337	380	ns max	$V_S = 2.5\text{ V}$ ; see Figure 29
$t_{ON}$ (EN)	135			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	174	194	212	ns max	$V_S = 2.5\text{ V}$ ; see Figure 31
$t_{OFF}$ (EN)	228			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	288	342	385	ns max	$V_S = 2.5\text{ V}$ ; see Figure 31
Break-Before-Make Time Delay, $t_D$	30			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
			21	ns min	$V_{S1} = V_{S2} = 2.5\text{ V}$ ; see Figure 30
Charge Injection	70			pC typ	$V_S = 2.5\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 32
Off Isolation	70			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 25
Channel-to-Channel Crosstalk	70			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 27
Total Harmonic Distortion + Noise	0.09			% typ	$R_L = 110\ \Omega$ , $f = 20\text{ Hz to } 20\text{ kHz}$ , $V_S = 3.5\text{ V p-p}$ ; see Figure 28
-3 dB Bandwidth	16			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 26
$C_S$ (Off)	70			pF typ	$V_S = 2.5\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)	300			pF typ	$V_S = 2.5\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ , $C_S$ (On)	400			pF typ	$V_S = 2.5\text{ V}$ , $f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = 5.5\text{ V}$
			1	$\mu\text{A}$ max	Digital inputs = 0 V or $V_{DD}$
$V_{DD}$			3.3/16	V min/max	

<sup>1</sup> Guaranteed by design, not subject to production test.

**3.3 V SINGLE SUPPLY**

$V_{DD} = 3.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 4.**

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	3.2	3.4	3.6	$\Omega$ typ	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_S = -10\text{ mA}$ , $V_{DD} = 3.3\text{ V}$ , $V_{SS} = 0\text{ V}$ ; see Figure 22
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.06	0.07	0.08	$\Omega$ typ	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_S = -10\text{ mA}$
On Resistance Flatness ( $R_{FLAT(ON)}$ )	1.2	1.3	1.4	$\Omega$ typ	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_S = -10\text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.02$			nA typ	$V_{DD} = 3.6\text{ V}$ , $V_{SS} = 0\text{ V}$
	$\pm 0.25$	$\pm 1$	$\pm 8$	nA max	$V_S = 0.6\text{ V}/3\text{ V}$ , $V_D = 3\text{ V}/0.6\text{ V}$ ; see Figure 23
Drain Off Leakage, $I_D$ (Off)	$\pm 0.02$			nA typ	$V_S = 0.6\text{ V}/3\text{ V}$ , $V_D = 3\text{ V}/0.6\text{ V}$ ; see Figure 23
	$\pm 0.25$	$\pm 2$	$\pm 16$	nA max	
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.05$			nA typ	$V_S = V_D = 0.6\text{ V}$ or $3\text{ V}$ ; see Figure 24
	$\pm 0.6$	$\pm 2$	$\pm 16$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.001			$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	8			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
Transition Time, $t_{TRANSITION}$	280			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	460	526	575	ns max	$V_S = 1.5\text{ V}$ ; see Figure 29
$t_{ON}$ (EN)	227			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	308	332	346	ns max	$V_S = 1.5\text{ V}$ ; see Figure 31
$t_{OFF}$ (EN)	357			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	480	549	601	ns max	$V_S = 1.5\text{ V}$ ; see Figure 31
Break-Before-Make Time Delay, $t_D$	25			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
			20	ns min	$V_{S1} = V_{S2} = 1.5\text{ V}$ ; see Figure 30
Charge Injection	60			pC typ	$V_S = 1.5\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 32
Off Isolation	70			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 25
Channel-to-Channel Crosstalk	70			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 27
Total Harmonic Distortion + Noise	0.15			% typ	$R_L = 110\ \Omega$ , $f = 20\text{ Hz}$ to $20\text{ kHz}$ , $V_S = 2\text{ V p-p}$ ; see Figure 28
-3 dB Bandwidth	15			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 26
$C_S$ (Off)	76			pF typ	$V_S = 1.5\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)	316			pF typ	$V_S = 1.5\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ , $C_S$ (On)	420			pF typ	$V_S = 1.5\text{ V}$ , $f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = 3.6\text{ V}$
		1.0	1.0	$\mu\text{A}$ max	Digital inputs = 0 V or $V_{DD}$
$V_{DD}$			3.3/16	V min/max	

<sup>1</sup> Guaranteed by design, not subject to production test.

**CONTINUOUS CURRENT PER CHANNEL, S OR D**

Table 5.

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, S OR D				
$V_{DD} = +5\text{ V}, V_{SS} = -5\text{ V}$				
TSSOP ( $\theta_{JA} = 150.4^\circ\text{C/W}$ )	315	189	95	mA maximum
LFCSP ( $\theta_{JA} = 48.7^\circ\text{C/W}$ )	504	259	112	mA maximum
$V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V}$				
TSSOP ( $\theta_{JA} = 150.4^\circ\text{C/W}$ )	378	221	112	mA maximum
LFCSP ( $\theta_{JA} = 48.7^\circ\text{C/W}$ )	627	311	126	mA maximum
$V_{DD} = 5\text{ V}, V_{SS} = 0\text{ V}$				
TSSOP ( $\theta_{JA} = 150.4^\circ\text{C/W}$ )	249	158	91	mA maximum
LFCSP ( $\theta_{JA} = 48.7^\circ\text{C/W}$ )	403	224	105	mA maximum
$V_{DD} = 3.3\text{ V}, V_{SS} = 0\text{ V}$				
TSSOP ( $\theta_{JA} = 150.4^\circ\text{C/W}$ )	256	165	98	mA maximum
LFCSP ( $\theta_{JA} = 48.7^\circ\text{C/W}$ )	410	235	116	mA maximum

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 6.**

Parameter	Rating
$V_{DD}$ to $V_{SS}$	18 V
$V_{DD}$ to GND	-0.3 V to +18 V
$V_{SS}$ to GND	+0.3 V to -18 V
Analog Inputs <sup>1</sup>	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs <sup>1</sup>	GND - 0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, S or D	1150 mA (pulsed at 1 ms, 10% duty-cycle maximum)
Continuous Current, S or D <sup>2</sup>	Data + 15%
Operating Temperature Range	
Industrial (Y Version)	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
$\theta_{JA}$ Thermal Impedance	
16-Lead TSSOP, 2-Layer Board	150.4°C/W
16-Lead LFCSP, 4-Layer Board	48.7°C/W
Reflow Soldering Peak Temperature, Pb free	260°C

<sup>1</sup> Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

<sup>2</sup> See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

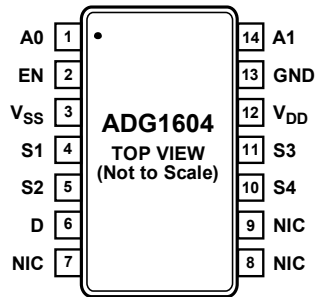
### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



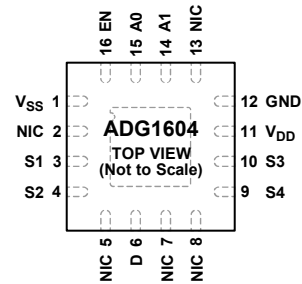
## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES  
1. NIC = NO INTERNAL CONNECTION.

Figure 2. 14-Lead TSSOP Pin Configuration

07982-002



NOTES  
1. NIC = NO INTERNAL CONNECTION.  
2. TIE THE EXPOSED PAD TO THE SUBSTRATE, VSS.

Figure 3. 16-Lead LFCSP Pin Configuration

07982-003

Table 7. Pin Function Descriptions

Pin No.		Mnemonic	Description
14-Lead TSSOP	16-Lead LFCSP		
1	15	A0	Logic Control Input.
2	16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, the Ax logic inputs determine the on switch.
3	1	V <sub>SS</sub>	Most Negative Power Supply Potential.
4	3	S1	Source Terminal. This pin can be an input or output.
5	4	S2	Source Terminal. This pin can be an input or output.
6	6	D	Drain Terminal. This pin can be an input or output.
7, 8, 9	2, 5, 7, 8, 13	NIC	No Internal Connection.
10	9	S4	Source Terminal. This pin can be an input or output.
11	10	S3	Source Terminal. This pin can be an input or output.
12	11	V <sub>DD</sub>	Most Positive Power Supply Potential.
13	12	GND	Ground (0 V) Reference.
14	14	A1	Logic Control Input.
N/A <sup>1</sup>	0	EPAD	Exposed Pad. Tie the exposed pad to the substrate, V <sub>SS</sub> .

<sup>1</sup> N/A means not applicable.

Table 8. ADG1604 Truth Table

EN	A1	A0	S1	S2	S3	S4
0	X	X	Off	Off	Off	Off
1	0	0	On	Off	Off	Off
1	0	1	Off	On	Off	Off
1	1	0	Off	Off	On	Off
1	1	1	Off	Off	Off	On

TYPICAL PERFORMANCE CHARACTERISTICS

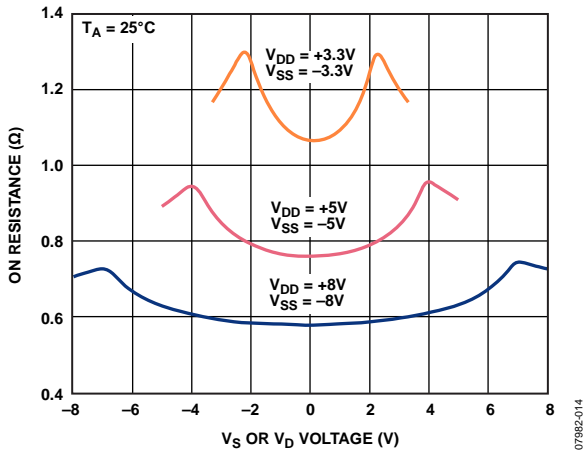


Figure 4. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Dual Supply

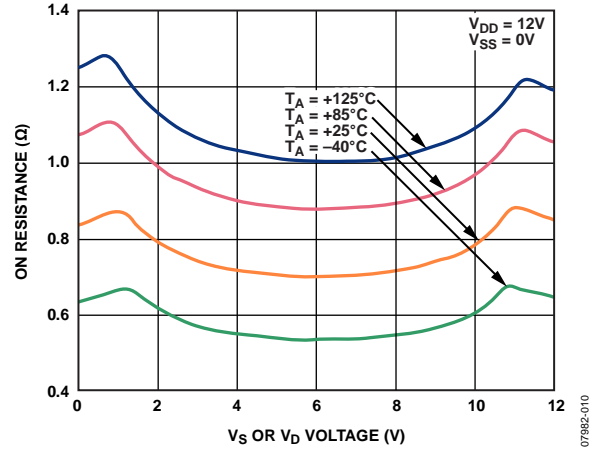


Figure 7. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, 12 V Single Supply

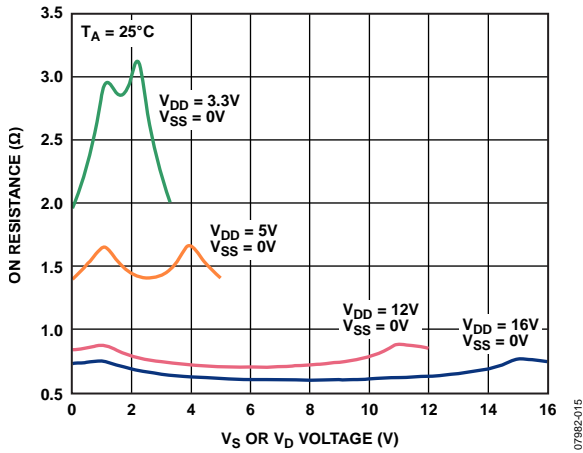


Figure 5. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Single Supply

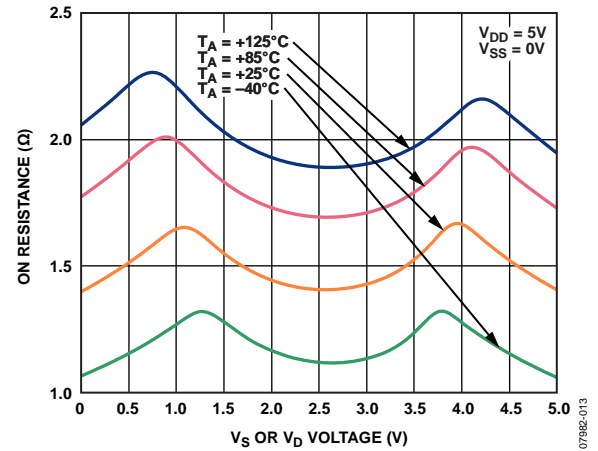


Figure 8. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, 5 V Single Supply

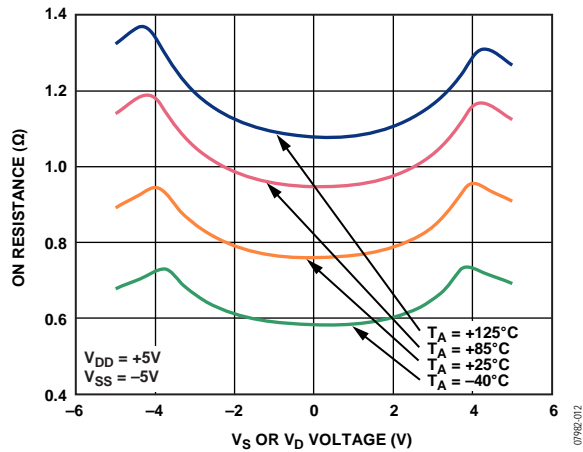


Figure 6. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures,  $\pm 5$  V Dual Supply

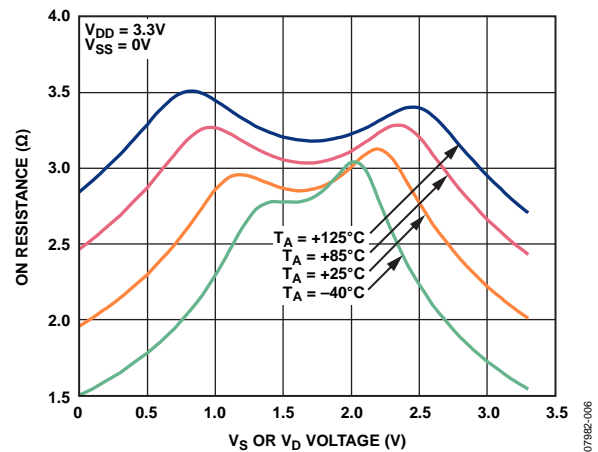


Figure 9. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, 3.3 V Single Supply

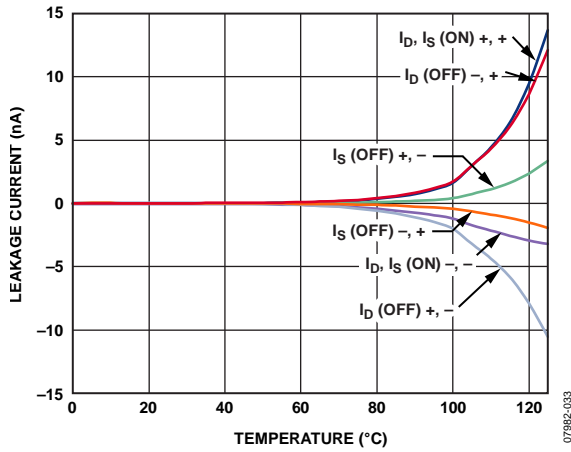


Figure 10. Leakage Currents as a Function of Temperature,  $\pm 5$  V Dual Supply

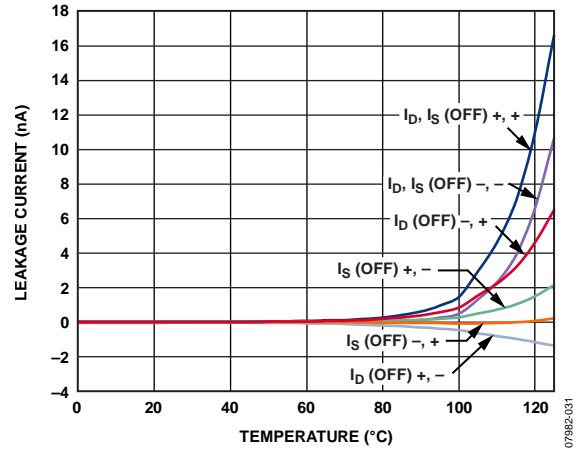


Figure 13. Leakage Currents as a Function of Temperature, 3.3 V Single Supply

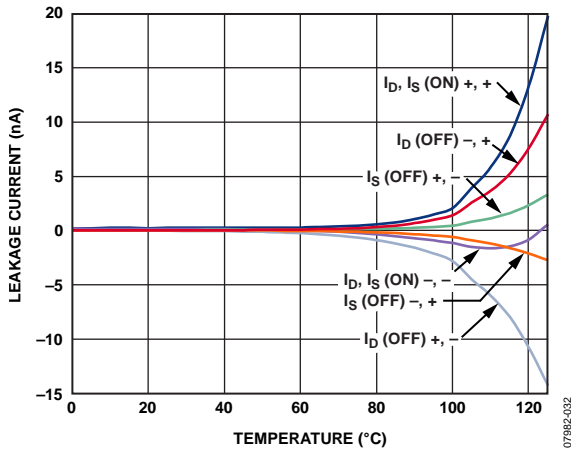


Figure 11. Leakage Currents as a Function of Temperature, 12 V Single Supply

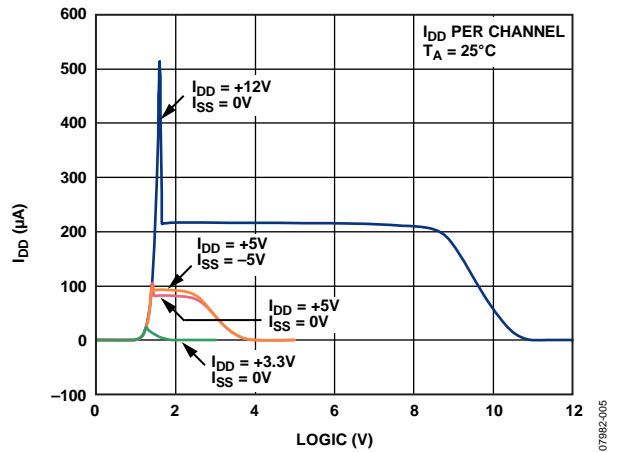


Figure 14.  $I_{DD}$  vs. Logic Level

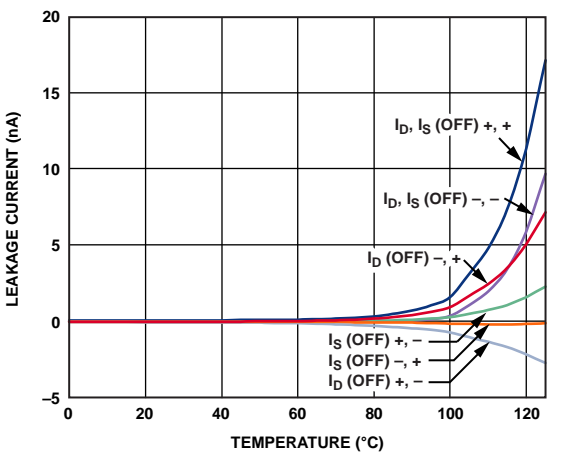


Figure 12. Leakage Currents as a Function of Temperature, 5 V Single Supply

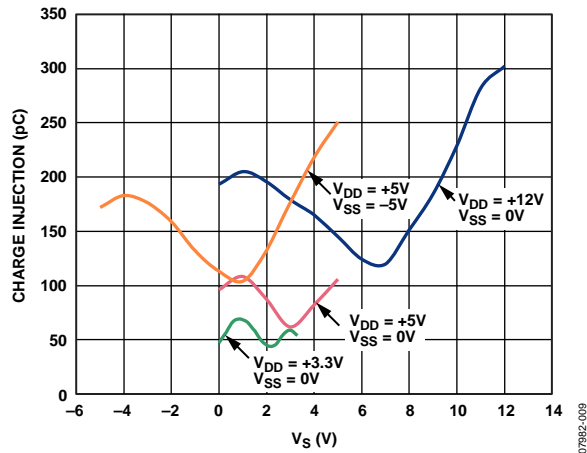


Figure 15. Charge Injection vs. Source Voltage

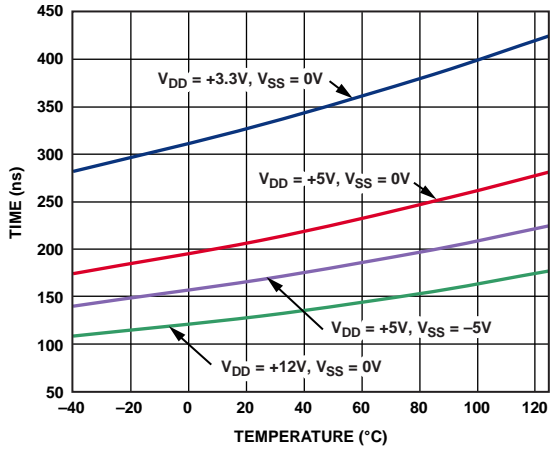


Figure 16.  $t_{ON}/t_{OFF}$  Times vs. Temperature

07982-019

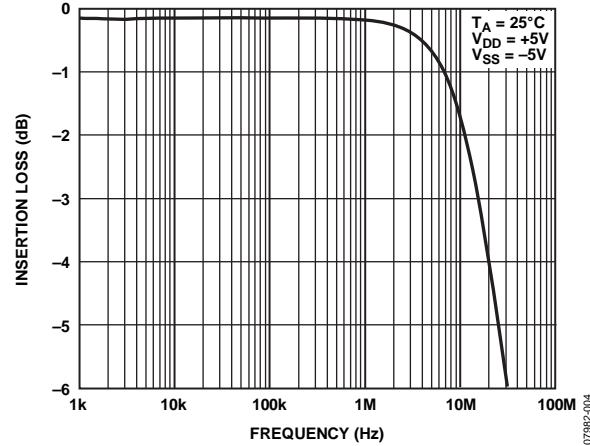


Figure 19. On Response vs. Frequency

07982-004

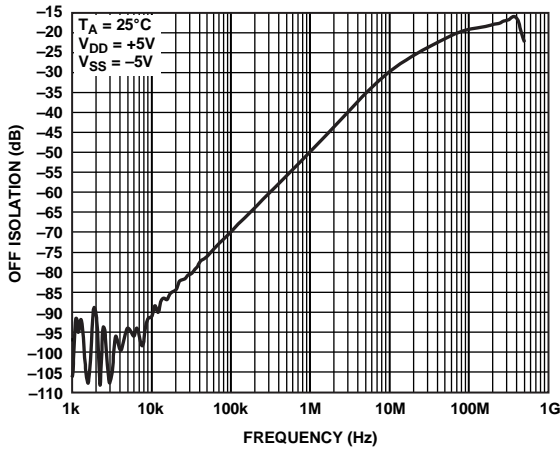


Figure 17. Off Isolation vs. Frequency

07982-007

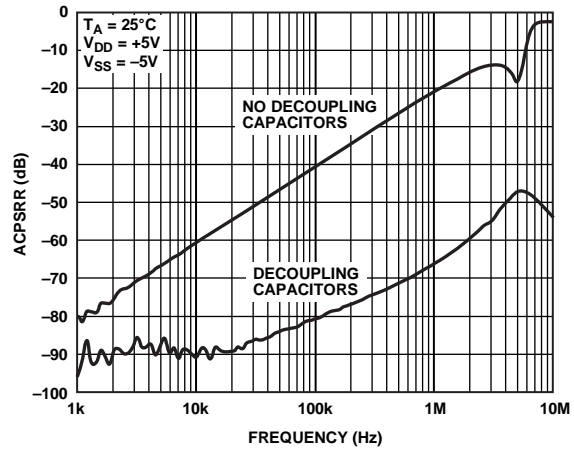


Figure 20. ACPSRR vs. Frequency

07982-008

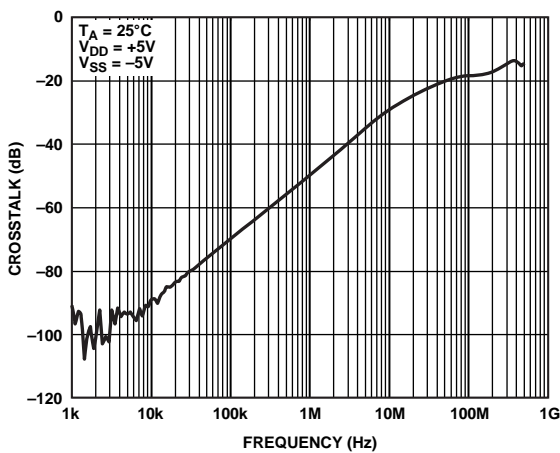


Figure 18. Crosstalk vs. Frequency

07982-018

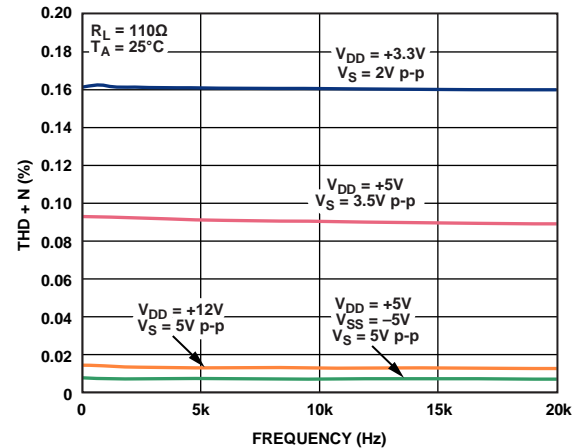


Figure 21. THD + N vs. Frequency

07982-017

TEST CIRCUITS

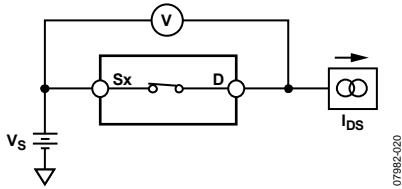
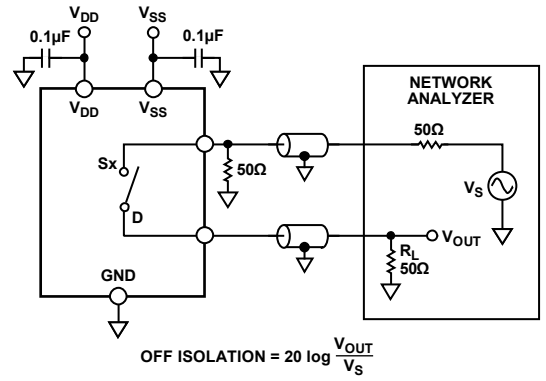


Figure 22. On Resistance

07982-020



$$\text{OFF ISOLATION} = 20 \log \frac{V_{\text{OUT}}}{V_s}$$

Figure 25. Off Isolation

07982-027

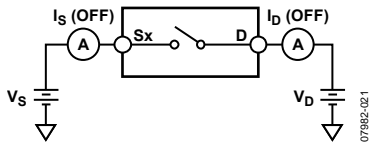
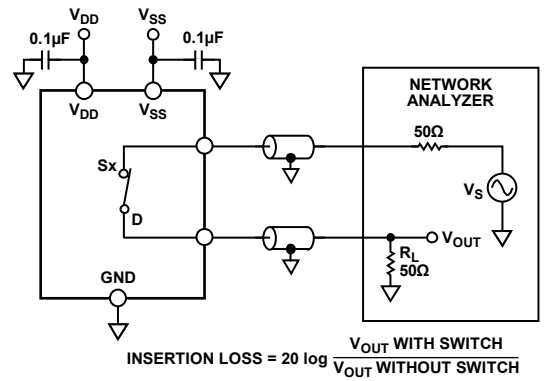


Figure 23. Off Leakage

07982-021



$$\text{INSERTION LOSS} = 20 \log \frac{V_{\text{OUT WITH SWITCH}}}{V_{\text{OUT WITHOUT SWITCH}}}$$

Figure 26. Bandwidth

07982-028

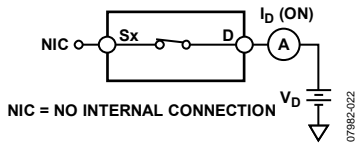
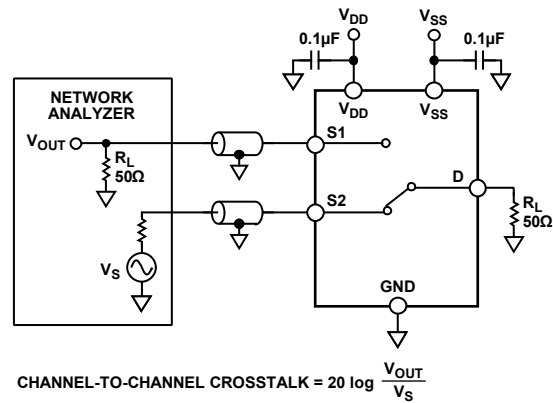


Figure 24. On Leakage

07982-022



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{\text{OUT}}}{V_s}$$

Figure 27. Channel-to-Channel Crosstalk

07982-029

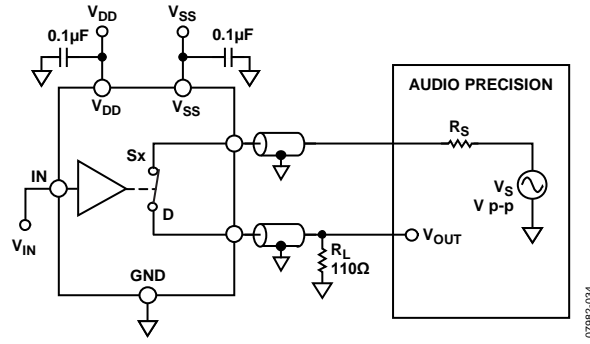


Figure 28. THD + Noise

07982-034

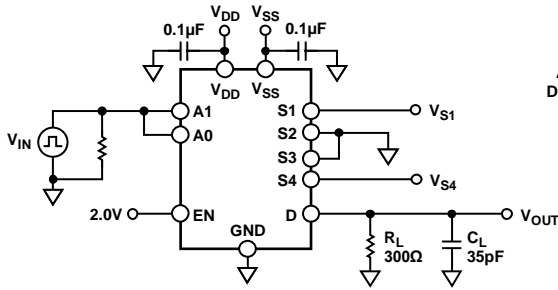
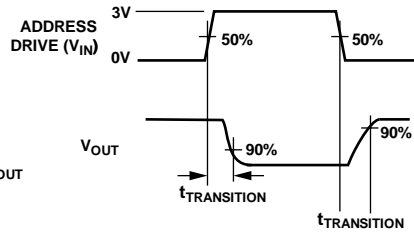


Figure 29. Address to Output Switching Times



07982-023

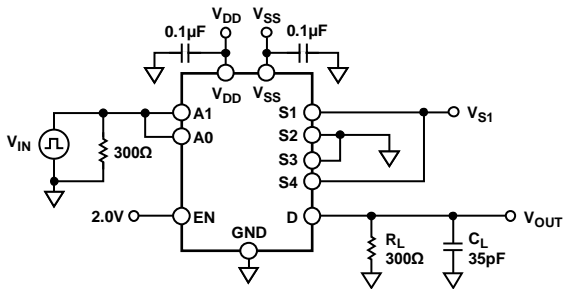
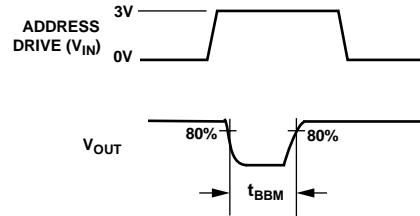


Figure 30. Break-Before-Make Time Delay



07982-024

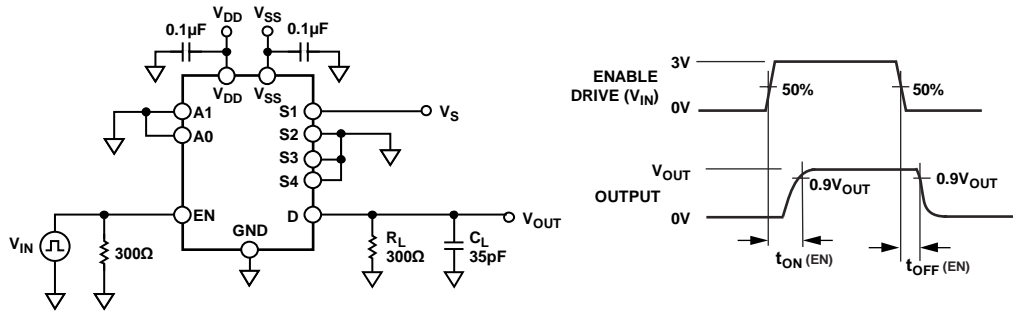


Figure 31. Enable-to-Output Switching Delay

07982-025

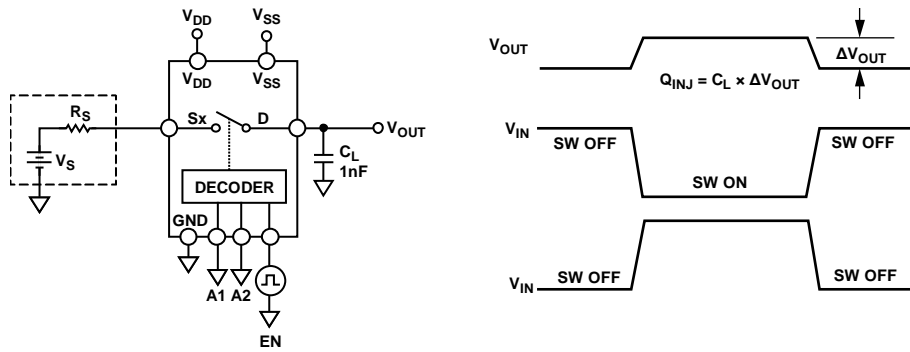


Figure 32. Charge Injection

07982-026

## TERMINOLOGY

### $I_{DD}$

The positive supply current.

### $I_{SS}$

The negative supply current.

### $V_D$ ( $V_S$ )

The analog voltage on Terminal D and Terminal S.

### $R_{ON}$

The ohmic resistance between Terminal D and Terminal S.

### $R_{FLAT(ON)}$

Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

### $I_S$ (Off)

The source leakage current with the switch off.

### $I_D$ (Off)

The drain leakage current with the switch off.

### $I_D, I_S$ (On)

The channel leakage current with the switch on.

### $V_{INL}$

The maximum input voltage for Logic 0.

### $V_{INH}$

The minimum input voltage for Logic 1.

### $I_{INL}$ ( $I_{INH}$ )

The input current of the digital input.

### $C_S$ (Off)

The off switch source capacitance, which is measured with reference to ground.

### $C_D$ (Off)

The off switch drain capacitance, which is measured with reference to ground.

### $C_D, C_S$ (On)

The on switch capacitance, which is measured with reference to ground.

### $C_{IN}$

The digital input capacitance.

### $t_{TRANSITION}$

The delay time between the 50% and 90% points of the digital input and switch on condition when switching from one address state to another. See Figure 29.

### $t_{ON}$ (EN)

The delay between applying the digital control input and the output switching on. See Figure 31.

### $t_{OFF}$ (EN)

The delay between applying the digital control input and the output switching off. See Figure 31.

### Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching. See Figure 32.

### Off Isolation

A measure of unwanted signal coupling through an off switch. See Figure 25.

### Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. See Figure 27.

### Bandwidth

The frequency at which the output is attenuated by 3 dB. See Figure 26.

### On Response

The frequency response of the on switch.

### Insertion Loss

The loss due to the on resistance of the switch.

### Total Harmonic Distortion + Noise (THD + N)

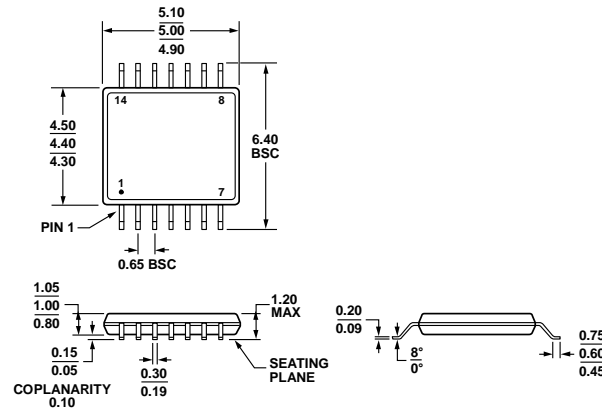
The ratio of the harmonic amplitude plus noise of the signal to the fundamental. See Figure 28.

### AC Power Supply Rejection Ratio (ACPSRR)

The ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.



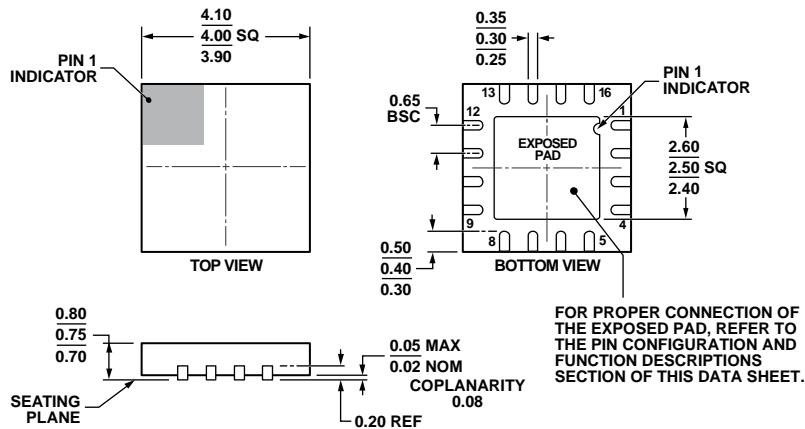
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 33. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 34. 16-Lead Lead Frame Chip Scale Package [LFCS] 4 mm x 4 mm Body and 0.75 mm Package Height (CP-16-26)

Dimensions shown in millimeters

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADG1604BRUZ	-40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
ADG1604BRUZ-REEL	-40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
ADG1604BRUZ-REEL7	-40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
ADG1604BCPZ-REEL	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCS]	CP-16-26
ADG1604BCPZ-REEL7	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCS]	CP-16-26

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

**NOTES**

**NOTES**



**Стандарт  
Электрон  
Связь**

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