

# 7.0V to 26V Input, 1.0A, Integrated MOSFET Single Synchronous Buck DC/DC Converter



## BD9E102FJ

### ● General Description

The BD9E102FJ is a synchronous buck switching regulator with low on-resistance built-in power MOSFETs. High efficiency at light load with a SLLM™. It is most suitable for use in the equipment to reduce the standby power is required. It is a current mode control DC/DC converter and features high-speed transient response. Phase compensation can also be set easily.

### ● Features

- Synchronous single DC/DC converter
- SLLM™ control (Simple Light Load Mode)
- Efficiency = 80% (@I<sub>OUT</sub>=10mA)
- Over current protection
- Short circuit protection
- Thermal shutdown protection
- Undervoltage lockout protection
- Soft start
- Reduce external diode
- SOP-J8 package

### ● Applications

- Consumer applications such as home appliance
- Secondary power supply and Adapter equipments
- Telecommunication devices

### ● Key Specifications

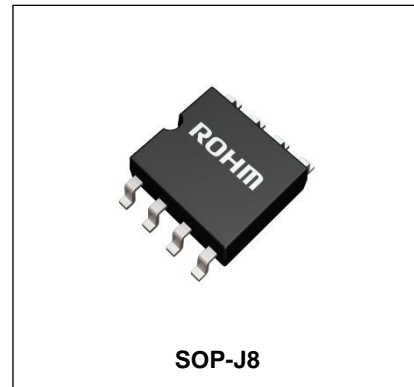
- Input voltage range: 7.0V to 26V
- Adjustable output voltage range: 1.0V to VIN x 0.7V
- Maximum output current: 1.0 A (Max.)
- Switching frequency: 570 kHz (Typ.)
- High-Side MOSFET on-resistance: 250 mΩ (Typ.)
- Low-Side MOSFET on-resistance: 200 mΩ (Typ.)
- Shutdown current: 0 μA (Typ.)

### ● Package

SOP-J8

### W (Typ.) x D (Typ.) x H (Max.)

4.90 mm x 6.00 mm x 1.65 mm



### ● Typical Application Circuit

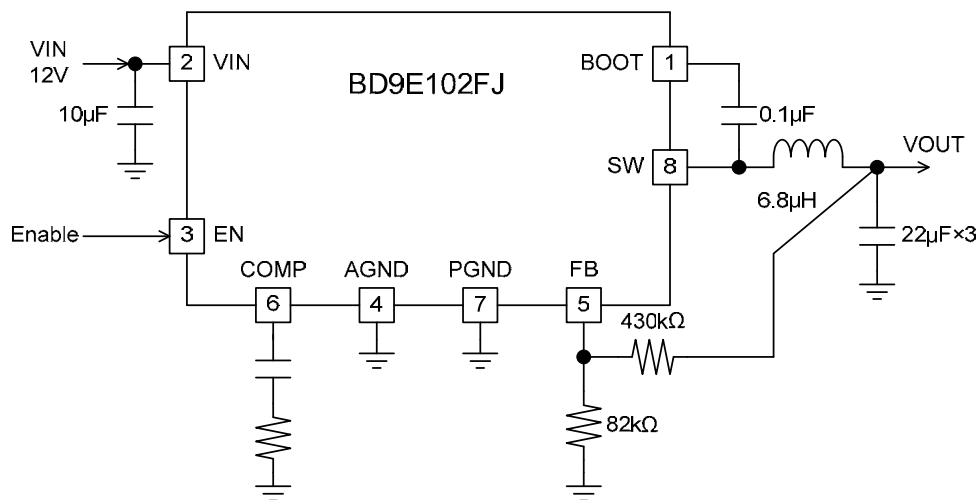


Figure 1. Application circuit

## ● Pin Configuration

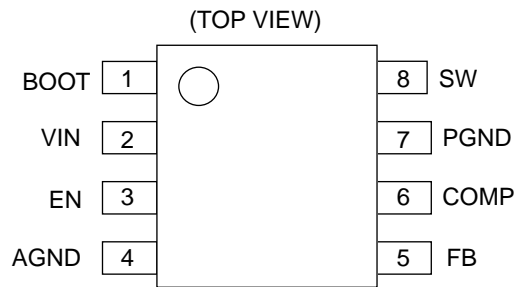


Figure 2. Pin assignment

## ● Pin Descriptions

Pin No.	Pin Name	Description
1	BOOT	Connect a bootstrap capacitor of 0.1 $\mu\text{F}$ between this terminal and SW terminals. The voltage of this capacitor is the gate drive voltage of the high-side MOSFET.
2	VIN	Power supply terminal for the switching regulator and control circuit. Connecting a 10 $\mu\text{F}$ ceramic capacitor is recommended.
3	EN	Turning this terminal signal low-level (0.8 V or lower) forces the device to enter the shut down mode. Turning this terminal signal high-level (2.0 V or higher) enables the device. This terminal must be terminated.
4	AGND	Ground terminal for the control circuit.
5	FB	Inverting input node for the gm error amplifier. See page 22 for how to calculate the resistance of the output voltage setting.
6	COMP	Input terminal for the gm error amplifier output and the output switch current comparator. Connect a frequency phase compensation component to this terminal. See page 22 for how to calculate the resistance and capacitance for phase compensation.
7	PGND	Ground terminals for the output stage of the switching regulator.
8	SW	Switch node. This terminal is connected to the source of the high-side MOSFET and drain of the low-side MOSFET. Connect a bootstrap capacitor of 0.1 $\mu\text{F}$ between these terminals and BOOT terminals. In addition, connect an inductor of 6.8 $\mu\text{H}$ with attention paid to the considering the direct current superimposition characteristic.

# ● Block Diagram

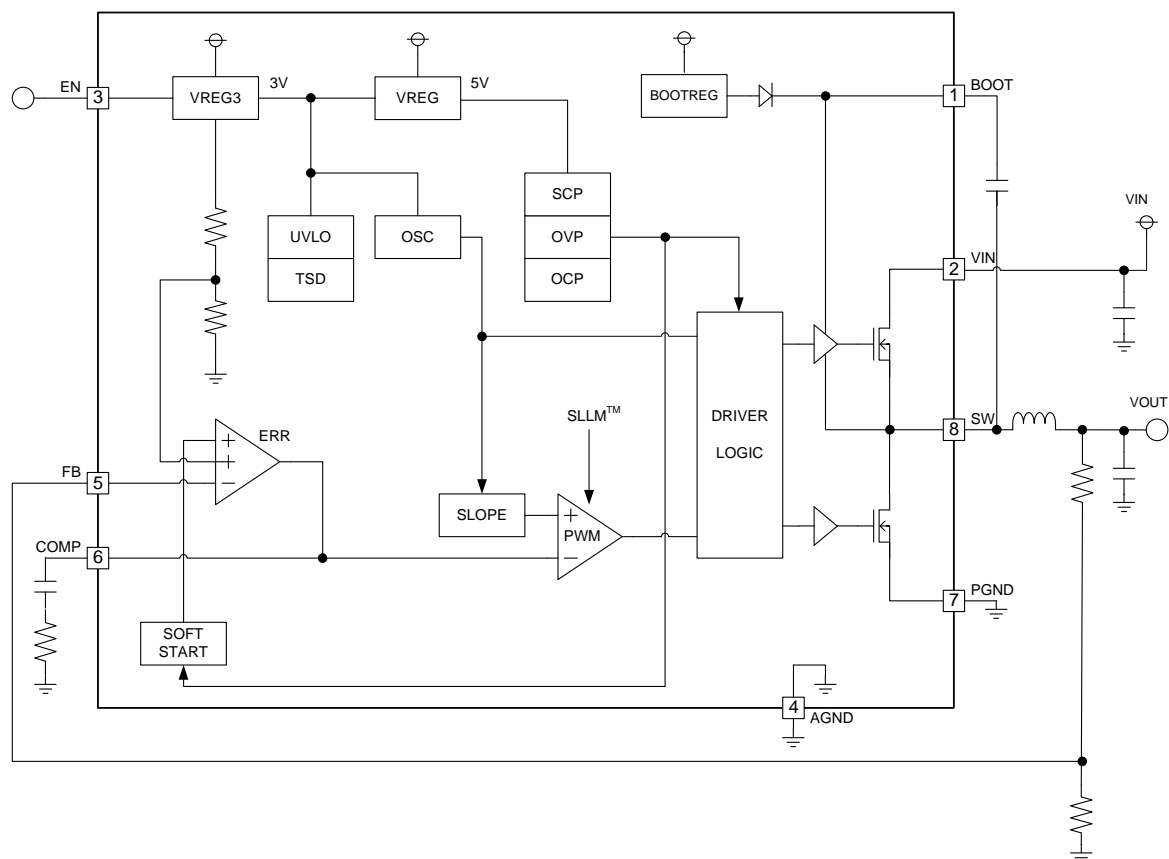


Figure 3. Block diagram

**● Description of Blocks**

- VREG3  
Block creating internal reference voltage 3V (typ.).
- VREG  
Block creating internal reference voltage 5V (typ.).
- BOOTREG  
Block creating gate drive voltage.
- TSD  
This is thermal shutdown block. Thermal shutdown circuit shuts down when inner part of IC becomes more than 175°C (typ.). Also when the temperature decrease it returns with hysteresis of 25°C (typ.).
- UVLO  
This is under voltage lockout block. IC shuts down with VIN under 6.4V (typ.). Still the threshold voltage has hysteresis of 200mV (typ.).
- ERR  
Circuit to compares the feedback voltage of standard and output voltage. Switching duty is settled by this compared result and COMP terminal voltage. Also, because soft start occurs at activation, COMP terminal voltage is controlled by internal slope voltage.
- OSC  
Block generating oscillation frequency.
- SLOPE  
Creates delta wave from clock, generated by OSC, and sends voltage composed by current sense signal of high side MOSFET and delta wave to PWM comparator.
- PWM  
Settles switching duty by comparing output COMP terminal voltage of error amplifier and signal of SLOPE part.
- DRIVER LOGIC  
This is DC/DC driver block. Input signal from PWM and drives MOSFET.
- SOFT START  
By controlling current output voltage starts calmly preventing over shoot of output voltage and inrush current.
- OCP  
Current flowing in high side MOSFET is controlled one circle each of switching frequency when over current occurs.
- SCP  
The short circuit protection block compares the FB terminal voltage with the internal standard voltage VREF. When the FB terminal voltage has fallen below 0.56 V (typ.) and remained there for 0.9 msec (typ.), SCP stops the operation for 14.4 msec (typ.) and subsequently initiates a restart.
- OVP  
Over voltage protection function (OVP) compares FB terminal voltage with the internal standard voltage VREF. When the FB terminal voltage exceeds 1.04V (typ.) it turns MOSFET of output part MOSFET OFF. After output voltage drop it returns with hysteresis.

### ● Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V <sub>IN</sub>	-0.3 to +30	V
EN Input Voltage	V <sub>EN</sub>	-0.3 to +30	V
Voltage from GND to BOOT	V <sub>BOOT</sub>	-0.3 to +35	V
Voltage from SW to BOOT	ΔV <sub>BOOT</sub>	-0.3 to +7	V
FB Input Voltage	V <sub>FB</sub>	-0.3 to +7	V
COMP Input Voltage	V <sub>COMP</sub>	-0.3 to +7	V
SW Input Voltage	V <sub>SW</sub>	-0.5 to +30	V
Output Current	I <sub>OUT</sub>	1.0	A
Allowable Power Dissipation	P <sub>d</sub>	0.675*1	W
Operating Ambient Temperature Range	T <sub>opr</sub>	-40 to +85	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C

\*1 When mounted on a 70 mm x 70 mm x 1.6 mm 1-layer glass epoxy board Derated by 5.4 mW/°C for Ta ≥ 25°C.

### ● Recommended Operating Ratings

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Supply Voltage	V <sub>IN</sub>	7.0	-	26	V
Output Current	I <sub>OUT</sub>	-	-	1.0	A
Output Voltage Range	V <sub>RANGE</sub>	1.0*2	-	V <sub>IN</sub> × 0.7	V

\*2 Please use it in I/O voltage setting of which output pulse width does not become 250nsec (typ.) or less. See the page 22 for how to calculate the resistance of the output voltage setting.

### ● Electrical Characteristics

(Ta = 25°C, V<sub>IN</sub> = 12 V, V<sub>EN</sub> = 3 V unless otherwise specified)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Supply Current in Operating	I <sub>opr</sub>	-	250	500	μA	V <sub>FB</sub> = 0.9V
Supply Current in Standby	I <sub>stby</sub>	-	0	10	μA	V <sub>EN</sub> = 0V
Reference Voltage	V <sub>FB</sub>	0.784	0.800	0.816	V	
FB Input Current	I <sub>FB</sub>	-1	0	1	μA	V <sub>FB</sub> = 0V
Switching frequency	F <sub>OSC</sub>	484	570	656	kHz	
Maximum Duty ratio	Maxduty	88	93	98	%	
High-side FET on-resistance	R <sub>ONH</sub>	-	250	-	mΩ	I <sub>SW</sub> = 100mA
Low-side FET on-resistance	R <sub>ONL</sub>	-	200	-	mΩ	I <sub>SW</sub> = 100mA
Over Current limit	I <sub>LIMIT</sub>	1.9	2.2	2.5	A	
UVLO detection voltage	V <sub>UVLO</sub>	6.1	6.4	6.7	V	V <sub>IN</sub> falling
UVLO hysteresis voltage	V <sub>UVLOHYS</sub>	100	200	300	mV	
EN high-level input voltage	V <sub>ENH</sub>	2.0	-	V <sub>IN</sub>	V	
EN low-level input voltage	V <sub>ENL</sub>	-	-	0.8	V	
EN Input current	I <sub>EN</sub>	2	4	8	μA	V <sub>EN</sub> = 3V
Soft Start time	T <sub>SS</sub>	1.2	2.5	5.0	msec	

- V<sub>FB</sub> : FB Input Voltage. V<sub>EN</sub> : EN Input Voltage.
- P<sub>d</sub> should not be exceeded.

# ● Typical Performance Curves

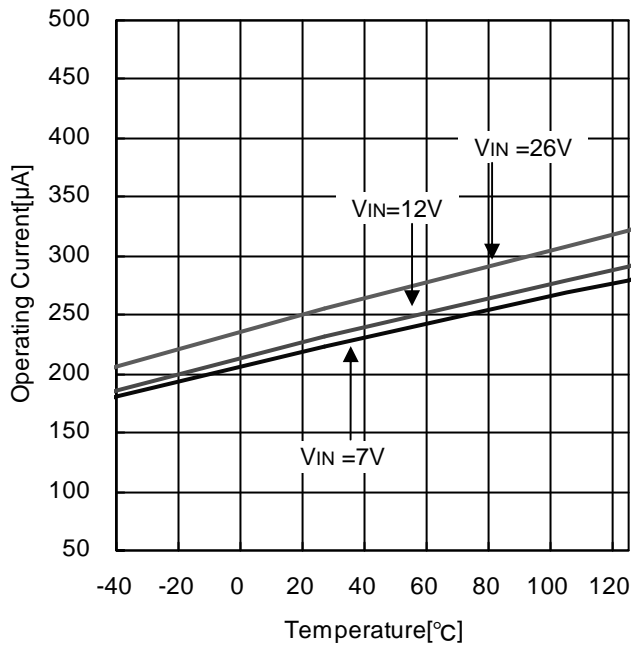


Figure 4. Operating Current - Temperature

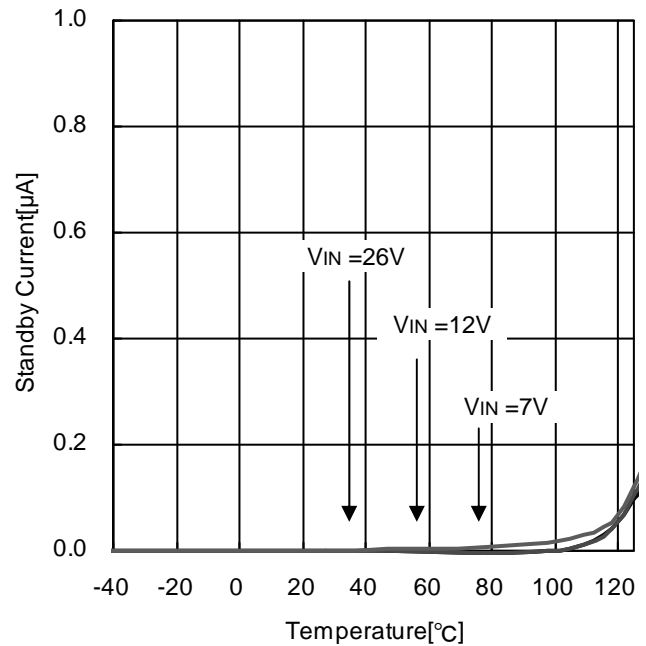


Figure 5. Stand-by Current - Temperature

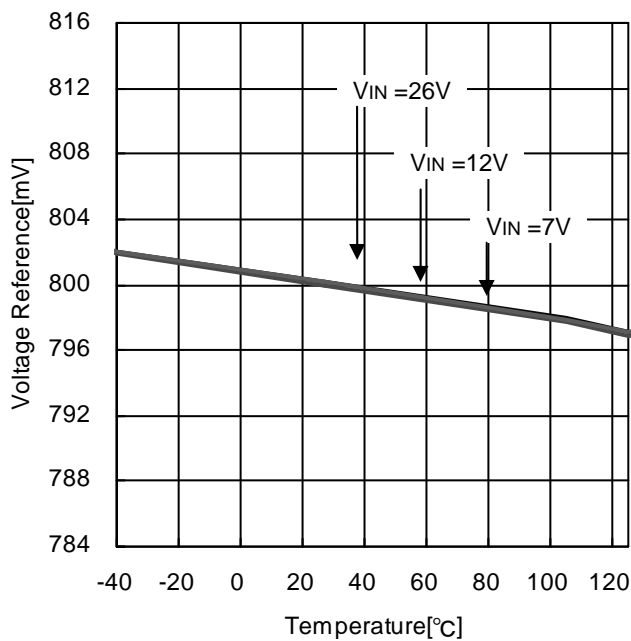


Figure 6. FB Voltage Reference - Temperature

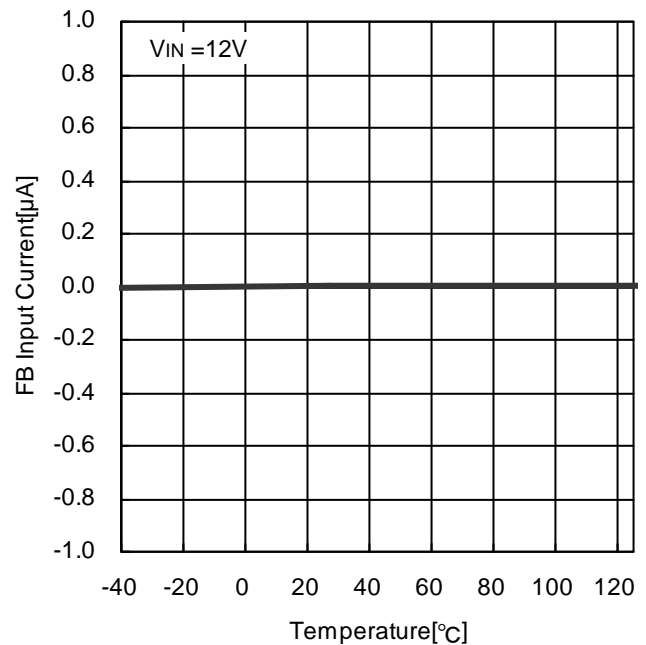


Figure 7. FB Input Current - Temperature

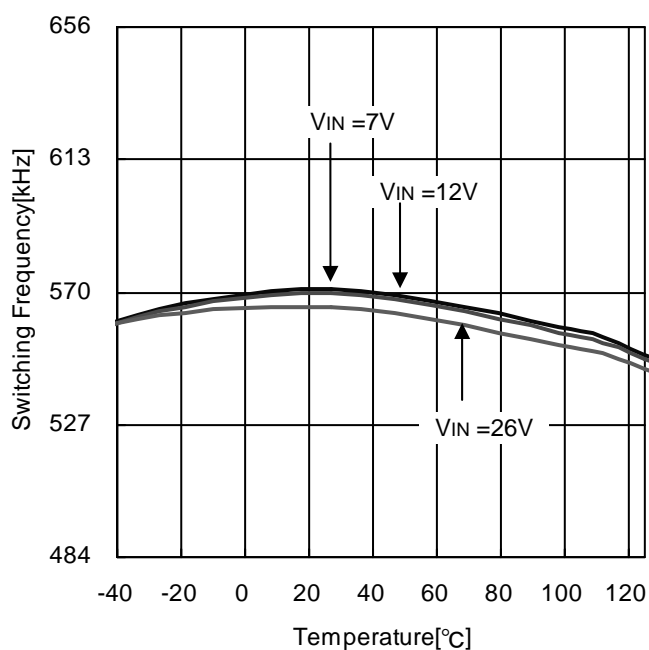


Figure 8. Switching Frequency - Temperature

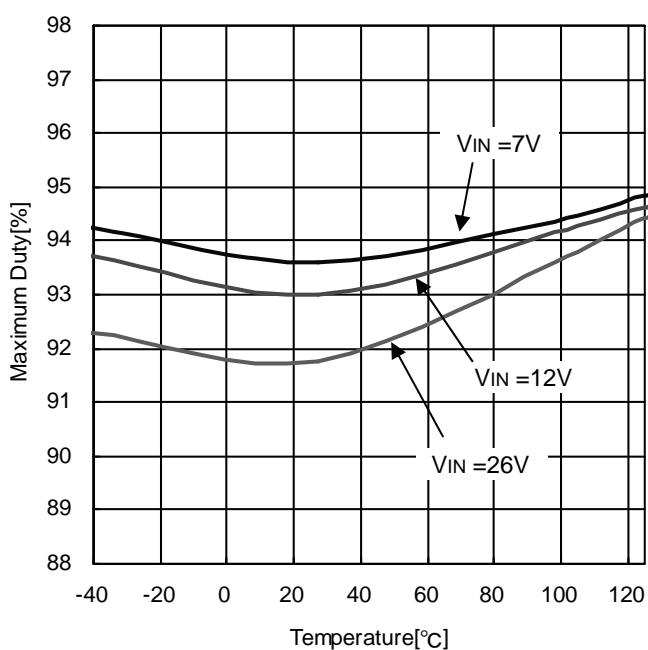
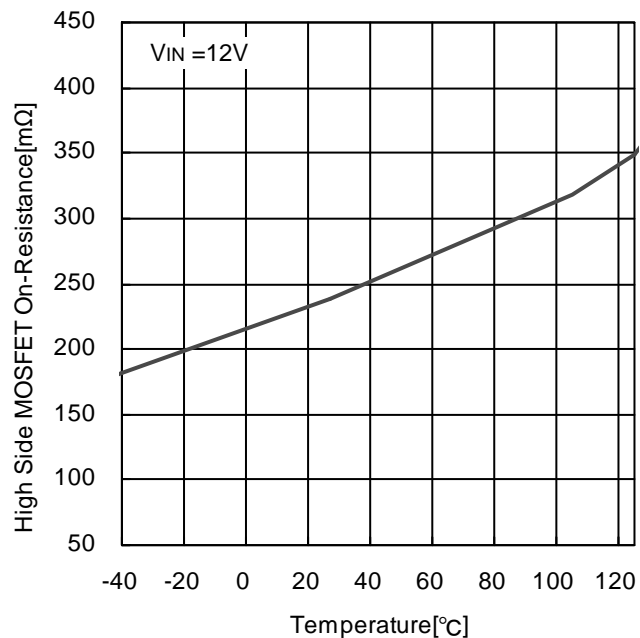
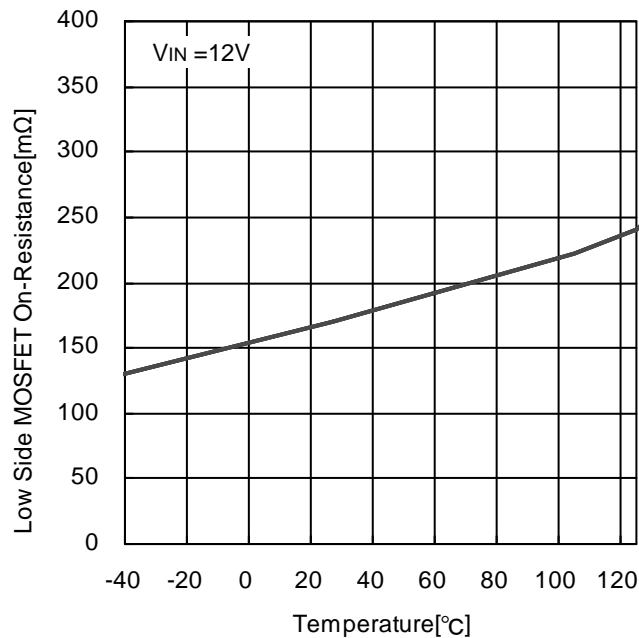


Figure 9. Maximum Duty - Temperature

Figure 10. High Side MOSFET On-Resistance-  
TemperatureFigure 11. Low Side MOSFET On-Resistance-  
Temperature

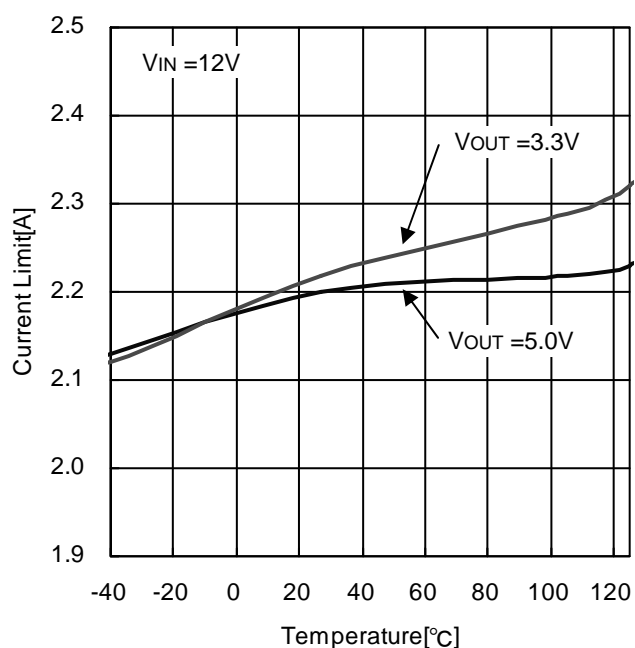


Figure 12. Current Limit - Temperature

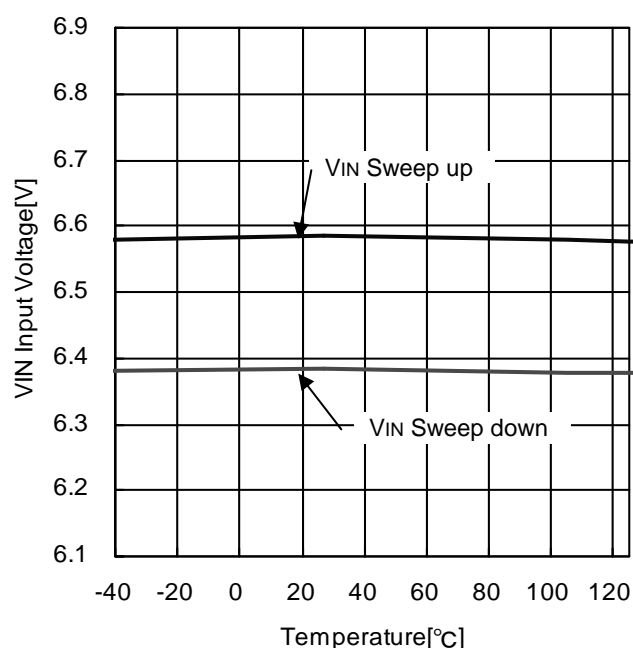


Figure 13. UVLO Threshold - Temperature

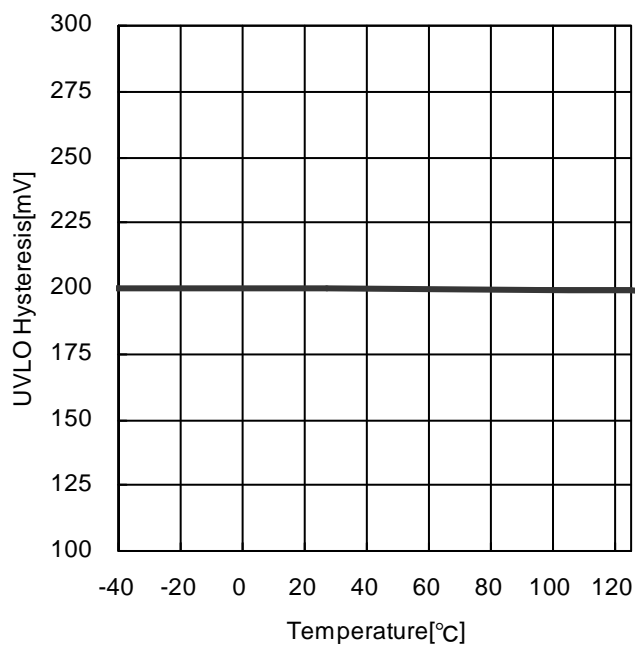


Figure 14. UVLO Hysteresis- Temperature

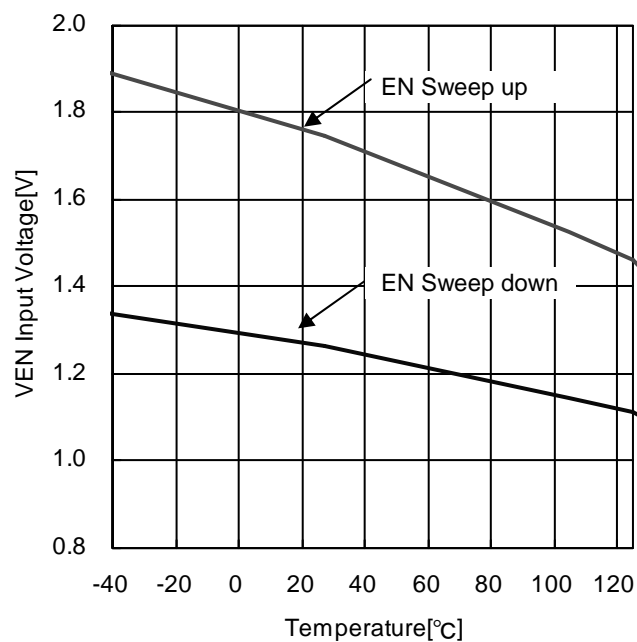


Figure 15. EN Threshold - Temperature



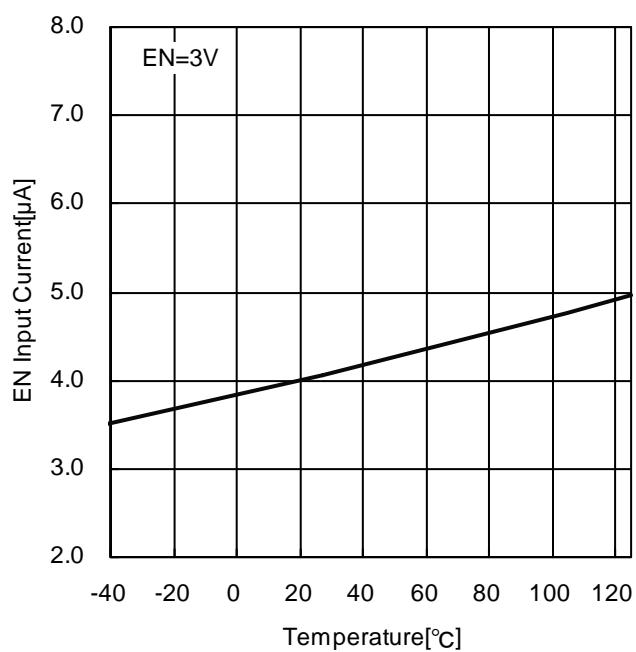


Figure 16. EN Input Current - Temperature

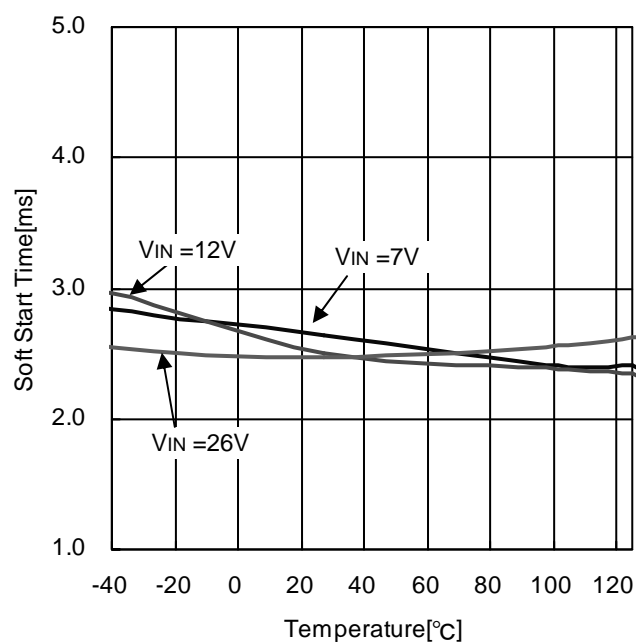


Figure 17. Soft Start Time - Temperature

# ● Typical Performance Curves (Application)

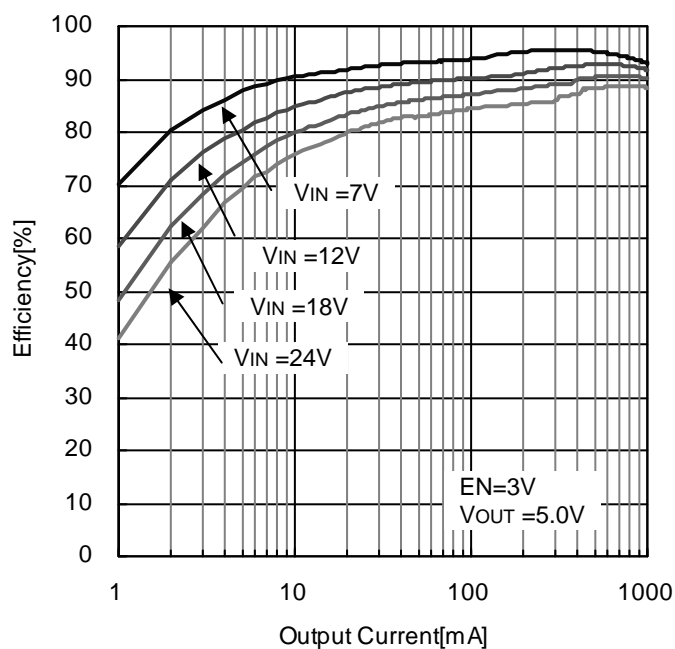


Figure 18. Efficiency - Output Current  
( $V_{OUT} = 5.0V$ )

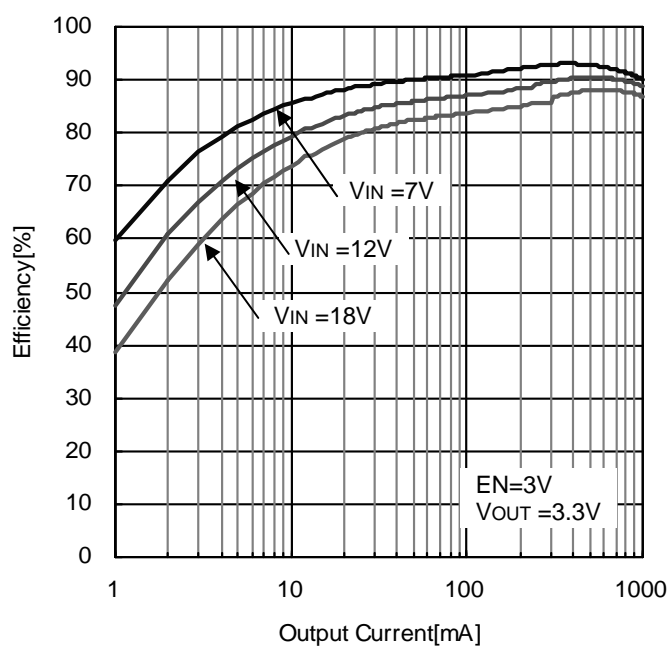


Figure 19. Efficiency - Output Current  
( $V_{OUT} = 3.3V$ )

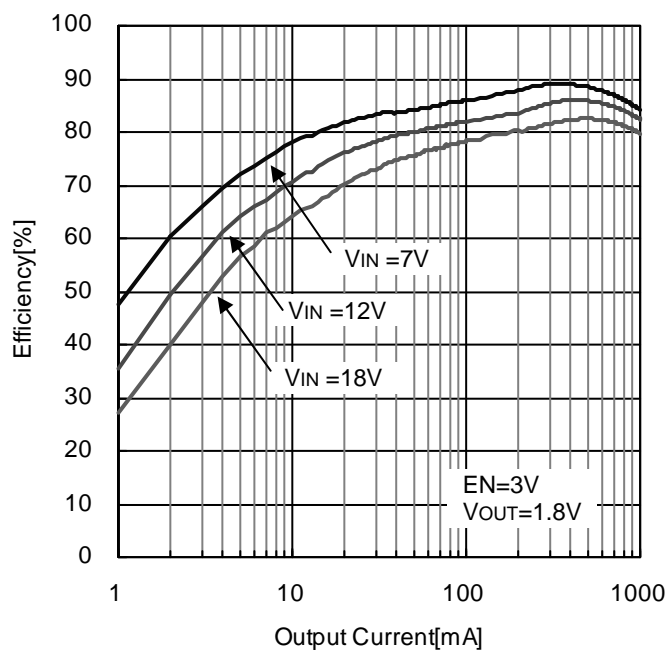
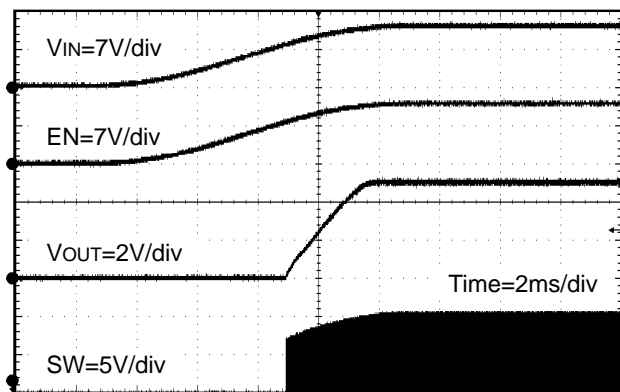
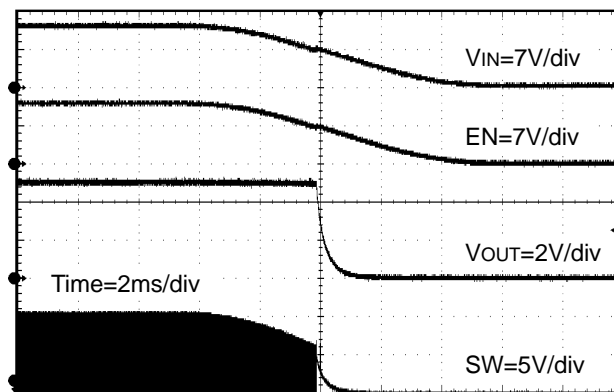
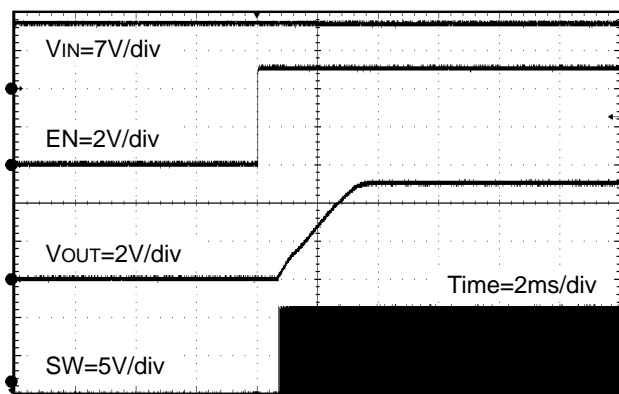
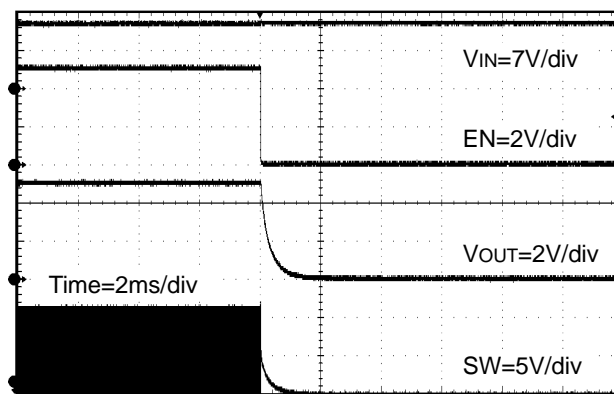


Figure 20. Efficiency - Output Current  
( $V_{OUT} = 1.8V$ )

Figure 21. Power Up ( $V_{IN} = EN$ )Figure 22. Power Down ( $V_{IN} = EN$ )Figure 23. Power Up ( $EN = 0V \rightarrow 5V$ )Figure 24. Power Down ( $EN = 5V \rightarrow 0V$ )

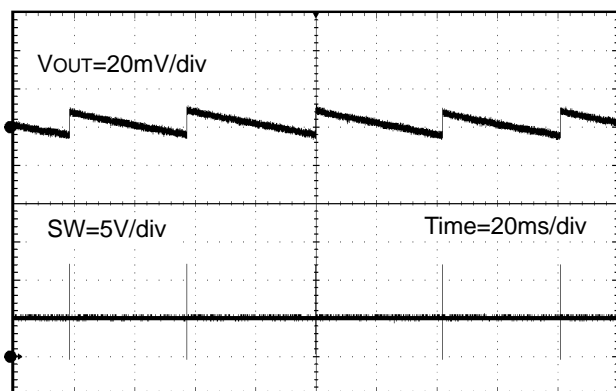


Figure 25. VOUT Ripple  
( $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 0A$ )

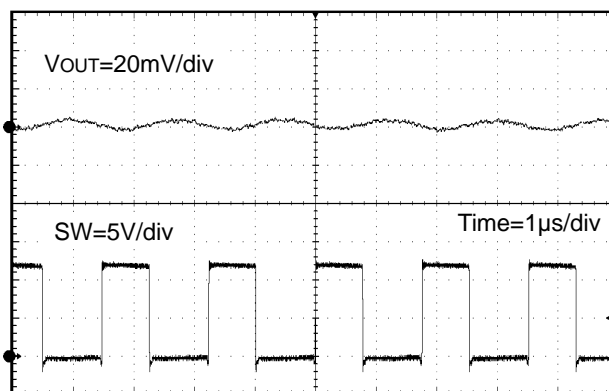


Figure 26. VOUT Ripple  
( $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 1A$ )

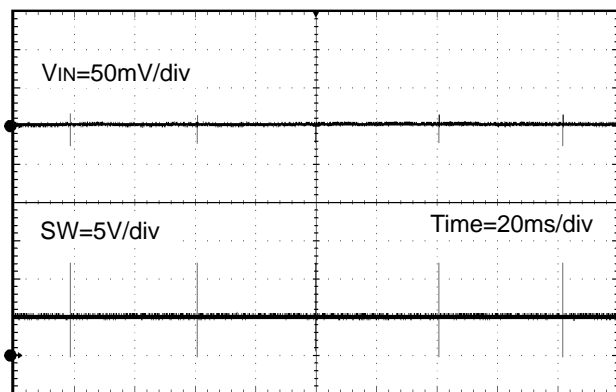


Figure 27.  $V_{IN}$  Ripple  
( $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 0A$ )

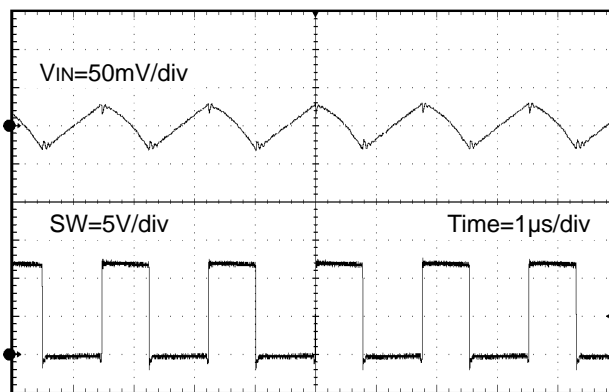


Figure 28.  $V_{IN}$  Ripple  
( $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 1A$ )

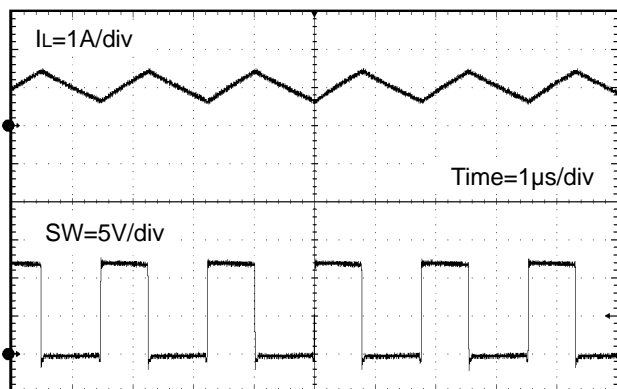


Figure 29. Switching Waveform  
( $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 1A$ )

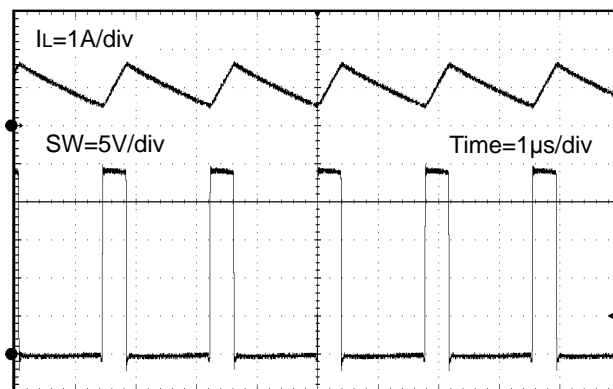


Figure 30. Switching Waveform  
( $V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 1A$ )

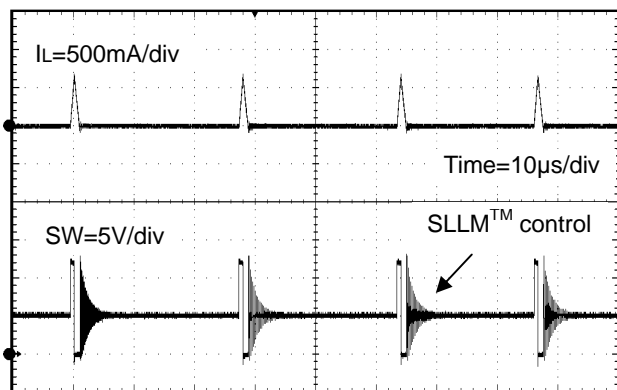


Figure 31. Switching Waveform  
( $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 20mA$ )

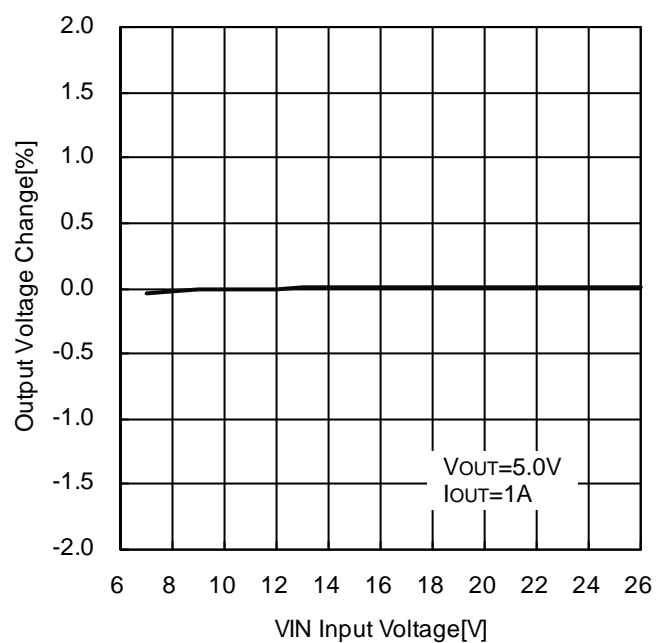


Figure 32. VOUT Line Regulation  
(VOUT = 5.0V)

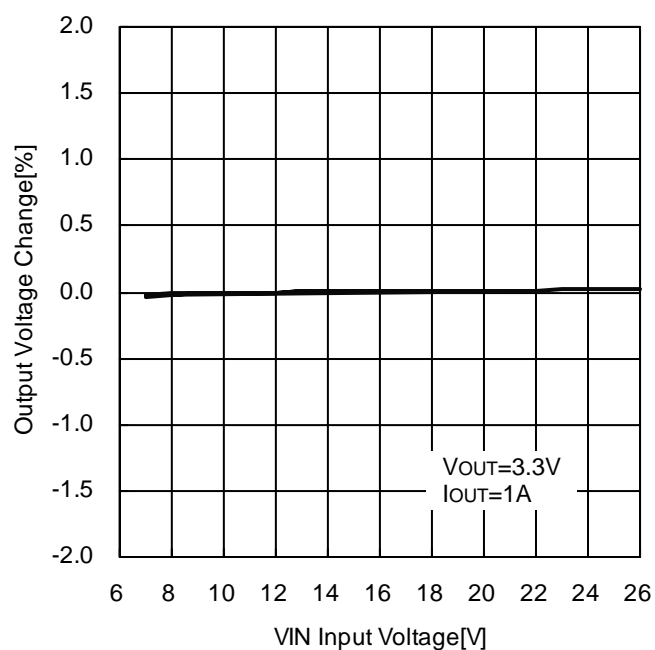


Figure 33. VOUT Line Regulation  
(VOUT = 3.3V)

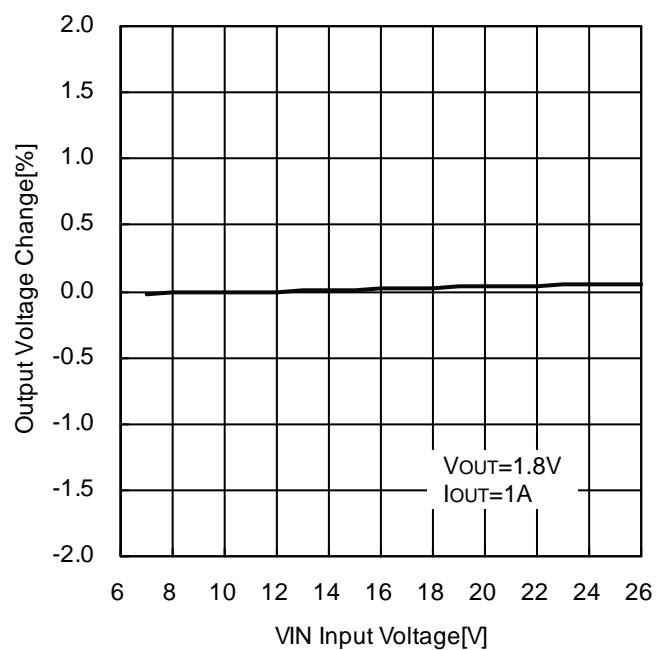


Figure 34. VOUT Line Regulation  
(VOUT = 1.8V)

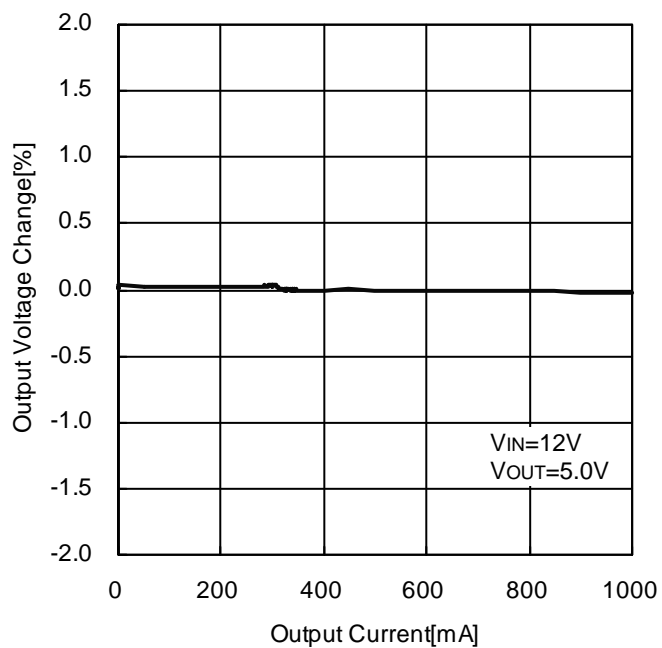


Figure 35. VOUT Load Regulation  
(VOUT = 5.0V)

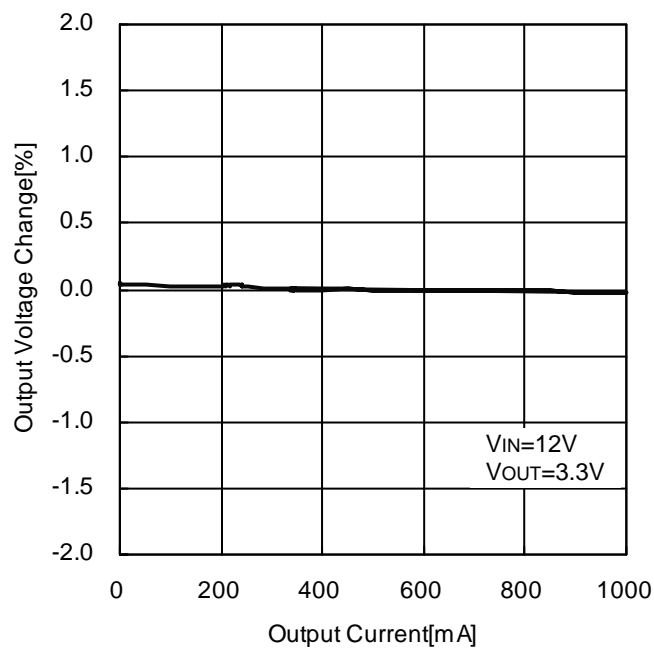


Figure 36. VOUT Load Regulation  
(VOUT = 3.3V)

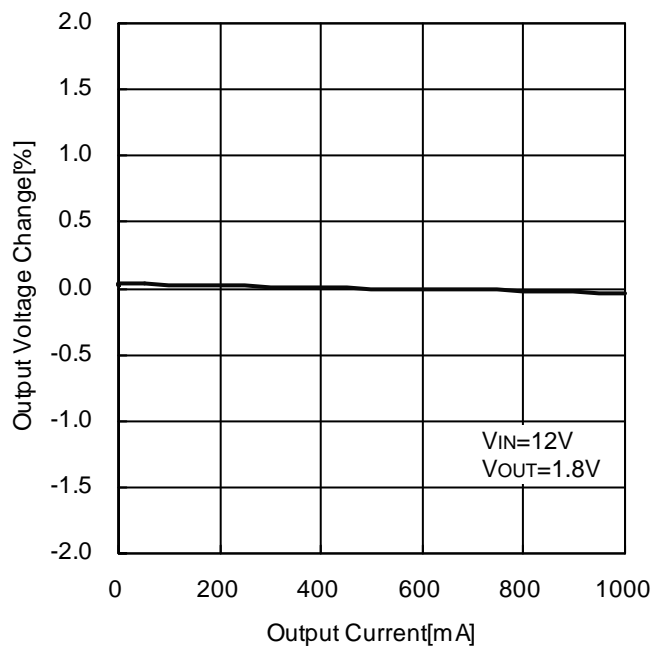


Figure 37. VOUT Load Regulation  
(VOUT = 1.8V)

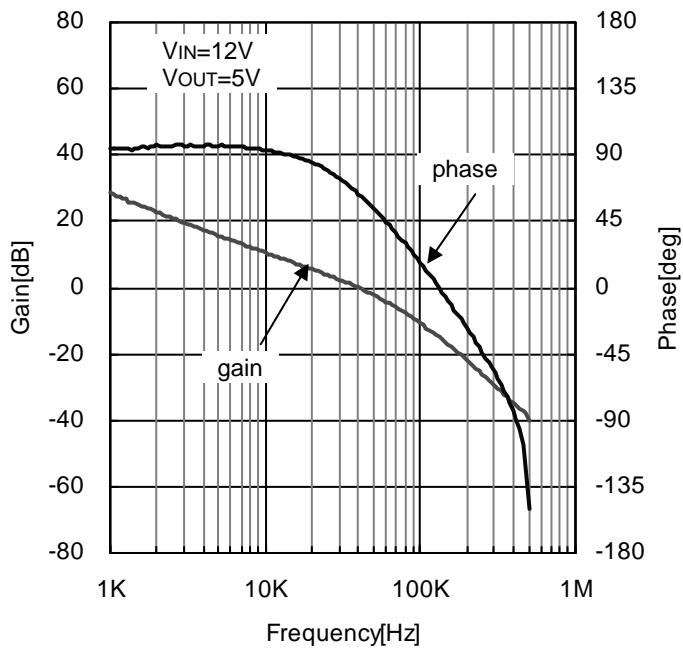


Figure 38. Loop Response  $I_{OUT}=1A$   
( $V_{IN}=12V$ ,  $V_{OUT}=5V$ ,  $C_{OUT}=\text{Ceramic}10\mu F \times 3$ )

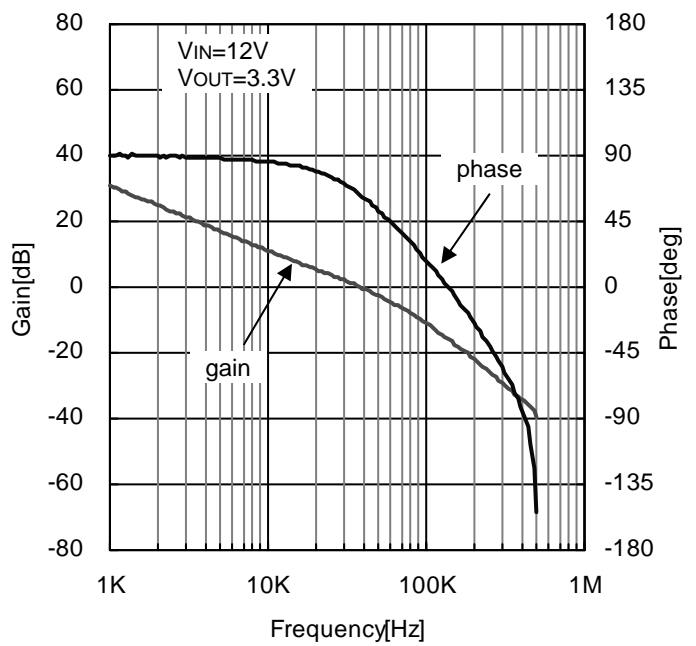


Figure 39. Loop Response  $I_{OUT}=1A$   
( $V_{IN}=12V$ ,  $V_{OUT}=3.3V$ ,  $C_{OUT}=\text{Ceramic}10\mu F \times 3$ )

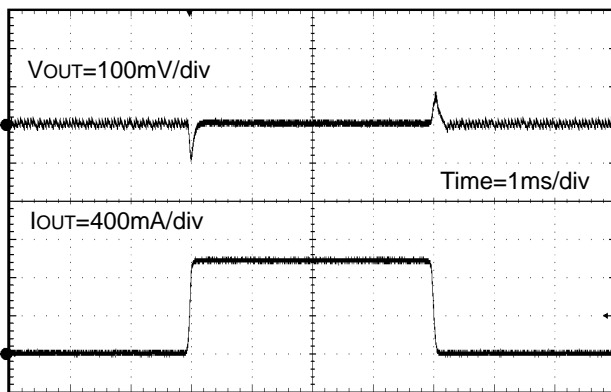


Figure 40. Load Transient Response  $I_{OUT}=10mA - 1A$   
( $V_{IN}=12V$ ,  $V_{OUT}=5V$ ,  $C_{OUT}=\text{Ceramic}10\mu F \times 3$ )

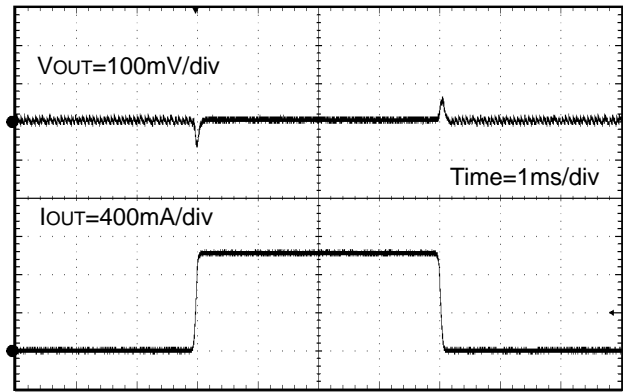


Figure 41. Load Transient Response  $I_{OUT}=10mA - 1A$   
( $V_{IN}=12V$ ,  $V_{OUT}=3.3V$ ,  $C_{OUT}=\text{Ceramic}10\mu F \times 3$ )



## ● Function Description

### 1) DC/DC converter operation

BD9E102FJ is a synchronous rectifying step-down switching regulator that achieves faster transient response by employing current mode PWM control system. It utilizes switching operation in PWM (Pulse Width Modulation) mode for heavier load, while it utilizes SLLM (Simple Light Load Mode) control for lighter load to improve efficiency.

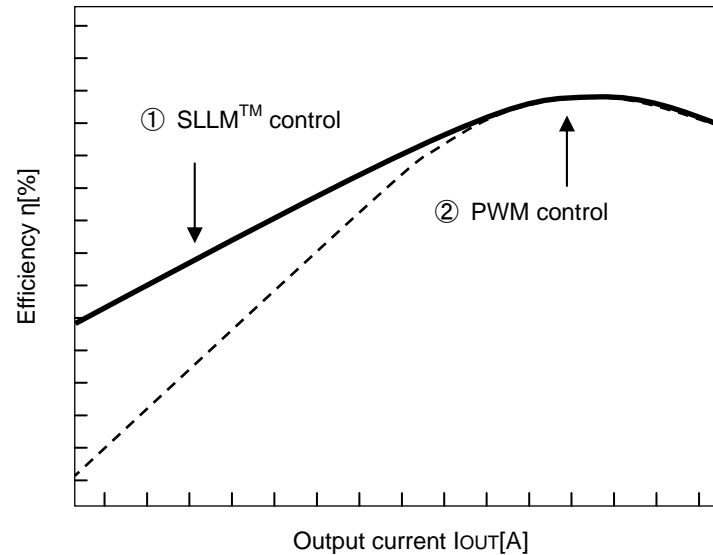


Figure 42. Efficiency (SLLM™ control and PWM control)

① SLLM™ control

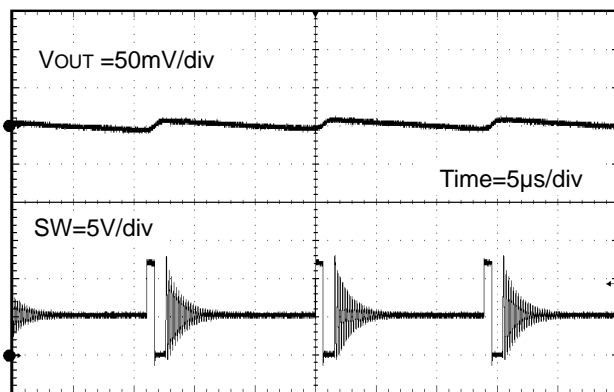


Figure 43. SW Waveform (① SLLM™ control)  
(VIN = 12V, VOUT = 5.0V, IOUT = 50mA)

② PWM control

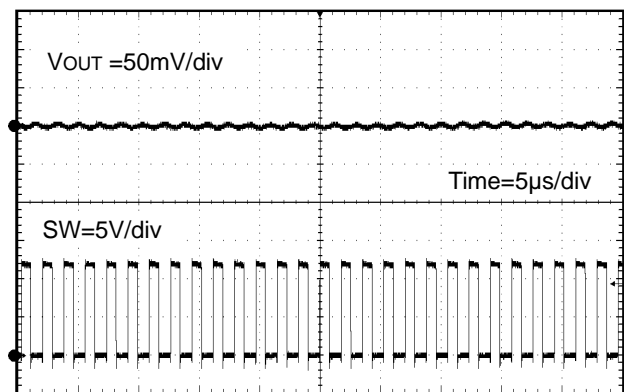


Figure 44. SW Waveform (② PWM control)  
(VIN = 12V, VOUT = 5.0V, IOUT = 1A)

## 2) Enable Control

The IC shutdown can be controlled by the voltage applied to the EN terminal. When EN voltage reaches 2.0 V (typ.), the internal circuit is activated and the IC starts up. To enable shutdown control with the EN terminal, set the shutdown interval (Low level interval of EN) must be set to 100  $\mu$ s or longer.

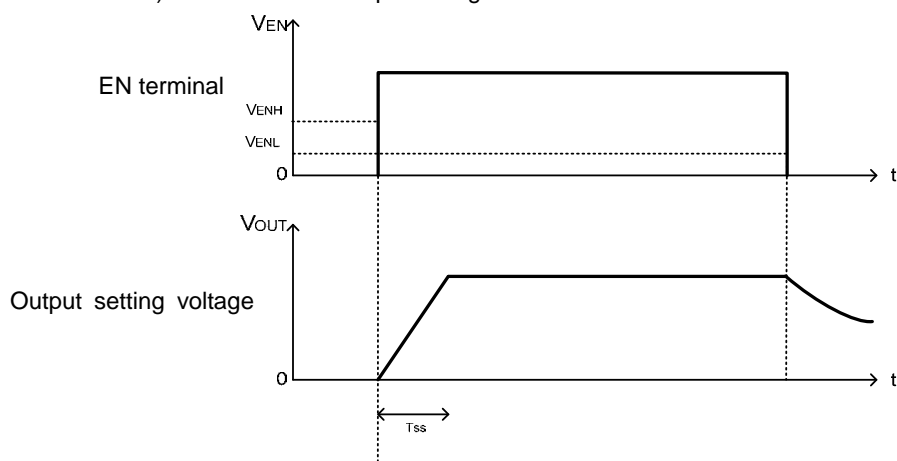


Figure 45. Timing Chart with Enable Control

## 3) Protective Functions

The protective circuits are intended for prevention of damage caused by unexpected accidents. Do not use them for continuous protective operation.

### 3-1) Short Circuit Protection (SCP)

The short circuit protection block compares the FB terminal voltage with the internal reference voltage VREF. When the FB terminal voltage has fallen below 0.56 V (typ.) and remained there for 0.9 msec (typ.), SCP stops the operation for 14.4 msec (typ.) and subsequently initiates a restart.

Table 1. Short circuit protection function

EN pin	FB pin	Short circuit protection	Short circuit protection operation
2.0 V or higher	< 0.56 V (typ.)	Enabled	ON
	> 0.56 V (typ.)		OFF
0.8 V or lower	-	Disabled	OFF

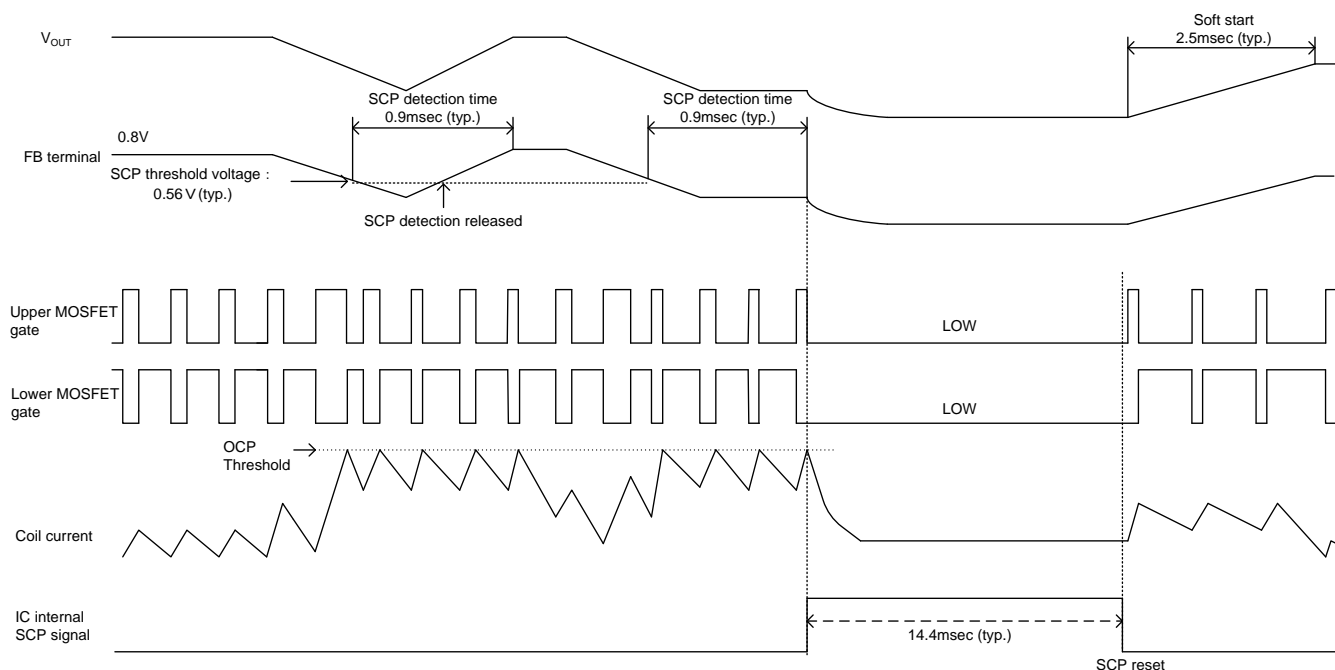


Figure 46. Short circuit protection function (SCP) timing chart

### 3-2) Under Voltage Lockout Protection (UVLO)

The under voltage lockout protection circuit monitors the VIN terminal voltage.

The operation enters standby when the VIN terminal voltage is 6.4 V (typ.) or lower.

The operation starts when the VIN terminal voltage is 6.6 V (typ.) or higher.

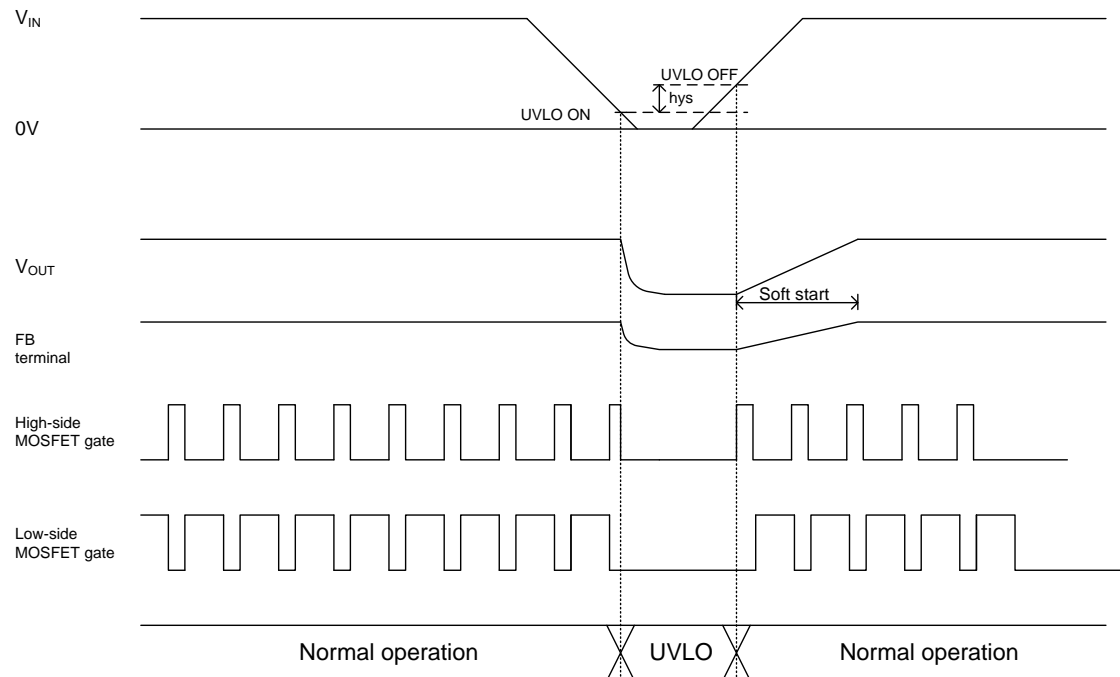


Figure 47. UVLO Timing Chart

### 3-3) Thermal Shutdown Function (TSD)

When the chip temperature exceeds  $T_j = 175^{\circ}\text{C}$ , the DC/DC converter output is stopped. The thermal shutdown circuit is intended for shutting down the IC from thermal runaway in an abnormal state with the temperature exceeding  $T_{j\text{max}} = 150^{\circ}\text{C}$ . It is not meant to protect or guarantee the soundness of the application. Do not use the function of this circuit for application protection design.

### 3-4) Over Current Protection Function (OCP)

The overcurrent protection function is realized by using the current mode control to limit the current that flows through the high-side MOSFET at each cycle of the switching frequency.

### 3-5) Over Voltage Protection Function (OVP)

Over voltage protection function (OVP) compares FB terminal voltage with internal standard voltage  $V_{\text{REF}}$  and when FB terminal voltage exceeds 1.04V (typ) it turns MOSFET of output part MOSFET OFF. After output voltage drop it returns with hysteresis.

● Application Example

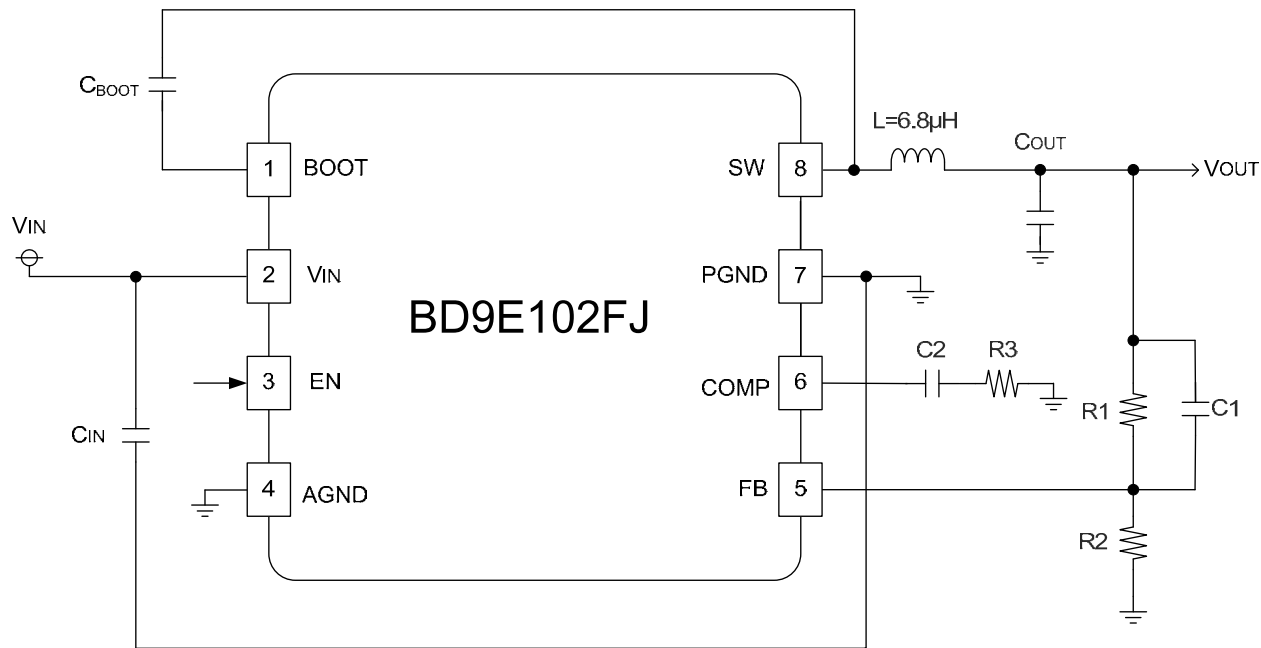


Figure 48. Application Circuit

Table 2. Recommendation Circuit constants

VIN	12V					
VOUT	5V			3.3V		
CIN	10μF	10μF	10μF	10μF	10μF	10μF
CBOOT	0.1μF	0.1μF	0.1μF	0.1μF	0.1μF	0.1μF
L	6.8μH	6.8μH	6.8μH	6.8μH	6.8μH	6.8μH
R1	430kΩ	430kΩ	430kΩ	470kΩ	470kΩ	470kΩ
R2	82kΩ	82kΩ	82kΩ	150kΩ	150kΩ	150kΩ
R3	91kΩ	82kΩ	51kΩ	68kΩ	56kΩ	43kΩ
C1	-	13pF	10pF	-	13pF	10pF
C2	680pF	360pF	100pF	1200pF	470pF	160pF
COUT	Ceramic 22μF×3	Ceramic 10μF×3	Ceramic 10μF and Aluminum 100μF	Ceramic 22μF×3	Ceramic 10μF×3	Ceramic 10μF and Aluminum 100μF

## ● Selection of Components Externally Connected

### 1) Output LC Filter

The DC/DC converter requires an LC filter for smoothing the output voltage in order to supply a continuous current to the load. BD9E102FJ is returned to the IC and IL ripple current flowing through the inductor for SLLM™ control. This feedback current, Inductance value is the behavior of the best when the 6.8μH. Therefore, the inductor to use is recommended 6.8μH.

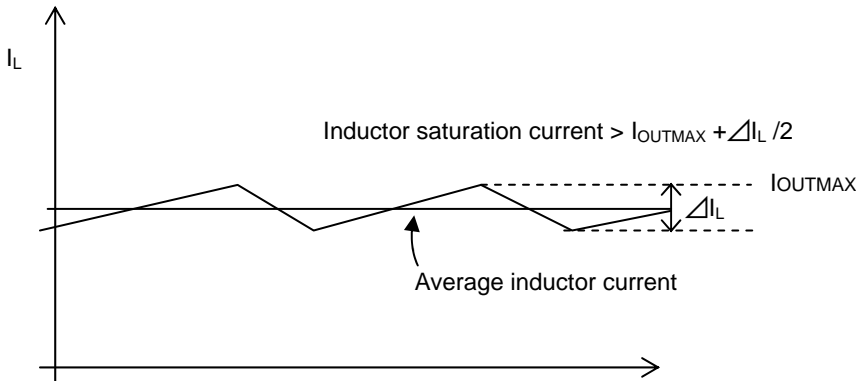


Figure 49. Waveform of current through inductor

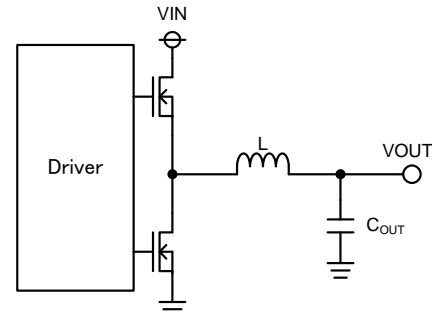


Figure 50. Output LC filter circuit

Computation with  $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 6.8\mu H$ , switching frequency  $F_{OSC} = 570kHz$ , the method is as below.

Inductor ripple current

$$\Delta I_L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times F_{OSC} \times L} = 752 \text{ mA}$$

Also for saturation current of inductor, select the one with larger current than maximum output current added by 1/2 of inductor ripple current  $\Delta I_L$ .

Output capacitor  $C_{OUT}$  affects output ripple voltage characteristics. Select output capacitor  $C_{OUT}$  so that necessary ripple voltage characteristics are satisfied.

Output ripple voltage can be expressed in the following method.

$$\Delta V_{RPL} = \Delta I_L \times \left( R_{ESR} + \frac{1}{8 \times C_{OUT} \times F_{OSC}} \right) V$$

$R_{ESR}$  is the serial equivalent series resistance here.

With  $C_{OUT} = 66\mu F$ ,  $R_{ESR} = 10m\Omega$  the output ripple voltage is calculated as

$$\Delta V_{RPL} = 0.75 \times (10m + 1 / (8 \times 66\mu \times 570k)) = 10mV$$

\*Be careful of total capacitance value, when additional capacitor  $C_{LOAD}$  is connected in addition to output capacitor  $C_{OUT}$ . Use maximum additional capacitor  $C_{LOAD(max.)}$  condition which satisfies the following method.

$$\text{Maximum starting inductor ripple current } I_{LSTART} < \text{Over Current limit } 1.9A \text{ (min.)}$$

Maximum starting inductor ripple current  $I_{LSTART}$  can be expressed in the following method.

$$I_{LSTART} = \text{Maximum starting output current (I}_{OMAX}) + \text{Charge current to output capacitor (I}_{CAP}) + \frac{\Delta I_L}{2}$$

Charge current to output capacitor  $I_{CAP}$  can be expressed in the following method.

$$I_{CAP} = \frac{(C_{OUT} + C_{LOAD}) \times V_{OUT}}{T_{SS}} \text{ A}$$

Computation with  $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 6.8\mu H$ ,  $I_{OMAX} = 1A$  (max.), switching frequency  $F_{OSC} = 484kHz$  (min.), Output capacitor  $C_{OUT} = 66\mu F$ , Soft Start time  $T_{SS} = 1.2ms$  (min.), the method is as below.

$$C_{LOAD} \text{ (max.)} < \frac{(1.9 - I_{OMAX} - \Delta I_L / 2) \times T_{SS}}{V_{OUT}} - C_{OUT} = 43.6\mu F$$

## 2) Output Voltage Set Point

The output voltage value can be set by the feedback resistance ratio.

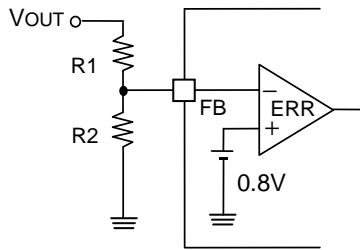


Figure 51. Feedback resistor circuit

$$V_{OUT} = \frac{R1 + R2}{R2} \times 0.8 \text{ V}$$

※ Minimum pulse range that output can output stably through all the load area is 250nsec for BD9E102FJ. Use input/output condition which satisfies the following method.

$$250 \text{ nsec} \leq \frac{V_{OUT}}{V_{IN}} \times 1.75 \mu\text{sec}$$

## 3) Phase Compensation

A current mode control buck DC/DC converter is a two-pole, one-zero system: two poles formed by an error amplifier and load and one zero point added by phase compensation. The phase compensation resistor  $R_{CMP}$  determines the crossover frequency  $F_{CRS}$  where the total loop gain of the DC/DC converter is 0 dB. Specifying a high value for this crossover frequency  $F_{CRS}$  provides a good load transient response characteristic but inferior stability. Conversely, specifying a low value for the crossover frequency  $F_{CRS}$  greatly stabilizes the characteristics but the load transient response characteristic is impaired.

### 3-1) Selection of Phase Compensation Resistor $R_{CMP}$

The phase compensation resistance  $R_{CMP}$  can be determined by using the following equation.

$$R_{CMP} = \frac{2\pi \times V_{OUT} \times F_{CRS} \times C_{OUT}}{V_{FB} \times G_{MP} \times G_{MA}} \Omega$$

$V_{OUT}$ : output voltage

$F_{CRS}$ : crossover frequency

$C_{OUT}$ : output capacitance

$V_{FB}$ : feedback reference voltage (0.8 V (typ.))

$G_{MP}$ : current sense gain (7 A/V (typ.))

$G_{MA}$ : error amplifier transconductance (82  $\mu\text{A/V}$  (typ.))

### 3-2) Selection of phase compensation capacitance $C_{CMP}$

For stable operation of the DC/DC converter, inserting a zero point at 1/6 of the zero crossover frequency that cancels the phase delay due to the pole formed by the load often provides favorable characteristics.

The phase compensation capacitance  $C_{CMP}$  can be determined by using the following equation.

$$C_{CMP} = \frac{1}{2\pi \times R_{CMP} \times F_Z} \text{ F}$$

$F_Z$ : Zero point inserted

### 3-3) Loop stability

To ensure the stability of the DC/DC converter, use the actual device to make sure that a sufficient phase margin is provided. Ensuring a phase margin of at least 45 degrees in the worst conditions is recommended. The feed forward capacitor  $C_{RUP}$  is used for the purpose of forming a zero point together with the resistor  $R_{UP}$  to increase the phase margin within the limited frequency range. Using a  $C_{RUP}$  is effective when the  $R_{UP}$  resistance is larger than the combined parallel resistance of  $R_{UP}$  and  $R_{DW}$ .

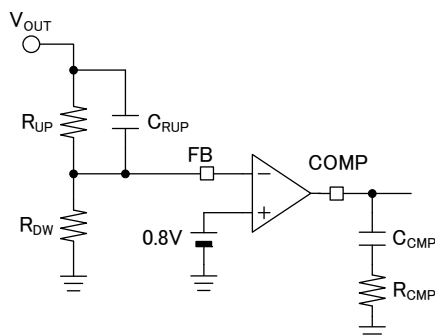


Figure 52. Phase compensation circuit

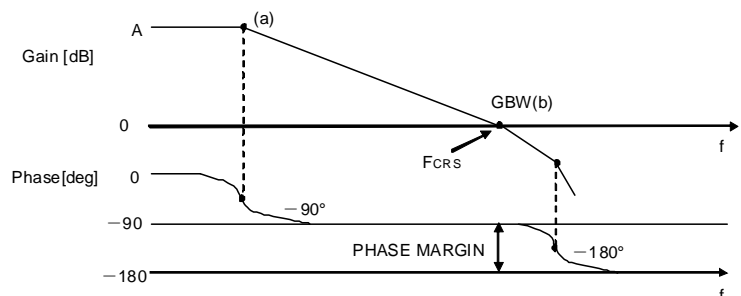


Figure 53. Bode plot

### ● PCB Layout Design

In the buck DC/DC converter, a large pulsed current flows in two loops. The first loop is the one into which the current flows when the High Side FET is turned on. The flow starts from the input capacitor  $C_{IN}$ , runs through the FET, inductor  $L$  and output capacitor  $C_{OUT}$  and back to ground of  $C_{IN}$  via ground of  $C_{OUT}$ . The second loop is the one into which the current flows when the Low Side FET is turned on. The flow starts from the Low Side FET, runs through the inductor  $L$  and output capacitor  $C_{OUT}$  and back to ground of the Low Side FET via ground of  $C_{OUT}$ . Tracing these two loops as thick and short as possible allows noise to be reduced for improved efficiency. It is recommended to connect the input and output capacitors, in particular, to the ground plane. The PCB layout has a great influence on the DC/DC converter in terms of all of the heat generation, noise and efficiency characteristics.

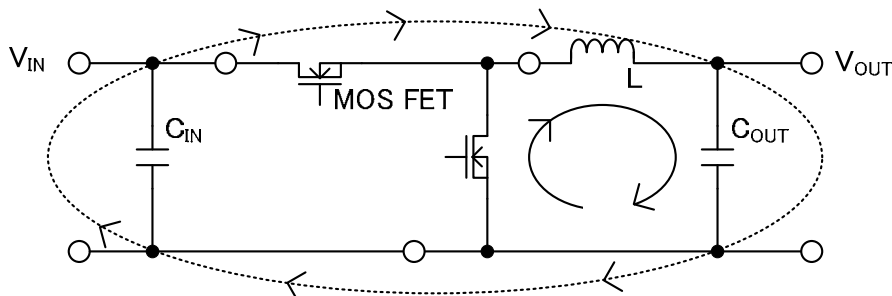
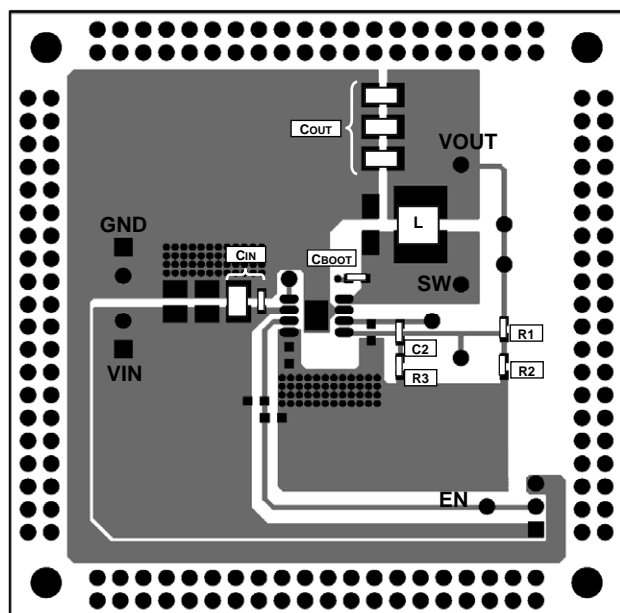


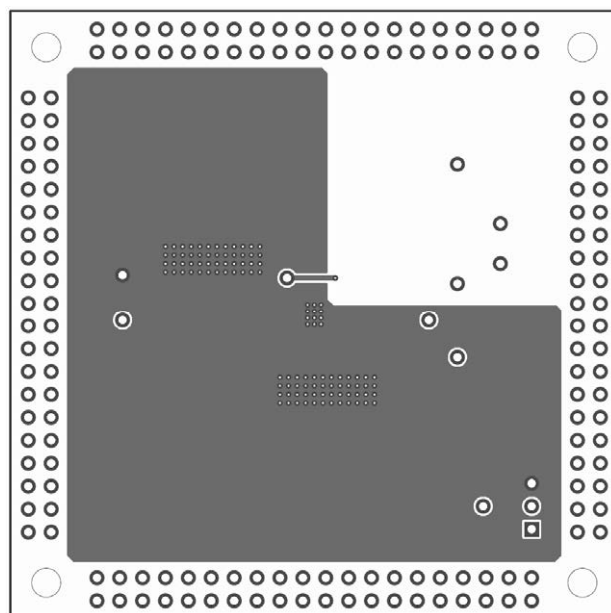
Figure 54. Current loop of buck converter

Accordingly, design the PCB layout with particular attention paid to the following points.

- Provide the input capacitor as close to the IC VIN terminal as possible on the same plane as the IC.
- If there is any unused area on the PCB, provide a copper foil plane for the ground node to assist heat dissipation from the IC and the surrounding components.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Trace to the coil as thick and as short as possible.
- Provide lines connected to FB and COMP as far away from the SW node.
- Provide the output capacitor away from the input capacitor in order to avoid the effect of harmonic noise from the input.



Top Layer



Bottom Layer

Figure 55. Example of sample board layout pattern

### ● Power Dissipation

When designing the PCB layout and peripheral circuitry, sufficient consideration must be given to ensure that the power dissipation is within the allowable dissipation curve.

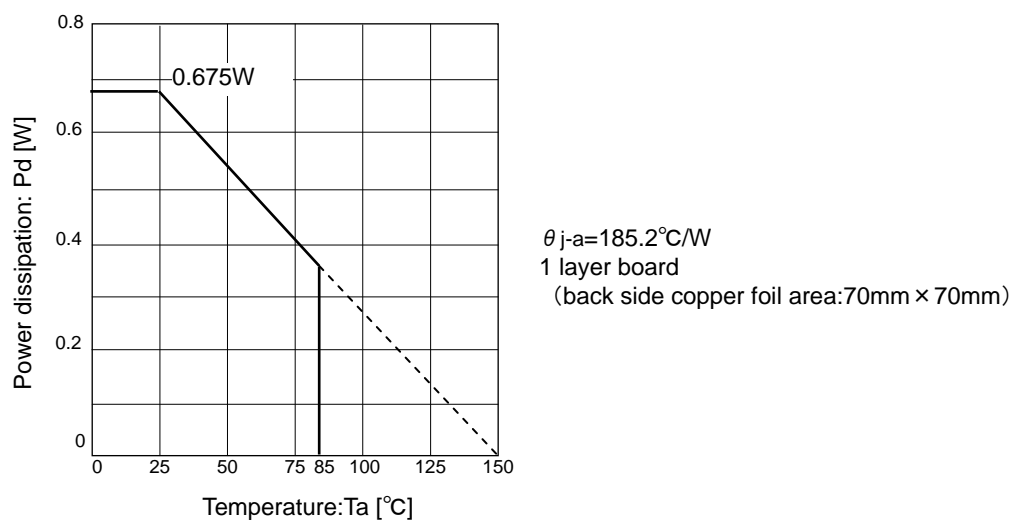


Figure 56. Power dissipation (SOP-J8)

### ● I/O Equivalence Circuit

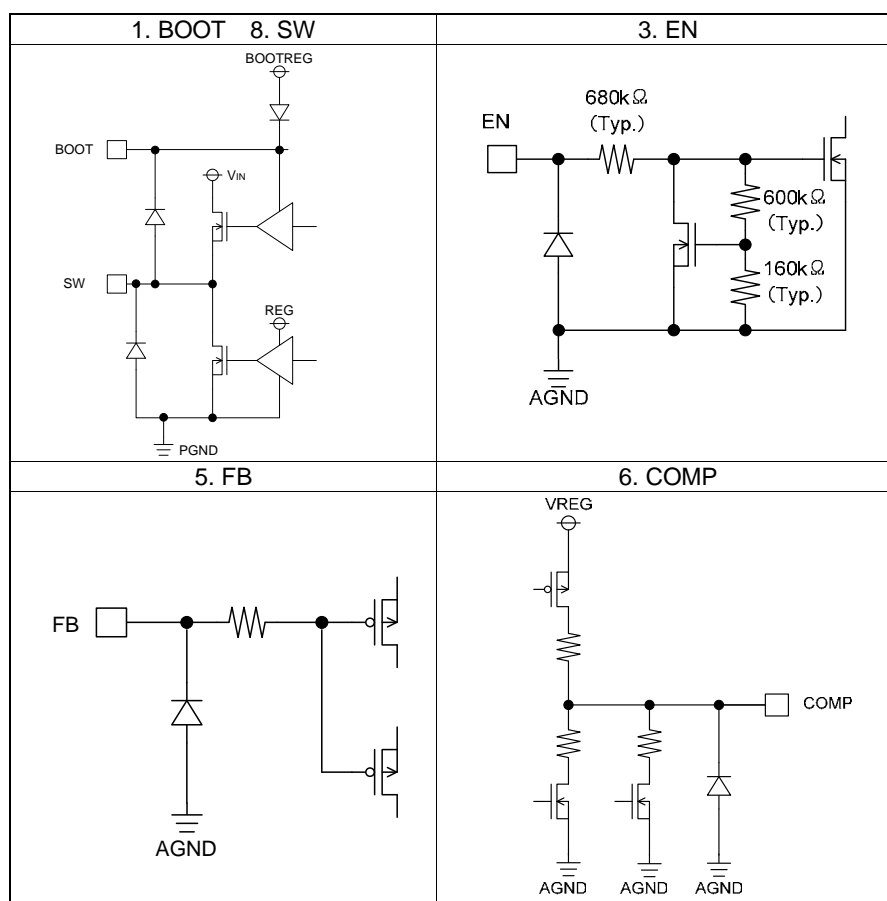


Figure 57. I/O equivalence circuit



## ● Operational Notes

### 1) Absolute Maximum Ratings

While abundant attention is paid to quality management of this IC, use of the IC in excess of absolute maximum ratings such as the applied voltage and operating temperature range may result in deterioration or damage. For design, ensure that it is always used within the guaranteed range. Use of the IC in excess of absolute maximum ratings such as the applied voltage and operating temperature range may result in damage. The state of the IC (short mode, open mode, etc.) cannot be identified if such damage occurs. Physical safety measures such as provision of a fuse should be taken when a special mode in which the absolute maximum ratings may be exceeded is anticipated.

### 2) GND Potential

Ensure the minimum GND pin potential in all operating conditions.

### 3) Thermal Design

Use a thermal design that allows for a sufficient margin in light of the power dissipation ( $P_d$ ) in actual operating conditions.

### 4) Pin Short and Faulty Mounting

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Avoid short-circuiting between VIN and VOUT/SW. Short-circuiting between these may result in damage to the IC and smoke generation. In a case that has been applied  $V_{IN} = 20V$  or more, when there is a possibility the BOOT terminal and SW terminal is short-circuited, please insert a resistance of about 10 ohms between the bootstrap capacitor  $0.1\mu F$  and BOOT terminal. Short-circuiting between these without inserting this resistance may result in damage to the IC and smoke generation.

### 5) Actions is Strong Magnetic Field

Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

### 6) Testing on Application Boards

When testing the IC on an application board, connecting a capacitor to a pin with a low impedance may subject the IC to stress. Always discharge capacitors after each process. Always turn the power supply off before connecting it to or removing it from a jig or fixture during the inspection process. As an antistatic measure, ground the IC during assembly steps and use similar caution when transporting or storage the IC.

### 7) PCB Layout

Be sure to connect VIN to the power supply on the board.

Be sure to connect PGND and AGND to the GND on the board.

Ensure that the VIN wiring is thick and short for a sufficiently low impedance.

Ensure that the PGND and AGND wiring is thick and short for a sufficiently low impedance.

Take the output voltage of the DC/DC converter from the two ends of the output capacitor.

The PCB layout and peripheral components may influence the performance of the DC/DC converter. Give sufficient consideration to the design of the peripheral circuitry.

### 8) IC Pin Input

This IC is a monolithic IC and, between each element, it has P+ isolation for element separation and P substrate. With this P layer and the N layer of the respective elements, P-N junctions are formed to constitute a variety of parasitic elements. For example, when a resistor and transistor are connected to terminals as shown in the figure below, reversal of the terminal voltage and GND voltage activates the parasitic diode and transistor.

Parasitic elements are inevitably generated by the potential relationship due to the IC structure. Activation of a parasitic element may cause interference in circuit operation, possibly leading to damage. Accordingly, use abundance of caution to avoid use that causes the parasitic elements to operate such as applying a voltage that is lower than the GND (P substrate) to an I/O terminal.

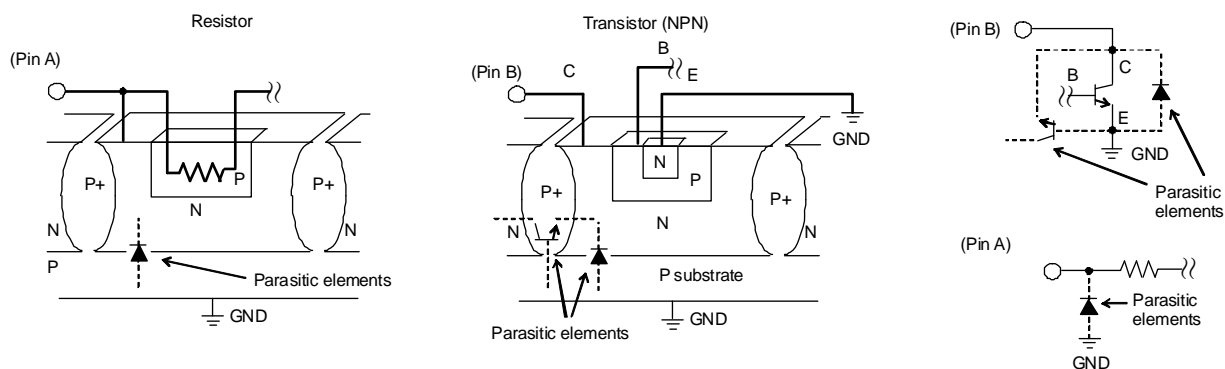


Figure 58. Example of simplified structure of monolithic IC

## 9) Overcurrent protection Circuit

The DC/DC converter output terminal integrates an overcurrent protection function, which is effective in protecting the IC from damage caused by unexpected GND short circuit. Avoid use on the premise of continuous operation of the protection circuit.

## 10) Thermal Shutdown Circuit

If the chip temperature reaches  $T_j = 175^{\circ}\text{C}$  (typ.), the thermal shutdown function is activated and the DC/DC converter stops switching.

The thermal shutdown circuit is intended for shutting down the IC from thermal runaway and is not meant to protect or guarantee the soundness of the application. Accordingly, avoid use on the premise of continuous use or operation after the activation of this circuit.

## 11) Enable Function

If the rate of fall of the EN terminal signal is too low, chattering may occur. Chattering with the output voltage remaining may generate a reverse current that boosts the voltage from the output to the input, possibly leading to damage. For on/off control with the EN signal, ensure that the signal falls within 100  $\mu\text{sec}$ .

## 12) Load at Startup

Ensure that the respective output has light load at startup of this IC.

Restrain the power supply line noise at startup and voltage drop generated by operating current within the hysteresis width of UVLO. Input of any noise exceeding the hysteresis noise width may cause malfunction.

## 13) External Elements

Use a ceramic capacitor with a low ESR for the bypass capacitor between VIN and PGND and provide it as close to the IC as possible. For external components such as inductors and capacitors, use those recommended in this specification and provide as close to the IC as possible. For those through which large current flows, in particular, ensure that the wiring is thick and short.

## 14) IC Applications

This IC is not developed for in-vehicle or military applications or equipment/devices that may affect human lives. Do not use the IC for such applications. If this IC is used by customers in any of such applications as described above, ROHM shall not be held responsible for failure to satisfy the requirements concerned.

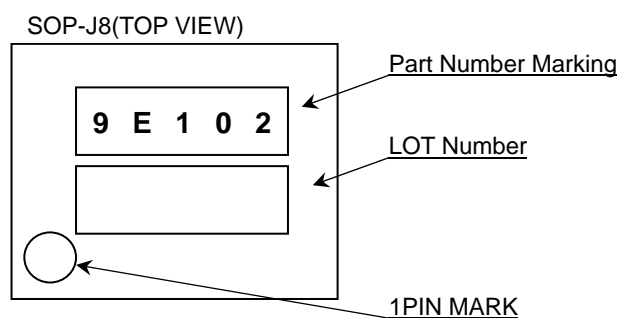
## 15) Use Environment

The operating temperature range is intended to guarantee functional operation and does not guarantee the life of the IC within this range. The life of the IC may be subject to derating depending on use environment such as the voltage applied, ambient temperature and humidity. Design equipment and devices in view of derating.

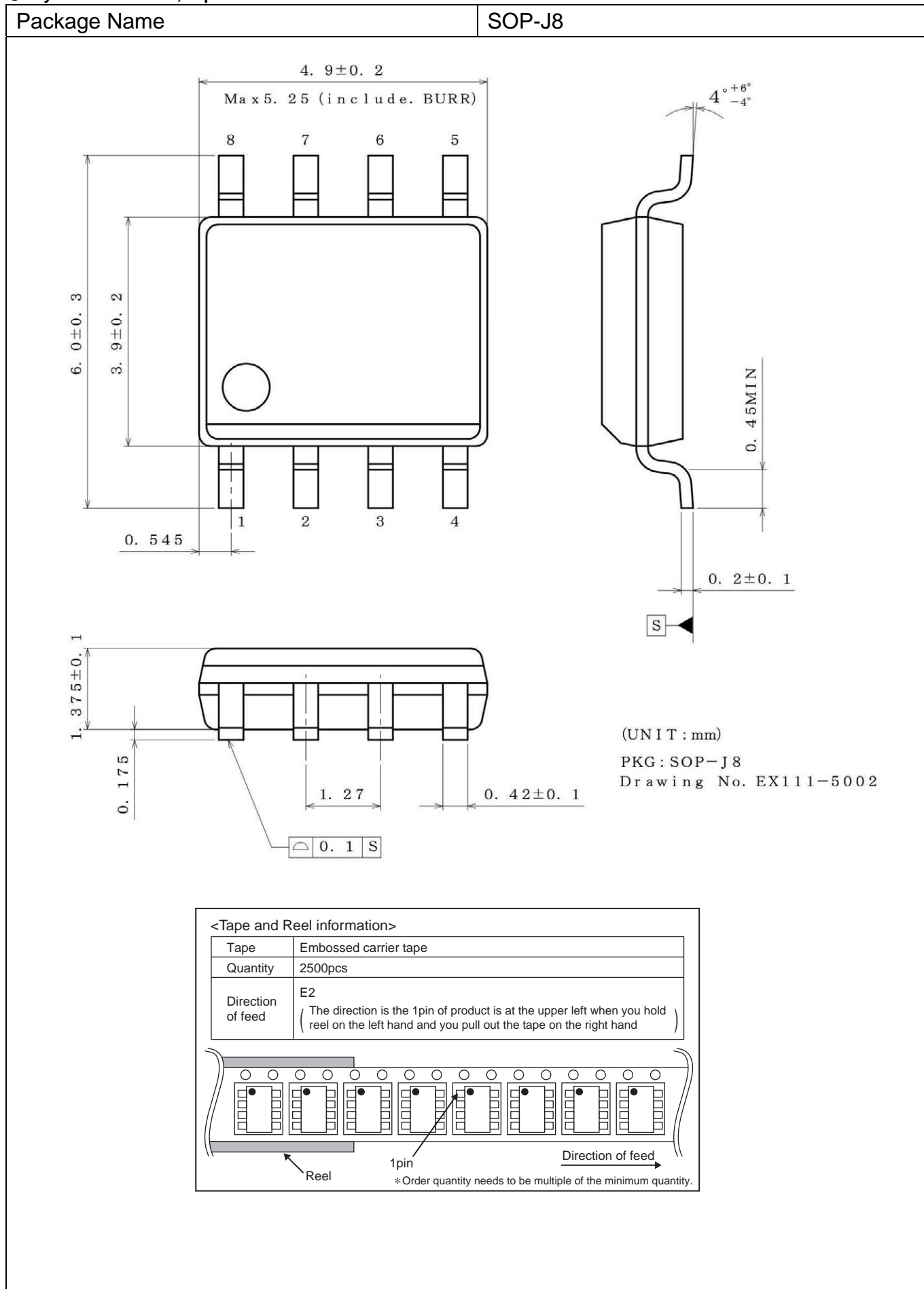
### ●Ordering Information

B D 9 E 1 0 2 F J	-	E 2
Part Number	Package FJ: SOP-J8	Packaging and forming specification E2: Embossed tape and reel

### ●Marking Diagram



## ●Physical Dimension, Tape and Reel Information – continued



## ●Revision History

Date	Revision	Description
1. May. '13	001	Created

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  - Sealing or coating our Products with resin or other coating materials
  - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
  - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
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- In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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