32K x 16 HIGH-SPEED CMOS STATIC RAM

SEPTEMBER 2005

FEATURES

- High-speed access time: 12 ns
- Low Active Power: 175 mW (typical)
- Low Standby Power: 1 mW (typical) CMOS standby
- TTL compatible interface levels
- Single 5V ± 10% power supply
- Fully static operation: no clock or refresh required
- Available in 44-pin SOJ package and 44-pin TSOP (Type II)
- Commercial and Industrial temperature ranges available
- Lead-free available

DESCRIPTION

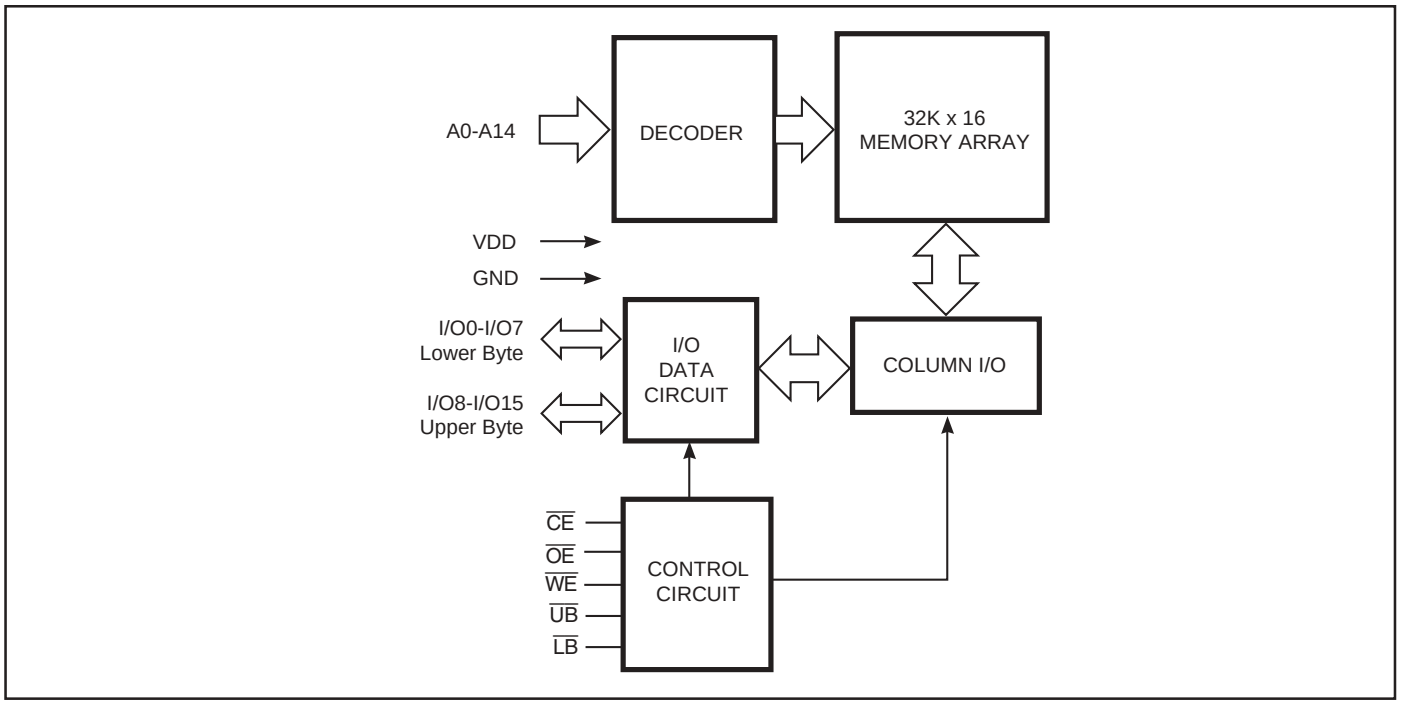
The *ISSI* IS61C3216AL is high-speed, 512Kb static RAMs organized as 32,768 words by 16 bits. They are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 12 ns with low power consumption.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

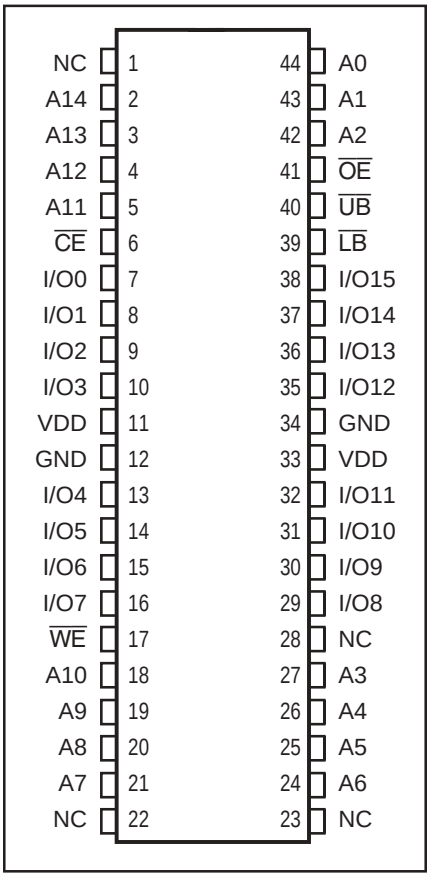
The IS61C3216AL is packaged in the JEDEC standard 44-pin 400-mil SOJ and 44-pin TSOP (Type II).

FUNCTIONAL BLOCK DIAGRAM

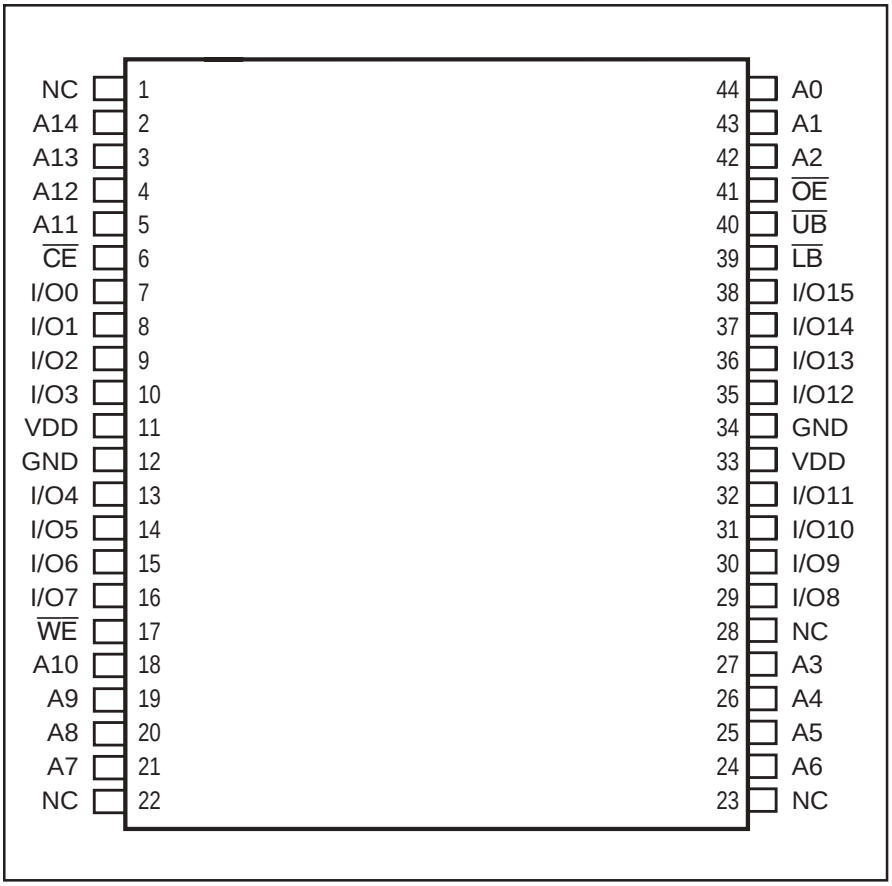


PIN CONFIGURATIONS

44-Pin SOJ



44-Pin TSOP (Type II)



PIN DESCRIPTIONS

A0-A14	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V_{DD}	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN I/O0-I/O7	I/O PIN I/O8-I/O15	V_{DD} Current
Not Selected	X	H	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	X	X	High-Z	High-Z	I_{CC1}, I_{CC2}
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	D_{OUT}	High-Z	I_{CC1}, I_{CC2}
	H	L	L	H	L	High-Z	D_{OUT}	
	H	L	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	X	L	H	D_{IN}	High-Z	I_{CC1}, I_{CC2}
	L	L	X	H	L	High-Z	D_{IN}	
	L	L	X	L	L	D_{IN}	D_{IN}	

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE (IS61C3216AL)

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 5.0V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{DD} + 0.5	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	Com. Ind.	–1 –2	1 2	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD} Outputs Disabled	Com. Ind.	–1 –2	1 2	µA

Note:
1. V_{IL} = –3.0V for pulse width less than 10 ns.

IS61C3216AL

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-12 ns Min.	-12 ns Max.	Unit
I_{CC1}	V_{DD} Operating Supply Current	$V_{DD} = V_{DD\ MAX.}$, $\overline{CE} = V_{IL}$ $I_{OUT} = 0$ mA, f = 0	Com. Ind.	— —	40 45	mA
I_{CC2}	V_{DD} Dynamic Operating Supply Current	$V_{DD} = V_{DD\ MAX.}$, $\overline{CE} = V_{IL}$ $I_{OUT} = 0$ mA, f = f_{MAX}	Com. Ind. typ.[2]	— — 	50 55 35	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	$V_{DD} = V_{DD\ MAX.}$, $V_{IN} = V_{IH}$ or V_{IL} $\overline{CE} \geq V_{IH}$, f = 0	Com. Ind.	— —	1 1	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	$V_{DD} = V_{DD\ MAX.}$, $\overline{CE} \leq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0	Com. Ind. typ.[2]	— — 	350 400 200	µA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-12 Min.	-12 Max.	Unit
t_{RC}	Read Cycle Time	12	—	ns
t_{AA}	Address Access Time	—	12	ns
t_{OHA}	Output Hold Time	3	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	12	ns
t_{DOE}	$\overline{OE}$ Access Time	—	6	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	6	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	7	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	2	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	6	ns
t_{HZB}	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	6	ns
t_{LZB}	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	0	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

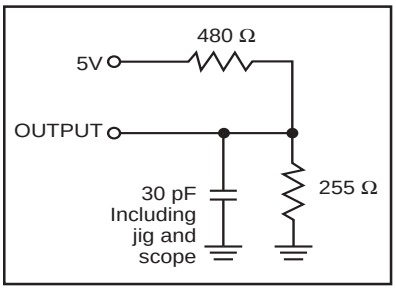


Figure 1

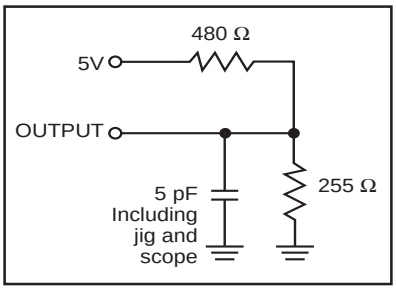
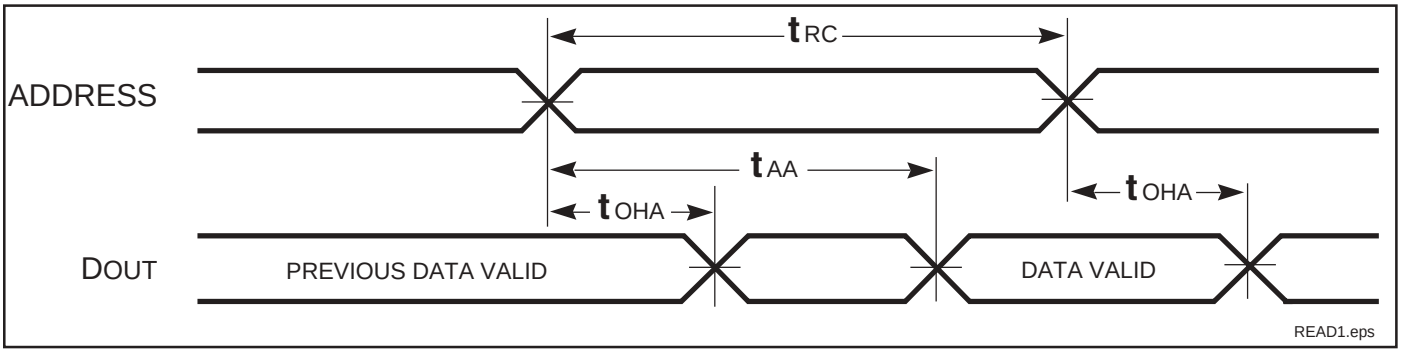


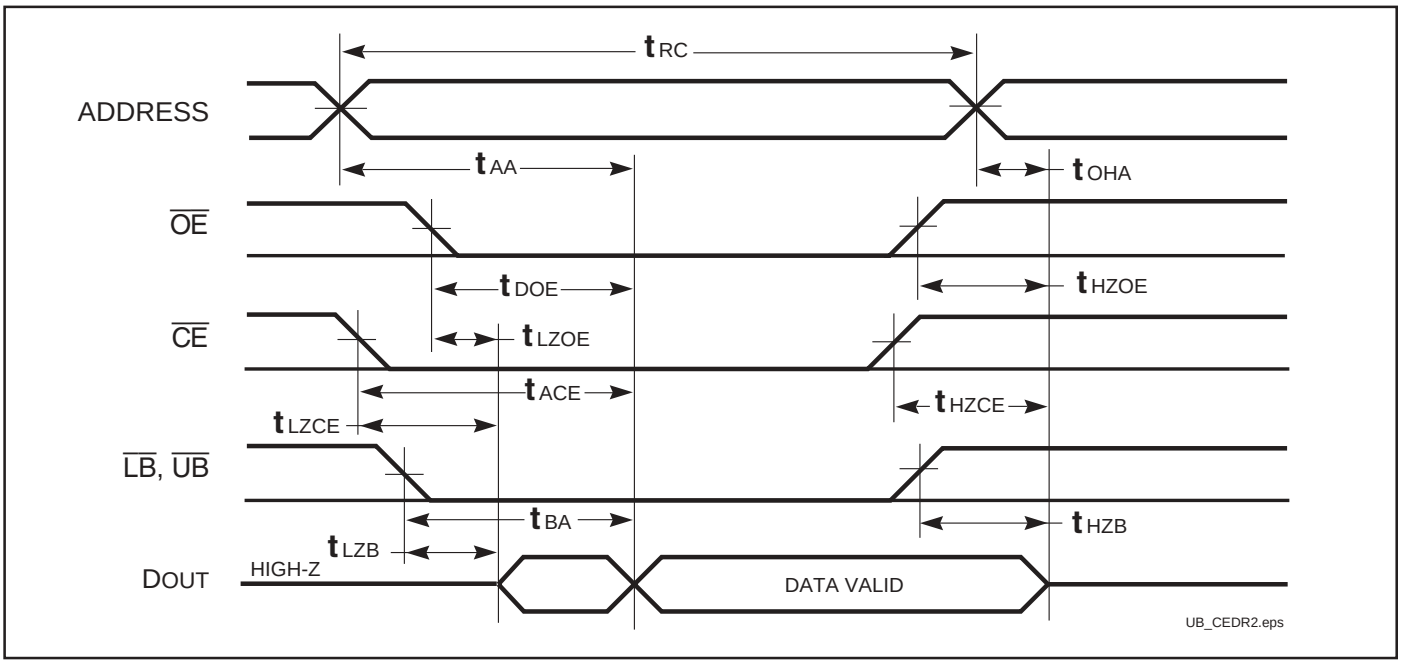
Figure 2

AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL})



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{UB}$, or $\overline{LB}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transition.

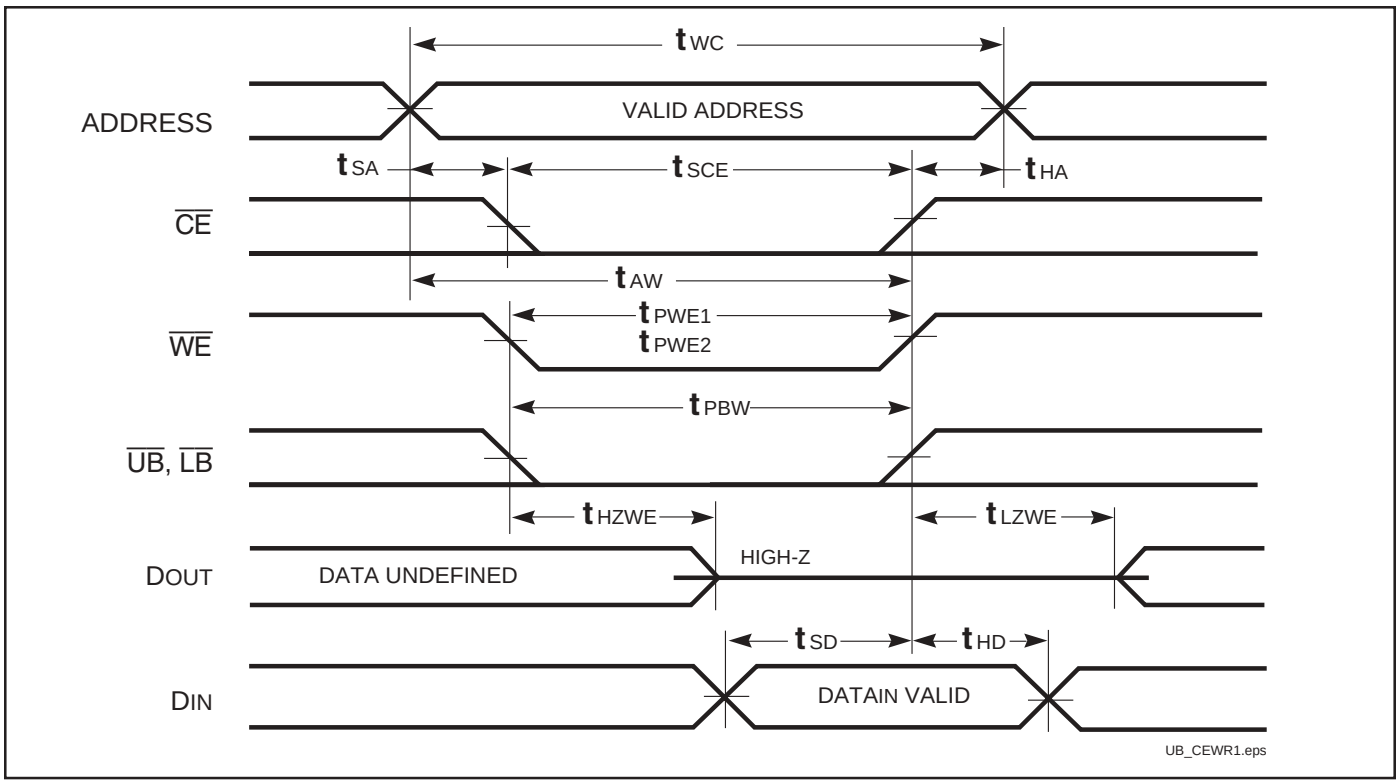
WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-12 Min.	-12 Max.	Unit
t_{WC}	Write Cycle Time	12	—	ns
t_{SCE}	$\overline{CE}$ to Write End	9	—	ns
t_{AW}	Address Setup Time to Write End	9	—	ns
t_{HA}	Address Hold from Write End	0	—	ns
t_{SA}	Address Setup Time	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	9	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ =High)	9	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ =Low)	9	—	ns
t_{SD}	Data Setup to Write End	6	—	ns
t_{HD}	Data Hold from Write End	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	6	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	3	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS

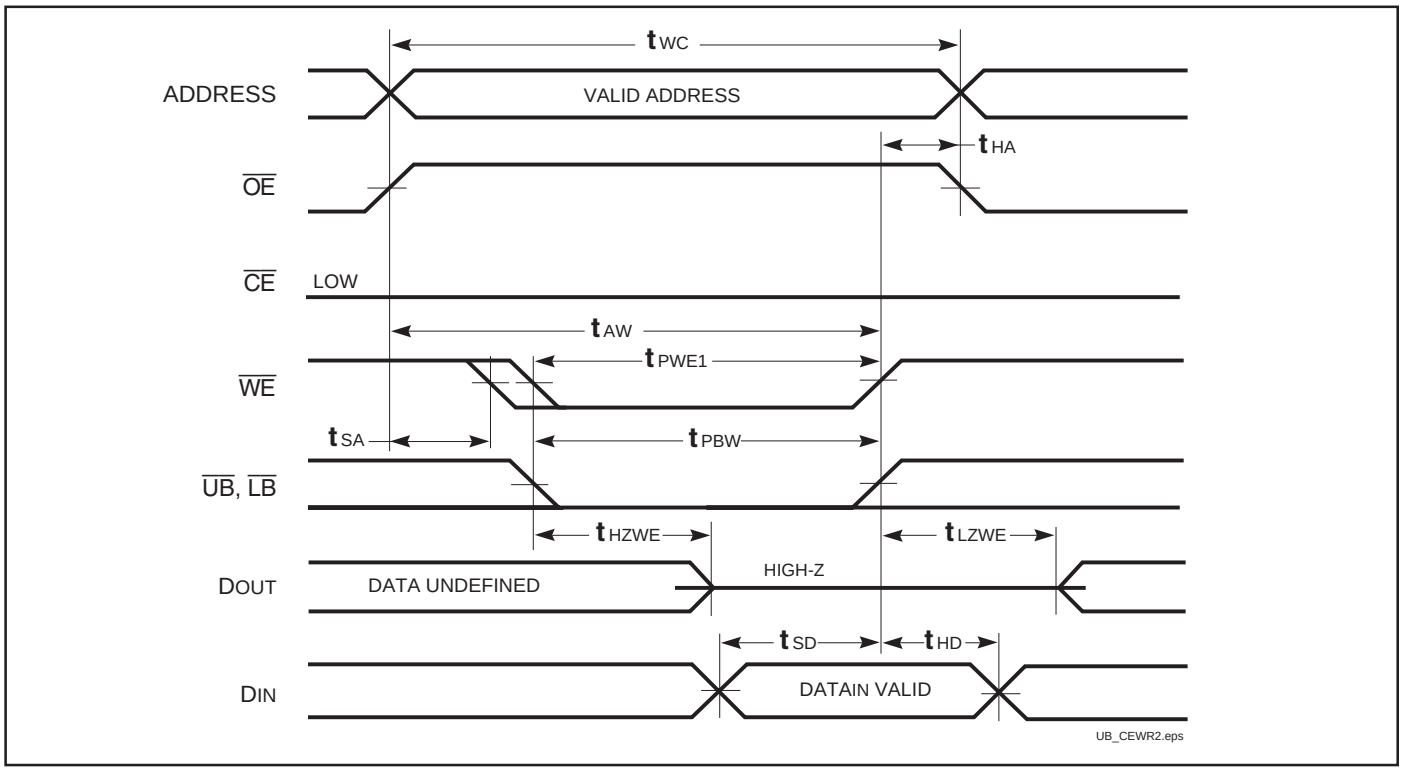
WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]



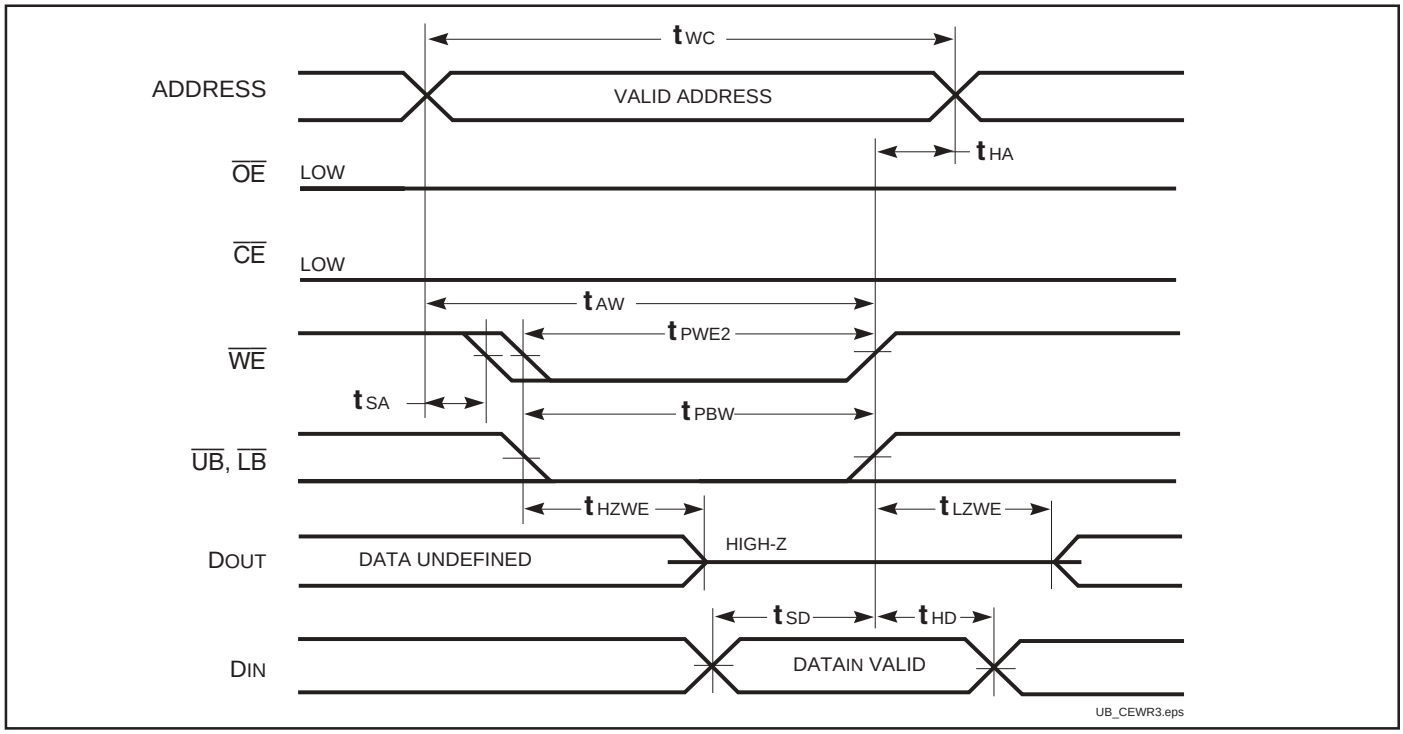
Notes:

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CE}$ and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = ($\overline{CE}$) [($\overline{LB}$) = ($\overline{UB}$)] ($\overline{WE}$).

WRITE CYCLE NO. 2 ($\overline{OE}$ is HIGH During Write Cycle) [1,2]



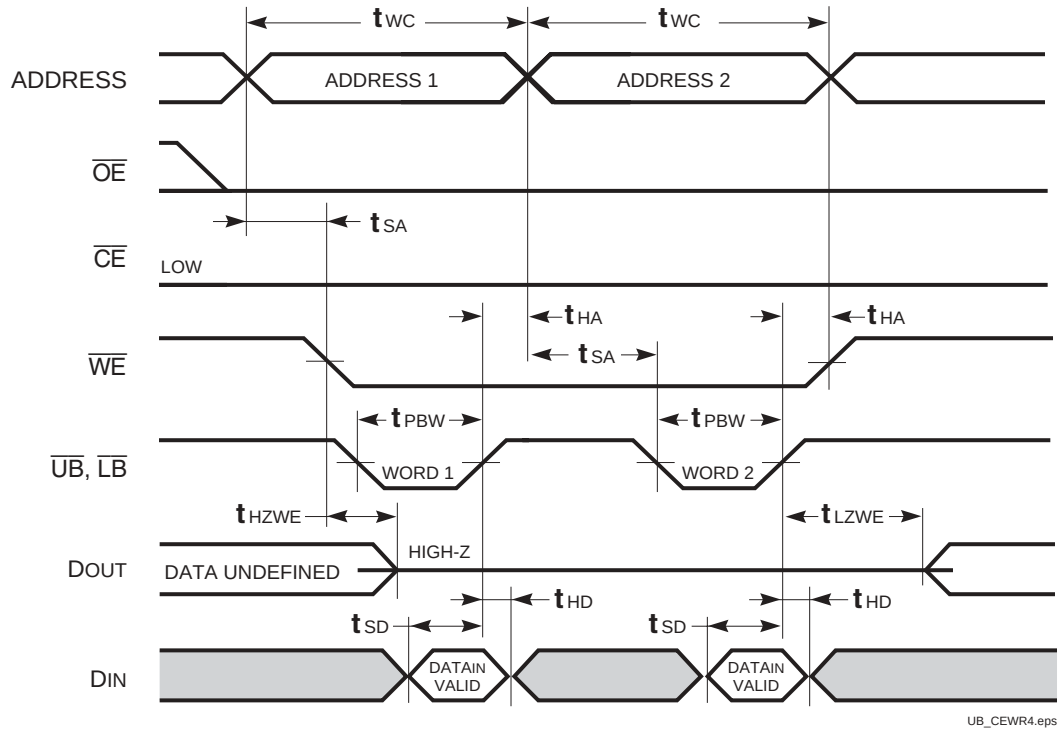
WRITE CYCLE NO. 3 ($\overline{OE}$ is LOW During Write Cycle) [1]



Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

WRITE CYCLE NO. 4 ($\overline{UB}$/$\overline{LB}$ Back to Back Write)



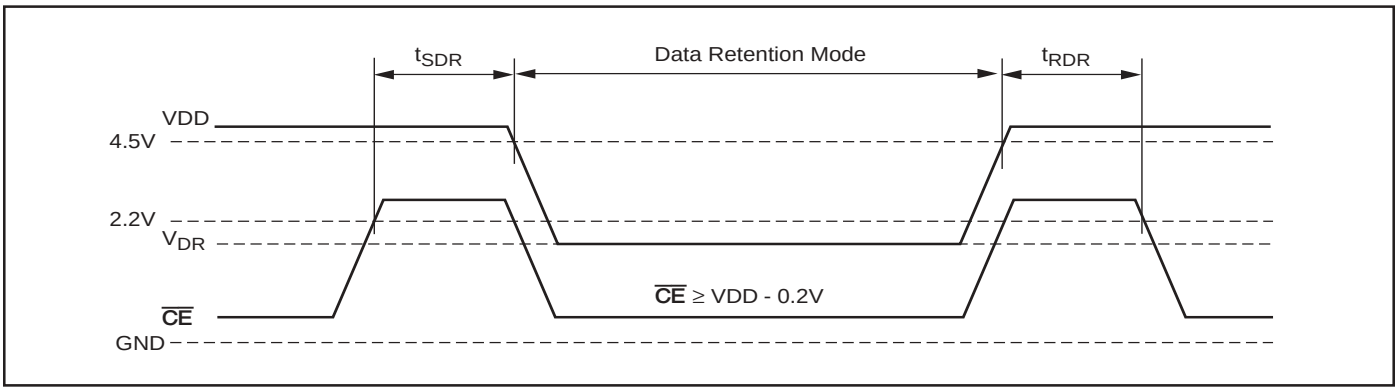
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.0		5.5	V
I_{DR}	Data Retention Current	V_{DD} = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$	Com.	—	—	350	µA
		$V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$	Ind.	—	—	400	
			typ.(1)		200		
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0		—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}		—	ns

Note:

1. Typical Values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



ORDERING INFORMATION: IS61C3216AL
Commercial Range: 0°C to +70°C

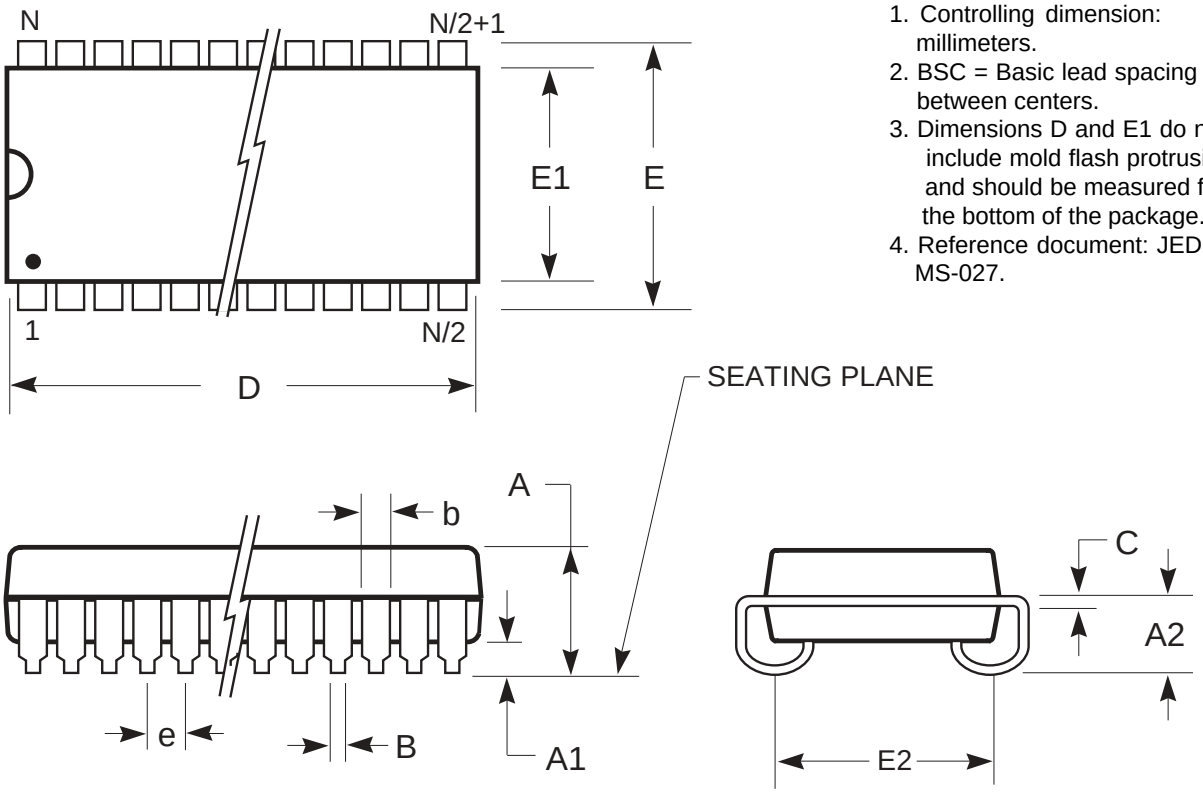
Speed (ns)	Order Part No.	Package
12	IS61C3216AL-12K	400-mil Plastic SOJ
	IS61C3216AL-12T	44-pin TSOP-II

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
12	IS61C3216AL-12KI	400-mil Plastic SOJ
	IS61C3216AL-12KLI	400-mil Plastic SOJ, Lead-free
	IS61C3216AL-12TI	44-pin TSOP-II
	IS61C3216AL-12TLI	44-pin TSOP-II, Lead-free

PACKAGING INFORMATION

400-mil Plastic SOJ
Package Code: K



Notes:
1. Controlling dimension: millimeters.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Reference document: JEDEC MS-027.

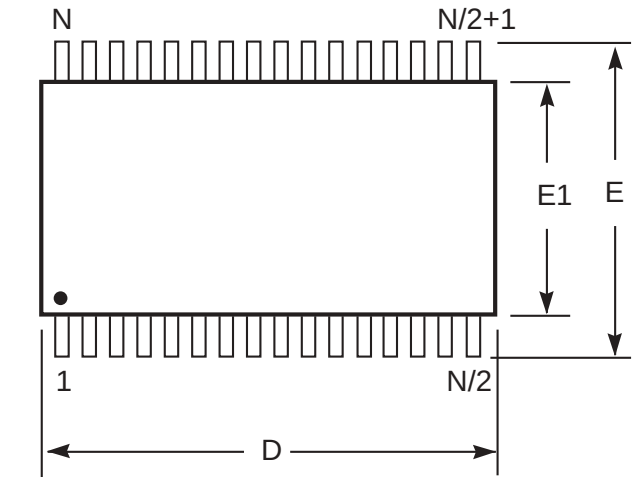
	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
No. Leads (N)		**28**				**32**				**36**		
A	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148
A1	0.64	—	0.025	—	0.64	—	0.025	—	0.64	—	0.025	—
A2	2.08	—	0.082	—	2.08	—	0.082	—	2.08	—	0.082	—
B	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020
b	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032
C	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013
D	18.29	18.54	0.720	0.730	20.82	21.08	0.820	0.830	23.37	23.62	0.920	0.930
E	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445
E1	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E2	9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC	
e	1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC	

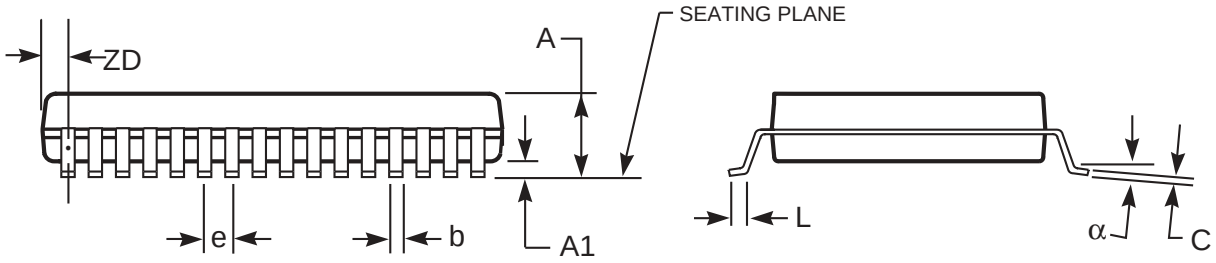
	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
No. Leads (N)		40				42				44		
A	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148
A1	0.64	—	0.025	—	0.64	—	0.025	—	0.64	—	0.025	—
A2	2.08	—	0.082	—	2.08	—	0.082	—	2.08	—	0.082	—
B	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020
b	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032
C	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013
D	25.91	26.16	1.020	1.030	27.18	27.43	1.070	1.080	28.45	28.70	1.120	1.130
E	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445
E1	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E2	9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC	
e	1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC	

PACKAGING INFORMATION

ISSI®

Plastic TSOP
Package Code: T (Type II)





Notes:
1. Controlling dimension: millimieters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

Plastic TSOP (T - Type II)

	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Ref. Std.												
No. Leads (N)		**32**				**44**				**50**		
A	—	1.20	—	0.047	—	1.20	—	0.047	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006
b	0.30	0.52	0.012	0.020	0.30	0.45	0.012	0.018	0.30	0.45	0.012	0.018
C	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008
D	20.82	21.08	0.820	0.830	18.31	18.52	0.721	0.729	20.82	21.08	0.820	0.830
E1	10.03	10.29	0.391	0.400	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E	11.56	11.96	0.451	0.466	11.56	11.96	0.455	0.471	11.56	11.96	0.455	0.471
e	1.27 BSC		0.050 BSC		0.80 BSC		0.032 BSC		0.80 BSC		0.031 BSC	
L	0.40	0.60	0.016	0.024	0.41	0.60	0.016	0.024	0.40	0.60	0.016	0.024
ZD	0.95 REF		0.037 REF		0.81 REF		0.032 REF		0.88 REF		0.035 REF	
α	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°

Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

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