

General Description

The 9ZML1232 is a 2-input/12-output differential mux for use in servers. It meets the demanding DB1200ZL performance specifications and utilizes Low-Power HCSL-compatible outputs to reduce power consumption and termination components. It is suitable for PCI-Express Gen1/2/3 or QPI/UPI applications, and uses a fixed external feedback to maintain low drift for demanding QPI applications.

Recommended Application

Clock Mux for Romley, Grantley and Purley Servers

Output Features

- 12 - Low-Power (LP) HCSL Output Pairs

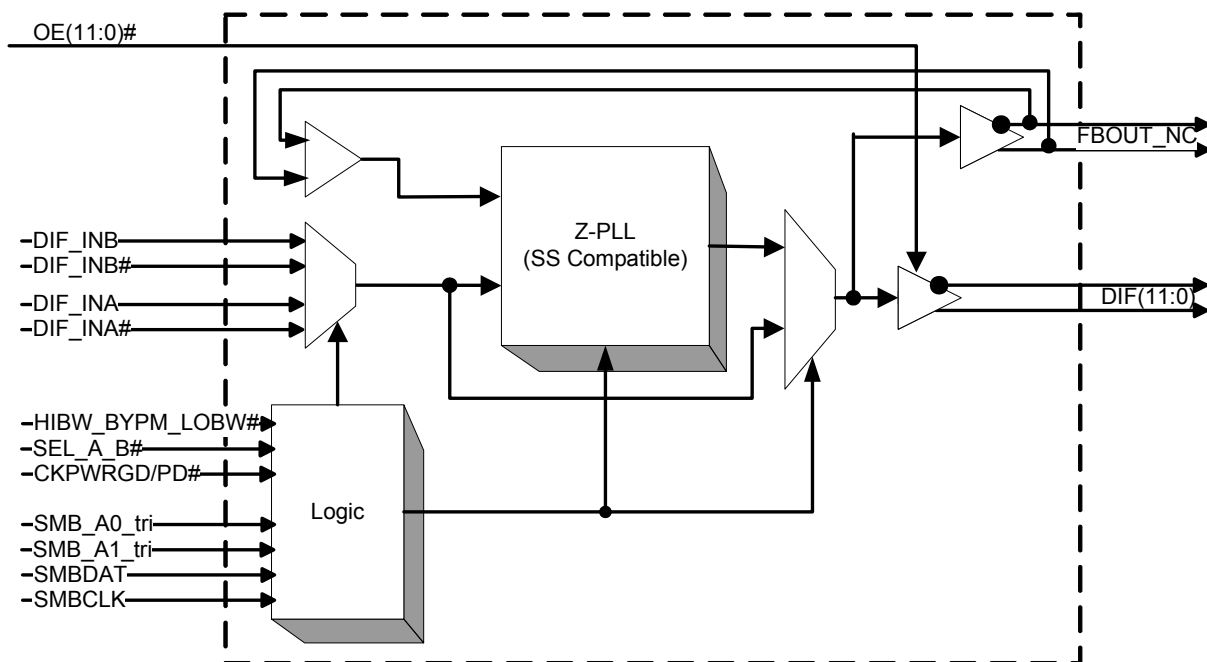
Features/Benefits

- Fixed feedback path; 0ps input-to-output delay
- 9 Selectable SMBus addresses; multiple devices can share same SMBus segment
- Separate VDDIO for outputs; allows maximum power savings
- PLL or bypass mode; PLL can dejitter incoming clock
- Hardware or Software-selectable PLL BW; minimizes jitter peaking in downstream PLL's
- Spread spectrum compatible; tracks spreading input clock for EMI reduction
- SMBus Interface; unused outputs can be disabled
- Differential outputs are Low/Low in power down; maximum power savings

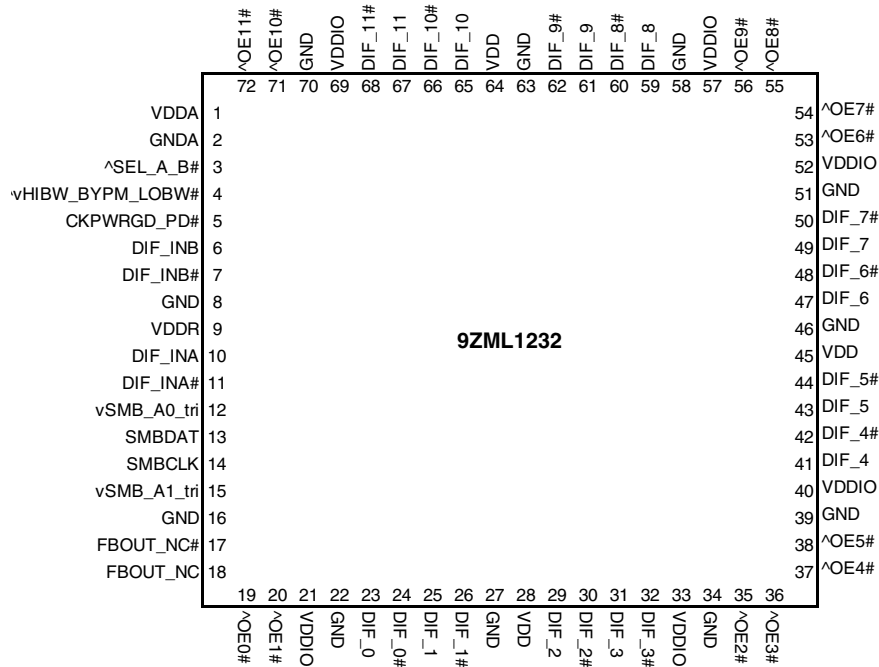
Key Specifications

- Cycle-to-cycle jitter <50ps
- Output-to-output skew <65 ps
- Input-to-output delay: Fixed at 0 ps
- Input-to-output delay variation <50ps
- Phase jitter: PCIe Gen3 <1ps rms
- Phase jitter: QPI/UPI 9.6GB/s <0.2ps rms

Block Diagram



Pin Configuration



^ prefix indicates internal 120Kohm Pull Up
 v prefix indicates internal 120Kohm Pull down
 10mm x 10mm 72-MLF, 0.5mm pin pitch

Power Management Table

| Inputs | | Control Bits | Outputs | | PLL State |
|-------------|--------------------|-----------------|----------------|-------------------------|-----------|
| CKPWRGD_PD# | DIF_IN/ DIF_IN# | SMBus EN bit | DIFx/ DIFx# | FBOUT_NC/ FB_OUT_NC# | |
| 0 | X | X | Low/Low | Low/Low | OFF |
| 1 | Running | 0 | Low/Low | Running | ON |
| | | 1 | Running | Running | ON |

PLL Operating Mode Table

| HiBW_BypM_LoBW# | Byte0, bit (7:6) |
|--------------------|------------------|
| Low (PLL Low BW) | 00 |
| Mid (Bypass) | 01 |
| High (PLL High BW) | 11 |

NOTE: PLL is off in Bypass mode

Tri-Level Input Thresholds

| Level | Voltage |
|-------|--------------|
| Low | <0.8V |
| Mid | 1.2<Vin<1.8V |
| High | Vin > 2.2V |

Power Connections

| Pin Number | | | Description |
|------------|---------------------------|--|--------------|
| VDD | VDDIO | GND | |
| 1 | | 2 | Analog PLL |
| 9 | | 8 | Analog Input |
| 28, 45, 64 | 21, 33, 40, 52, 57, 69 | 16, 22, 27, 34, 39, 46, 51, 58, 63, 70 | DIF clocks |

9ZML1232 SMBus Addressing

| SMB A(1:0)_tri | SMBus Address (Rd/Wrt bit = 0) |
|----------------|--------------------------------|
| 00 | D8 |
| 0M | DA |
| 01 | DE |
| M0 | C2 |
| MM | C4 |
| M1 | C6 |
| 10 | CA |
| 1M | CC |
| 11 | CE |

Pin Descriptions

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|-------|-------------------|------------|---|
| 1 | VDDA | PWR | 3.3V power for the PLL core. |
| 2 | GNDA | PWR | Ground pin for the PLL core. |
| 3 | ^SEL_A_B# | IN | Input to select differential input clock A or differential input clock B. This input has an internal pull-up resistor. 0 = Input B selected, 1 = Input A selected. |
| 4 | ^vHIBW_BYPM_LOBW# | LATCHED IN | Trilevel input to select High BW, Bypass or Low BW mode. See PLL Operating Mode Table for Details. |
| 5 | CKPWRGD_PD# | IN | 3.3V Input notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode. |
| 6 | DIF_INB | IN | 0.7 V HCSL-Compatible Differential True input |
| 7 | DIF_INB# | IN | 0.7 V HCSL-Compatible Differential Complement Input |
| 8 | GND | PWR | Ground pin. |
| 9 | VDDR | PWR | 3.3V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. |
| 10 | DIF_INA | IN | 0.7 V HCSL-Compatible Differential True input |
| 11 | DIF_INA# | IN | 0.7 V HCSL-Compatible Differential Complement Input |
| 12 | vSMB_A0_tri | IN | SMBus address bit. This is a tri-level input that works in conjunction with the SMB_A1 to decode 1 of 9 SMBus Addresses. It has an internal 120Kohm pull down resistor. |
| 13 | SMBDAT | I/O | Data pin of SMBUS circuitry, 5V tolerant |
| 14 | SMBCLK | IN | Clock pin of SMBUS circuitry, 5V tolerant |
| 15 | vSMB_A1_tri | IN | SMBus address bit. This is a tri-level input that works in conjunction with the SMB_A0 to decode 1 of 9 SMBus Addresses. It has an internal 120Kohm pull down resistor. |
| 16 | GND | PWR | Ground pin. |
| 17 | FBOUT_NC# | OUT | Complementary half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay. |
| 18 | FBOUT_NC | OUT | True half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay. |
| 19 | ^OE0# | IN | Active low input for enabling DIF pair 0. This pin has an internal pull-up resistor. 1 =disable outputs, 0 = enable outputs |
| 20 | ^OE1# | IN | Active low input for enabling DIF pair 1. This pin has an internal pull-up resistor. 1 =disable outputs, 0 = enable outputs |
| 21 | VDDIO | PWR | Power supply for differential outputs |
| 22 | GND | PWR | Ground pin. |
| 23 | DIF_0 | OUT | 0.7V differential true clock output |
| 24 | DIF_0# | OUT | 0.7V differential Complementary clock output |
| 25 | DIF_1 | OUT | 0.7V differential true clock output |
| 26 | DIF_1# | OUT | 0.7V differential Complementary clock output |
| 27 | GND | PWR | Ground pin. |
| 28 | VDD | PWR | Power supply, nominal 3.3V |
| 29 | DIF_2 | OUT | 0.7V differential true clock output |
| 30 | DIF_2# | OUT | 0.7V differential Complementary clock output |
| 31 | DIF_3 | OUT | 0.7V differential true clock output |
| 32 | DIF_3# | OUT | 0.7V differential Complementary clock output |
| 33 | VDDIO | PWR | Power supply for differential outputs |
| 34 | GND | PWR | Ground pin. |

Pin Descriptions (cont.)

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|-------|----------|----------|--|
| 35 | ^OE2# | IN | Active low input for enabling DIF pair 2. This pin has an internal pull-up resistor. 1 =disable outputs, 0 = enable outputs |
| 36 | ^OE3# | IN | Active low input for enabling DIF pair 3. This pin has an internal pull-up resistor. 1 =disable outputs, 0 = enable outputs |
| 37 | ^OE4# | IN | Active low input for enabling DIF pair 4. This pin has an internal pull-up resistor. 1 =disable outputs, 0 = enable outputs |
| 38 | ^OE5# | IN | Active low input for enabling DIF pair 5. This pin has an internal pull-up resistor. 1 =disable outputs, 0 = enable outputs |
| 39 | GND | PWR | Ground pin. |
| 40 | VDDIO | PWR | Power supply for differential outputs |
| 41 | DIF_4 | OUT | 0.7V differential true clock output |
| 42 | DIF_4# | OUT | 0.7V differential Complementary clock output |
| 43 | DIF_5 | OUT | 0.7V differential true clock output |
| 44 | DIF_5# | OUT | 0.7V differential Complementary clock output |
| 45 | VDD | PWR | Power supply, nominal 3.3V |
| 46 | GND | PWR | Ground pin. |
| 47 | DIF_6 | OUT | 0.7V differential true clock output |
| 48 | DIF_6# | OUT | 0.7V differential Complementary clock output |
| 49 | DIF_7 | OUT | 0.7V differential true clock output |
| 50 | DIF_7# | OUT | 0.7V differential Complementary clock output |
| 51 | GND | PWR | Ground pin. |
| 52 | VDDIO | PWR | Power supply for differential outputs |
| 53 | ^OE6# | IN | Active low input for enabling DIF pair 6. This pin has an internal pull-up resistor. 1 =disable outputs, 0 = enable outputs |
| 54 | ^OE7# | IN | Active low input for enabling DIF pair 7. This pin has an internal pull-up resistor. 1 =disable outputs, 0 = enable outputs |
| 55 | ^OE8# | IN | Active low input for enabling DIF pair 8. This pin has an internal pull-up resistor. 1 =disable outputs, 0 = enable outputs |
| 56 | ^OE9# | IN | Active low input for enabling DIF pair 9. This pin has an internal pull-up resistor. 1 =disable outputs, 0 = enable outputs |
| 57 | VDDIO | PWR | Power supply for differential outputs |
| 58 | GND | PWR | Ground pin. |
| 59 | DIF_8 | OUT | 0.7V differential true clock output |
| 60 | DIF_8# | OUT | 0.7V differential Complementary clock output |
| 61 | DIF_9 | OUT | 0.7V differential true clock output |
| 62 | DIF_9# | OUT | 0.7V differential Complementary clock output |
| 63 | GND | PWR | Ground pin. |
| 64 | VDD | PWR | Power supply, nominal 3.3V |
| 65 | DIF_10 | OUT | 0.7V differential true clock output |
| 66 | DIF_10# | OUT | 0.7V differential Complementary clock output |
| 67 | DIF_11 | OUT | 0.7V differential true clock output |
| 68 | DIF_11# | OUT | 0.7V differential Complementary clock output |
| 69 | VDDIO | PWR | Power supply for differential outputs |
| 70 | GND | PWR | Ground pin. |
| 71 | ^OE10# | IN | Active low input for enabling DIF pair 10. This pin has an internal pull-up resistor. 1 =disable outputs, 0 = enable outputs |
| 72 | ^OE11# | IN | Active low input for enabling DIF pair 11. This pin has an internal pull-up resistor. 1 =disable outputs, 0 = enable outputs |

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9ZML1232. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------|--------------------|----------------------------|---------|-----|-----------------------|-------|-------|
| 3.3V Core Supply Voltage | VDDA, R | | | | 4.6 | V | 1,2 |
| 3.3V Logic Supply Voltage | VDD | | | | 4.6 | V | 1,2 |
| I/O Supply Voltage | VDDIO | | | | 4.6 | V | 1,2 |
| Input Low Voltage | V _{IL} | | GND-0.5 | | | V | 1 |
| Input High Voltage | V _{IH} | Except for SMBus interface | | | V _{DD} +0.5V | V | 1 |
| Input High Voltage | V _{IHSMB} | SMBus clock and data pins | | | 5.5V | V | 1 |
| Storage Temperature | T _s | | -65 | | 150 | °C | 1 |
| Junction Temperature | T _j | | | | 125 | °C | 1 |
| Input ESD protection | ESD_prot | Human Body Model | 2000 | | | V | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics–DIF_IN Clock Input Parameters

TA = T_{COM}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|----------------------------------|--------------------|---|-----|-----|-----|-------|-------|
| Input Crossover Voltage - DIF_IN | V _{CROSS} | Cross Over Voltage | 150 | | 900 | mV | 1 |
| Input Swing - DIF_IN | V _{SWING} | Differential value | 300 | | | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.4 | | 8 | V/ns | 1,2 |
| Input Leakage Current | I _{IN} | V _{IN} = V _{DD} , V _{IN} = GND | -5 | | 5 | uA | |
| Input Duty Cycle | d _{tin} | Measurement from differential waveform | 45 | | 55 | % | 1 |
| Input Jitter - Cycle to Cycle | J _{DIFIN} | Differential Measurement | 0 | | 125 | ps | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics–Input/Supply/Common Output Parameters

TA = T_{COM}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|-------------------------------|-----------------------|---|-----------|--------|-----------------------|--------|-------|
| Ambient Operating Temperature | T _{COM} | Commercial range | 0 | 25 | 70 | °C | 1 |
| Input High Voltage | V _{IH} | Single-ended inputs, except SMBus, low threshold and tri-level inputs | 2 | | V _{DD} + 0.3 | V | 1 |
| Input Low Voltage | V _{IL} | Single-ended inputs, except SMBus, low threshold and tri-level inputs | GND - 0.3 | | 0.8 | V | 1 |
| Input Current | I _{IN} | Single-ended inputs, V _{IN} = GND, V _{IN} = VDD | -5 | -0.12 | 5 | uA | 1 |
| | I _{INP} | Single-ended inputs V _{IN} = 0 V; Inputs with internal pull-up resistors V _{IN} = VDD; Inputs with internal pull-down resistors | -200 | -0.02 | 200 | uA | 1 |
| Input Frequency | F _{ibyp} | V _{DD} = 3.3 V, Bypass mode | 33 | | 150 | MHz | 2 |
| | F _{ipll} | V _{DD} = 3.3 V, 100MHz PLL mode | 90 | 100.00 | 110 | MHz | 2 |
| Pin Inductance | L _{pin} | | | | 7 | nH | 1 |
| Capacitance | C _{IN} | Logic Inputs, except DIF_IN | 1.5 | | 5 | pF | 1 |
| | C _{INDIF_IN} | DIF_IN differential clock inputs | 1.5 | | 2.7 | pF | 1,4 |
| | C _{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| Clk Stabilization | T _{STAB} | From V _{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | | 1 | ms | 1,2 |
| Input SS Modulation Frequency | f _{MODIN} | Allowable Frequency (Triangular Modulation) | 30 | | 33 | kHz | 1 |
| OE# Latency | t _{LATOE#} | DIF start after OE# assertion DIF stop after OE# deassertion | 4 | | 12 | clocks | 1 |
| Tdrive_PD# | t _{DRVPD} | DIF output enable after PD# de-assertion | | | 300 | us | 1,3 |
| Tfall | t _F | Fall time of control inputs | | | 5 | ns | 1,2 |
| Trise | t _R | Rise time of control inputs | | | 5 | ns | 1,2 |
| SMBus Input Low Voltage | V _{ILSMB} | | | | 0.8 | V | 1 |
| SMBus Input High Voltage | V _{IHSMB} | | 2.1 | | V _{DDSMB} | V | 1 |
| SMBus Output Low Voltage | V _{OLSMB} | @ I _{PULLUP} | | | 0.4 | V | 1 |
| SMBus Sink Current | I _{PULLUP} | @ V _{OL} | 4 | | | mA | 1 |
| Nominal Bus Voltage | V _{DDSMB} | 3V to 5V +/- 10% | 2.7 | | 5.5 | V | 1 |
| SCLK/SDATA Rise Time | t _{RSMB} | (Max VIL - 0.15) to (Min VIH + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | t _{FSMB} | (Min VIH + 0.15) to (Max VIL - 0.15) | | | 300 | ns | 1 |
| SMBus Operating Frequency | f _{MAXSMB} | Maximum SMBus operating frequency | | | 400 | kHz | 1,5 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Control input must be monotonic from 20% to 80% of input swing.

³Time from deassertion until outputs are >200 mV

⁴DIF_IN input

⁵The differential input clock must be running for the SMBus to be active

Electrical Characteristics–DIF 0.7V Low Power Differential Outputs

TA = T_{COMI}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|------------|---|------|------|------|-------|---------|
| Slew rate | Trf | Scope averaging on | 1 | 3.3 | 4 | V/ns | 1, 2, 3 |
| Slew rate matching | ΔTrf | Slew rate matching, Scope averaging on | | 2 | 20 | % | 1, 2, 4 |
| Voltage High | VHigh | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660 | 804 | 850 | mV | 1 |
| Voltage Low | VLow | | -150 | 19 | 150 | | 1 |
| Max Voltage | Vmax | Measurement on single ended signal using absolute value. (Scope averaging off) | | 885 | 1150 | mV | 1 |
| Min Voltage | Vmin | | -300 | -29 | | | 1 |
| Vswing | Vswing | Scope averaging off | 300 | 1569 | | mV | 1, 2 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off | 300 | 465 | 550 | mV | 1, 5 |
| Crossing Voltage (var) | Δ-Vcross | Scope averaging off | | 12 | 140 | mV | 1, 6 |

¹Guaranteed by design and characterization, not 100% tested in production. C_L = 2pF with R_S = 27Ω for Zo = 85Ω differential trace impedance).

² Measured from differential waveform

³ Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

Electrical Characteristics–Current Consumption

TA = T_{COMI}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|-------------------------|--|-----|-----|-----|-------|-------|
| Operating Supply Current | I _{DDVDD} | All outputs @100MHz, C _L = 2pF; Zo=85 Ω | | 13 | 35 | mA | 1 |
| | I _{DDVDDA/R} | All outputs @100MHz, C _L = 2pF; Zo=85 Ω | | 14 | 20 | mA | 1 |
| | I _{DDVDDIO} | All outputs @100MHz, C _L = 2pF; Zo=85 Ω | | 86 | 100 | mA | 1 |
| Powerdown Current | I _{DDVDDPD} | All differential pairs low/low | | 0.7 | 4 | mA | 1,2 |
| | I _{DDVDDA/RPD} | All differential pairs low/low | | | 5 | mA | 1,2 |
| | I _{DDVDDIOPD} | All differential pairs low/low | | | 0.2 | mA | 1,2 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² With input clock running. Stopping the input clock will result in lower numbers.

Electrical Characteristics—Skew and Differential Jitter Parameters

TA = T_{COM}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|------------------------|--|------|------|------|----------|-----------|
| CLK_IN, DIF[x:0] | t _{SPO_PLL} | Input-to-Output Skew in PLL mode nominal value @ 25°C, 3.3V | -325 | -225 | -125 | ps | 1,2,4,5,8 |
| CLK_IN, DIF[x:0] | t _{PD_BYP} | Input-to-Output Skew in Bypass mode nominal value @ 25°C, 3.3V | 3 | 3.8 | 4.5 | ns | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t _{DSPO_PLL} | Input-to-Output Skew Variation in PLL mode across voltage and temperature | -50 | 0 | 50 | ps | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t _{DSPO_BYP} | Input-to-Output Skew Variation in Bypass mode across voltage and temperature | -250 | | 250 | ps | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t _{DTE} | Random Differential Tracking error between two 9ZM devices in Hi BW Mode | | | 5 | ps (rms) | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t _{DSSTE} | Random Differential Spread Spectrum Tracking error between two 9ZM devices in Hi BW Mode | | | 75 | ps | 1,2,3,5,8 |
| DIF{x:0} | t _{SKREW_ALL} | Output-to-Output Skew across all outputs (Common to Bypass and PLL mode) | | 40 | 65 | ps | 1,2,3,8 |
| PLL Jitter Peaking | j _{peak-hibw} | LOBW#_BYPASS_HIBW = 1 | 0 | | 2.5 | dB | 7,8 |
| PLL Jitter Peaking | j _{peak-lobw} | LOBW#_BYPASS_HIBW = 0 | 0 | | 2 | dB | 7,8 |
| PLL Bandwidth | pll _{HIBW} | LOBW#_BYPASS_HIBW = 1 | 2 | | 4 | MHz | 8,9 |
| PLL Bandwidth | pll _{LOBW} | LOBW#_BYPASS_HIBW = 0 | 0.7 | | 1.4 | MHz | 8,9 |
| Duty Cycle | t _{DC} | Measured differentially, PLL Mode | 45 | 50.2 | 55 | % | 1 |
| Duty Cycle Distortion | t _{DCD} | Measured differentially, Bypass Mode @100MHz | -2 | 0.8 | 2 | % | 1,10 |
| Jitter, Cycle to cycle | t _{jyc-cyc} | PLL mode | | 10 | 50 | ps | 1,11 |
| | | Additive Jitter in Bypass Mode | | 0.1 | 50 | ps | 1,11 |

Notes for preceding table:

- ¹ Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.
- ² Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.
- ³ All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.
- ⁴ This parameter is deterministic for a given device
- ⁵ Measured with scope averaging on to find mean value.
- ⁶ t is the period of the input clock
- ⁷ Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.
- ⁸ Guaranteed by design and characterization, not 100% tested in production.
- ⁹ Measured at 3 db down or half power point.
- ¹⁰ Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode
- ¹¹ Measured from differential waveform

Electrical Characteristics–Phase Jitter Parameters

TA = T_{COM}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | INDUSTRY LIMIT | UNITS | Notes |
|---------------------------------------|-------------------------|--|------|------|------|----------------|----------|---------|
| Phase Jitter, PLL Mode | t _{jphPCIEG1} | PCIe Gen 1 | 23 | 36 | 44 | 86 | ps (p-p) | 1,2,3 |
| | t _{jphPCIEG2} | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | 0.84 | 1.18 | 1.41 | 3 | ps (rms) | 1,2 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | 1.44 | 2.01 | 2.48 | 3.1 | ps (rms) | 1,2 |
| | t _{jphPCIEG3} | PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz) | 0.37 | 0.49 | 0.59 | 1 | ps (rms) | 1,2,4 |
| | t _{jphQPI_SMI} | QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) | 0.20 | 0.25 | 0.35 | 0.5 | ps (rms) | 1,5 |
| | | QPI & SMI (100MHz, 8.0Gb/s, 12UI) | 0.08 | 0.16 | 0.28 | 0.3 | ps (rms) | 1,5 |
| | | QPI & SMI (100MHz, 9.6Gb/s, 12UI) | 0.07 | 0.12 | 0.19 | 0.2 | ps (rms) | 1,5 |
| Additive Phase Jitter, Bypass mode | t _{jphPCIEG1} | PCIe Gen 1 | 0 | 3 | 10 | N/A | ps (p-p) | 1,2,3 |
| | t _{jphPCIEG2} | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | 0.09 | 0.13 | 0.30 | N/A | ps (rms) | 1,2,6 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | 0.00 | 0.10 | 0.70 | N/A | ps (rms) | 1,2,6 |
| | t _{jphPCIEG3} | PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz) | 0.00 | 0.10 | 0.30 | N/A | ps (rms) | 1,2,4,6 |
| | t _{jphQPI_SMI} | QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) | 0.00 | 0.10 | 0.30 | N/A | ps (rms) | 1,5,6 |
| | | QPI & SMI (100MHz, 8.0Gb/s, 12UI) | 0.04 | 0.05 | 0.10 | N/A | ps (rms) | 1,5,6 |
| | | QPI & SMI (100MHz, 9.6Gb/s, 12UI) | 0.04 | 0.05 | 0.10 | N/A | ps (rms) | 1,5,6 |

¹ Applies to all outputs.

² See <http://www.pcisig.com> for complete specs

³ Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴ Subject to final ratification by PCI SIG.

⁵ Calculated from Intel-supplied Clock Jitter Tool v 1.6.3

⁶ For RMS figures, additive jitter is calculated by solving the following equation: (Additive jitter)² = (total jitter)² - (input jitter)²

Clock Periods–Differential Outputs with Spread Spectrum Disabled

| SSC OFF | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|---------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|-------|
| | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| DIF | 100.00 | 9.94900 | | 9.99900 | 10.00000 | 10.00100 | | 10.05100 | ns | 1,2,3 |

Clock Periods–Differential Outputs with Spread Spectrum Enabled

| SSC ON | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|--------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|-------|
| | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| DIF | 99.75 | 9.94906 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.10107 | ns | 1,2,3 |

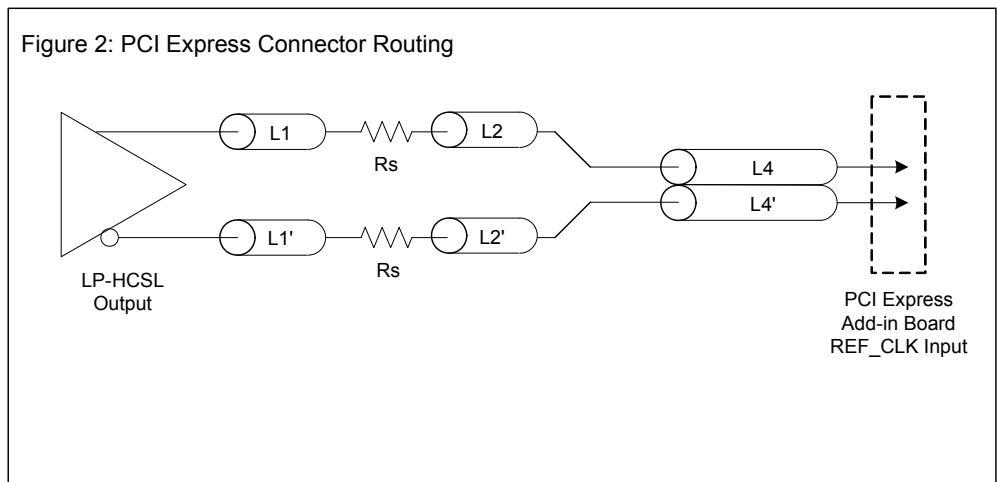
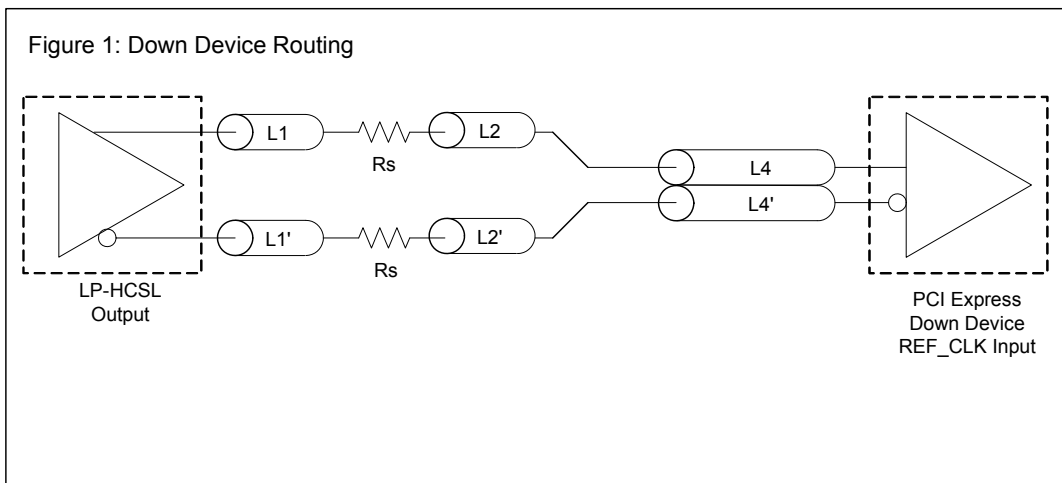
Notes:

- ¹ Guaranteed by design and characterization, not 100% tested in production.
- ² All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ accuracy requirements (+/-100ppm). The 9ZML1232 itself does not contribute to ppm error.
- ³ Driven by SRC output of main clock, 100 MHz PLL Mode or Bypass mode
- ⁴ Driven by CPU output of main clock, 133 MHz PLL Mode or Bypass mode

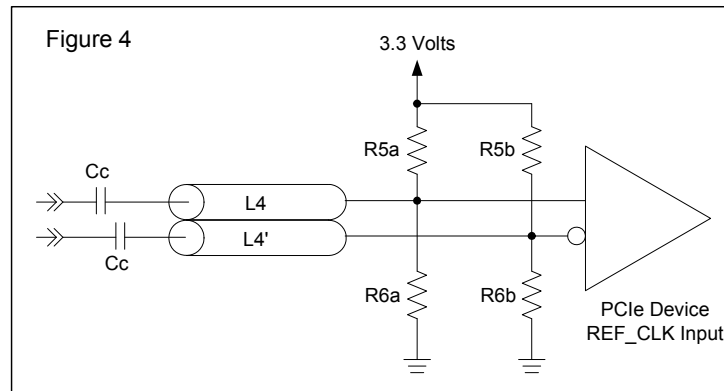
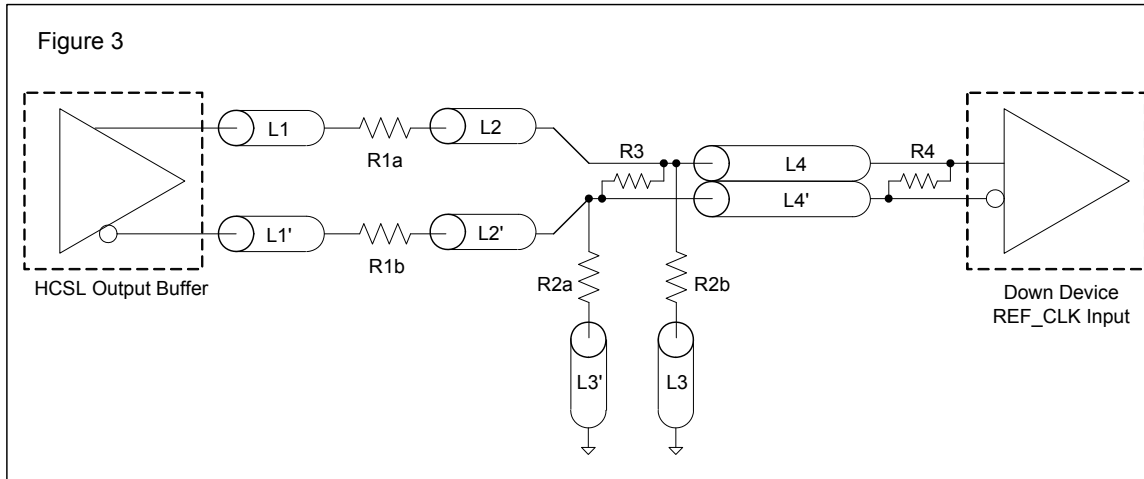
| DIF Reference Clock | | | |
|---|--------------------|------|--------|
| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
| L1 length, route as non-coupled 50ohm trace | 0.5 max | inch | 1 |
| L2 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| L3 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| Rs (100 ohm differential traces) | 33 | ohm | 1 |
| Rs (85 ohm differential traces) | 27 | ohm | 1 |

| Down Device Differential Routing | | | |
|--|---------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 2 min to 16 max | inch | 1 |
| L4 length, route as coupled stripline 100ohm differential trace | 1.8 min to 14.4 max | inch | 1 |

| Differential Routing to PCI Express Connector | | | |
|--|-----------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 0.25 to 14 max | inch | 2 |
| L4 length, route as coupled stripline 100ohm differential trace | 0.225 min to 12.6 max | inch | 2 |



| Cable Connected AC Coupled Application (Figure 3) | | |
|---|-------------|------|
| Component | Value | Note |
| R5a, R5b | 8.2K 5% | |
| R6a, R6b | 1K 5% | |
| Cc | 0.1 μ F | |
| Vcm | 0.350 volts | |



General SMBus Serial Interface Information for 9ZML1232

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation | | |
|-----------------------------|-----------|----------------------|
| Controller (Host) | | IDT (Slave/Receiver) |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| Beginning Byte = N | | ACK |
| Data Byte Count = X | | ACK |
| Beginning Byte N | | ACK |
| O | X Byte | O |
| O | | O |
| O | | O |
| Byte N + X - 1 | | ACK |
| P | stoP bit | |

9ZML1232 SMBus Addressing

| SMB_A(1:0) tri | SMBus Address (Rd/Wrt bit = 0) |
|----------------|--------------------------------|
| 00 | D8 |
| 0M | DA |
| 01 | DE |
| M0 | C2 |
| MM | C4 |
| M1 | C6 |
| 10 | CA |
| 1M | CC |
| 11 | CE |

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | |
|----------------------------|-----------------|----------------------|
| Controller (Host) | | IDT (Slave/Receiver) |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| Beginning Byte = N | | ACK |
| RT Repeat starT | | ACK |
| Slave Address | | |
| RD | ReaD | |
| Data Byte Count=X | | ACK |
| ACK | | |
| ACK | | Beginning Byte N |
| O | X Byte | O |
| O | | O |
| O | | O |
| Byte N + X - 1 | | ACK |
| N | Not acknowledge | |
| P | stoP bit | |

SMBusTable: PLL Mode, and Frequency Select Register

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|-------------|---|------|---------------------------------------|---------------|---------|
| Bit 7 | 4 | PLL Mode 1 | PLL Operating Mode Rd back 1 | R | See PLL Operating Mode Readback Table | | Latch |
| Bit 6 | 4 | PLL Mode 0 | PLL Operating Mode Rd back 0 | R | See PLL Operating Mode Readback Table | | Latch |
| Bit 5 | 3 | SEL_A_B# | Input Select Readback | R | DIF_INA | DIF_INB | Latch |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | Software_EN | Enable S/W control of PLL BW and Input Select | RW | HW Latch | SMBus Control | 0 |
| Bit 2 | | PLL Mode 1 | PLL Operating Mode 1 | RW | See PLL Operating Mode Readback Table | | 1 |
| Bit 1 | | PLL Mode 0 | PLL Operating Mode 1 | RW | See PLL Operating Mode Readback Table | | 1 |
| Bit 0 | | SEL_A_B# | Input Select | RW | DIF_INB | DIF_INA | 1 |

Note: Setting bit 3 to '1' allows the user to override the Latch value from pins 4 and 5 via use of bits [2:0]. Use the values from the PLL Operating Mode Readback Table. Note that Bits [7:5] will keep the value originally latched on pins 4 and 5. A warm reset of the system will have to be accomplished if the user changes Bits [2:0] bits.

SMBusTable: Output Control Register

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------|--|------|---------|--------|---------|
| Bit 7 | 49/50 | DIF 7 En | Output Control - '0' overrides OE# pin | RW | Low/Low | Enable | 1 |
| Bit 6 | 47/48 | DIF 6 En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 5 | 43/44 | DIF 5 En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 4 | 41/42 | DIF 4 En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 3 | 31/32 | DIF 3 En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 2 | 29/30 | DIF 2 En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 1 | 25/26 | DIF 1 En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 0 | 23/24 | DIF 0 En | Output Control - '0' overrides OE# pin | RW | | | 1 |

SMBusTable: Output Control Register

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|-----------|--|------|---------|--------|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | 67/68 | DIF 11 En | Output Control - '0' overrides OE# pin | RW | Low/Low | Enable | 1 |
| Bit 2 | 65/66 | DIF 10 En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 1 | 61/62 | DIF 9 En | Output Control - '0' overrides OE# pin | RW | | | 1 |
| Bit 0 | 59/60 | DIF 8 En | Output Control - '0' overrides OE# pin | RW | | | 1 |

SMBusTable: Output Amplitude Control Register

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | | Reserved | | | | 0 |
| Bit 2 | | AMP2 | Output Amplitude | RW | 000=350mV, 001=450mV, 010=550mV, 011=650mV, 100=750mV 101=850mV, 110=950mV, 111=Reserved | | 1 |
| Bit 1 | | AMP1 | | RW | | | 0 |
| Bit 0 | | AMP0 | | RW | | | 0 |

SMBusTable: Reserved Register

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | | Reserved | | | | 0 |
| Bit 2 | | | Reserved | | | | 0 |
| Bit 1 | | | Reserved | | | | 0 |
| Bit 0 | | | Reserved | | | | 0 |

SMBusTable: Vendor & Revision ID Register

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|------------------------------|---|---------|
| Bit 7 | - | RID3 | REVISION ID | R | A rev = 0000 B rev = 0001 | | X |
| Bit 6 | - | RID2 | | R | | | X |
| Bit 5 | - | RID1 | | R | | | X |
| Bit 4 | - | RID0 | | R | | | X |
| Bit 3 | - | VID3 | VENDOR ID | R | - | - | 0 |
| Bit 2 | - | VID2 | | R | - | - | 0 |
| Bit 1 | - | VID1 | | R | - | - | 0 |
| Bit 0 | - | VID0 | | R | - | - | 1 |

SMBusTable: DEVICE ID

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|-------------------|------------------|------|-------------------|---|---------|
| Bit 7 | - | Device ID 7 (MSB) | | R | 9ZML1231 = F1 hex | | 1 |
| Bit 6 | - | Device ID 6 | | R | | | 1 |
| Bit 5 | - | Device ID 5 | | R | | | 1 |
| Bit 4 | - | Device ID 4 | | R | | | 1 |
| Bit 3 | - | Device ID 3 | | R | | | 0 |
| Bit 2 | - | Device ID 2 | | R | | | 0 |
| Bit 1 | - | Device ID 1 | | R | | | 0 |
| Bit 0 | - | Device ID 0 | | R | | | 1 |

SMBusTable: Byte Count Register

| Byte 7 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|---|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | - | BC4 | Writing to this register configures how many bytes will be read back. | RW | Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default. | | 0 |
| Bit 3 | - | BC3 | | RW | | | 1 |
| Bit 2 | - | BC2 | | RW | | | 0 |
| Bit 1 | - | BC1 | | RW | | | 0 |
| Bit 0 | - | BC0 | | RW | | | 0 |

SMBusTable: Reserved Register

| Byte 8 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | | Reserved | | | | 0 |
| Bit 2 | | | Reserved | | | | 0 |
| Bit 1 | | | Reserved | | | | 0 |
| Bit 0 | | | Reserved | | | | 0 |

Marking Diagram



Notes:

1. "L" denotes RoHS compliant package.
2. 'LOT' denotes the lot number.
3. "COO": country of origin.
4. YYWW is the last two digits of the year and week that the part was assembled.

Revision History

| Rev. | Issuer | Issue Date | Description | Page # |
|------|--------|------------|---|--------|
| A | RDW | 8/17/2012 | Updated electrical characteristics and move to final. | |
| B | RDW | 10/2/2012 | Corrected Phase Jitter Parameters | 9 |
| C | RDW | 3/24/2014 | 1. Corrected pin references in Byte 0, bits (7:5) from 4 and 5 to 3 and 4. | 14 |
| D | RDW | 9/16/2015 | Corrected typo in general description; changed DB1900Z to DB1200ZL | 1 |
| E | RDW | 11/20/2015 | 1. Updated QPI references to QPI/UPI 2. Updated DIF_IN table to match PCI SIG specification, no silicon change | 1,5 |

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