

## PRECISION TIMERS

### Description

These devices are precision timing circuits capable of producing accurate time delays or oscillation. In the timedelay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

The threshold and trigger levels normally are two-thirds and one-third, respectively, of  $V_{CC}$ . These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set, and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset, and the output goes low. When the output is low, a low-impedance path is provided between discharge (DISCH) and ground.

The output circuit is capable of sinking or sourcing current up to 200mA. Operation is specified for supplies of 5V to 15V. With a 5-V supply, output levels are compatible with TTL inputs.

## **Pin Assignments**



### Features

- Timing from microseconds to hours
- Astable or monostable operation
- Adjustable duty cycle
- TTL compatible output can source or sink up to 200mA
- "Green" Molding Compound (No Br, Sb)
- Lead Free Finish/ RoHS Compliant (Note 1)
- Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at http://www.diodes.com/products/lead\_free.html.



## PRECISION TIMERS

## **Pin Descriptions**

Pin Name	Pin Number	Description
GND	1	Ground
TRIG	2	Trigger set 1/3V <sub>CC</sub>
OUT	3	Timer output
RESET	4	Reset active low
CONT	5	External adjustment of internal threshold and trigger voltages
THRES	6	Threshold set to 2/3 V <sub>CC</sub>
DISCH	7	Low impedance discharge path
V <sub>CC</sub>	8	Chip supply voltage

## **Functional Block Diagram**



#### **RESET** can override TRIG, which can override THRESH

## **Functional Table**

Pin Name	Nominal Trigger Voltage	Threshold Voltage	Output	Discharge Switch
GND	Irrelevant	Irrelevant	Low	On
TRIG	<1/3V <sub>CC</sub>	Irrelevant	High	Off
OUT	<1/3V <sub>CC</sub>	<2/3V <sub>CC</sub>	Low	On
RESET	<1/3V <sub>CC</sub>	<2/3V <sub>CC</sub>	As previou	isly established



## **PRECISION TIMERS**

### Absolute Maximum Ratings (Note 2) @ T<sub>A</sub> = 25°C unless otherwise stated

Symbol	Para	Rating	Unit	
V <sub>CC</sub>	Supply voltage (Note 3)		18	V
VI	Input voltage	CONT, RESET, THRES, TRIG	V <sub>CC</sub>	V
Ι <sub>Ο</sub>	Output current		±225	mA
θ <sub>JA</sub>	Package thermal resistance Junction	130	°C/W	
θ <sub>JC</sub>	Package thermal resistance Juncti	15	°C/W	
ΤJ	Junction temperature	150	°C	
T <sub>STG</sub>	Storage temperature	-65 to 150	°C	

### **Recommended Operating Conditions** (T<sub>A</sub> = 25°C)

Symbol	Para	meter	Min	Max	Unit
V <sub>CC</sub>	Supply voltage	4.5	16	V	
VI	Input voltage	CONT, RESET, THRES, TRIG		V <sub>CC</sub>	V
Ι <sub>Ο</sub>	Output current		±200	mA	
		NE555	0	70	
T <sub>A</sub>	Operating Ambient Temperature	SA555	-40	85	°C
		NA555	-40	105	

Notes: 2. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3. All voltage values are with respect ground.

4. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.

5. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JC}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) - T_C)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.

### Electrical Characteristics ( $V_{CC} = 5V$ to 15V, $T_A = 25^{\circ}C$ unless otherwise stated)

Symbol	Parameter	Test conditions	Min	Тур.	Max	Unit	
V		$V_{CC} = 15V$	8.8	10	11.2	N	
∨тн	Threshold voltage level	$V_{CC} = 5V$	2.4	3.3	4.2	v	
I <sub>TH</sub>	Threshold current (Note 6)			30	250	nA	
\/		$V_{CC} = 15V$	4.5	5	5.6		
۷TR	l rigger voltage level	$V_{CC} = 5V$	1.1	1.67	2.2	v	
I <sub>TR</sub>	Trigger current	TRIG at 0V		0.5	2	μA	
V <sub>RST</sub>	RESET voltage level		0.3	0.7	1	V	
I		RESET at V <sub>CC</sub>		0.1	0.4		
IRST	RESET current	RESET at 0V		-0.4	-1.5	ШA	
I <sub>DIS</sub>	DISCH switch off-state current			20	100	nA	
M	DISCH saturation voltage with	V <sub>CC</sub> = 15V, I <sub>DIS</sub> = 15mA		180	480		
V DIS	output low (Note 7)	$V_{CC} = 5V$ , $I_{DIS} = 4.5mA$		80	200	mv	
Maari		$V_{CC} = 15V$	9	10	11	V	
V CON	CONT voltage (open circuit)	$V_{CC} = 5V$	2.6	3.3	4	V	



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### Electrical Characteristics (V<sub>CC</sub> = 5V to 15V, T<sub>A</sub> = 25°C unless otherwise stated)

Symbol	Parameter	Test conditio	ons	Min	Тур.	Max	Unit
		V <sub>CC</sub> = 15V, I <sub>OL</sub> = 10mA			0.1	0.25	
		V <sub>CC</sub> = 15V, I <sub>OL</sub> = 50mA		0.4	0.75		
		V <sub>CC</sub> = 15V, I <sub>OL</sub> = 100mA			2	2.5	
VOL	Low level output voltage	V <sub>CC</sub> = 15V, I <sub>OL</sub> = 200mA			2.5		V
		$V_{CC} = 5V, I_{OL} = 5mA$			0.1	0.35	
		$V_{CC} = 5V, I_{OL} = 8mA$			0.15	0.4	
		V <sub>CC</sub> = 15V, I <sub>OH</sub> = -100mA	١	12.75	13.3		
V <sub>OH</sub>	High level output voltage	V <sub>CC</sub> = 15V, I <sub>OH</sub> = -200mA	۸		12.5		V
		V <sub>CC</sub> = 5V, I <sub>OH</sub> = -100mA		2.75	3.3		
			$V_{CC} = 15V$		10	15	- mA
	Supply current	Output low, no load	$V_{CC} = 5V$		3	6	
ICC		Output high, no load	$V_{CC} = 15V$		9	13	
			$V_{CC} = 5V$		2	5	
		Each time, monostable			4	0	
<b>T</b>	Initial error of timing interval (Note 8)	(Note 9)			1	3	3 %
I ER		Each time, astable			2 25		
		(Note 10)			2.25		
		Each time, monostable			50		
TTC	Temperature coefficient of timing	(Note 9)	$T_A = full$				ppm/°C
	Interval	Each time, astable	range		150		PP
		(Note 10)					
T <sub>VCC</sub>	Supply voltage consitivity of	Each time, monostable			0.1	0.5	
	Supply voltage sensitivity of	Fach time astable	_				%/V
		(Note 10)			0.3		
TRI	Output pulse rise time		C <sub>1</sub> = 15pF		100	300	ns
TFA	Output pulse fall time		$C_1 = 15 pF$		100	300	ns

6. This parameter influences the maximum value of the timing resistors RA and RB in the circuit of Figure 12. For example, when V<sub>CC</sub> = 5 V, the Notes:

maximum value is R = RA + RB  $\approx$  3.4MΩ, and for V\_{CC} = 15 V, the maximum value is 10MΩ.

No protection against excessive pin 7 current is necessary providing package dissipation rating is not exceeded
Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.

9. Values specified are for a device in a monostable circuit similar to Figure 9, with the following component values:  $R_A = 2k\Omega$  to  $100k\Omega$ , C = 0.1uF. 10. Values specified are for a device in an astable circuit similar to Figure 12, with the following component values: RA = 1kΩ to 100kΩ, C = 0.1uF.



## PRECISION TIMERS

## **Typical Performance Characteristics**



NE555/SA555/NA555 Document number: DS35112 Rev. 4 - 2



## PRECISION TIMERS

## Typical Performance Characteristics (cont.)





NE555/SA555/NA555 Document number: DS35112 Rev. 4 - 2



## PRECISION TIMERS

### **Typical Applications Characteristics**

#### **Monostable Operation**

For monostable operation, any of the '555 timers can be connected as shown in Figure 1. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the internal flip-flop and drives the output high. Capacitor C is then charged through  $R_A$  until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the internal flip-flop, drives the output low, and discharges C.



#### Fig 1. Monostable operation

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high for at least 10µs before the end of the timing interval. When the trigger is grounded, the comparator storage time can be as long as 10µs, which limits the minimum monostable pulse width to 10µs. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately  $t_W = 1.1R_AC$ . Figure 3 is a plot of the time constant for various values of  $R_A$  and C. The threshold levels and charge rates both are directly proportional to the supply voltage, V<sub>CC</sub>. The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used, it should be connected to  $V_{CC}$ .







Fig. 3 Output Pulse Duration vs. Capacitance



### **Typical Applications Characteristics (cont.)**

#### **Astable Operation**

As shown in Figure 4, adding a second resistor,  $R_B$ , to the circuit of Figure 1 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor C charges through  $R_A$  and  $R_B$  and then discharges through  $R_B$ . Therefore, the duty cycle is controlled by the values of  $R_A$  and  $R_B$ .

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ( $\approx 0.67 V_{CC}$ ) and the trigger-voltage level ( $\approx 0.33 V_{CC}$ ). As in the monostable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.



Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

#### Fig. 4 Circuit for Astable Operation



Time – 0.5ms/div

#### Fig. 5 Typical Astable Waveforms

Figure 5 shows typical waveforms generated during astable operation. The output high-level duration  $t_H$  and low-level duration  $t_I$  can be calculated as follows:

 $t_{H} = 0.693(R_{A} + R_{B})C$ 

 $t_{L} = 0.693(R_{B})C$ 

Other useful equations are:

 $period = t_H + t_L = 0.693(R_A + 2R_B)C$ 

frequency = 
$$1.44/(R_A + 2R_B)C$$

output driver duty cycle =  $t_L/(t_H + t_L) = R_B/(R_A + 2R_B)$ 

output waveform duty cycle =  $t_H/(t_H + t_L) = 1 - R_B/(R_A + 2R_B)$ 

low to high ratio =  $t_L/t_H = R_B/(R_A + R_B)$ 



Fig. 6 Free Running Frequency



## PRECISION TIMERS

### **Typical Applications Characteristics (cont.)**

#### **Missing Pulse Detector**

The circuit shown in Figure 7 can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is retriggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in Figure 8.



Fig. 7 Circuit for Missing Pulse Dectector



#### Fig. 8 Timing Waveforms for Missing Pulse Dectector

#### **Frequency Divider**

By adjusting the length of the timing cycle, the basic circuit of Figure 1 can be made to operate as a frequency divider. Figure 9 shows a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.



Time – 0.1ms/div

Fig. 9 Divide by Three Circuit Waveforms



## PRECISION TIMERS

## **Typical Applications Characteristics (cont.)**

#### **Pulse Width Modulation**

The operation of the timer can be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 10 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 11 shows the resulting output pulse-width modulation. While a sine-wave modulation signal is shown, any wave shape could be used.



The modulating signal can be directly or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

#### Fig 10. Circuit for Pulse width modulation



Fig 11. Pulse width modulation timing diagrams

#### **Pulse Position Modulation**

As shown in Figure 12, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and, thereby, the time delay, of a free-running oscillator. Figure 13 shows a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.



The modulating signal can be directly or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

#### Fig 12. Circuit for pulse position modulation







## PRECISION TIMERS

## **Typical Applications Characteristics (cont.)**

#### **Sequential Timer**

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits can be connected to provide such sequential control. The timers can be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 14 shows a sequencer circuit with possible applications in many systems, and Figure 15 shows the output waveforms.





Fig 14. Circuit for Sequential Timer



t - Time - 1s/div

Fig 15. Sequential timer waveforms



## **PRECISION TIMERS**

## **Ordering Information**



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	Dovice	Operating	Package	Packaging	13" Tape and Reel		
	Device	Temperature	Code	(Note 10)	Quantity	Part Number Suffix	
Pb,	NE555S-13	0 to 70°C	S	SO-8	2500/Tape & Reel	-13	
B	SA555S-13	-40 to 85°C	S	SO-8	2500/Tape & Reel	-13	
Po	NA555S-13	-40 to 105°C	S	SO-8	2500/Tape & Reel	-13	

 Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.

## **Marking Information**



Notes:





## PRECISION TIMERS

## Package Outline Dimensions (All Dimensions in mm)

#### SO-8



	SO-8					
Dim	Min	Max				
Α	-	1.75				
A1	0.10	0.20				
A2	1.30	1.50				
A3	0.15	0.25				
b	0.3	0.5				
D	4.85	4.95				
Е	5.90	6.10				
E1	3.85	3.95				
е	1.27	Тур				
h	-	0.35				
L	0.62	0.82				
θ	0°	8°				
All Di	mensions	in mm				

## **Suggested Pad Layout**

#### SO-8



Dimensions	Value (in mm)
Х	0.60
Y	1.55
C1	5.4
C2	1.27



## PRECISION TIMERS

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