

# MC74LCX02

## Low-Voltage CMOS Quad 2-Input NOR Gate

### With 5 V-Tolerant Inputs

The MC74LCX02 is a high performance, quad 2-input NOR gate operating from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_I$  specification of 5.5 V allows MC74LCX02 inputs to be safely driven from 5 V devices.

Current drive capability is 24 mA at the outputs.

#### Features

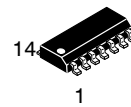
- Designed for 2.3 V to 3.6 V  $V_{CC}$  Operation
- 5 V Tolerant Inputs – Interface Capability With 5 V TTL Logic
- LVTTL Compatible
- LVC MOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10  $\mu$ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance: Human Body Model >2000 V;  
Machine Model >200 V
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



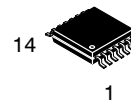
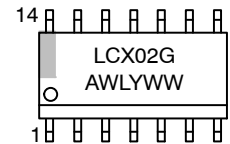
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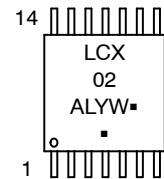
#### MARKING DIAGRAMS



SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



A = Assembly Location  
WL, L = Wafer Lot  
Y = Year  
WW, W = Work Week  
G or ▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

# MC74LCX02

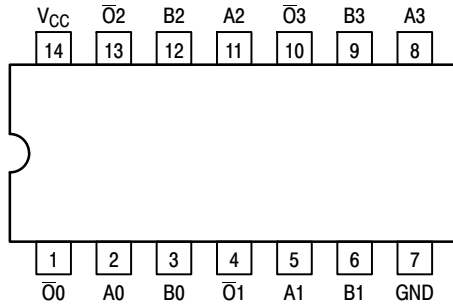


Figure 1. Pinout: 14-Lead (Top View)

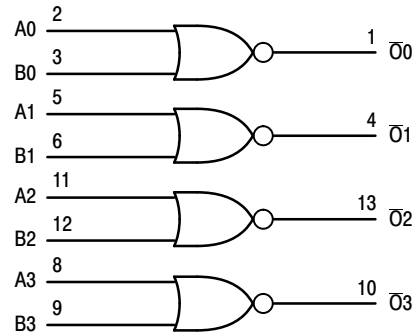


Figure 2. Logic Diagram

## PIN NAMES

Pins	Function
An, Bn	Data Inputs
$\bar{O}_n$	Outputs

## TRUTH TABLE

Inputs		Outputs
An	Bn	$\bar{O}_n$
L	L	H
L	H	L
H	L	L
H	H	L

H = High Voltage Level  
L = Low Voltage Level

For  $I_{CC}$  reasons, DO NOT FLOAT Inputs

## MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
$V_{CC}$	DC Supply Voltage	-0.5 to +7.0		V
$V_I$	DC Input Voltage	$-0.5 \leq V_I \leq +7.0$		V
$V_O$	DC Output Voltage	$-0.5 \leq V_O \leq V_{CC} + 0.5$	Output in HIGH or LOW State (Note 1)	V
$I_{IK}$	DC Input Diode Current	-50	$V_I < GND$	mA
$I_{OK}$	DC Output Diode Current	-50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA
$I_{CC}$	DC Supply Current Per Supply Pin	$\pm 100$		mA
$I_{GND}$	DC Ground Current Per Ground Pin	$\pm 100$		mA
$T_{STG}$	Storage Temperature Range	-65 to +150		$^{\circ}C$
MSL	Moisture Sensitivity		Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1.  $I_O$  absolute maximum rating must be observed.

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## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Type	Max	Unit
V <sub>CC</sub>	Supply Voltage	Operating	2.5, 3.3	3.6	V
		Data Retention Only	2.5, 3.3	3.6	
V <sub>I</sub>	Input Voltage	0		5.5	V
V <sub>O</sub>	Output Voltage (HIGH or LOW State) (3-State)	0		V <sub>CC</sub>	V
I <sub>OH</sub>	HIGH Level Output Current			-24 -12 -8	mA
I <sub>OL</sub>	LOW Level Output Current	V <sub>CC</sub> = 3.0 V – 3.6 V		+24	mA
		V <sub>CC</sub> = 2.7 V – 3.0 V		+12	
		V <sub>CC</sub> = 2.3 V – 2.7 V		+8	
T <sub>A</sub>	Operating Free-Air Temperature	-40		+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V <sub>IN</sub> from 0.8 V to 2.0 V, V <sub>CC</sub> = 3.0 V	0		10	ns/V

## DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T <sub>A</sub> = -40°C to +85°C		Unit
			Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage (Note 2)	2.3 V ≤ V <sub>CC</sub> ≤ 2.7 V	1.7		V
		2.7 V ≤ V <sub>CC</sub> ≤ 3.6 V	2.0		
V <sub>IL</sub>	LOW Level Input Voltage (Note 2)	2.3 V ≤ V <sub>CC</sub> ≤ 2.7 V		0.7	V
		2.7 V ≤ V <sub>CC</sub> ≤ 3.6 V		0.8	
V <sub>OH</sub>	HIGH Level Output Voltage	2.3 V ≤ V <sub>CC</sub> ≤ 3.6 V; I <sub>OH</sub> = -100 μA	V <sub>CC</sub> - 0.2		V
		V <sub>CC</sub> = 2.3 V; I <sub>OH</sub> = -8 mA	1.8		
		V <sub>CC</sub> = 2.7 V; I <sub>OH</sub> = -12 mA	2.2		
		V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -18 mA	2.4		
		V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -24 mA	2.2		
V <sub>OL</sub>	LOW Level Output Voltage	2.3 V ≤ V <sub>CC</sub> ≤ 3.6 V; I <sub>OL</sub> = 100 μA		0.2	V
		V <sub>CC</sub> = 2.3 V; I <sub>OL</sub> = 8 mA		0.6	
		V <sub>CC</sub> = 2.7 V; I <sub>OL</sub> = 12 mA		0.4	
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 16 mA		0.4	
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 24 mA		0.55	
I <sub>OFF</sub>	Power Off Leakage Current	V <sub>CC</sub> = 0, V <sub>IN</sub> = 5.5 V or V <sub>OUT</sub> = 5.5 V		10	μA
I <sub>IN</sub>	Input Leakage Current	V <sub>CC</sub> = 3.6 V, V <sub>IN</sub> = 5.5 V or GND		±5	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>CC</sub> = 3.6 V, V <sub>IN</sub> = 5.5 V or GND		10	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	2.3 ≤ V <sub>CC</sub> ≤ 3.6 V; V <sub>IH</sub> = V <sub>CC</sub> - 0.6 V		500	μA

2. These values of V<sub>I</sub> are used to test DC electrical characteristics only.

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## AC CHARACTERISTICS ( $t_R = t_F = 2.5 \text{ ns}$ ; $R_L = 500 \Omega$ )

Symbol	Parameter	Waveform	Limits						Unit
			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$						
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		
			$C_L = 50 \text{ pF}$		$C_L = 50 \text{ pF}$		$C_L = 30 \text{ pF}$		
			Min	Max	Min	Max	Min	Max	
$t_{PLH}$	Propagation Delay Time	1	1.5	5.5	1.5	6.2	1.5	6.6	ns
$t_{PHL}$	Input-to-Output		1.5	5.5	1.5	6.2	1.5	6.6	
$t_{OSHL}$	Output-to-Output Skew			1.0					ns
$t_{OSLH}$	(Note 3)			1.0					

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ); parameter guaranteed by design.

## DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25^\circ\text{C}$			Unit
			Min	Typ	Max	
$V_{OLP}$	Dynamic LOW Peak Voltage (Note 4)	$V_{CC} = 3.3 \text{ V}$ , $C_L = 50 \text{ pF}$ , $V_{IH} = 3.3 \text{ V}$ , $V_{IL} = 0 \text{ V}$		0.8		V
		$V_{CC} = 2.5 \text{ V}$ , $C_L = 30 \text{ pF}$ , $V_{IH} = 2.5 \text{ V}$ , $V_{IL} = 0 \text{ V}$		0.6		V
$V_{OLV}$	Dynamic LOW Valley Voltage (Note 4)	$V_{CC} = 3.3 \text{ V}$ , $C_L = 50 \text{ pF}$ , $V_{IH} = 3.3 \text{ V}$ , $V_{IL} = 0 \text{ V}$		-0.8		V
		$V_{CC} = 2.5 \text{ V}$ , $C_L = 30 \text{ pF}$ , $V_{IH} = 2.5 \text{ V}$ , $V_{IL} = 0 \text{ V}$		-0.6		V

4. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
$C_{IN}$	Input Capacitance	$V_{CC} = 3.3 \text{ V}$ , $V_I = 0 \text{ V}$ or $V_{CC}$	7	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = 3.3 \text{ V}$ , $V_I = 0 \text{ V}$ or $V_{CC}$	8	pF
$C_{PD}$	Power Dissipation Capacitance	10 MHz, $V_{CC} = 3.3 \text{ V}$ , $V_I = 0 \text{ V}$ or $V_{CC}$	25	pF

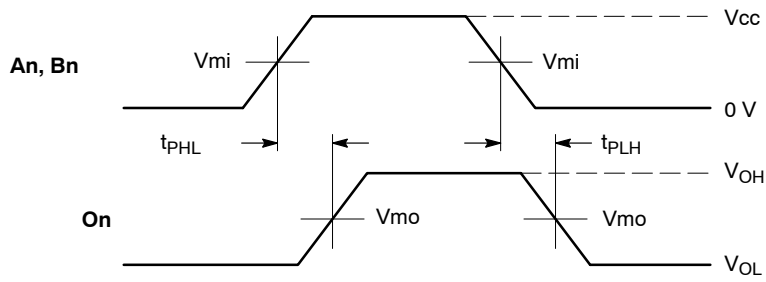
## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC74LCX02DG	SOIC-14 (Pb-Free)	55 Units / Rail
MC74LCX02DR2G	SOIC-14 (Pb-Free)	2500 Tape & Reel
MC74LCX02DTG	TSSOP-14 (Pb-Free)	96 Units / Rail
MC74LCX02DTR2G	TSSOP-14 (Pb-Free)	2500 Tape & Reel
NLV74LCX02DTR2G*	TSSOP-14 (Pb-Free)	2500 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

# MC74LCX02

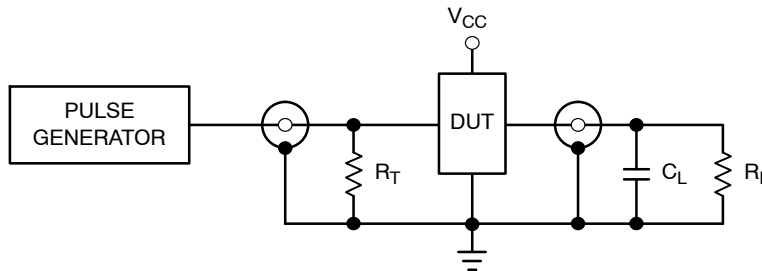


### WAVEFORM 1 - PROPAGATION DELAYS

$t_R = t_F = 2.5 \text{ ns}$ , 10% to 90%;  $f = 1 \text{ MHz}$ ;  $t_W = 500 \text{ ns}$

Symbol	Vcc		
	3.3 V ± 0.3 V	2.7 V	2.5 V ± 0.2 V
Vmi	1.5 V	1.5 V	Vcc/2
Vmo	1.5 V	1.5 V	Vcc/2

Figure 3. AC Waveforms



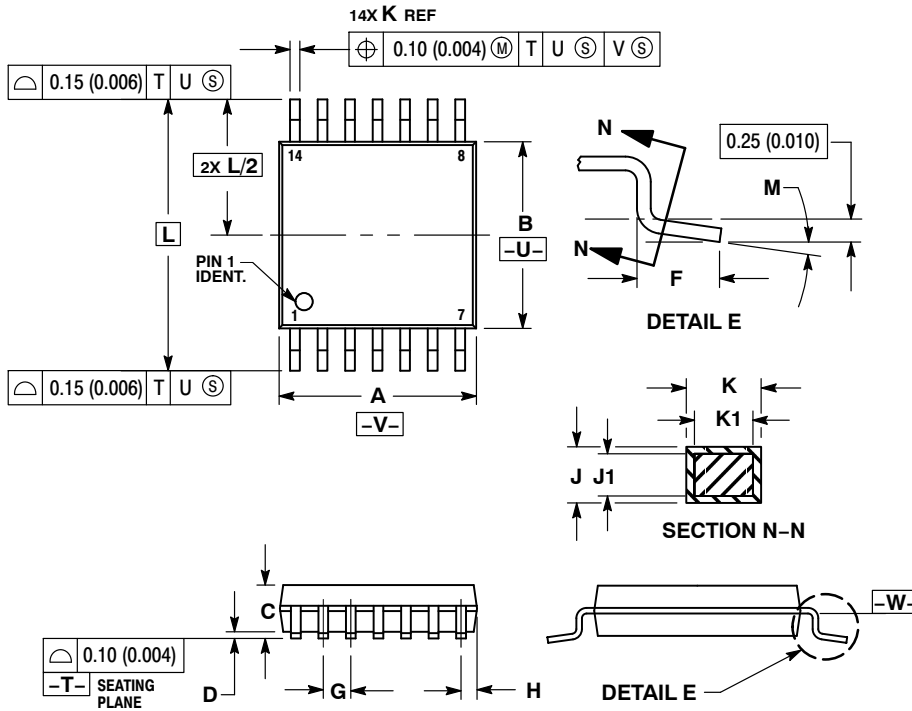
$C_L = 50 \text{ pF}$  at  $V_{CC} = 3.3 \pm 0.3 \text{ V}$  or equivalent (includes jig and probe capacitance)  
 $C_L = 30 \text{ pF}$  at  $V_{CC} = 2.5 \pm 0.2 \text{ V}$  or equivalent (includes jig and probe capacitance)  
 $R_L = R_1 = 500 \Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50 \Omega$ )

Figure 4. Test Circuit

# MC74LCX02

## PACKAGE DIMENSIONS

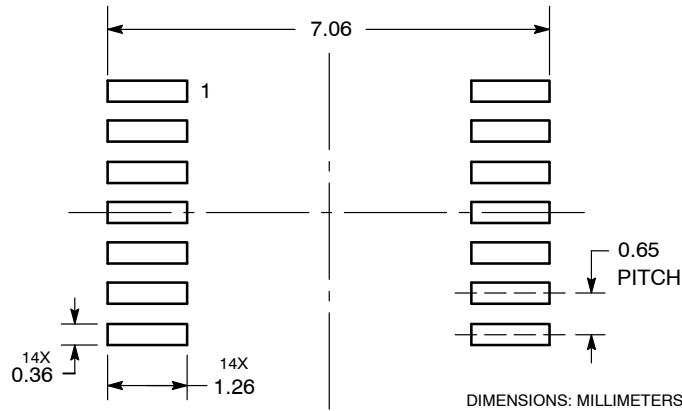
TSSOP-14  
DT SUFFIX  
CASE 948G  
ISSUE B



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

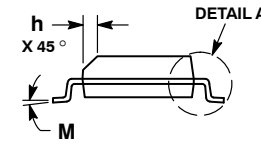
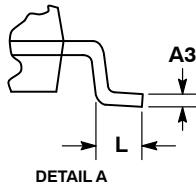
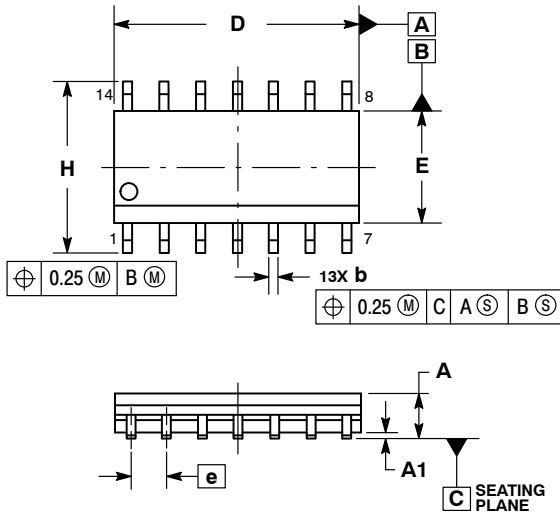
### SOLDERING FOOTPRINT



# MC74LCX02

## PACKAGE DIMENSIONS

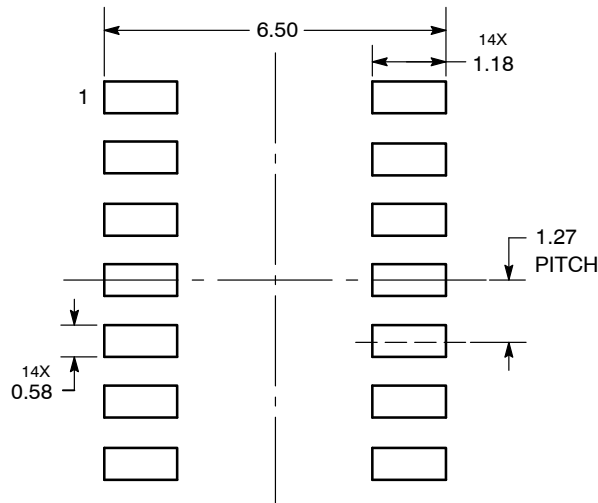
SOIC-14 NB  
CASE 751A-03  
ISSUE K



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
  5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

### SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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