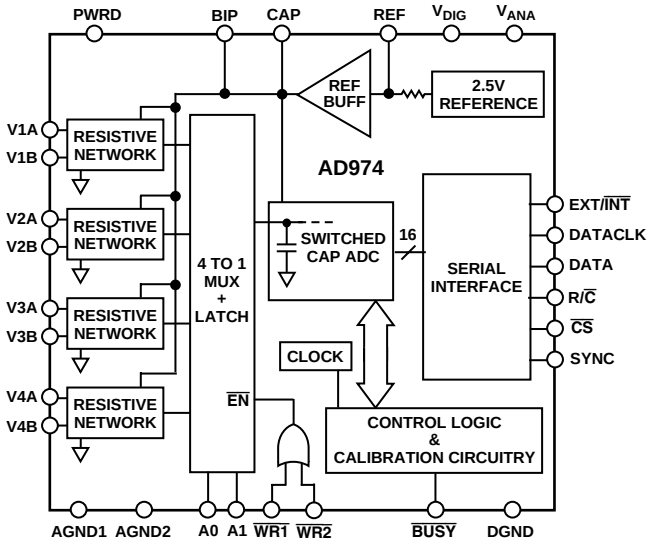
4-Channel, 16-Bit, 200 kSPS Data Acquisition System

AD974

FEATURES

Fast 16-Bit ADC with 200 kSPS Throughput
Four Single-Ended Analog Input Channels
Single +5 V Supply Operation
Input Ranges: 0 V to +4 V, 0 V to +5 V and ±10 V
120 mW Max Power Dissipation
Power-Down Mode 50 μW
Choice of External or Internal 2.5 V Reference
On-Chip Clock
Power-Down Mode

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD974 is a four-channel, data acquisition system with a serial interface. The part contains an input multiplexer, a high-speed 16-bit sampling ADC and a +2.5 V reference. All of this operates from a single +5 V power supply that also has a power-down mode. The part will accommodate 0 V to +4 V, 0 V to +5 V or ±10 V analog input ranges.

The interface is designed for an efficient transfer of data while requiring a low number of interconnects.

The AD974 is comprehensively tested for ac parameters such as SNR and THD, as well as the more traditional parameters of offset, gain and linearity.

The AD974 is fabricated on Analog Devices' BiCMOS process, which has high performance bipolar devices along with CMOS transistors.

The AD974 is available in 28-lead DIP, SOIC and SSOP packages.

PRODUCT HIGHLIGHTS

1. The AD974 is a complete data acquisition system combining a four-channel multiplexer, a 16-bit sampling ADC and a +2.5 V reference on a single chip.
2. The part operates from a single +5 V supply and also has a power-down feature.
3. Interfacing to the AD974 is simple with a low number of interconnect signals.
4. The AD974 is comprehensively specified for ac parameters such as SNR and THD, as well as dc parameters such as linearity and offset and gain errors.

REV. A

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AD974—SPECIFICATIONS (–40°C to +85°C, f_S = 200 kHz, V_{DIG} = V_{ANA} = +5 V, unless otherwise noted)

Parameter	Conditions	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Units
RESOLUTION		16			16			Bits
ANALOG INPUT								
Voltage Range		±10 V, 0 V to +4 V, 0 V to +5 V (See Table I)						
Impedance	Channel On or Off	(See Table I)						
Sampling Capacitance			40			40		pF
THROUGHPUT SPEED								
Complete Cycle (Acquire and Convert)				5			5	µs
Throughput Rate		200			200			kHz
DC ACCURACY								
Integral Linearity Error				±3			±2.0	LSB[1]
Differential Linearity Error		–2		+3	–1		+1.75	LSB
No Missing Codes		15			16			Bits
Transition Noise[2]			1.0			1.0		LSB
Full-Scale Error[3]	Internal Reference			±0.5			±0.25	%
Full-Scale Error Drift	Internal Reference		±7			±7		ppm/°C
Full-Scale Error	Ext. REF = +2.5 V			±0.5			±0.25	%
Full-Scale Error Drift	Ext. REF = +2.5 V		±2			±2		ppm/°C
Bipolar Zero Error	Bipolar Range			±10			±10	mV
Bipolar Zero Error Drift	Bipolar Range		±2			±2		ppm/°C
Unipolar Zero Error	Unipolar Ranges			±10			±10	mV
Unipolar Zero Error Drift	Unipolar Ranges		±2			±2		ppm/°C
Channel-to-Channel Matching				±0.1			±0.05	% FSR
Recovery to Rated Accuracy After Power-Down[4]	2.2 µF to CAP		1			1		ms
Power Supply Sensitivity V_{ANA} = V_{DIG} = V_D	V_D = 5 V ± 5%			±8			±8	LSB
AC ACCURACY								
Spurious Free Dynamic Range	f_{IN} = 20 kHz	90			96			dB[5]
Total Harmonic Distortion	f_{IN} = 20 kHz			–90			–96	dB
Signal-to-(Noise+Distortion)	f_{IN} = 20 kHz	83			85			dB
	–60 dB Input		27			28		dB
Signal-to-Noise	f_{IN} = 20 kHz	83			85			dB
Channel-to-Channel Isolation	f_{IN} = 20 kHz		–110	–100		–110	–100	dB
Full Power Bandwidth[6]			1			1		MHz
–3 dB Input Bandwidth			2.7			2.7		MHz
SAMPLING DYNAMICS								
Aperture Delay			40			40		ns
Transient Response	Full-Scale Step			1			1	µs
Overvoltage Recovery[7]			150			150		ns
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	2.48	2.5	2.52	V
Internal Reference Source Current			1			1		µA
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	2.3	2.5	2.7	V
External Reference Current Drain	Ext. REF = +2.5 V			100			100	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	–0.3		+0.8	V
V_{IH}		+2.0		V_{DIG} + 0.3	+2.0		V_{DIG} + 0.3	V
I_{IL}				±10			±10	µA
I_{IH}				±10			±10	µA

Parameter	Conditions	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Units
DIGITAL OUTPUTS								
Data Format				Serial 16 Bits				
Data Coding				Straight Binary				
V_{OL}	I_{SINK} = 1.6 mA			+0.4			+0.4	V
V_{OH}	I_{SOURCE} = 500 µA	+4			+4			V
Output Capacitance	High-Z State			15			15	pF
Leakage Current	High-Z State							
	V_{OUT} = 0 V to V_{DIG}			±5			±5	µA
POWER SUPPLIES								
Specified Performance								
V_{DIG}		+4.75	+5	+5.25	+4.75	+5	+5.25	V
V_{ANA}		+4.75	+5	+5.25	+4.75	+5	+5.25	V
I_{DIG}			4.5			4.5		mA
I_{ANA}			14			14		mA
Power Dissipation								
PWRD LOW				120			120	mW
PWRD HIGH			50			50		µW
TEMPERATURE RANGE								
Specified Performance	T_{MIN} to T_{MAX}	–40		+85	–40		+85	°C

NOTES
[1]LSB means Least Significant Bit. With a ±10 V input, one LSB is 305 µV.
[2]Typical rms noise at worst case transitions and temperatures.
[3]Full-Scale Error is expressed as the % difference between the actual full-scale code transition voltage and the ideal full-scale transition voltage, and includes the effect of offset error. For bipolar input, the Full-Scale Error is the worst case of either the –Full-Scale or +Full-Scale code transition voltage errors. For unipolar input ranges, Full-Scale Error is with respect to the +Full-Scale code transition voltage.
[4]External 2.5 V reference connected to REF.
[5]All specifications in dB are referred to a full-scale ±10 V input.
[6]Full-Power Bandwidth is defined as full-scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60 dB, or 10 bits of accuracy.
[7]Recovers to specified performance after a 2 × FS input overvoltage.

Specifications subject to change without notice.

TIMING SPECIFICATIONS (f_S = 200 kHz, $V_{DIG} = V_{ANA}$ = +5 V, –40°C to +85°C)

Parameter	Symbol	Min	Typ	Max	Units
Convert Pulsewidth	t_1	50			ns
R/$\overline{C}$, $\overline{CS}$ to $\overline{BUSY}$ Delay	t_2			100	ns
$\overline{BUSY}$ LOW Time	t_3			4.0	µs
$\overline{BUSY}$ Delay after End of Conversion	t_4		50		ns
Aperture Delay	t_5		40		ns
Conversion Time	t_6		3.8	4.0	µs
Acquisition Time	t_7	1.0			µs
Throughput Time	$t_6 + t_7$			5	µs
R/$\overline{C}$ Low to DATACLK Delay	t_8		220		ns
DATACLK Period	t_9		220		ns
DATA Valid Setup Time	t_{10}	50			ns
DATA Valid Hold Time	t_{11}	20			ns
EXT. DATACLK Period	t_{12}	66			ns
EXT. DATACLK HIGH	t_{13}	20			ns
EXT. DATACLK LOW	t_{14}	30			ns
R/$\overline{C}$, $\overline{CS}$ to EXT. DATACLK Setup Time	t_{15}	20		t_{12} + 5	ns
R/$\overline{C}$ to $\overline{CS}$ Setup Time	t_{16}	10			ns
EXT. DATACLK to SYNC Delay	t_{17}	15		66	ns
EXT. DATACLK to DATA Valid Delay	t_{18}	25		66	ns
$\overline{CS}$ to EXT. DATACLK Rising Edge Delay	t_{19}	10			ns
Previous DATA Valid after $\overline{CS}$, R/$\overline{C}$ Low	t_{20}	3.5			µs
$\overline{BUSY}$ to EXT. DATACLK Setup Time	t_{21}	5			ns
Final EXT. DATACLK to $\overline{BUSY}$ Rising Edge	t_{22}			1.7	µs
A0, A1 to $\overline{WR1}$, $\overline{WR2}$ Setup Time	t_{23}	10			ns
A0, A1 to $\overline{WR1}$, $\overline{WR2}$ Hold Time	t_{24}	10			ns
$\overline{WR1}$, $\overline{WR2}$ Pulsewidth	t_{25}	50			ns

Specifications subject to change without notic e.

ABSOLUTE MAXIMUM RATINGS[1]

Analog Inputs
- VxA, VxB . . . . . ±25 V
- CAP . . . . . $+V_{ANA}$ + 0.3 V to AGND2 – 0.3 V
- REF . . . . . Indefinite Short to AGND2, Momentary Short to V_{ANA}

Ground Voltage Differences
- DGND, AGND1, AGND2 . . . . . ±0.3 V

Supply Voltages
- V_{ANA} . . . . . +7 V
- V_{DIG} to V_{ANA} . . . . . ±7 V
- V_{DIG} . . . . . +7 V

Digital Inputs . . . . . –0.3 V to V_{DIG} + 0.3 V

Internal Power Dissipation[2]
- PDIP (N), SOIC (R), SSOP (RS) . . . . . 700 mW

Junction Temperature . . . . . +150°C

Storage Temperature Range N, R . . . . . –65°C to +150°C

Lead Temperature Range
- (Soldering 10 sec) . . . . . +300°C

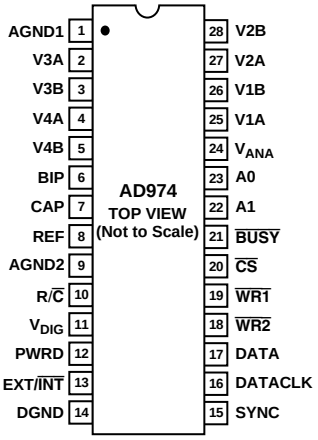
NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air:
28-Lead PDIP: θ_{JA} = 100°C/W, θ_{JC} = 31°C/W
28-Lead SOIC: θ_{JA} = 75°C/W, θ_{JC} = 24°C/W
28-Lead SSOP: θ_{JA} = 109°C/W, θ_{JC} = 39°C/W

PIN CONFIGURATION

SOIC, DIP AND SSOP



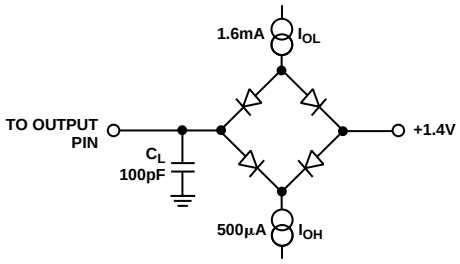


Figure 1. Load Circuit for Digital Interface Timing

ORDERING GUIDE

Model	Temperature Range	Max INL	Min S/(N+D)	Package Description	Package Options
AD974AN	–40°C to +85°C	±3.0 LSB	83 dB	28-Lead Plastic DIP	N-28B
AD974BN	–40°C to +85°C	±2.0 LSB	85 dB	28-Lead Plastic DIP	N-28B
AD974AR	–40°C to +85°C	±3.0 LSB	83 dB	28-Lead SOIC	R-28
AD974BR	–40°C to +85°C	±2.0 LSB	85 dB	28-Lead SOIC	R-28
AD974ARS	–40°C to +85°C	±3.0 LSB	83 dB	28-Lead SSOP	RS-28
AD974BRS	–40°C to +85°C	±2.0 LSB	85 dB	28-Lead SSOP	RS-28

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD974 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	AGND1	Analog Ground. Used as the ground reference point for the REF pin.
2–5, 25–28	VxA, VxB	Analog Input. Refer to Table I for input range configuration.
6	BIP	Bipolar Offset. Connect VxA inputs to provide Bipolar input range.
7	CAP	Reference Buffer Output. Connect a 2.2 μF tantalum capacitor between CAP and Analog Ground.
8	REF	Reference Input/Output. The internal +2.5 V reference is available at this pin. Alternatively an external reference can be used to override the internal reference. In either case, connect a 2.2 μF tantalum capacitor between REF and Analog Ground.
9	AGND2	Analog Ground.
10	R/$\overline{C}$	Read/$\overline{\text{Convert}}$ Input. Used to control the conversion and read modes. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ holds the analog input signal internally and starts a conversion; a rising edge enables the transmission of the conversion result.
11	V_{DIG}	Digital Power Supply. Nominally +5 V.
12	PWRD	Power-Down Input. When set to a logic HIGH, power consumption is reduced and conversions are inhibited. The conversion result from the previous conversion is stored in the onboard shift register.
13	EXT/$\overline{INT}$	Digital select input for choosing the internal or an external data clock. With EXT/$\overline{INT}$ tied LOW, after initiating a conversion, 16 DATACLK pulses transmit the previous conversion result as shown in Figure 3. With EXT/$\overline{INT}$ set to a Logic HIGH, output data is synchronized to an external clock signal connected to the DATACLK input. Data is output as indicated in Figure 4 through Figure 9.
14	DGND	Digital Ground.
15	SYNC	Digital output frame synchronization for use with an external data clock (EXT/$\overline{INT}$ = Logic HIGH). When a read sequence is initiated, a pulse one DATACLK period wide is output synchronous to the external data clock.
16	DATACLK	Serial data clock input or output, dependent upon the logic state of the EXT/$\overline{INT}$ pin. When using the internal data clock (EXT/$\overline{INT}$ = Logic LOW), a conversion start sequence will initiate transmission of 16 DATACLK periods. Output data is synchronous to this clock and is valid on both its rising and falling edges (Figure 3). When using an external data clock (EXT/$\overline{INT}$ = Logic HIGH), the $\overline{CS}$ and R/$\overline{C}$ signals control how conversion data is accessed.
17	DATA	The serial data output is synchronized to DATACLK. Conversion results are stored in an on-chip register. The AD974 provides the conversion result, MSB first, from its internal shift register. When using the internal data clock (EXT/$\overline{INT}$ = Logic LOW), DATA is valid on both the rising and falling edges of DATACLK. Using an external data clock (EXT/$\overline{INT}$ = Logic HIGH) allows previous conversion data to be accessed during a conversion (Figures 5, 7 and 9) or the conversion result can be accessed after the completion of a conversion (Figures 4, 6 and 8).
18, 19	$\overline{WR1}$, $\overline{WR2}$	Multiplexer Write Inputs. These inputs are internally ORed to generate the mux latch inputs. The latch is transparent when $\overline{WR1}$ and $\overline{WR2}$ are tied low.
20	$\overline{CS}$	Chip Select Input. With R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH, a falling edge on $\overline{CS}$ will enable the serial data output sequence.
21	$\overline{BUSY}$	Busy Output. Goes LOW when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the on-chip shift register.
22, 23	A1, A0	Address multiplexer inputs latched with the $\overline{WR1}$, $\overline{WR2}$ inputs.
24	V_{ANA}	Analog Power Supply. Nominally +5 V.

A1	A0	Data Available from Channel
0	0	AIN 1
0	1	AIN 2
1	0	AIN 3
1	1	AIN 4

DEFINITION OF SPECIFICATIONS

INTEGRAL NONLINEARITY ERROR (INL)

Linearity error refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

DIFFERENTIAL NONLINEARITY ERROR (DNL)

In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

FULL-SCALE ERROR

The last + transition (from 011 . . . 10 to 011 . . . 11) should occur for an analog voltage 1 1/2 LSB below the nominal full scale (9.9995422 V for a ±10 V range). The full-scale error is the deviation of the actual level of the last transition from the ideal level.

BIPOLAR ZERO ERROR

Bipolar zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

UNIPOLAR ZERO ERROR

In unipolar mode, the first transition should occur at a level 1/2 LSB above analog ground. Unipolar zero error is the deviation of the actual transition from that point.

SPURIOUS FREE DYNAMIC RANGE

The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

SIGNAL TO (NOISE AND DISTORTION) (S/[N+D]) RATIO

S/(N+D) is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in decibels.

FULL POWER BANDWIDTH

The full power bandwidth is defined as the full-scale input frequency at which the S/(N+D) degrades to 60 dB, 10 bits of accuracy.

APERTURE DELAY

Aperture delay is a measure of the acquisition performance, and is measured from the falling edge of the R/$\overline{C}$ input to when the input signal is held for a conversion.

TRANSIENT RESPONSE

The time required for the AD974 to achieve its rated accuracy after a full-scale step function is applied to its input.

OVERVOLTAGE RECOVERY

The time required for the ADC to recover to full accuracy after an analog input signal 150% of full-scale is reduced to 50% of the full-scale value.

CONVERSION CONTROL

The AD974 is controlled by two signals: R/$\overline{C}$ and $\overline{CS}$. When R/$\overline{C}$ is brought low, with $\overline{CS}$ low, for a minimum of 50 ns, the input signal will be held on the internal capacitor array and a conversion "n" will begin. Once the conversion process does begin, the $\overline{BUSY}$ signal will go low until the conversion is complete. Internally, the signals R/$\overline{C}$ and $\overline{CS}$ are ORed together and there is no requirement on which signal is taken low first when initiating a conversion. The only requirement is that there be at least 10 ns of delay between the two signals being taken low. After the conversion is complete, the $\overline{BUSY}$ signal will return high and the AD974 will again resume tracking the input signal. Under certain conditions the $\overline{CS}$ pin can be tied Low and R/$\overline{C}$ will be used to determine whether you are initiating a conversion or reading data. On the first conversion, after the AD974 is powered up, the DATA output will be indeterminate.

Conversion results can be clocked serially, using either an internal clock generated by the AD974 or an external clock. The AD974 is configured for the internal data clock mode by pulling the EXT/$\overline{INT}$ pin low. It is configured for the external clock mode by pulling the EXT/$\overline{INT}$ pin high.

INTERNAL DATA CLOCK MODE

The AD974 is configured to generate and provide the data clock when the EXT/$\overline{INT}$ pin is held low. Typically $\overline{CS}$ will be tied low and R/$\overline{C}$ will be used to initiate a conversion "n." During the conversion the AD974 will output 16 bits of data, MSB first, from conversion "n-1" on the DATA pin. This data will be synchronized with 16 clock pulses provided on the DATACLK pin. The output data will be valid on both the rising and falling edge of the data clock as shown in Figure 3. After the LSB has been presented, the DATACLK pin will stay low until another conversion is initiated.

In this mode, the digital input/output pins' transitions are suitably positioned to minimize degradation on the conversion result, mainly during the second half of the conversion process.

EXTERNAL DATA CLOCK MODE

The AD974 is configured to accept an externally supplied data clock when the EXT/$\overline{INT}$ pin is held high. This mode of operation provides several methods by which conversion results can be read. The output data from conversion "n-1" can be read during conversion "n," or the output data from conversion "n"

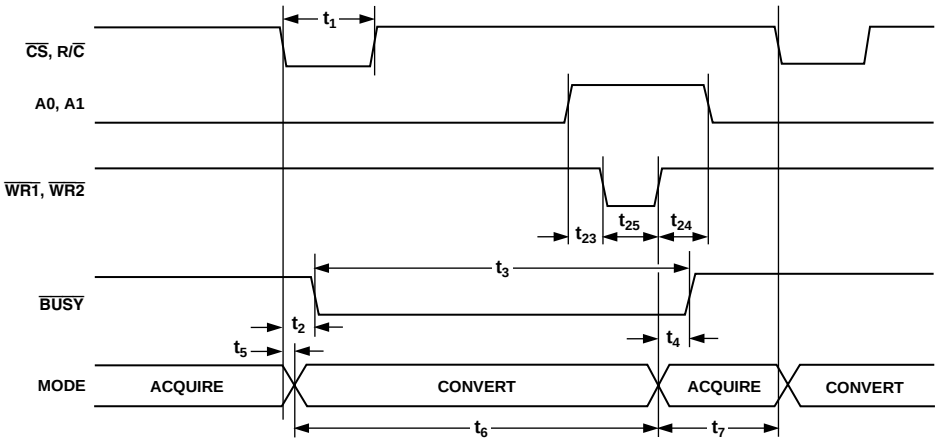


Figure 2. Basic Conversion Timing

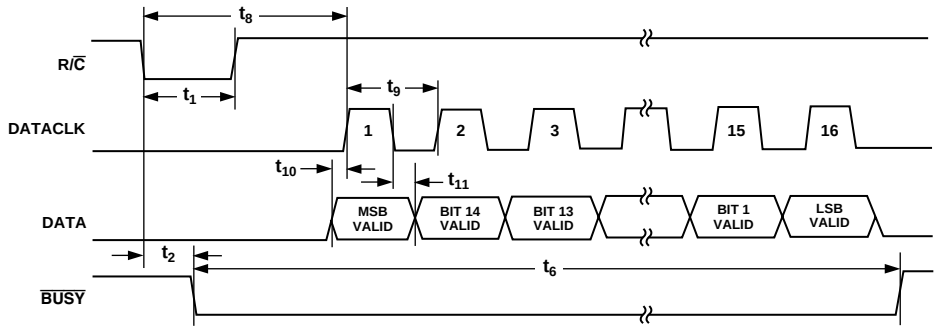


Figure 3. Serial Data Timing for Reading Previous Conversion Results with Internal Clock ($\overline{CS}$ and EXT/$\overline{INT}$ Set to Logic Low)

can be read after the conversion is complete. The external clock can be either a continuous or discontinuous clock. A discontinuous clock can be either normally low or normally high when inactive. In the case of the discontinuous clock, the AD974 can be configured to either generate or not generate a SYNC output (with a continuous clock a SYNC output will always be produced).

Each of the methods will be described in the following sections and are illustrated in Figures 4 through 9. It should be noted that all timing diagrams assume that the receiving device is latching data on the rising edge of the external clock. If the falling edge of DATACLK is used then, in the case of a discontinuous clock, one less clock pulse is required than shown in Figures 4 through 7 to latch in a 16-bit word. Note that data is valid on the falling edge of a clock pulse (for t_{13} greater than t_{18}) and the rising edge of the next clock pulse.

The AD974 provides error correction circuitry that can correct for an improper bit decision made during the first half of the conversion cycle. Normally the occurrence of an incorrect bit decision during a conversion cycle is irreversible. This error occurs as a result of noise during the time of the decision or due to insufficient settling time. As the AD974 is performing a conversion it is important that transitions not occur on digital input/output pins or degradation of the conversion result could occur. This is particularly important during the second half of the conversion process. For this reason it is recommended that when an external clock is being provided it be a discontinuous clock that is not toggling during the time that $\overline{BUSY}$ is low or, more importantly, that it does not transition during the latter half of $\overline{BUSY}$ low.

EXTERNAL DISCONTINUOUS CLOCK DATA READ AFTER CONVERSION WITH NO SYNC OUTPUT GENERATED

Figure 4 illustrates the method by which data from conversion "n" can be read after the conversion is complete using a discontinuous external clock without the generation of a SYNC output. After a conversion is complete, indicated by $\overline{BUSY}$ returning high, the result of that conversion can be read while $\overline{CS}$ is Low and R/$\overline{C}$ is high. In this mode $\overline{CS}$ can be tied low. The MSB will be valid on the first falling edge and the second rising edge of DATACLK. The LSB will be valid on the 16th falling edge and the 17th rising edge of DATACLK. A minimum of 16 clock pulses are required for DATACLK if the receiving device will be latching data on the falling edge of DATACLK. A minimum of 17 clock pulses are required for DATACLK if the receiving device will be latching data on the rising edge of DATACLK.

The advantage of this method of reading data is that data is not being clocked out during a conversion and therefore conversion performance is not degraded.

When reading data after the conversion is complete, with the highest frequency permitted for DATACLK (15.15 MHz), the maximum possible throughput is approximately 195 kHz, and not the rated 200 kHz.

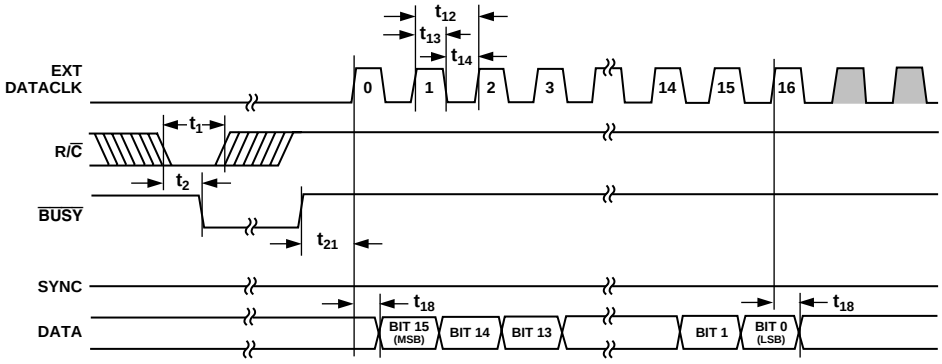


Figure 4. Conversion and Read Timing Using an External Discontinuous Data Clock (EXT/$\overline{INT}$ Set to Logic High, $\overline{CS}$ Set to Logic Low)

EXTERNAL DISCONTINUOUS CLOCK DATA READ DURING CONVERSION WITH NO SYNC OUTPUT GENERATED

Figure 5 illustrates the method by which data from conversion "n-1" can be read during conversion "n" while using a discontinuous external clock, without the generation of a SYNC output. After a conversion is initiated, indicated by $\overline{BUSY}$ going low, the result of the previous conversion can be read while $\overline{CS}$ is low and R/$\overline{C}$ is high. In this mode $\overline{CS}$ can be tied low. The MSB will be valid on the 1st falling edge and the 2nd rising edge of DATACLK. The LSB will be valid on the 16th falling edge and the 17th rising edge of DATACLK. A minimum of 16 clock pulses are required for DATACLK if the receiving device will be latching data on the falling edge of DATACLK. A minimum of 17 clock pulses are required for DATACLK if the receiving device will be latching data on the rising edge of DATACLK.

In this mode the data should be clocked out during the first half of $\overline{BUSY}$ so not to degrade conversion performance. This requires use of a 10 MHz DATACLK or greater, with data being read out as soon as the conversion process begins.

EXTERNAL DISCONTINUOUS CLOCK DATA READ AFTER CONVERSION WITH SYNC OUTPUT GENERATED

Figure 6 illustrates the method by which data from conversion "n" can be read after the conversion is complete using a discontinuous external clock, with the generation of a SYNC output. What permits the generation of a SYNC output is a transition of DATACLK while either $\overline{CS}$ is high or while both $\overline{CS}$ and R/$\overline{C}$ are low. After a conversion is complete, indicated by $\overline{BUSY}$ returning high, the result of that conversion can be read while $\overline{CS}$ is Low and R/$\overline{C}$ is high. In this mode $\overline{CS}$ can be tied low. In Figure 6 clock pulse #0 is used to enable the generation of a SYNC pulse. The SYNC pulse is actually clocked out approximately 40 ns after the rising edge of clock pulse #1. The SYNC pulse will be valid on the falling edge of clock pulse #1 and the rising edge of clock pulse #2. The MSB will be valid on the falling edge of clock pulse #2 and the rising edge of clock pulse #3. The LSB will be valid on the falling edge of clock pulse #17 and the rising edge of clock pulse #18. The advantage of this method of reading data is that it is not being clocked out during a conversion and therefore conversion performance is not degraded.

When reading data after the conversion is complete, with the highest frequency permitted for DATACLK (15.15 MHz), the maximum possible throughput is approximately 195 kHz and not the rated 200 kHz.

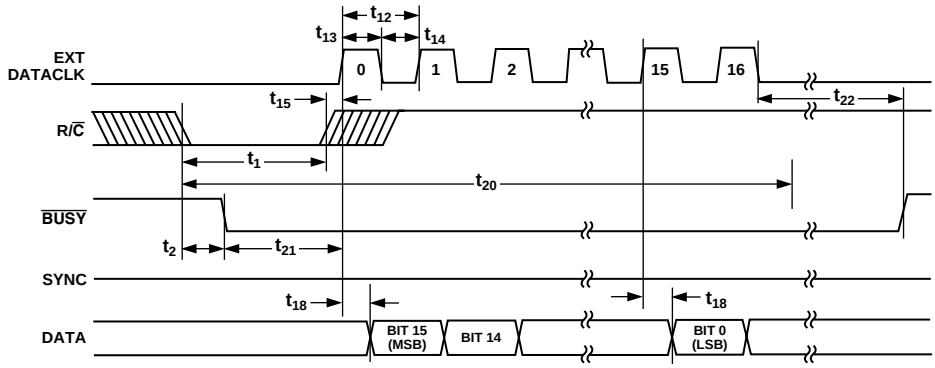


Figure 5. Conversion and Read Timing for Reading Previous Conversion Results During a Conversion Using External Discontinuous Data Clock (EXT/$\overline{INT}$ Set to Logic High, $\overline{CS}$ Set to Logic Low)

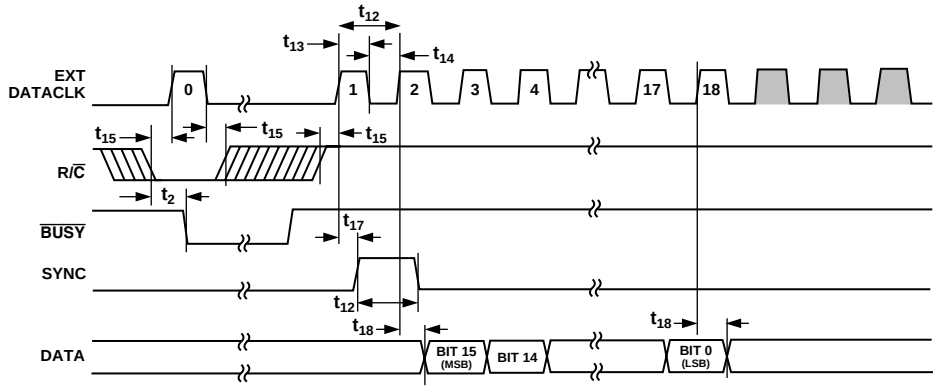


Figure 6. Conversion and Read Timing Using An External Discontinuous Data Clock (EXT/$\overline{INT}$ Set to Logic High, $\overline{CS}$ Set to Logic Low)

EXTERNAL DISCONTINUOUS CLOCK DATA READ DURING CONVERSION WITH SYNC OUTPUT GENERATED

Figure 7 illustrates the method by which data from conversion "n-1" can be read during conversion "n" while using a discontinuous external clock, with the generation of a SYNC output. What permits the generation of a SYNC output is a transition of DATACLK while either $\overline{CS}$ is High or while both $\overline{CS}$ and R/$\overline{C}$ are low. In Figure 7 a conversion is initiated by taking R/$\overline{C}$ low with $\overline{CS}$ tied low. While this condition exists a transition of DATACLK, clock pulse #0, will enable the generation of a SYNC pulse. Less then 83 ns after R/$\overline{C}$ is taken low the $\overline{BUSY}$ output will go low to indicate that the conversion process has begun. Figure 7 shows R/$\overline{C}$ then going high and after a delay of greater than 15 ns (t_{15}) clock pulse #1 can be taken high to request the SYNC output. The SYNC output will appear approximately 40 ns after this rising edge and will be valid on the falling edge of clock pulse #1 and the rising edge of clock pulse #2. The MSB will be valid approximately 40 ns after the rising edge of clock pulse #2 and can be latched off either the falling edge of clock pulse #2 or the rising edge of clock pulse #3. The LSB will be valid on the falling edge of clock pulse #17 and the rising edge of clock pulse #18.

Data should be clocked out during the first half of $\overline{BUSY}$ to avoid degrading conversion performance. This requires use of a 10 MHz DATACLK or greater, with data being read out as soon as the conversion process begins.

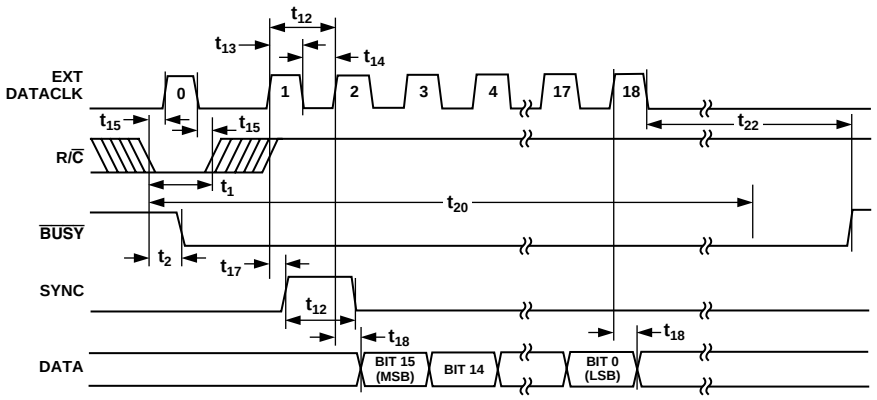


Figure 7. Conversion and Read Timing for Reading Previous Conversion Results During a Conversion Using External Discontinuous Data Clock (EXT/$\overline{INT}$ Set to Logic High, $\overline{CS}$ Set to Logic Low)

EXTERNAL CONTINUOUS CLOCK DATA READ AFTER CONVERSION WITH SYNC OUTPUT GENERATED

Figure 8 illustrates the method by which data from conversion "n" can be read after the conversion is complete using a continuous external clock, with the generation of a SYNC output. What permits the generation of a SYNC output is a transition of DATACLK either while $\overline{CS}$ is high or while both $\overline{CS}$ and R/$\overline{C}$ are low.

With a continuous clock the $\overline{CS}$ pin cannot be tied low as it could be with a discontinuous clock. Use of a continuous clock, while a conversion is occurring, can increase the DNL and Transition Noise of the AD974.

After a conversion is complete, indicated by $\overline{BUSY}$ returning high, the result of that conversion can be read while $\overline{CS}$ is low and R/$\overline{C}$ is high. In Figure 8 clock pulse #0 is used to enable the generation of a SYNC pulse. The SYNC pulse is actually clocked out approximately 40 ns after the rising edge of clock pulse #1. The SYNC pulse will be valid on the falling edge of clock pulse #1 and the rising edge of clock pulse #2. The MSB will be valid on the falling edge of clock pulse #2 and the rising edge of clock pulse #3. The LSB will be valid on the falling edge of clock pulse #17 and the rising edge of clock pulse #18.

When reading data after the conversion is complete, with the highest frequency permitted for DATACLK (15.15 MHz) the maximum possible throughput is approximately 195 kHz and not the rated 200 kHz.

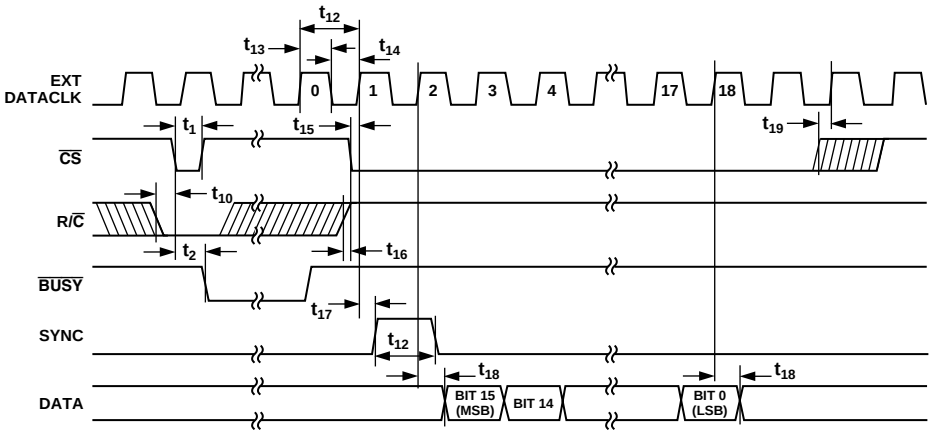


Figure 8. Conversion and Read Timing Using an External Continuous Data Clock (EXT/$\overline{INT}$ Set to Logic High)

EXTERNAL CONTINUOUS CLOCK DATA READ DURING CONVERSION WITH SYNC OUTPUT GENERATED

Figure 9 illustrates the method by which data from conversion "n-1" can be read during conversion "n" while using a continuous external clock with the generation of a SYNC output. What permits the generation of a SYNC output is a transition of DATACLK either while $\overline{CS}$ is high or while both $\overline{CS}$ and R/$\overline{C}$ are low.

With a continuous clock the $\overline{CS}$ pin cannot be tied low as it could be with a discontinuous clock. Use of a continuous clock while a conversion is occurring can increase the DNL and Transition Noise.

In Figure 9 a conversion is initiated by taking R/$\overline{C}$ low with $\overline{CS}$ held low. While this condition exists a transition of DATACLK, clock pulse #0, will enable the generation of a SYNC pulse. Less then 83 ns after R/$\overline{C}$ is taken low the $\overline{BUSY}$ output will go low to indicate that the conversion process has began. Figure 9 shows R/$\overline{C}$ then going high and after a delay of greater than 15 ns (t_{15}), clock pulse #1 can be taken high to request the SYNC output. The SYNC output will appear approximately 50 ns after this rising edge and will be valid on the falling edge of clock pulse #1 and the rising edge of clock pulse #2. The MSB will be valid approximately 40 ns after the rising edge of clock pulse #2 and can be latched off either the falling edge of clock pulse #2 or the rising edge of clock pulse #3. The LSB will be valid on the falling edge of clock pulse #17 and the rising edge of clock pulse #18.

Data should be clocked out during the 1st half of $\overline{BUSY}$ to not degrade conversion performance. This requires use of a 10 MHz DATACLK or greater, with data being read out as soon as the conversion process begins.

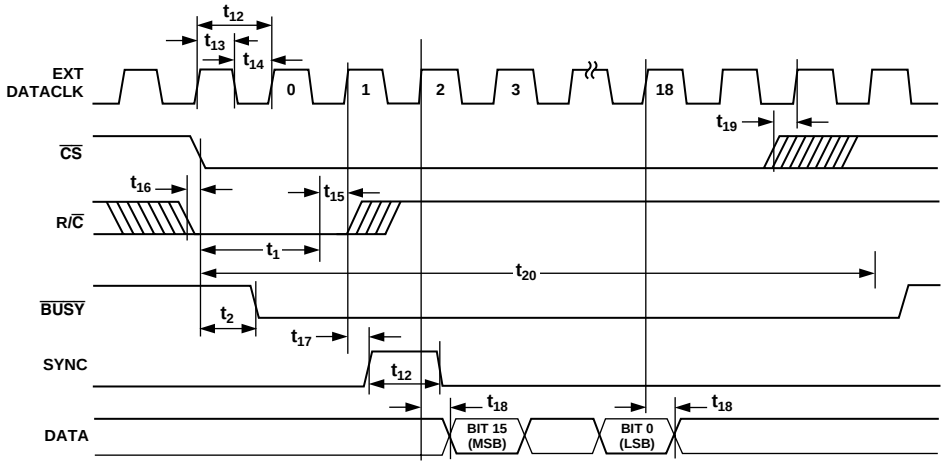


Figure 9. Conversion and Read Timing for Reading Previous Conversion Results During a Conversion Using An External Continuous Data Clock (EXT/$\overline{INT}$ Set to Logic High)

Table I. Analog Input Configuration

Input Voltage Range	Connect VxA to	Connect VxB to	Input Impedance
±10 V	BIP	V_{IN}	13.7 kΩ
0 V to +5 V	V_{IN}	GND	6.0 kΩ
0 V to +4 V	V_{IN}	V_{IN}	6.4 kΩ

Table II. Output Codes and Ideal Input Voltage

Description	Analog Input			Digital Input Straight Binary
Full-Scale Range	±10 V	0 V to +5 V	0 V to +4 V	
Least Significant Bit	305 μV	76 μV	61 μV	
+Full Scale (FS – 1 LSB)	+9.999695 V	+4.999847 V	+3.999939 V	1111 1111 1111 1111
Midscale	0 V	+2.5 V	+2 V	1000 0000 0000 0000
One LSB Below Midscale	–305 μV	+2.499924 V	+1.999939 V	0111 1111 1111 1111
–Full Scale	–10 V	0 V	0 V	0000 0000 0000 0000

ANALOG INPUTS

The AD974 is specified to operate with three full-scale analog input ranges. Connections required for each of the eight analog inputs, VxA and VxB and the resulting full-scale ranges, are shown in Table I. The nominal input impedance for each analog input range is also shown. Table II shows the output codes for the ideal input voltages of each of the analog input ranges.

The analog input section has a ±25 V overvoltage protection on VxA and VxB. Since the AD974 has two analog grounds it is important to ensure that the analog input is referenced to the AGND1 pin, the low current ground. This will minimize any problems associated with a resistive ground drop. It is also important to ensure that the analog inputs are driven by a low impedance source. With its primarily resistive analog input circuitry, the ADC can be driven by a wide selection of general purpose amplifiers.

To achieve the low distortion capability of the AD974 care should be taken in the selection of the drive circuitry op amp.

Figure 10 shows the simplified analog input section for the AD974. Since the AD974 can operate with an internal or external reference, and three different analog input ranges, the full-scale analog input range is best represented with a voltage that spans 0 V to V_{REF} across the 40 pF sampling capacitor. The on-chip resistors are laser trimmed to ratio match for adjustment of offset and full-scale error using fixed external resistors.

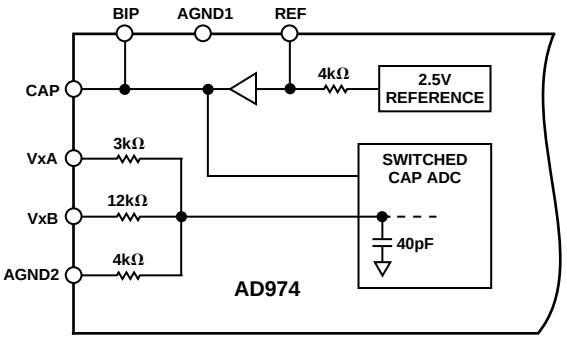


Figure 10. Simplified Analog Input

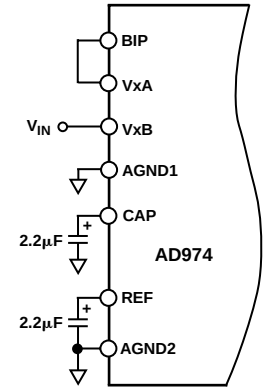
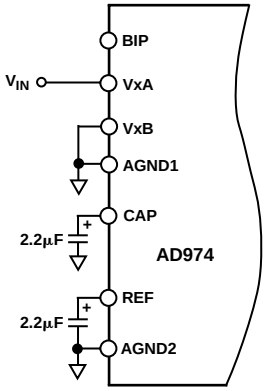
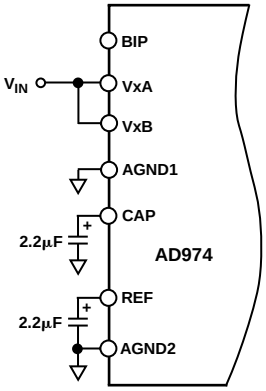
INPUT RANGE	BASIC CONNECTIONS FOR AD974
±10V	
0V TO +5V	
0V TO +4V	

Figure 11. Analog Input Configurations

OFFSET AND GAIN ADJUSTMENT

The AD974 is factory trimmed to minimize gain, offset and linearity errors. There are no internal provisions to allow for any further adjustment of offset error through external circuitry. The reference of the AD974 can be adjusted as shown in Figure 12. This will allow the full-scale error of any one channel to be adjusted to zero or will allow the average full-scale error of the four channels to be minimized.

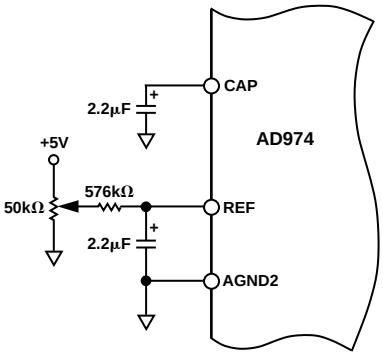


Figure 12. AD974 Full-Scale Trim

VOLTAGE REFERENCE

The AD974 has an on-chip temperature compensated bandgap voltage reference that is factory trimmed to +2.5 V ± 20 mV. The accuracy of the AD974 over the specified temperature range is dominated by the drift performance of the voltage reference. The on-chip voltage reference is laser-trimmed to provide a typical drift of 7 ppm/°C. This typical drift characteristic is shown in Figure 13, which is a plot of the change in reference voltage (in mV) versus the change in temperature—notice the plot is normalized for zero error at +25°C. If improved drift performance is required, an external reference such as the AD780 should be used to provide a drift as low as 3 ppm/°C. In order to simplify the drive requirements of the voltage reference (internal or external), an on-chip reference buffer is provided.

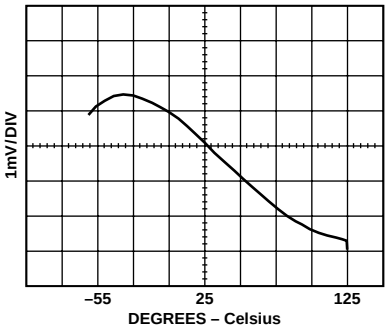


Figure 13. Reference Drift

The output of this buffer is provided at the CAP pin and is available to the user; however, when externally loading the reference buffer, it is important to make sure that proper precautions are taken to minimize any degradation in the ADC's performance. Figure 14 shows the load regulation of the reference buffer. Notice that this figure is also normalized so that there is zero error with no dc load. In the linear region, the output impedance at this point is typically 1 Ω. Because of this output impedance, it is important to minimize any ac- or input-dependent loads that will lead to increased distortion. Any dc load will simply act as a gain error. Although the typical characteristic of Figure 14 shows that the AD974 is capable of driving loads greater than 15 mA, it is recommended that the steady state current not exceed 2 mA.

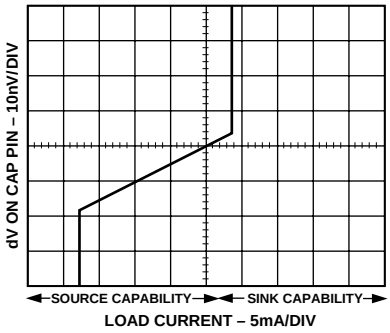


Figure 14. CAP Pin Load Regulation

Using an External Reference

In addition to the on-chip reference, an external 2.5 V reference can be applied. When choosing an external reference for a 16-bit application, however, careful attention should be paid to noise and temperature drift. These critical specifications can have a significant effect on the ADC performance.

Figure 15 shows the AD974 used in bipolar mode with the AD780 voltage reference applied to the REF pin. The AD780 is a bandgap reference that exhibits ultralow drift, low initial error and low output noise. For low power applications, the AD780 provides a low quiescent current, high accuracy and low temperature drift solution.

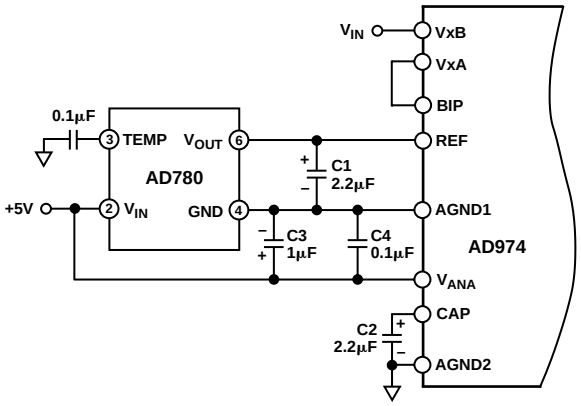


Figure 15. External Reference to AD974 Configured for ±10 V Input Range

AC PERFORMANCE

The AD974 is fully specified and tested for dynamic performance specifications. The ac parameters are required for signal processing applications such as speech recognition and spectrum analysis. These applications require information on the ADC's effect on the spectral content of the input signal. Hence, the parameters for which the AD974 is specified include S/(N+D), THD and Spurious Free Dynamic Range. These terms are discussed in greater detail in the following sections.

As a general rule, it is recommended that the results from several conversions be averaged to reduce the effects of noise and thus improve parameters such as S/(N+D) and THD. AC performance can be optimized by operating the ADC at its maximum sampling rate of 200 kHz and digitally filtering the resulting bit stream to the desired signal bandwidth. By distributing noise over a wider frequency range the noise density in the frequency band of interest can be reduced. For example, if the required input bandwidth is 50 kHz, the AD974 could be oversampled by a factor of 4. This would yield a 6 dB improvement in the effective SNR performance.

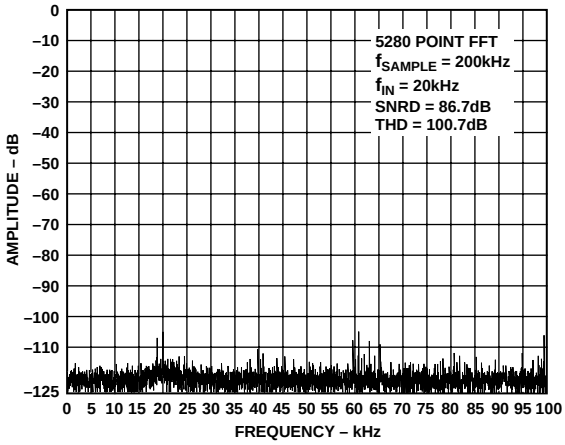


Figure 16. FFT Plot

DC PERFORMANCE

The factory calibration scheme used for the AD974 compensates for bit weight errors that may exist in the capacitor array. The mismatch in capacitor values is adjusted (using the calibration coefficients) during a conversion, resulting in excellent dc linearity performance. Figures 17 and 18, respectively, show typical INL and DNL plots for the AD974 at +25°C.

A histogram test is a statistical method for deriving an A/D converter's differential nonlinearity. A ramp input is sampled by the ADC and a large number of conversions are taken at each voltage level, averaged and then stored. The effect of averaging is to reduce the transition noise by 1/n. If 64 samples are averaged at each point, the effect of transition noise is reduced by a factor of 8; i.e., a transition noise of 0.8 LSBs rms is reduced to 0.1 LSBs rms. Theoretically the codes, during a test of DNL, would all be the same size and therefore have an equal number of occurrences. A code with an average number of occurrences would have a DNL of "0." A code that is different from the average would have a DNL that was either greater or less than zero LSB. A DNL of –1 LSB indicates that there is a missing code present at the 16-bit level and that the ADC exhibits 15-bit performance.

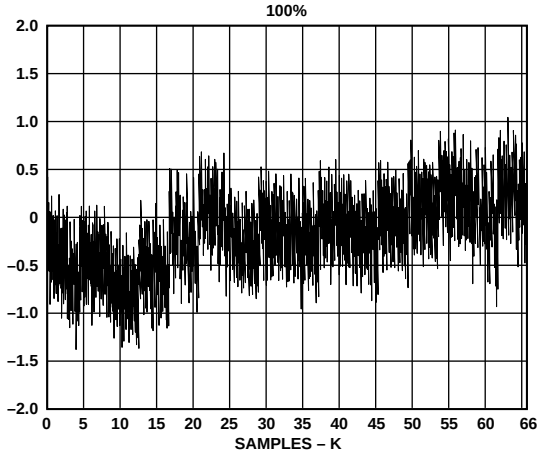


Figure 17. INL Plot

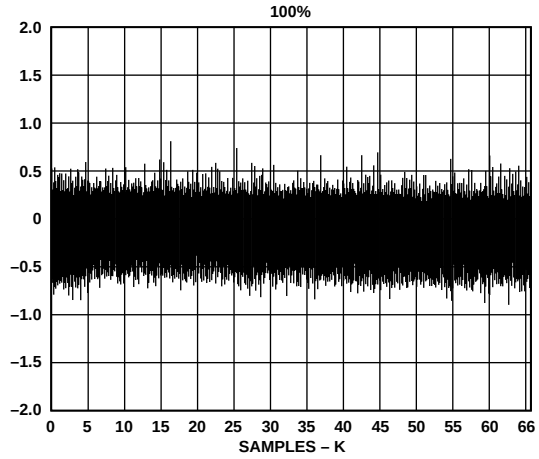


Figure 18. DNL Plot

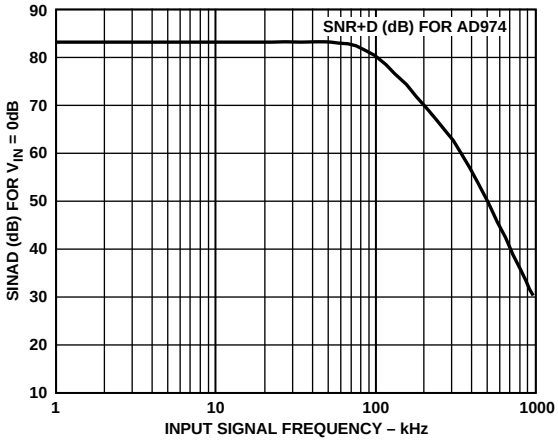


Figure 19. S/(N+D) vs. Input Frequency

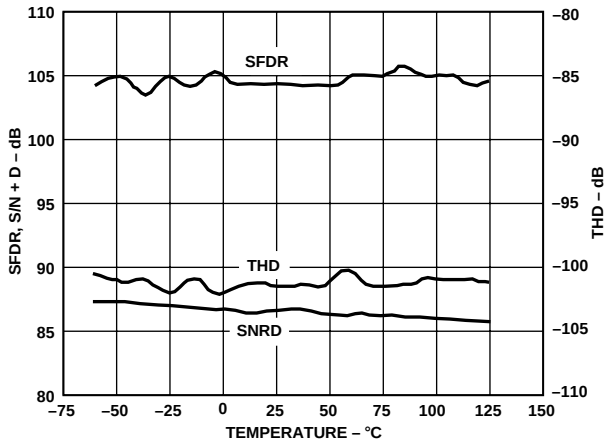


Figure 20. AC Parameters vs. Temperature

DC CODE UNCERTAINTY

Ideally, a fixed dc input should result in the same output code for repetitive conversions; however, as a consequence of unavoidable circuit noise within the wideband circuits of the ADC, a range of output codes may occur for a given input voltage. Thus, when a dc signal is applied to the AD974 input, and 10,000 conversions are recorded, the result will be a distribution of codes as shown in Figure 21. This histogram shows a bell shaped curve consistent with the Gaussian nature of thermal noise. The histogram is approximately seven codes wide. The standard deviation of this Gaussian distribution results in a code transition noise of 1 LSB rms.

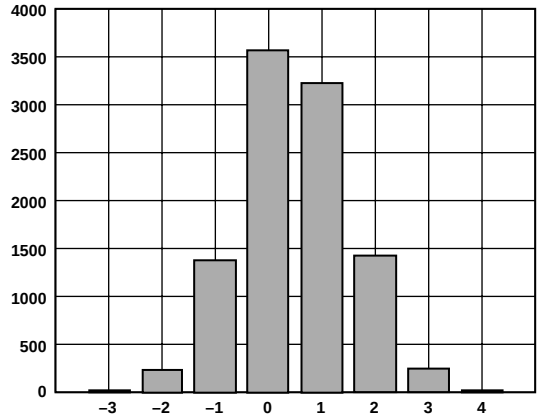


Figure 21. Histogram of 10,000 Conversions of a DC Input

POWER-DOWN FEATURE

The AD974 has analog and reference power-down capability through the PWRD pin. When the PWRD pin is taken high, the power consumption drops from a maximum value of 100 mW to a typical value of 50 µW. When in the power-down mode the previous conversion results are still available in the internal registers and can be read out providing it has not already been shifted out.

When used with an external reference, connected to the REF pin and a 2.2 µF capacitor, connected to the CAP pin, the power-up recovery time is typically 1 ms. This typical value of 1 ms for recovery time depends on how much charge has decayed from the external 2.2 µF capacitor on the CAP pin and assumes that it has decayed to zero. The 1 ms recovery time has been specified such that settling to 16 bits has been achieved.

When used with the internal reference, the dominant time constant for power-up recovery is determined by the external capacitor on the REF pin and the internal 4K impedance seen at that pin. An external 2.2 µF capacitor is recommended for the REF pin.

CROSSTALK

The crosstalk between adjacent channels, nonadjacent channels and worst-case adjacent channels is shown in Figures 22 to 24. The worst-case crosstalk occurs between channels 1 and 2.

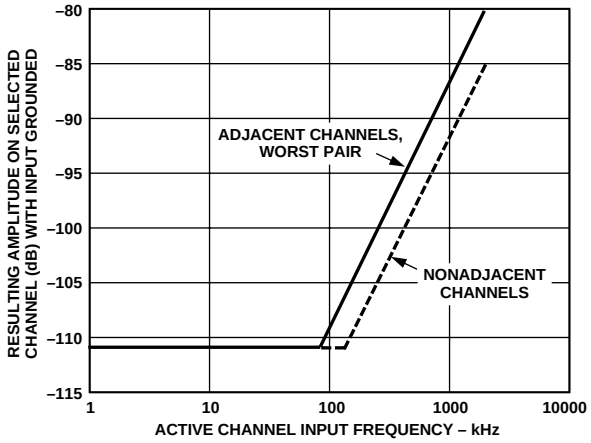


Figure 22. Crosstalk vs. Input Frequency (kHz)

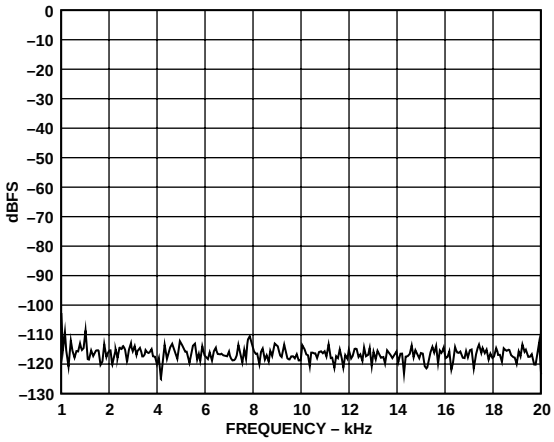


Figure 23. Adjacent Channel Crosstalk, Worst Pair (8192 Point FFT; AIN 2 = 1.02 kHz, –0.1 dB; AIN 1 = AGND)

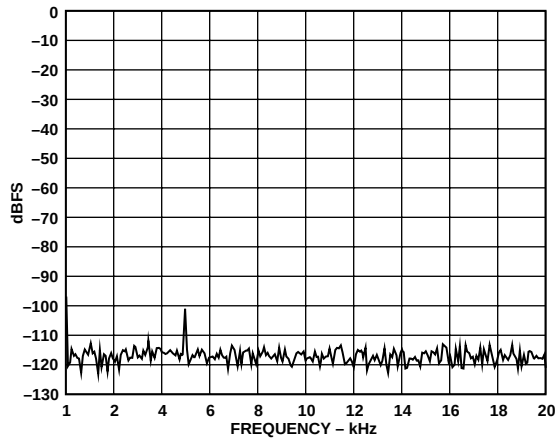


Figure 24. Adjacent Channel Crosstalk, Worst Pair (8192 Point FFT; AIN 2 = 220 kHz, –0.1 dB; AIN 1 = AGND)

MICROPROCESSOR INTERFACING

The AD974 is ideally suited for traditional dc measurement applications supporting a microprocessor, and ac signal processing applications interfacing to a digital signal processor. The AD974 is designed to interface with a general purpose serial port or I/O ports on a microcontroller. A variety of external buffers can be used with the AD974 to prevent digital noise from coupling into the ADC. The following sections illustrate the use of the AD974 with an SPI equipped microcontroller and the ADSP-2181 signal processor.

SPI INTERFACE

Figure 25 shows a general interface diagram between the AD974 and an SPI equipped microcontroller. This interface assumes that the convert pulses will originate from the microcontroller and that the AD974 will act as the slave device. The convert pulse could be initiated in response to an internal timer interrupt. The reading of output data, one byte at a time, if necessary, could be initiated in response to the end-of-conversion signal ($\overline{BUSY}$ going high).

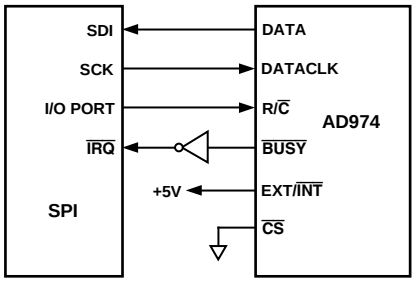


Figure 25. AD974-to-SPI Interface

ADSP-2181 INTERFACE

Figure 26 shows an interface between the AD974 and the ADSP-2181 Digital Signal Processor. The AD974 is configured for the Internal Clock mode (EXT/$\overline{INT}$ = 0) and will therefore act as the master device. The convert command is shown generated from an external oscillator in order to provide a low jitter signal appropriate for both dc and ac measurements. Because the SPORT, within the ADSP-2181, will be seeing a discontinuous external clock, some steps are required to ensure that the serial port is properly synchronized to this clock during each data read operation. The recommended procedure to ensure this is as follows:

- Enable SPORT0 through the System Control register.
- Set the SCLK Divide register to zero.
- Setup PF0 and PF1 as outputs by setting bits 0 and 1 in PFTYPE.
- Force RFS0 low through PF0. The Receive Frame Sync signal has been programmed active high.
- Enable AD974 by forcing $\overline{CS}$ = 0 through PF1.
- Enable SPORT0 Receive Interrupt through the IMASK register.
- Wait for at least one full conversion cycle of the AD974 and throw away the received data.
- Disable the AD974 by forcing $\overline{CS}$ = 1 through PF1.
- Wait for a period of time equal to one conversion cycle.
- Force RFS0 high through PF0.
- Enable the AD974 by forcing $\overline{CS}$ = 0 through PF1.

The ADSP-2181 SPORT0 will now remain synchronized to the external discontinuous clock for all subsequent conversions.

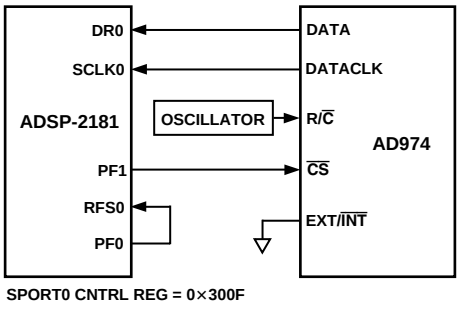


Figure 26. AD974-to-ADSP-2181 Interface

POWER SUPPLIES AND DECOUPLING

The AD974 has two power supply input pins. V_{ANA} and V_{DIG} provide the supply voltages to the analog and digital portions, respectively. V_{ANA} is the +5 V supply for the on-chip analog circuitry, and V_{DIG} is the +5 V supply for the on-chip digital circuitry. The AD974 is designed to be independent of power supply sequencing and thus free from supply voltage induced latchup.

With high performance linear circuits, changes in the power supplies can result in undesired circuit performance. Optimally, well regulated power supplies should be chosen with less than 1% ripple. The ac output impedance of a power supply is a complex function of frequency and will generally increase with frequency. Thus, high frequency switching, such as that encountered with digital circuitry, requires the fast transient currents that most power supplies cannot adequately provide. Such a situation results in large voltage spikes on the supplies. To compensate for the finite ac output impedance of most supplies, charge "reserves" should be stored in bypass capacitors. This will effectively lower the supplies impedance presented to the AD974 V_{ANA} and V_{DIG} pins and reduce the magnitude of these spikes. Decoupling capacitors, typically 0.1 μF, should be placed close to the power supply pins of the AD974 to minimize any inductance between the capacitors and the V_{ANA} and V_{DIG} pins.

The AD974 may be operated from a single +5 V supply. When separate supplies are used, however, it is beneficial to have larger (10 μF) capacitors placed between the logic supply (V_{DIG}) and digital common (DGND), and between the analog supply (V_{ANA}) and the analog common (AGND2). Additionally, 10 μF capacitors should be located in the vicinity of the ADC to further reduce low frequency ripple. In systems where the device will be subjected to harsh environmental noise, additional decoupling may be required.

GROUNDING

The AD974 has three ground pins; AGND1, AGND2 and DGND. The analog ground pins are the "high quality" ground reference points and should be connected to the system analog common. AGND2 is the ground to which most internal ADC analog signals are referenced. This ground is most susceptible to current-induced voltage drops and thus must be connected with the least resistance back to the power supply. AGND1 is the low current analog supply ground and should be the analog common for the external reference, input op amp drive circuitry and the input resistor divider circuit. By applying the inputs referenced to this ground, any ground variations will be offset and have a minimal effect on the resulting analog input to the ADC. The digital ground pin, DGND, is the reference point for all of the digital signals that control the AD974.

The AD974 can be powered with two separate power supplies or with a single analog supply. When the system digital supply is noisy, or fast switching digital signals are present, it is recommended to connect the analog supply to both the V_{ANA} and V_{DIG} pins of the AD974 and the system supply to the remaining digital circuitry. With this configuration, AGND1, AGND2 and DGND should be connected back at the ADC. When there is significant bus activity on the digital output pins, the digital and analog supply pins on the ADC should be separated. This would eliminate any high speed digital noise from coupling back to the analog portion of the AD974. In this configuration, the digital ground pin DGND should be connected to the system digital ground and be separate from the AGND pins.

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout and trace impedance is a significant issue. A 1.22 mA current through a 0.5 Ω trace will develop a voltage drop of 0.6 mV, which is 2 LSBs at the 16-bit level over the 20 volt full-scale range. Ground circuit impedances should be reduced as much as possible since any ground potential differences between the signal source and the ADC appear as an error voltage in series with the input signal. In addition to ground drops, inductive and capacitive coupling needs to be considered. This is especially true when high accuracy analog input signals share the same board with digital signals. Thus, to minimize input noise coupling, the input signal leads to V_{IN} and the signal return leads from AGND should be kept as short as possible. In addition, power supplies should also be decoupled to filter out ac noise.

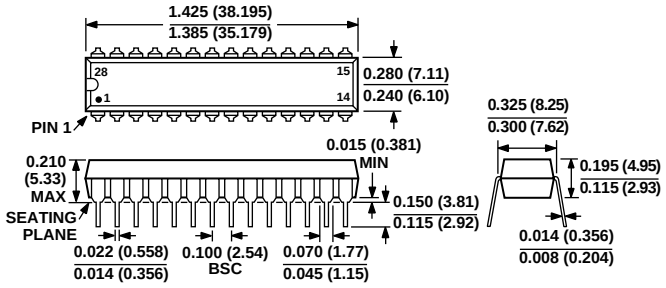
Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also recommended with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from high speed digital signals and if absolutely necessary, should only cross them at right angles.

In addition, it is recommended that multilayer PC boards be used with separate power and ground planes. When designing the separate sections, careful attention should be paid to the layout.

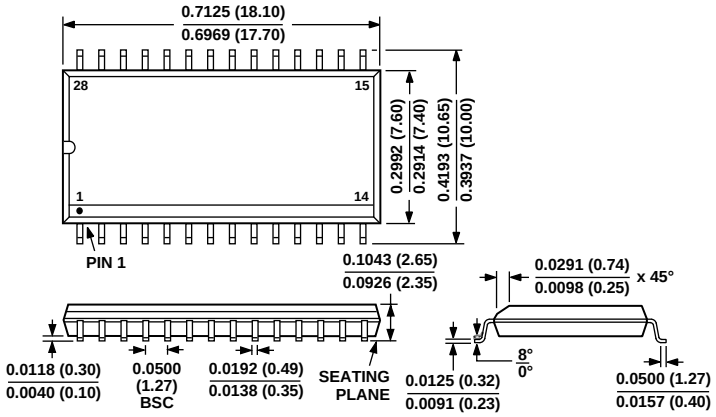
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

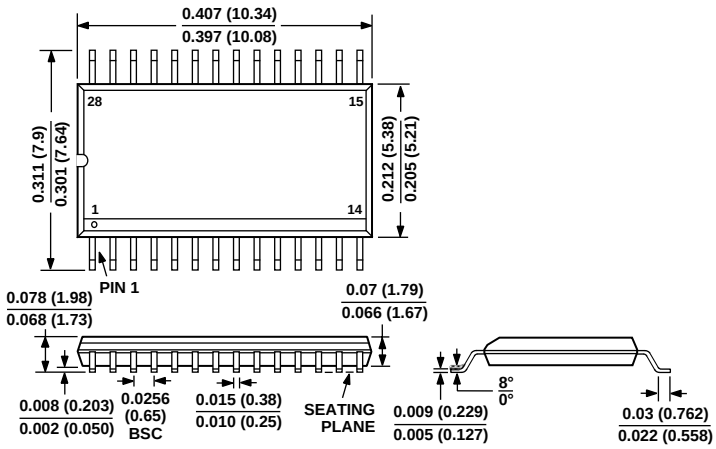
28-Lead 300 Mil Plastic DIP
(N-28B)



28-Lead Wide Body (SOIC)
(R-28)



28-Lead Shrink Small Outline Package (SSOP)
(RS-28)



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