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**Continuity of ordering part numbers**

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# CY7C68013A/CY7C68014A
# CY7C68015A/CY7C68016A

# EZ-USB® FX2LP™ USB Microcontroller High-Speed USB Peripheral Controller

## Features

- USB 2.0 USB IF Hi-Speed certified (TID # 40460272)
- Single-chip integrated USB 2.0 transceiver, smart SIE, and enhanced 8051 microprocessor
- Fit-, form-, and function-compatible with the FX2
  - Pin-compatible0
  - Object-code-compatible
  - Functionally compatible (FX2LP is a superset)
- Ultra-low power: $I_{CC}$ no more than 85 mA in any mode
  - Ideal for bus- and battery-powered applications
- Software: 8051 code runs from:
  - Internal RAM, which is downloaded through USB
  - Internal RAM, which is loaded from EEPROM
  - External memory device (128-pin package)
- 16 KB of on-chip code/data RAM
- Four programmable BULK, INTERRUPT, and ISOCHRONOUS endpoints
  - Buffering options: Double, triple, and quad
- Additional programmable (BULK/INTERRUPT) 64-byte endpoint
- 8-bit or 16-bit external data interface
- Smart media standard ECC generation
- GPIF™ (general programmable interface)
  - Enables direct connection to most parallel interfaces
  - Programmable waveform descriptors and configuration registers to define waveforms
  - Supports multiple ready (RDY) inputs and control (CTL) outputs
- Integrated, industry-standard, enhanced 8051
  - 48-MHz, 24-MHz, or 12-MHz CPU operation
  - Four clocks per instruction cycle
  - Two USARTs
  - Three counter/timers
  - Expanded interrupt system
  - Two data pointers
- 3.3-V operation with 5-V tolerant inputs
- Vectored USB interrupts and GPIF/FIFO interrupts
- Separate data buffers for the setup and data portions of a CONTROL transfer
- Integrated $I^2C$ controller; runs at 100 or 400 kHz[1]
- Four integrated FIFOs
  - Integrated glue logic and FIFOs lower system cost
  - Automatic conversion to and from 16-bit buses
  - Master or slave operation
  - Uses external clock or asynchronous strobes
  - Easy interface to ASIC and DSP ICs
- Available in commercial and industrial temperature grades (all packages except VFBGA)

### Features (CY7C68013A/14A only)

- CY7C68014A: Ideal for battery-powered applications
  - Suspend current: 100 µA (typ)
- CY7C68013A: Ideal for nonbattery-powered applications
  - Suspend current: 300 µA (typ)
- Available in five Pb-free packages with up to 40 GPIOs
  - 128-pin TQFP (40 GPIOs), 100-pin TQFP (40 GPIOs), 56-pin QFN (24 GPIOs), 56-pin SSOP (24 GPIOs), and 56-pin VFBGA (24 GPIOs)

### Features (CY7C68015A/16A only)

- CY7C68016A: Ideal for battery-powered applications
  - Suspend current: 100 µA (typ)
- CY7C68015A: Ideal for nonbattery-powered applications
  - Suspend current: 300 µA (typ)
- Available in Pb-free 56-pin QFN package (26 GPIOs)
- Two more GPIOs than CY7C68013A/14A enabling additional features in the same footprint

## Functional Description

For a complete list of related resources, click here.

Errata: For information on silicon errata, see "Errata" on page 68. Details include trigger conditions, devices affected, and proposed workaround.

**Note**
1. The actual $I^2C$ clock frequency will be different. The measured $I^2C$ clock frequency when set for 100 kHz and 400 kHz is around 85 kHz and 300 kHz respectively.

## More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the application note AN65209 - Getting Started with FX2LP.

- Overview: USB Portfolio, USB Roadmap
- USB 2.0 Product Selectors: FX2LP, AT2LP, NX2LP-Flex, SX2
- Application notes: Cypress offers a large number of USB application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with FX2LP are:
  - AN65209 - Getting Started with FX2LP
  - AN15456 - Guide to Successful EZ-USB® FX2LP™ and EZ-USB FX1™ Hardware Design and Debug
  - AN50963 - EZ-USB® FX1™/FX2LP™ Boot Options
  - AN66806 - EZ-USB® FX2LP™ GPIF Design Guide
  - AN61345 - Implementing an FX2LP™- FPGA Interface
  - AN57322 - Interfacing SRAM with FX2LP over GPIF
  - AN4053 - Streaming Data through Isochronous/Bulk Endpoints on EZ-USB® FX2 and EZUSB FX2LP
  - AN63787 - EZ-USB® FX2LP™ GPIF and Slave FIFO Configuration Examples using 8-bit Asynchronous Interface

For complete list of Application notes, click here.

- Code Examples:
  - USB Hi-Speed
- Technical Reference Manual (TRM):
  - EZ-USB FX2LP Technical Reference Manual
- Reference Designs:
  - CY4661 - External USB Hard Disk Drives (HDD) with Fingerprint Authentication Security
  - FX2LP DMB-T/H TV Dongle reference design
- Models: IBIS

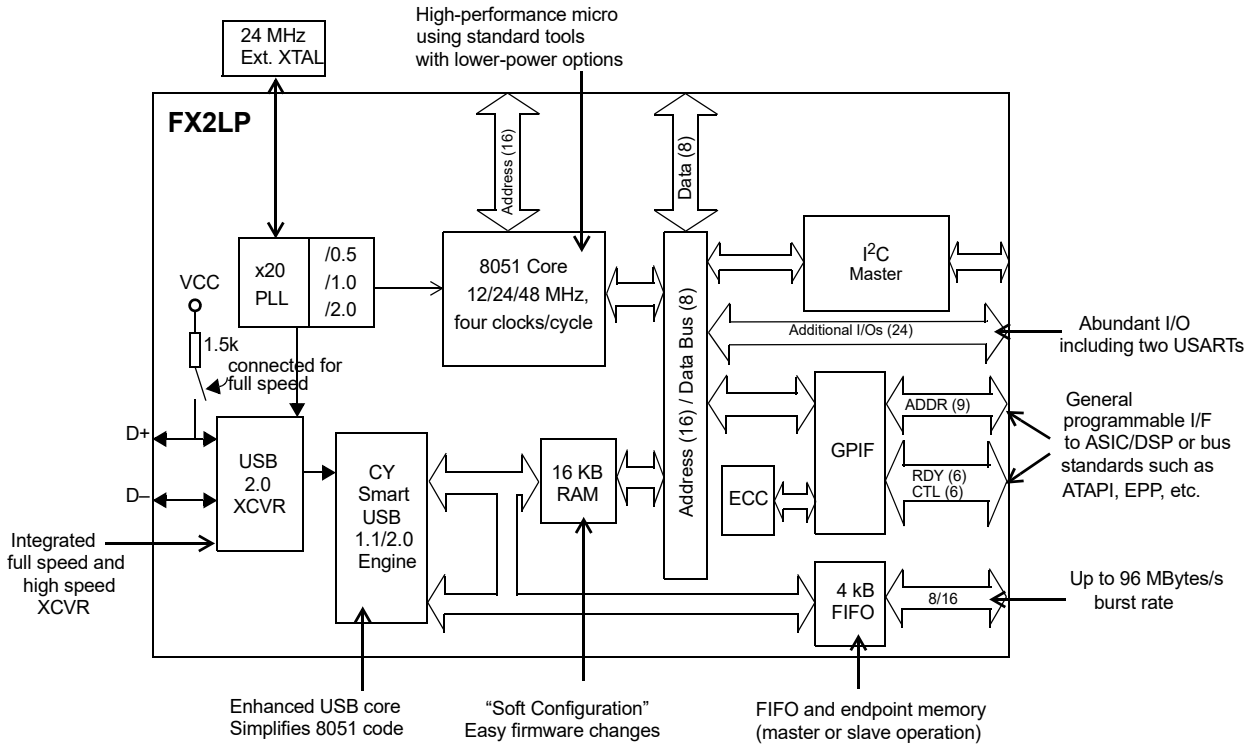
### EZ-USB FX2LP Development Kit

The CY3684 EZ-USB FX2LP Development Kit is a complete development resource for FX2LP. It provides a platform to develop and test custom projects using FX2LP. The development kit contains collateral materials for the firmware, hardware, and software aspects of a design using FX2LP.

### GPIF™ Designer

FX2LP™ General Programmable Interface (GPIF) provides an independent hardware unit, which creates the data and control signals required by an external interface. FX2LP GPIF Designer allows users to create and modify GPIF waveform descriptors for EZ-USB FX2/ FX2LP family of chips using a graphical user interface. Extensive discussion of general GPIF discussion and programming using GPIF Designer is included in *FX2LP Technical Reference Manual* and *GPIF Designer User Guide*, distributed with GPIF Designer. *AN66806 - Getting Started with EZ-USB® FX2LP™ GPIF* can be a good starting point.

## Logic Block Diagram




Cypress's EZ-USB® FX2LP™ (CY7C68013A/14A) is a low-power version of the EZ-USB FX2™ (CY7C68013), which is a highly integrated, low-power USB 2.0 microcontroller. By integrating the USB 2.0 transceiver, serial interface engine (SIE), enhanced 8051 microcontroller, and a programmable peripheral interface in a single chip, Cypress has created a cost-effective solution that provides superior time-to-market advantages with low power to enable bus-powered applications.

The ingenious architecture of FX2LP results in data transfer rates of over 53 Mbytes per second (the maximum allowable USB 2.0 bandwidth), while still using a low-cost 8051 microcontroller in a package as small as a 56 VFBGA (5 mm × 5 mm). Because it incorporates the USB 2.0 transceiver, the FX2LP is more economical, providing a smaller-footprint solution than a USB 2.0 SIE or external transceiver implementations.

With EZ-USB FX2LP, the Cypress Smart SIE handles most of the USB 1.1 and 2.0 protocol in hardware, freeing the embedded microcontroller for application-specific functions and decreasing the development time to ensure USB compatibility.

The general programmable interface (GPIF) and Master/Slave Endpoint FIFO (8-bit or 16-bit data bus) provide an easy and glueless interface to popular interfaces such as ATA, UTOPIA, EPP, PCMCIA, and most DSP/processors.

The FX2LP draws less current than the FX2 (CY7C68013), has double the on-chip code/data RAM, and is fit, form, and function compatible with the 56-, 100-, and 128-pin FX2.

Five packages are defined for the family: 56-ball VFBGA, 56-pin SSOP, 56-pin QFN, 100-pin TQFP, and 128-pin TQFP.

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## Applications

- Portable video recorder
- MPEG/TV conversion
- DSL modems
- ATA interface
- Memory card readers
- Legacy conversion devices
- Cameras
- Scanners
- Wireless LAN
- MP3 players
- Networking

The "Reference Designs" section of the Cypress web site provides additional tools for typical USB 2.0 applications. Each reference design comes complete with firmware source and object code, schematics, and documentation. Visit www.cypress.com for more information.

## Functional Overview

### USB Signaling Speed

FX2LP operates at two of the three rates defined in the USB Specification Revision 2.0, dated April 27, 2000:

- Full speed, with a signaling bit rate of 12 Mbps
- High speed, with a signaling bit rate of 480 Mbps

FX2LP does not support the Low Speed signaling mode of 1.5 Mbps.

### 8051 Microprocessor

The 8051 microprocessor embedded in the FX2LP family has 256 bytes of register RAM, an expanded interrupt system, three timer/counters, and two USARTs.

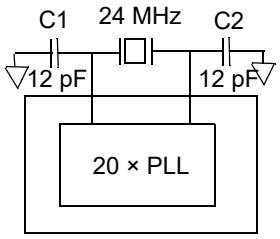
*8051 Clock Frequency*

FX2LP has an on-chip oscillator circuit that uses an external 24-MHz (±100 ppm) crystal with the following characteristics:

- Parallel resonant
- Fundamental mode
- 500-µW drive level
- 12-pF (5% tolerance) load capacitors

An on-chip PLL multiplies the 24-MHz oscillator up to 480 MHz, as required by the transceiver/PHY; internal counters divide it down for use as the 8051 clock. The default 8051 clock frequency is 12 MHz. The clock frequency of the 8051 can be changed by the 8051 through the CPUCS register, dynamically.

**Figure 1. Crystal Configuration**




12-pF capacitor values assume a trace capacitance of 3 pF per side on a four-layer FR4 PCA

The CLKOUT pin, which can be three-stated and inverted using internal control bits, outputs the 50% duty cycle 8051 clock, at the selected 8051 clock frequency: 48 MHz, 24 MHz, or 12 MHz.

*USARTs*

FX2LP contains two standard 8051 USARTs, addressed through Special Function Register (SFR) bits. The USART interface pins are available on separate I/O pins, and are not multiplexed with port pins.

UART0 and UART1 can operate using an internal clock at 230 KBaud with no more than 1% baud rate error. 230 KBaud operation is achieved by an internally derived clock source that generates overflow pulses at the appropriate time. The internal clock adjusts for the 8051 clock rate (48 MHz, 24 MHz, and 12 MHz) such that it always presents the correct frequency for the 230-KBaud operation[2].

*Special Function Registers*

Certain 8051 SFR addresses are populated to provide fast access to critical FX2LP functions. These SFR additions are shown in Table 1 on page 6. Bold type indicates nonstandard, enhanced 8051 registers. The two SFR rows that end with "0" and "8" contain bit-addressable registers. The four I/O ports A to D use the SFR addresses used in the standard 8051 for ports 0 to 3, which are not implemented in FX2LP. Because of the faster and more efficient SFR addressing, the FX2LP I/O ports are not addressable in external RAM space (using the MOVX instruction).

### $I^2C$ Bus

FX2LP supports the $I^2C$ bus as a master only at 100/400 kHz[3]. SCL and SDA pins have open-drain outputs and hysteresis inputs. These signals must be pulled up to 3.3 V, even if no $I^2C$ device is connected.

### Buses

All packages, 8-bit or 16-bit "FIFO" bidirectional data bus, multiplexed on I/O ports B and D. 128-pin package: adds 16-bit output-only 8051 address bus, 8-bit bidirectional data bus.

**Notes**
2. 115-KBaud operation is also possible by programming the 8051 SMOD0 or SMOD1 bits to a "1" for UART0, UART1, or both respectively.
3. The actual $I^2C$ clock frequency will be different.The measured $I^2C$ clock frequency when set for 100 kHz and 400 kHz is around 85 kHz and 300 kHz respectively.

**Table 1. Special Function Registers**

| x | 8x | 9x | Ax | Bx | Cx | Dx | Ex | Fx |
|---|---|---|---|---|---|---|---|---|
| 0 | **IOA** | **IOB** | **IOC** | **IOD** | SCON1 | PSW | ACC | B |
| 1 | SP | **EXIF** | **INT2CLR** | **IOE** | SBUF1 | – | – | – |
| 2 | DPL0 | **MPAGE** | **INT4CLR** | **OEA** | – | – | – | – |
| 3 | DPH0 | – | – | **OEB** | – | – | – | – |
| 4 | **DPL1** | – | – | **OEC** | – | – | – | – |
| 5 | **DPH1** | – | – | **OED** | – | – | – | – |
| 6 | **DPS** | – | – | **OEE** | – | – | – | – |
| 7 | PCON | – | – | – | – | – | – | – |
| 8 | TCON | SCON0 | IE | IP | T2CON | **EICON** | **EIE** | **EIP** |
| 9 | TMOD | SBUF0 | – | – | – | – | – | – |
| A | TL0 | **AUTOPTRH1** | **EP2468STAT** | **EP01STAT** | RCAP2L | – | – | – |
| B | TL1 | **AUTOPTRL1** | **EP24FIFOFLGS** | **GPIFTRIG** | RCAP2H | – | – | – |
| C | TH0 | **reserved** | **EP68FIFOFLGS** | | TL2 | – | – | – |
| D | TH1 | **AUTOPTRH2** | – | **GPIFSGLDATH** | TH2 | – | – | – |
| E | **CKCON** | **AUTOPTRL2** | – | **GPIFSGLDATLX** | – | – | – | – |
| F | – | **reserved** | **AUTOPTRSET-UP** | **GPIFSGLDATLNOX** | – | – | – | – |

## USB Boot Methods

During the power-up sequence, internal logic checks the $I^2C$ port for the connection of an EEPROM whose first byte is either 0xC0 or 0xC2. If found, it uses the VID/PID/DID values in the EEPROM in place of the internally stored values (0xC0), or it boot-loads the EEPROM contents into internal RAM (0xC2). If no EEPROM is detected, FX2LP enumerates using internally stored descriptors. The default ID values for FX2LP are VID/PID/DID (0x04B4, 0x8613, 0xAxxx where xxx = Chip revision)[4].

**Table 2. Default ID Values for FX2LP**

| Default VID/PID/DID | | |
|---|---|---|
| Vendor ID | 0x04B4 | Cypress Semiconductor |
| Product ID | 0x8613 | EZ-USB FX2LP |
| Device release | 0xAnnn | Depends on chip revision (nnn = chip revision where first silicon = 001) |

## ReNumeration

Because the FX2LP's configuration is soft, one chip can take on the identities of multiple distinct USB devices.

When first plugged into USB, the FX2LP enumerates automatically and downloads firmware and USB descriptor tables over the USB cable. Next, the FX2LP enumerates again, this time as a device defined by the downloaded information. This patented two step process called ReNumeration™ happens instantly when the device is plugged in, without a hint that the initial download step has occurred.

Two control bits in the USBCS (USB Control and Status) register control the ReNumeration process: DISCON and RENUM. To simulate a USB disconnect, the firmware sets DISCON to 1. To reconnect, the firmware clears DISCON to 0.

Before reconnecting, the firmware sets or clears the RENUM bit to indicate whether the firmware or the Default USB Device handles device requests over endpoint zero: if RENUM = 0, the Default USB Device handles device requests; if RENUM = 1, the firmware services the requests.

## Bus-Powered Applications

The FX2LP fully supports bus-powered designs by enumerating with less than 100 mA as required by the USB 2.0 specification.

## Interrupt System

*INT2 Interrupt Request and Enable Registers*

FX2LP implements an autovector feature for INT2 and INT4. There are 27 INT2 (USB) vectors, and 14 INT4 (FIFO/GPIF) vectors. See EZ-USB Technical Reference Manual (TRM) for more details.

*USB Interrupt Autovectors*

The main USB interrupt is shared by 27 interrupt sources. To save the code and processing time that is required to identify the individual USB interrupt source, the FX2LP provides a second level of interrupt vectoring, called Autovectoring. When a USB interrupt is asserted, the FX2LP pushes the program counter to its stack, and then jumps to the address 0x0043 where it expects to find a "jump" instruction to the USB interrupt service routine.

**Note**
4. The $I^2C$ bus SCL and SDA pins must be pulled up, even if an EEPROM is not connected. Otherwise this detection method does not work properly.

The FX2LP jump instruction is encoded as follows:

**Table 3. INT2 USB Interrupts**

| USB INTERRUPT TABLE FOR INT2 | | | |
|---|---|---|---|
| **Priority** | **INT2VEC Value** | **Source** | **Notes** |
| 1 | 00 | SUDAV | Setup data available |
| 2 | 04 | SOF | Start of frame (or microframe) |
| 3 | 08 | SUTOK | Setup token received |
| 4 | 0C | SUSPEND | USB suspend request |
| 5 | 10 | USB RESET | Bus reset |
| 6 | 14 | HISPEED | Entered high speed operation |
| 7 | 18 | EP0ACK | FX2LP ACK'd the CONTROL Handshake |
| 8 | 1C | | reserved |
| 9 | 20 | EP0-IN | EP0-IN ready to be loaded with data |
| 10 | 24 | EP0-OUT | EP0-OUT has USB data |
| 11 | 28 | EP1-IN | EP1-IN ready to be loaded with data |
| 12 | 2C | EP1-OUT | EP1-OUT has USB data |
| 13 | 30 | EP2 | IN: buffer available. OUT: buffer has data |
| 14 | 34 | EP4 | IN: buffer available. OUT: buffer has data |
| 15 | 38 | EP6 | IN: buffer available. OUT: buffer has data |
| 16 | 3C | EP8 | IN: buffer available. OUT: buffer has data |
| 17 | 40 | IBN | IN-Bulk-NAK (any IN endpoint) |
| 18 | 44 | | reserved |
| 19 | 48 | EP0PING | EP0 OUT was pinged and it NAK'd |
| 20 | 4C | EP1PING | EP1 OUT was pinged and it NAK'd |
| 21 | 50 | EP2PING | EP2 OUT was pinged and it NAK'd |
| 22 | 54 | EP4PING | EP4 OUT was pinged and it NAK'd |
| 23 | 58 | EP6PING | EP6 OUT was pinged and it NAK'd |
| 24 | 5C | EP8PING | EP8 OUT was pinged and it NAK'd |
| 25 | 60 | ERRLIMIT | Bus errors exceeded the programmed limit |
| 26 | 64 | – | – |
| 27 | 68 | – | Reserved |
| 28 | 6C | – | Reserved |
| 29 | 70 | EP2ISOERR | ISO EP2 OUT PID sequence error |
| 30 | 74 | EP4ISOERR | ISO EP4 OUT PID sequence error |
| 31 | 78 | EP6ISOERR | ISO EP6 OUT PID sequence error |
| 32 | 7C | EP8ISOERR | ISO EP8 OUT PID sequence error |

If Autovectoring is enabled (AV2EN = 1 in the INTSET-UP register), the FX2LP substitutes its INT2VEC byte. Therefore, if the high byte ("page") of a jump table address is preloaded at the location 0x0044, the automatically inserted INT2VEC byte at 0x0045 directs the jump to the correct address out of the 27 addresses within the page.

*FIFO/GPIF Interrupt (INT4)*

Just as the USB Interrupt is shared among 27 individual USB interrupt sources, the FIFO/GPIF interrupt is shared among 14 individual FIFO/GPIF sources. The FIFO/GPIF Interrupt, similar to the USB Interrupt, can employ autovectoring.

Table 4 shows the priority and INT4VEC values for the 14 FIFO/GPIF interrupt sources.

**Table 4. Individual FIFO/GPIF Interrupt Sources**

| Priority | INT4VEC Value | Source | Notes |
|---|---|---|---|
| 1 | 80 | EP2PF | Endpoint 2 programmable flag |
| 2 | 84 | EP4PF | Endpoint 4 programmable flag |
| 3 | 88 | EP6PF | Endpoint 6 programmable flag |
| 4 | 8C | EP8PF | Endpoint 8 programmable flag |
| 5 | 90 | EP2EF | Endpoint 2 empty flag [5] |
| 6 | 94 | EP4EF | Endpoint 4 empty flag |
| 7 | 98 | EP6EF | Endpoint 6 empty flag |
| 8 | 9C | EP8EF | Endpoint 8 empty flag |
| 9 | A0 | EP2FF | Endpoint 2 full flag |
| 10 | A4 | EP4FF | Endpoint 4 full flag |
| 11 | A8 | EP6FF | Endpoint 6 full flag |
| 12 | AC | EP8FF | Endpoint 8 full flag |
| 13 | B0 | GPIFDONE | GPIF operation complete |
| 14 | B4 | GPIFWF | GPIF waveform |

If Autovectoring is enabled (AV4EN = 1 in the INTSET-UP register), the FX 2LP substitutes its INT4VEC byte. Therefore, if the high byte (“page”) of a jump-table address is preloaded at location 0x0054, the automatically inserted INT4VEC byte at 0x0055 directs the jump to the correct address out of the 14 addresses within the page. When the ISR occurs, the FX2LP pushes the program counter to its stack then jumps to address 0x0053, where it expects to find a “jump” instruction to the interrupt service routine (ISR).

**Note**

5. Errata: In Slave FIFO Asynchronous Word Wide mode, if a single word data is transferred from the USB host to EP2, configured as OUT Endpoint (EP) in the first transaction, then the Empty flag behaves incorrectly. This does not happen if the data size is more than one word in the first transaction. For more information, see the “Errata” on page 68.

## Reset and Wakeup

*Reset Pin*

The input pin, RESET#, resets the FX2LP when asserted. This pin has hysteresis and is active LOW. When a crystal is used with the CY7C680xxA, the reset period must enable stabilization of the crystal and the PLL. This reset period must be approximately 5 ms after VCC reaches 3.0 V. If the crystal input pin is driven by a clock signal, the internal PLL stabilizes in 200 µs after VCC has reached 3.0 V[6].

Figure 2 shows a power-on reset condition and a reset applied during operation. A power-on reset is defined as the time reset that is asserted while power is being applied to the circuit. A powered reset is when the FX2LP is powered on and operating and the RESET# pin is asserted.

Cypress provides an application note which describes and recommends power-on reset implementation. For more information about reset implementation for the FX2 family of products, visit http://www.cypress.com.

**Figure 2. Reset Timing Plots**

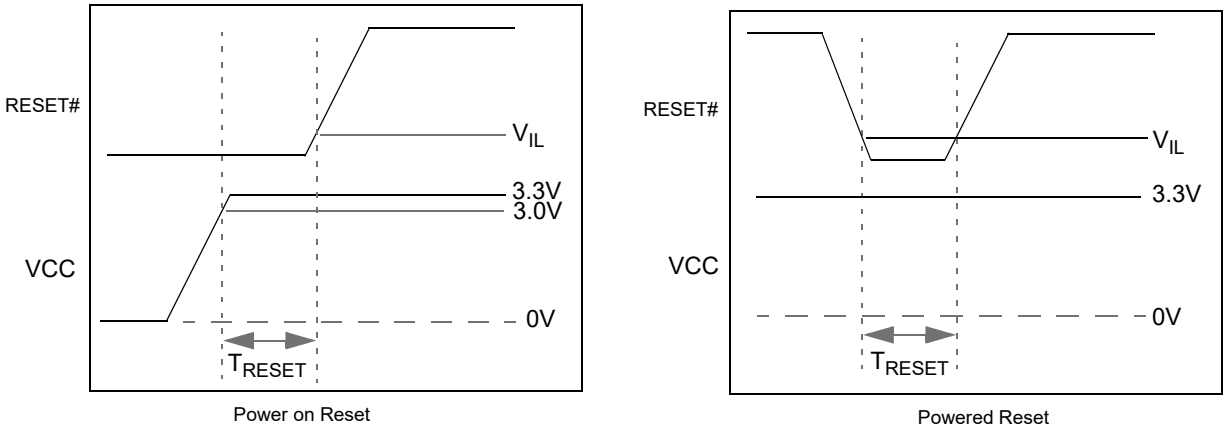



**Table 5. Reset Timing Values**

| Condition | $T_{RESET}$ |
|---|---|
| Power-on reset with crystal | 5 ms |
| Power-on reset with external clock | 200 µs + clock stability time |
| Powered reset | 200 µs |

*Wakeup Pins*

The 8051 puts itself and the rest of the chip into a power-down mode by setting PCON.0 = 1. This stops the oscillator and PLL. When WAKEUP is asserted by external logic, the oscillator restarts after the PLL stabilizes, and the 8051 receives a wakeup interrupt. This applies irrespective of whether FX2LP is connected to the USB.

The FX2LP exits the power-down (USB suspend) state by using one of the following methods:

- USB bus activity (if D+/D– lines are left floating, noise on these lines may indicate activity to the FX2LP and initiate a wakeup)
- External logic asserts the WAKEUP pin
- External logic asserts the PA3/WU2 pin

The second wakeup pin, WU2, can also be configured as a general-purpose I/O pin. This enables a simple external R-C network to be used as a periodic wakeup source. WAKEUP is by default active LOW.

## Program/Data RAM

*Size*

The FX2LP has 16 KB of internal program/data RAM, where PSEN#/RD# signals are internally ORed to enable the 8051 to access it as both program and data memory. No USB control registers appears in this space.

Two memory maps are shown in the following diagrams:

Figure 3 shows the Internal Code Memory, EA = 0.

Figure 4 on page 11 shows the External Code Memory, EA = 1.

*Internal Code Memory, EA = 0*

This mode implements the internal 16 KB block of RAM (starting at 0) as combined code and data memory. When external RAM or ROM is added, the external read and write strobes are suppressed for memory spaces that exist inside the chip. This enables the user to connect a 64 KB memory without requiring address decodes to keep clear of internal memory spaces.

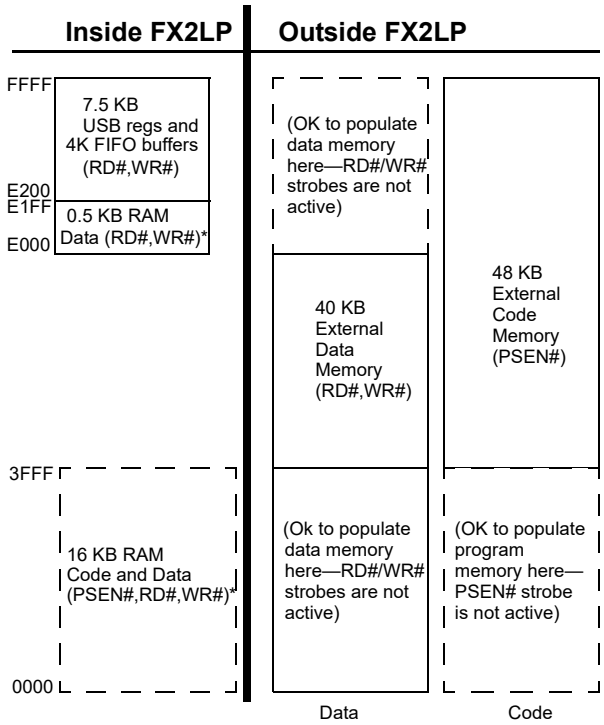
Only the internal 16 KB and scratch pad 0.5 KB RAM spaces have the following access:

- USB download
- USB upload
- Setup data pointer
- $I^2C$ interface boot load

*External Code Memory, EA = 1*

The bottom 16 KB of program memory is external and therefore the bottom 16 KB of internal RAM is accessible only as a data memory.

**Figure 3. Internal Code Memory, EA = 0**

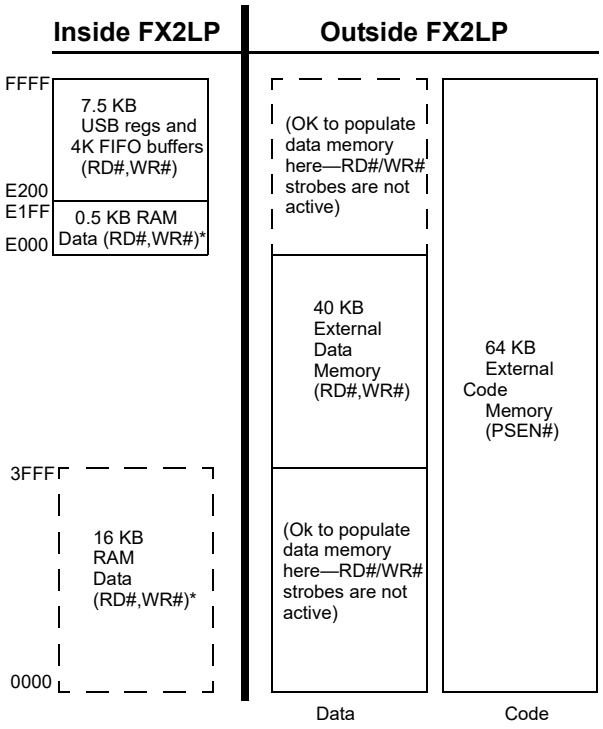



*SUDPTR, USB upload/download, $I^2C$ interface boot access

**Note**

6. If the external clock is powered at the same time as the CY7C680xxA and has a stabilization wait period, it must be added to the 200 µs.

**Figure 4. External Code Memory, EA = 1**




*SUDPTR, USB upload/download, $I^2C$ interface boot access

## Register Addresses

| | |
|---|---|
| FFFF<br>F000 | 4 KB EP2-EP8 buffers (8 x 512) |
| EFFF<br>E800 | 2 KB RESERVED |
| E7FF<br>E7C0 | 64 BEP1IN |
| E7BF<br>E780 | 64 Bytes EP1OUT |
| E77F<br>E740 | 64 Bytes EP0 IN/OUT |
| E73F<br>E700 | 64 Bytes RESERVED |
| E6FF<br>E500 | 8051 Addressable Registers (512) |
| E4FF<br>E480 | Reserved (128) |
| E47F<br>E400 | 128 Bytes GPIF Waveforms |
| E3FF<br>E200 | Reserved (512) |
| E1FF<br>E000 | 512 Bytes 8051 xdata RAM |

## Endpoint RAM

*Size*

- 3 × 64 bytes (Endpoints 0 and 1)
- 8 × 512 bytes (Endpoints 2, 4, 6, 8)

*Organization*

- EP0
- Bidirectional endpoint zero, 64-byte buffer
- EP1IN, EP1OUT
- 64 byte buffers, bulk or interrupt
- EP2, 4, 6, 8
- Eight 512-byte buffers, bulk, interrupt, or isochronous. EP4 and EP8 can be double buffered; EP2 and 6 can be either double, triple, or quad buffered. For Hi-Speed endpoint configuration options, see Figure 5.

*Setup Data Buffer*

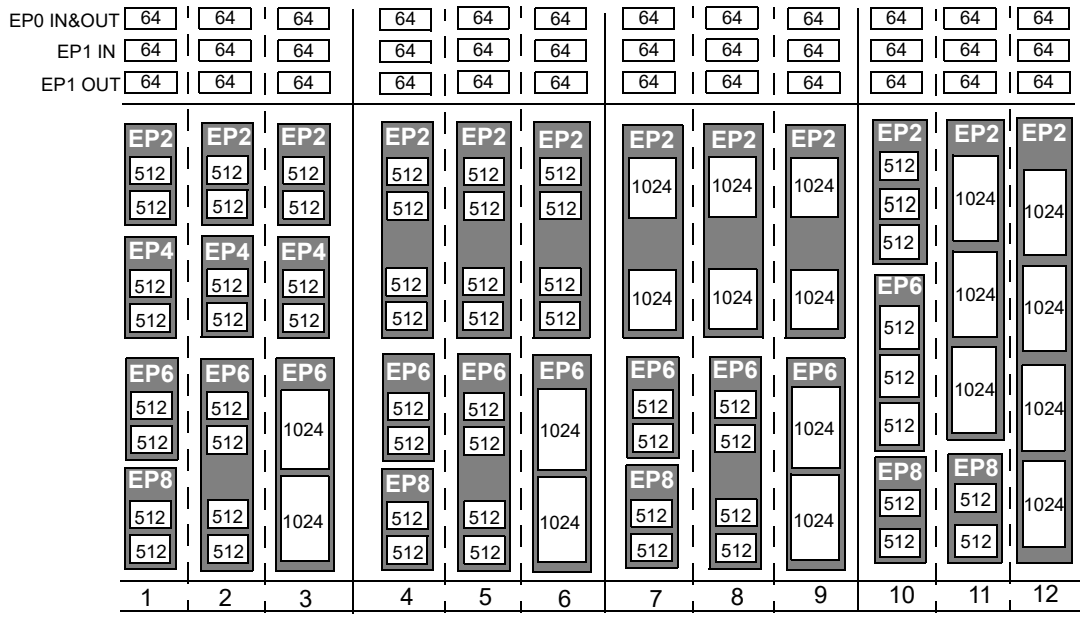
A separate 8-byte buffer at 0xE6B8-0xE6BF holds the setup data from a CONTROL transfer.

*Endpoint Configurations (Hi-Speed Mode)*

Endpoints 0 and 1 are the same for every configuration. Endpoint 0 is the only CONTROL endpoint, and endpoint 1 can be either BULK or INTERRUPT.

The endpoint buffers can be configured in any 1 of the 12 configurations shown in the vertical columns. When operating in the Full-Speed BULK mode, only the first 64 bytes of each buffer are used. For example, in Hi-Speed mode, the max packet size is 512 bytes, but in Full-Speed mode, it is 64 bytes. Even though a buffer is configured to a 512-byte buffer, in Full-Speed mode, only the first 64 bytes are used. The unused endpoint buffer space is not available for other operations. An example endpoint configuration is the EP2–1024 double-buffered; EP6–512 quad-buffered (column 8).

**Figure 5. Endpoint Configuration**



*Default Full-Speed Alternate Settings*

**Table 6. Default Full Speed Alternate Settings**[7, 8]

| Alternate Setting | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| ep0 | 64 | 64 | 64 | 64 |
| ep1out | 0 | 64 bulk | 64 int | 64 int |
| ep1in | 0 | 64 bulk | 64 int | 64 int |
| ep2 | 0 | 64 bulk out (2×) | 64 int out (2×) | 64 iso out (2×) |
| ep4 | 0 | 64 bulk out (2×) | 64 bulk out (2×) | 64 bulk out (2×) |
| ep6 | 0 | 64 bulk in (2×) | 64 int in (2×) | 64 iso in (2×) |
| ep8 | 0 | 64 bulk in (2×) | 64 bulk in (2×) | 64 bulk in (2×) |

*Default High Speed Alternate Settings*

**Table 7. Default Hi-Speed Alternate Settings**[7, 8]

| Alternate Setting | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| ep0 | 64 | 64 | 64 | 64 |
| ep1out | 0 | 512 bulk[9] | 64 int | 64 int |
| ep1in | 0 | 512 bulk[9] | 64 int | 64 int |
| ep2 | 0 | 512 bulk out (2×) | 512 int out (2×) | 512 iso out (2×) |
| ep4 | 0 | 512 bulk out (2×) | 512 bulk out (2×) | 512 bulk out (2×) |
| ep6 | 0 | 512 bulk in (2×) | 512 int in (2×) | 512 iso in (2×) |
| ep8 | 0 | 512 bulk in (2×) | 512 bulk in (2×) | 512 bulk in (2×) |

**Notes**
7. "0" means "not implemented."
8. "2×" means "double buffered."
9. Even though these buffers are 64 bytes, they are reported as 512 for USB 2.0 compliance. The user must never transfer packets larger than 64 bytes to EP1.

## External FIFO Interface

*Architecture*

The FX2LP slave FIFO architecture has eight 512-byte blocks in the endpoint RAM that directly serve as FIFO memories and are controlled by FIFO control signals (such as IFCLK, SLCS#, SLRD, SLWR, SLOE, PKTEND, and flags).

In operation, some of the eight RAM blocks fill or empty from the SIE, while the others are connected to the I/O transfer logic. The transfer logic takes two forms: the GPIF for internally generated control signals and the slave FIFO interface for externally controlled transfers.

*Master/Slave Control Signals*

The FX2LP endpoint FIFOs are implemented as eight physically distinct 256×16 RAM blocks. The 8051/SIE can switch any of the RAM blocks between two domains, the USB (SIE) domain and the 8051-I/O Unit domain. This switching is done virtually instantaneously, giving essentially zero transfer time between "USB FIFOs" and "Slave FIFOs." Because they are physically the same memory, no bytes are actually transferred between buffers.

At any time, some RAM blocks are filling/emptying with the USB data under SIE control, while other RAM blocks are available to the 8051, the I/O control unit, or both. The RAM blocks operates as single-port in the USB domain, and dual-port in the 8051-I/O domain. The blocks can be configured as single-, double-, triple-, or quad-buffered as previously shown.

The I/O control unit implements either an internal master (M for Master) or external master (S for Slave) interface.

In Master (M) mode, the GPIF internally controls FIFOADR[1..0] to select a FIFO. The RDY pins (two in the 56-pin package, six in the 100-pin and 128-pin packages) can be used as flag inputs from an external FIFO or other logic if desired. The GPIF can be run from either an internally derived clock or externally supplied clock (IFCLK), at a rate that transfers data up to 96 MBytes/s (48 Hz IFCLK with 16-bit interface).

In the Slave (S) mode, FX2LP accepts either an internally derived clock or externally supplied clock (IFCLK, max frequency 48 MHz) and SLCS#, SLRD, SLWR, SLOE, PKTEND signals from external logic. When using an external IFCLK, the external clock must be present before switching to the external clock with the IFCLKSRC bit. Each endpoint can individually be selected for byte or word operation by an internal configuration bit and a Slave FIFO Output Enable signal (SLOE) that enables data of the selected width. External logic must ensure that the output enable signal is inactive when writing data to a slave FIFO. The slave interface can also operate asynchronously, where the SLRD and SLWR signals act directly as strobes, rather than a clock qualifier as in synchronous mode. The signals SLRD, SLWR, SLOE, and PKTEND are gated by the signal SLCS#.

*GPIF and FIFO Clock Rates*

An 8051 register bit selects one of two frequencies for the internally supplied interface clock: 30 MHz and 48 MHz. Alternatively, an externally supplied clock of 5 MHz–48 MHz feeding the IFCLK pin can be used as the interface clock. IFCLK can be configured to function as an output clock when the GPIF and FIFOs are internally clocked. An output enable bit in the IFCONFIG register turns this clock output off, if desired. Another bit within the IFCONFIG register inverts the IFCLK signal whether internally or externally sourced.

## GPIF

The GPIF is a flexible 8-bit or 16-bit parallel interface driven by a user-programmable finite state machine. It enables the CY7C68013A/15A to perform local bus mastering and can implement a wide variety of protocols such as ATA interface, printer parallel port, and Utopia.

The GPIF has six programmable control outputs (CTL), nine address outputs (GPIFADRx), and six general-purpose ready inputs (RDY). The data bus width can be 8 or 16 bits. Each GPIF vector defines the state of the control outputs, and determines what state a ready input (or multiple inputs) must be before proceeding. The GPIF vector can be programmed to advance a FIFO to the next data value, advance an address, etc. A sequence of the GPIF vectors make up a single waveform that is executed to perform the desired data move between the FX2LP and the external device.

*Six Control OUT Signals*

The 100-pin and 128-pin packages bring out all six Control Output pins (CTL0-CTL5). The 8051 programs the GPIF unit to define the CTL waveforms. The 56-pin package brings out three of these signals, CTL0–CTL2. CTLx waveform edges can be programmed to make transitions as fast as once per clock (20.8 ns using a 48-MHz clock).

*Six Ready IN Signals*

The 100-pin and 128-pin packages bring out all six Ready inputs (RDY0–RDY5). The 8051 programs the GPIF unit to test the RDY pins for GPIF branching. The 56-pin package brings out two of these signals, RDY0–1.

*Nine GPIF Address OUT Signals*

Nine GPIF address lines are available in the 100-pin and 128-pin packages, GPIFADR[8..0]. The GPIF address lines enable indexing through up to a 512-byte block of RAM. If more address lines are needed, then I/O port pins are used.

*Long Transfer Mode*

In the master mode, the 8051 appropriately sets GPIF transaction count registers (GPIFTCB3, GPIFTCB2, GPIFTCB1, or GPIFTCB0) for unattended transfers of up to $2^{32}$ transactions. The GPIF automatically throttles data flow to prevent under or overflow until the full number of requested transactions complete. The GPIF decrements the value in these registers to represent the current status of the transaction.

## ECC Generation

The EZ-USB can calculate ECCs (Error Correcting Codes)[10] on data that passes across its GPIF or Slave FIFO interfaces. There are two ECC configurations: Two ECCs, each calculated over 256 bytes (SmartMedia Standard); and one ECC calculated over 512 bytes.

The ECC can correct any one-bit error or detect any two-bit error.

### *ECC Implementation*

The two ECC configurations are selected by the ECCM bit:

**ECCM = 0**

Two 3-byte ECCs, each calculated over a 256-byte block of data. This configuration conforms to the SmartMedia Standard.

Write any value to ECCRESET, then pass data across the GPIF or Slave FIFO interface. The ECC for the first 256 bytes of data is calculated and stored in ECC1. The ECC for the next 256 bytes is stored in ECC2. After the second ECC is calculated, the values in the ECCx registers do not change until ECCRESET is written again, even if more data is subsequently passed across the interface.

**ECCM = 1**

One 3-byte ECC calculated over a 512-byte block of data.

Write any value to ECCRESET then pass data across the GPIF or Slave FIFO interface. The ECC for the first 512 bytes of data is calculated and stored in ECC1; ECC2 is unused. After the ECC is calculated, the values in ECC1 do not change even if more data is subsequently passed across the interface, till ECCRESET is written again.

## USB Uploads and Downloads

The core has the ability to directly edit the data contents of the internal 16-KB RAM and of the internal 512-byte scratch pad RAM via a vendor-specific command. This capability is normally used when soft downloading the user code and is available only to and from the internal RAM, only when the 8051 is held in reset. The available RAM spaces are 16 KB from 0x0000–0x3FFF (code/data) and 512 bytes from 0xE000–0xE1FF (scratch pad data RAM)[11].

## Autopointer Access

FX2LP provides two identical autopointers. They are similar to the internal 8051 data pointers but with an additional feature: they can optionally increment after every memory access. This capability is available to and from both internal and external RAM. Autopointers are available in external FX2LP registers under the control of a mode bit (AUTOPTRSET-UP.0). Using the external FX2LP autopointer access (at 0xE67B–0xE67C) enables the autopointer to access all internal and external RAM to the part.

Also, autopointers can point to any FX2LP register or endpoint buffer space. When the autopointer access to external memory is enabled, locations 0xE67B and 0xE67C in XDATA and code space cannot be used.

## $I^2C$ Controller

FX2LP has one $I^2C$ port that is driven by two internal controllers, the one that automatically operates at boot time to load VID/PID/DID and configuration information, and another that the 8051 uses when running to control external $I^2C$ devices. The $I^2C$ port operates in master mode only.

### *$I^2C$ Port Pins*

The $I^2C$ pins SCL and SDA must have external 2.2-kΩ pull-up resistors even if no EEPROM is connected to the FX2LP. External EEPROM device address pins must be configured properly. See Table 8 for configuring the device address pins.

**Table 8. Strap Boot EEPROM Address Lines to These Values**

| Bytes | Example EEPROM | A2 | A1 | A0 |
|---|---|---|---|---|
| 16 | 24LC00[12] | N/A | N/A | N/A |
| 128 | 24LC01 | 0 | 0 | 0 |
| 256 | 24LC02 | 0 | 0 | 0 |
| 4K | 24LC32 | 0 | 0 | 1 |
| 8K | 24LC64 | 0 | 0 | 1 |
| 16K | 24LC128 | 0 | 0 | 1 |

### *$I^2C$ Interface Boot Load Access*

At power-on reset, the $I^2C$ interface boot loader loads the VID/PID/DID configuration bytes and up to 16 KB of program/data. The available RAM spaces are 16 KB from 0x0000–0x3FFF and 512 bytes from 0xE000–0xE1FF. The 8051 is in reset. $I^2C$ interface boot loads only occur after power-on reset.

### *$I^2C$ Interface General-Purpose Access*

The 8051 can control peripherals connected to the $I^2C$ bus using the I2CTL and I2DAT registers. FX2LP provides $I^2C$ master control only; it is never an $I^2C$ slave.

**Notes**
10. To use the ECC logic, the GPIF or Slave FIFO interface must be configured for byte-wide operation.
11. After the data is downloaded from the host, a “loader” can execute from internal RAM to transfer downloaded data to external memory.
12. This EEPROM does not have address pins.

## Compatible with Previous Generation EZ-USB FX2

The EZ-USB FX2LP is form-, fit-, and with minor exceptions, functionally-compatible with its predecessor, the EZ-USB FX2. This makes for an easy transition for designers wanting to upgrade their systems from the FX2 to the FX2LP. The pinout and package selection are identical and a vast majority of firmware previously developed for the FX2 functions in the FX2LP.

For designers migrating from the FX2 to the FX2LP, a change in the bill of material and review of the memory allocation (due to increased internal memory) is required. For more information about migrating from EZ-USB FX2 to EZ-USB FX2LP, see the application note titled *Migrating from EZ-USB FX2 to EZ-USB FX2LP* available in the Cypress web site.

**Table 9. Part Number Conversion Table**

| EZ-USB FX2 Part Number | EZ-USB FX2LP Part Number | Package Description |
|---|---|---|
| CY7C68013-56PVC | CY7C68013A-56PVXC or CY7C68014A-56PVXC | 56-pin SSOP |
| CY7C68013-56PVCT | CY7C68013A-56PVXCT or CY7C68014A-56PVXCT | 56-pin SSOP – Tape and Reel |
| CY7C68013-56LFC | CY7C68013A-56LFXC or CY7C68014A-56LFXC | 56-pin QFN |
| CY7C68013-100AC | CY7C68013A-100AXC or CY7C68014A-100AXC | 100-pin TQFP |
| CY7C68013-128AC | CY7C68013A-128AXC or CY7C68014A-128AXC | 128-pin TQFP |

## CY7C68013A/14A and CY7C68015A/16A Differences

CY7C68013A is identical to CY7C68014A in form, fit, and functionality. CY7C68015A is identical to CY7C68016A in form, fit, and functionality. CY7C68014A and CY7C68016A have a lower suspend current than CY7C68013A and CY7C68015A respectively and are ideal for power-sensitive battery applications.

CY7C68015A and CY7C68016A are available in 56-pin QFN package only. Two additional GPIO signals are available on the CY7C68015A and CY7C68016A to provide more flexibility when neither IFCLK or CLKOUT are needed in the 56-pin package.

USB developers wanting to convert their FX2 56-pin application to a bus-powered system directly benefit from these additional signals. The two GPIOs give developers the signals they need for the power-control circuitry of their bus-powered application without pushing them to a high-pincount version of FX2LP.

The CY7C68015A is only available in the 56-pin QFN package

**Table 10. CY7C68013A/14A and CY7C68015A/16A Pin Differences**

| CY7C68013A/CY7C68014A | CY7C68015A/CY7C68016A |
|---|---|
| IFCLK | PE0 |
| CLKOUT | PE1 |

## Pin Assignments

Figure 6 on page 19 identifies all signals for the five package types. The following pages illustrate the individual pin diagrams, plus a combination diagram showing which of the full set of signals are available in the 128-pin, 100-pin, and 56-pin packages.

The signals on the left edge of the 56-pin package in Figure 6 on page 19 are common to all versions in the FX2LP family with the noted differences between the CY7C68013A/14A and the CY7C68015A/16A.

Three modes are available in all package versions: Port, GPIF master, and Slave FIFO. These modes define the signals on the right edge of the diagram. The 8051 selects the interface mode using the IFCONFIG[1:0] register bits. Port mode is the power on default configuration.

The 100-pin package adds functionality to the 56-pin package by adding these pins:

- PORTC or alternate GPIFADR[7:0] address signals
- PORTE or alternate GPIFADR[8] address signal and seven additional 8051 signals
- Three GPIF Control signals
- Four GPIF Ready signals
- Nine 8051 signals (two USARTs, three timer inputs, INT4, and INT5#)
- BKPT, RD#, WR#.

The 128-pin package adds the 8051 address and data buses plus control signals. Note that two of the required signals, RD# and WR#, are present in the 100-pin version.

In the 100-pin and 128-pin versions, an 8051 control bit can be set to pulse the RD# and WR# pins when the 8051 reads from/writes to PORTC. This feature is enabled by setting the PORTCSTB bit in the CPUCS register.

PORTC Strobe Feature Timings on page 46 displays the timing diagram of the read and write strobing function on accessing PORTC.

**Figure 6. Signal**

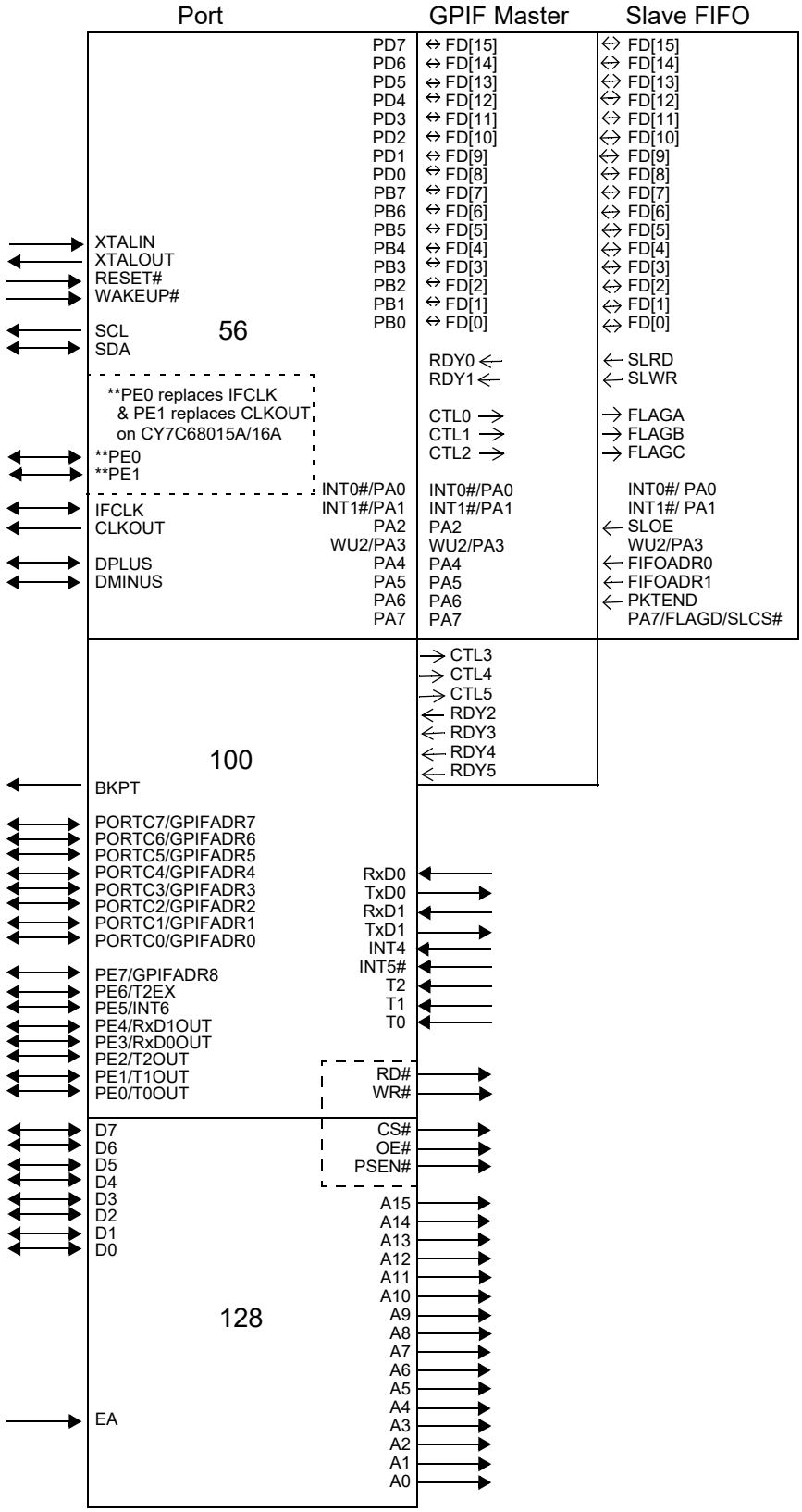
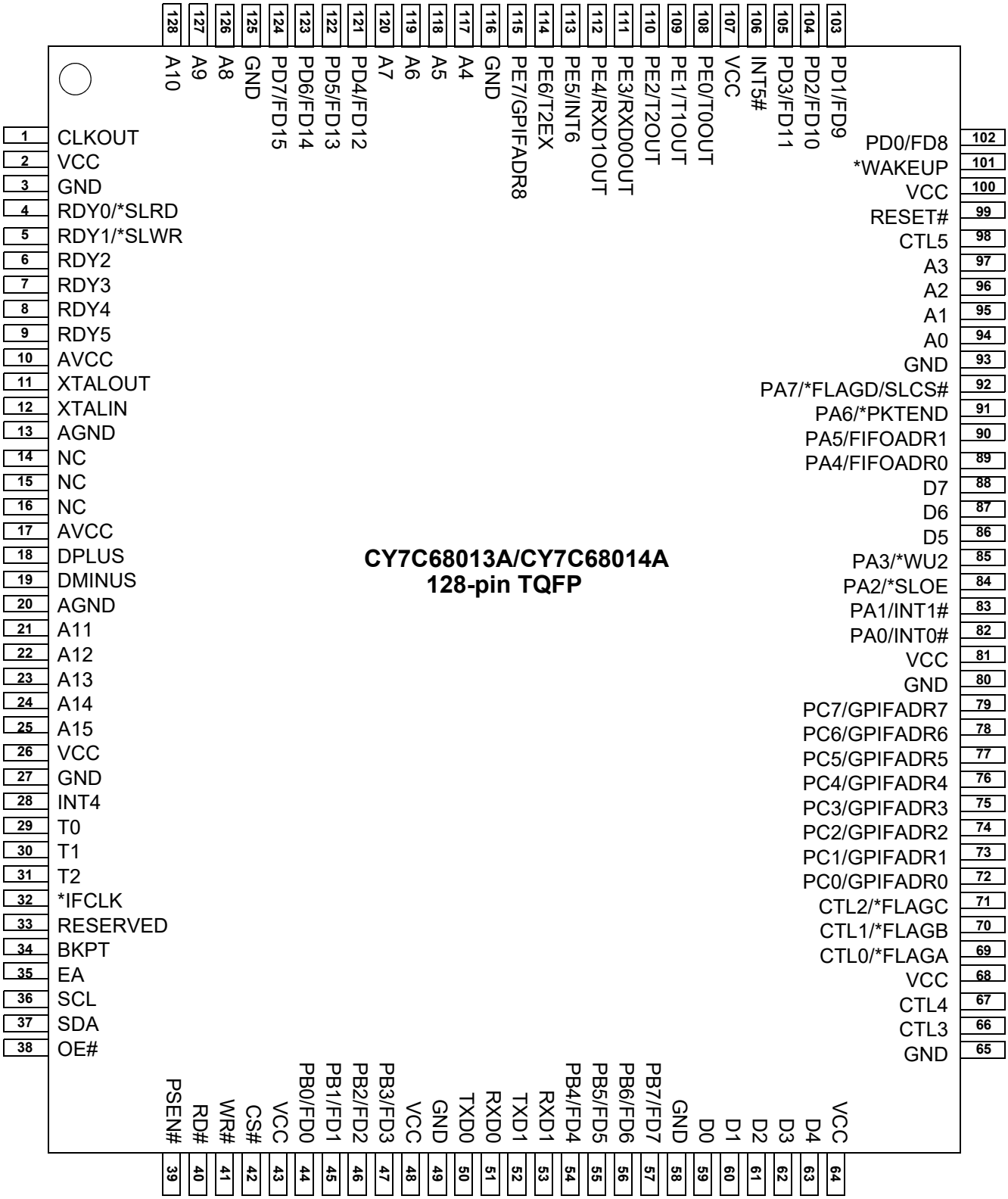
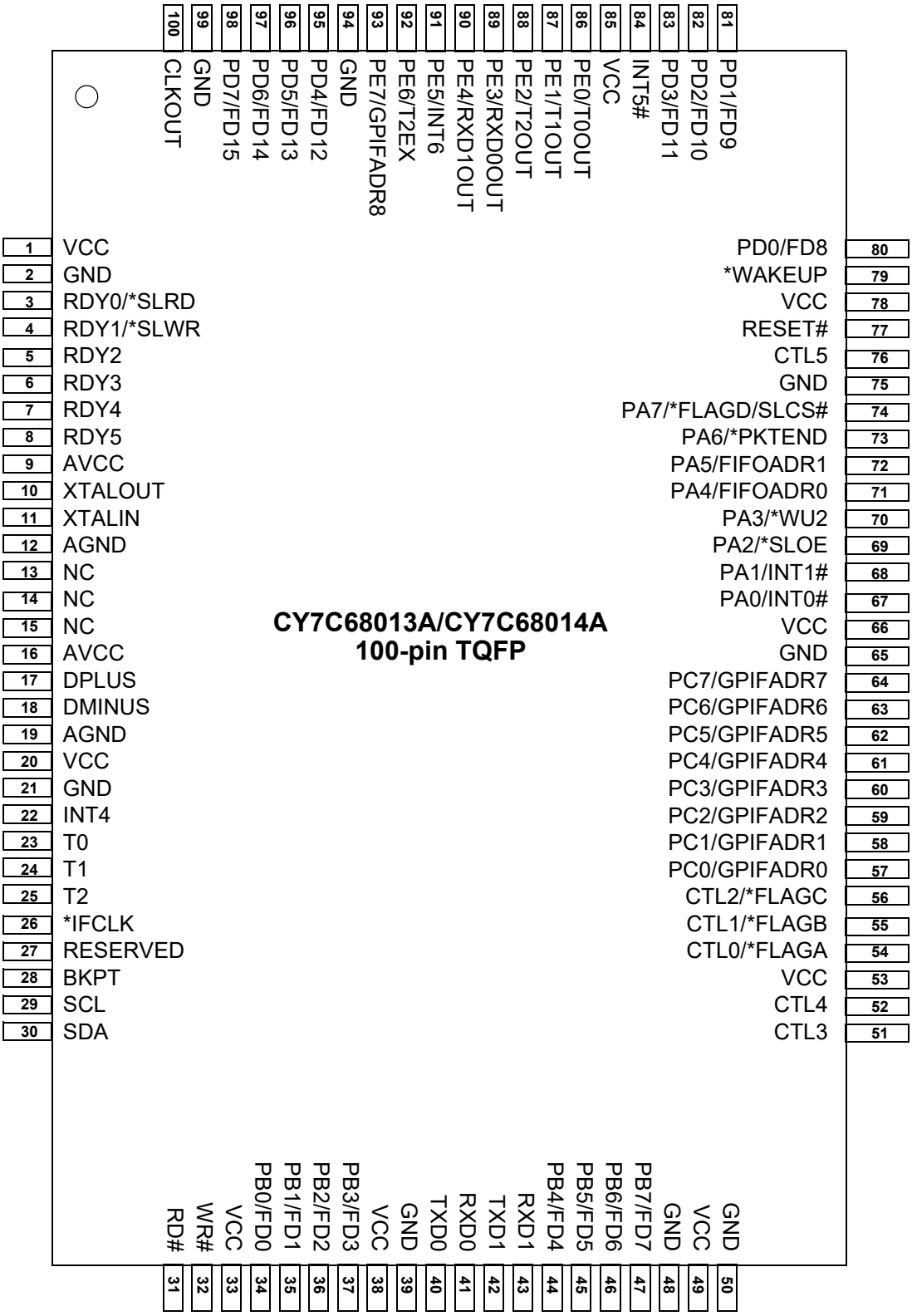


**Figure 7. CY7C68013A/CY7C68014A 128-Pin TQFP Pin Assignment**




* denotes programmable polarity

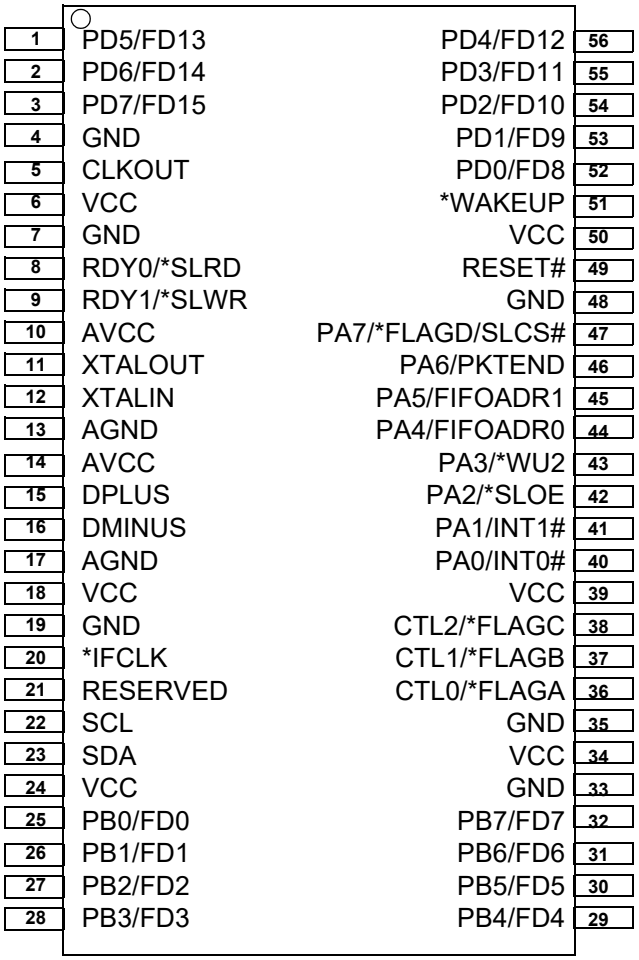
**Figure 8. CY7C68013A/CY7C68014A 100-Pin TQFP Pin Assignment**




* denotes programmable polarity

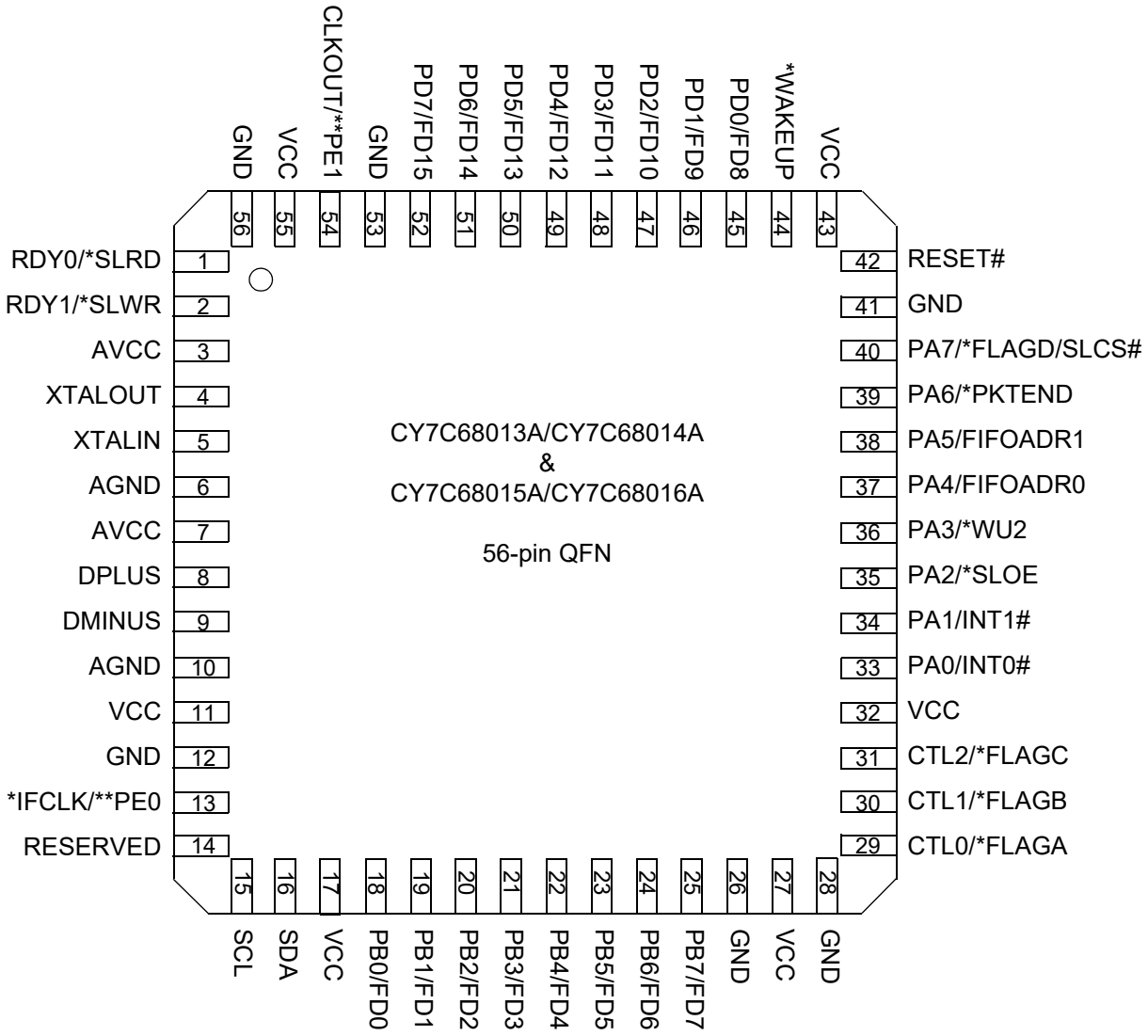
**Figure 9. CY7C68013A/CY7C68014A 56-Pin SSOP Pin Assignment**

**CY7C68013A/CY7C68014A**
**56-pin SSOP**



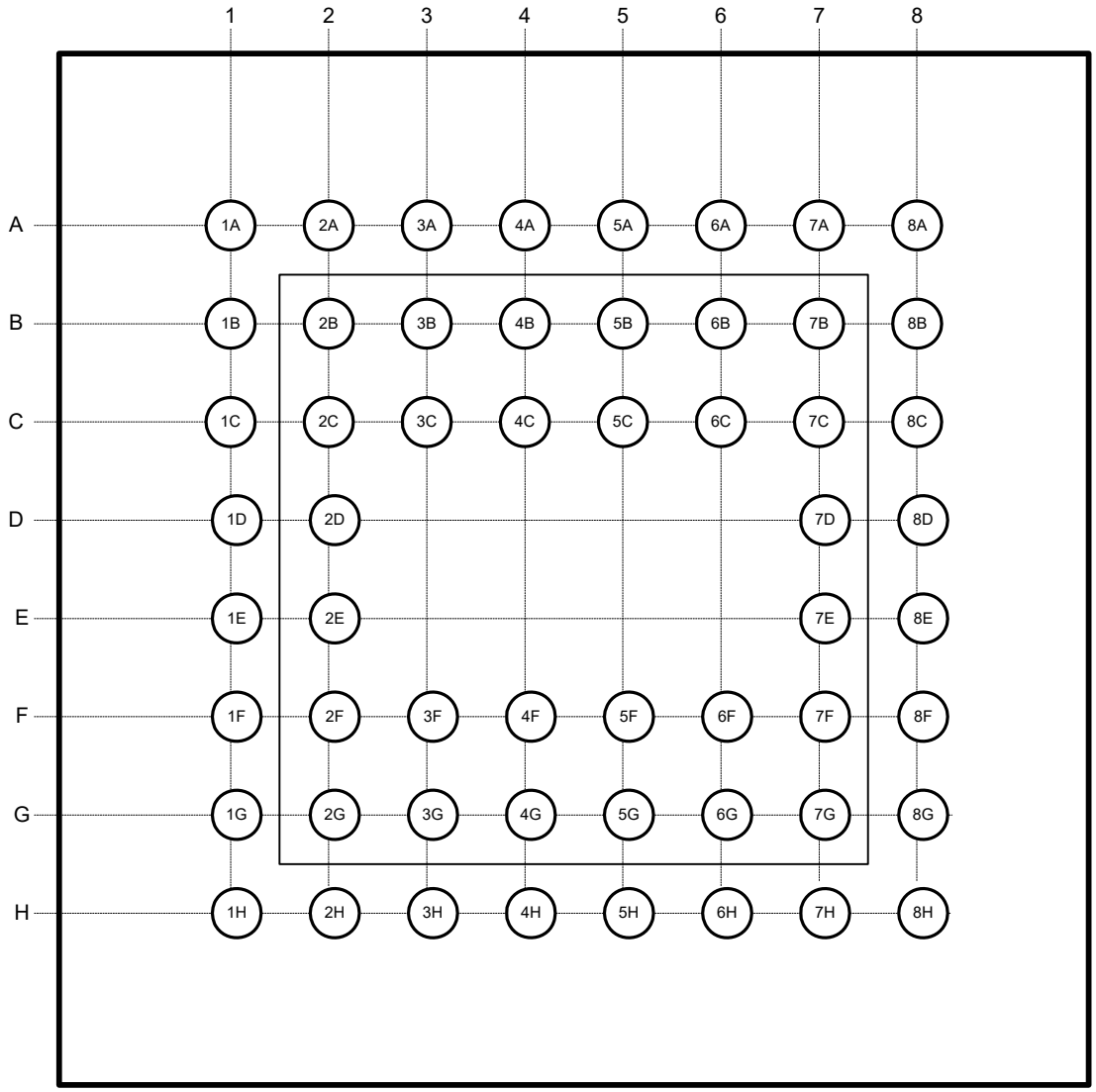

* denotes programmable polarity

**Figure 10. CY7C68013A/14A/15A/16A 56-Pin QFN Pin Assignment**




* denotes programmable polarity
** denotes CY7C68015A/CY7C68016A pinout

**Figure 11. CY7C68013A 56-pin VFBGA Pin Assignment – Top View**



## CY7C68013A/15A Pin Descriptions

**Table 11. FX2LP Pin Descriptions**[13]

| 128 TQFP | 100 TQFP | 56 SSOP | 56 QFN | 56 VFBGA | Name | Type | Default | Reset[14] | Description |
|---|---|---|---|---|---|---|---|---|---|
| 10 | 9 | 10 | 3 | 2D | AVCC | Power | N/A | N/A | **Analog VCC**. Connect this pin to the 3.3 V power source. This signal provides power to the analog section of the chip. |
| 17 | 16 | 14 | 7 | 1D | AVCC | Power | N/A | N/A | **Analog VCC**. Connect this pin to the 3.3 V power source. This signal provides power to the analog section of the chip. |
| 13 | 12 | 13 | 6 | 2F | AGND | Ground | N/A | N/A | **Analog Ground**. Connect to ground with as short a path as possible. |
| 20 | 19 | 17 | 10 | 1F | AGND | Ground | N/A | N/A | **Analog Ground**. Connect to ground with as short a path as possible. |
| 19 | 18 | 16 | 9 | 1E | DMINUS | I/O/Z | Z | N/A | **USB D– Signal**. Connect to the USB D– signal. |
| 18 | 17 | 15 | 8 | 2E | DPLUS | I/O/Z | Z | N/A | **USB D+ Signal**. Connect to the USB D+ signal. |
| 94 | – | – | – | – | A0 | Output | L | L | **8051 Address Bus**. This bus is driven at all times. When the 8051 is addressing internal RAM it reflects the internal address. |
| 95 | – | – | – | – | A1 | Output | L | L | |
| 96 | – | – | – | – | A2 | Output | L | L | |
| 97 | – | – | – | – | A3 | Output | L | L | |
| 117 | – | – | – | – | A4 | Output | L | L | |
| 118 | – | – | – | – | A5 | Output | L | L | |
| 119 | – | – | – | – | A6 | Output | L | L | |
| 120 | – | – | – | – | A7 | Output | L | L | |
| 126 | – | – | – | – | A8 | Output | L | L | |
| 127 | – | – | – | – | A9 | Output | L | L | |
| 128 | – | – | – | – | A10 | Output | L | L | |
| 21 | – | – | – | – | A11 | Output | L | L | |
| 22 | – | – | – | – | A12 | Output | L | L | |
| 23 | – | – | – | – | A13 | Output | L | L | |
| 24 | – | – | – | – | A14 | Output | L | L | |
| 25 | – | – | – | – | A15 | Output | L | L | |
| 59 | – | – | – | – | D0 | I/O/Z | Z | Z | **8051 Data Bus**. This bidirectional bus is high impedance when inactive, input for bus reads, and output for bus writes. The data bus is used for external 8051 program and data memory. The data bus is active only for external bus accesses, and is driven LOW in suspend. |
| 60 | – | – | – | – | D1 | I/O/Z | Z | Z | |
| 61 | – | – | – | – | D2 | I/O/Z | Z | Z | |
| 62 | – | – | – | – | D3 | I/O/Z | Z | Z | |
| 63 | – | – | – | – | D4 | I/O/Z | Z | Z | |
| 86 | – | – | – | – | D5 | I/O/Z | Z | Z | |
| 87 | – | – | – | – | D6 | I/O/Z | Z | Z | |
| 88 | – | – | – | – | D7 | I/O/Z | Z | Z | |
| 39 | – | – | – | – | PSEN# | Output | H | H | **Program Store Enable**. This active LOW signal indicates an 8051 code fetch from external memory. It is active for program memory fetches from 0x4000–0xFFFF when the EA pin is LOW, or from 0x0000–0xFFFF when the EA pin is HIGH. |

**Notes**

13. Unused inputs must not be left floating. Tie either HIGH or LOW as appropriate. Outputs should only be pulled up or down to ensure signals at power up and in standby. Note also that no pins should be driven while the device is powered down.
14. The Reset column indicates the state of signals during reset (RESET# asserted) or during Power on Reset (POR).

**Table 11. FX2LP Pin Descriptions**[13] (continued)

| 128 TQFP | 100 TQFP | 56 SSOP | 56 QFN | 56 VFBGA | Name | Type | Default | Reset[14] | Description |
|---|---|---|---|---|---|---|---|---|---|
| 34 | 28 | – | – | | BKPT | Output | L | L | **Breakpoint**. This pin goes active (HIGH) when the 8051 address bus matches the BPADDRH/L registers and breakpoints are enabled in the BREAKPT register (BPEN = 1). If the BPPULSE bit in the BREAKPT register is HIGH, this signal pulses HIGH for eight 12-/24-/48-MHz clocks. If the BPPULSE bit is LOW, the signal remains HIGH until the 8051 clears the BREAK bit (by writing 1 to it) in the BREAKPT register. |
| 99 | 77 | 49 | 42 | 8B | RESET# | Input | N/A | N/A | **Active LOW Reset**. Resets the entire chip. See section "Reset and Wakeup" on page 9 for more details. |
| 35 | – | – | – | – | EA | Input | N/A | N/A | **External Access**. This pin determines where the 8051 fetches code between addresses 0x0000 and 0x3FFF. If EA = 0 the 8051 fetches this code from its internal RAM. IF EA = 1 the 8051 fetches this code from external memory. |
| 12 | 11 | 12 | 5 | 1C | XTALIN | Input | N/A | N/A | **Crystal Input**. Connect this signal to a 24-MHz parallel-resonant, fundamental mode crystal and load capacitor to GND.<br>It is also correct to drive XTALIN with an external 24-MHz square wave derived from another clock source. When driving from an external source, the driving signal should be a 3.3-V square wave. |
| 11 | 10 | 11 | 4 | 2C | XTALOUT | Output | N/A | N/A | **Crystal Output**. Connect this signal to a 24-MHz parallel-resonant, fundamental mode crystal and load capacitor to GND.<br>If an external clock is used to drive XTALIN, leave this pin open. |
| 1 | 100 | 5 | 54 | 2B | CLKOUT on CY7C68013A and CY7C68014A<br>----------<br>PE1 on CY7C68015A and CY7C68016A | O/Z<br>----------<br>I/O/Z | 12 MHz<br>----------<br>I | Clock Driven<br>----------<br>Z | **CLKOUT:** 12-, 24- or 48-MHz clock, phase-locked to the 24-MHz input clock. The 8051 defaults to 12-MHz operation. The 8051 may three-state this output by setting CPUCS.1 = 1.<br>----------<br>------**PE1** is a bidirectional I/O port pin. |
| **Port A** | | | | | | | | | |
| 82 | 67 | 40 | 33 | 8G | PA0 or INT0# | I/O/Z | I (PA0) | Z (PA0) | Multiplexed pin whose function is selected by PORTACFG.0<br>**PA0** is a bidirectional I/O port pin.<br>**INT0#** is the active-LOW 8051 INT0 interrupt input signal, which is either edge-triggered (IT0 = 1) or level-triggered (IT0 = 0). |
| 83 | 68 | 41 | 34 | 6G | PA1 or INT1# | I/O/Z | I (PA1) | Z (PA1) | Multiplexed pin whose function is selected by: PORTACFG.1<br>**PA1** is a bidirectional I/O port pin.<br>**INT1#** is the active-LOW 8051 INT1 interrupt input signal, which is either edge-triggered (IT1 = 1) or level-triggered (IT1 = 0). |

**Table 11. FX2LP Pin Descriptions**[13] (continued)

| 128 TQFP | 100 TQFP | 56 SSOP | 56 QFN | 56 VFBGA | Name | Type | Default | Reset[14] | Description |
|---|---|---|---|---|---|---|---|---|---|
| 84 | 69 | 42 | 35 | 8F | PA2 or SLOE | I/O/Z | I (PA2) | Z (PA2) | Multiplexed pin whose function is selected by two bits: IFCONFIG[1:0]. **PA2** is a bidirectional I/O port pin. **SLOE** is an input-only output enable with programmable polarity (FIFOPINPOLAR.4) for the slave FIFOs connected to FD[7..0] or FD[15..0]. |
| 85 | 70 | 43 | 36 | 7F | PA3 or WU2 | I/O/Z | I (PA3) | Z (PA3) | Multiplexed pin whose function is selected by: WAKEUP.7 and OEA.3 **PA3** is a bidirectional I/O port pin. **WU2** is an alternate source for **USB Wakeup,** enabled by WU2EN bit (WAKEUP.1) and polarity set by WU2POL (WAKEUP.4). If the 8051 is in suspend and WU2EN = 1, a transition on this pin starts up the oscillator and interrupts the 8051 to enable it to exit the suspend mode. Asserting this pin inhibits the chip from suspending if WU2EN = 1. |
| 89 | 71 | 44 | 37 | 6F | PA4 or FIFOADR0 | I/O/Z | I (PA4) | Z (PA4) | Multiplexed pin whose function is selected by: IFCONFIG[1..0]. **PA4** is a bidirectional I/O port pin. **FIFOADR0** is an input-only address select for the slave FIFOs connected to FD[7..0] or FD[15..0]. |
| 90 | 72 | 45 | 38 | 8C | PA5 or FIFOADR1 | I/O/Z | I (PA5) | Z (PA5) | Multiplexed pin whose function is selected by: IFCONFIG[1..0]. **PA5** is a bidirectional I/O port pin. **FIFOADR1** is an input-only address select for the slave FIFOs connected to FD[7..0] or FD[15..0]. |
| 91 | 73 | 46 | 39 | 7C | PA6 or PKTEND | I/O/Z | I (PA6) | Z (PA6) | Multiplexed pin whose function is selected by the IFCONFIG[1:0] bits. **PA6** is a bidirectional I/O port pin. **PKTEND** is an input used to commit the FIFO packet data to the endpoint and whose polarity is programmable via FIFOPINPOLAR.5. |
| 92 | 74 | 47 | 40 | 6C | PA7 or FLAGD or SLCS# | I/O/Z | I (PA7) | Z (PA7) | Multiplexed pin whose function is selected by the IFCONFIG[1:0] and PORTACFG.7 bits. **PA7** is a bidirectional I/O port pin. **FLAGD** is a programmable slave-FIFO output status flag signal. **SLCS#** gates all other slave FIFO enable/strobes |
| **Port B** | | | | | | | | | |
| 44 | 34 | 25 | 18 | 3H | PB0 or FD[0] | I/O/Z | I (PB0) | Z (PB0) | Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB0** is a bidirectional I/O port pin. **FD[0]** is the bidirectional FIFO/GPIF data bus. |
| 45 | 35 | 26 | 19 | 4F | PB1 or FD[1] | I/O/Z | I (PB1) | Z (PB1) | Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB1** is a bidirectional I/O port pin. **FD[1]** is the bidirectional FIFO/GPIF data bus. |
| 46 | 36 | 27 | 20 | 4H | PB2 or FD[2] | I/O/Z | I (PB2) | Z (PB2) | Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB2** is a bidirectional I/O port pin. **FD[2]** is the bidirectional FIFO/GPIF data bus. |

**Table 11. FX2LP Pin Descriptions**[13] (continued)

| 128 TQFP | 100 TQFP | 56 SSOP | 56 QFN | 56 VFBGA | Name | Type | Default | Reset[14] | Description |
|---|---|---|---|---|---|---|---|---|---|
| 47 | 37 | 28 | 21 | 4G | PB3 or FD[3] | I/O/Z | I (PB3) | Z (PB3) | Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0].<br>**PB3** is a bidirectional I/O port pin.<br>**FD[3]** is the bidirectional FIFO/GPIF data bus. |
| 54 | 44 | 29 | 22 | 5H | PB4 or FD[4] | I/O/Z | I (PB4) | Z (PB4) | Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0].<br>**PB4** is a bidirectional I/O port pin.<br>**FD[4]** is the bidirectional FIFO/GPIF data bus. |
| 55 | 45 | 30 | 23 | 5G | PB5 or FD[5] | I/O/Z | I (PB5) | Z (PB5) | Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0].<br>**PB5** is a bidirectional I/O port pin.<br>**FD[5]** is the bidirectional FIFO/GPIF data bus. |
| 56 | 46 | 31 | 24 | 5F | PB6 or FD[6] | I/O/Z | I (PB6) | Z (PB6) | Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0].<br>**PB6** is a bidirectional I/O port pin.<br>**FD[6]** is the bidirectional FIFO/GPIF data bus. |
| 57 | 47 | 32 | 25 | 6H | PB7 or FD[7] | I/O/Z | I (PB7) | Z (PB7) | Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0].<br>**PB7** is a bidirectional I/O port pin.<br>**FD[7]** is the bidirectional FIFO/GPIF data bus. |
| **PORT C** | | | | | | | | | |
| 72 | 57 | – | – | – | PC0 or GPIFADR0 | I/O/Z | I (PC0) | Z (PC0) | Multiplexed pin whose function is selected by PORTCCFG.0<br>**PC0** is a bidirectional I/O port pin.<br>**GPIFADR0** is a GPIF address output pin. |
| 73 | 58 | – | – | – | PC1 or GPIFADR1 | I/O/Z | I (PC1) | Z (PC1) | Multiplexed pin whose function is selected by PORTCCFG.1<br>**PC1** is a bidirectional I/O port pin.<br>**GPIFADR1** is a GPIF address output pin. |
| 74 | 59 | – | – | – | PC2 or GPIFADR2 | I/O/Z | I (PC2) | Z (PC2) | Multiplexed pin whose function is selected by PORTCCFG.2<br>**PC2** is a bidirectional I/O port pin.<br>**GPIFADR2** is a GPIF address output pin. |
| 75 | 60 | – | – | – | PC3 or GPIFADR3 | I/O/Z | I (PC3) | Z (PC3) | Multiplexed pin whose function is selected by PORTCCFG.3<br>**PC3** is a bidirectional I/O port pin.<br>**GPIFADR3** is a GPIF address output pin. |
| 76 | 61 | – | – | – | PC4 or GPIFADR4 | I/O/Z | I (PC4) | Z (PC4) | Multiplexed pin whose function is selected by PORTCCFG.4<br>**PC4** is a bidirectional I/O port pin.<br>**GPIFADR4** is a GPIF address output pin. |
| 77 | 62 | – | – | – | PC5 or GPIFADR5 | I/O/Z | I (PC5) | Z (PC5) | Multiplexed pin whose function is selected by PORTCCFG.5<br>**PC5** is a bidirectional I/O port pin.<br>**GPIFADR5** is a GPIF address output pin. |
| 78 | 63 | – | – | – | PC6 or GPIFADR6 | I/O/Z | I (PC6) | Z (PC6) | Multiplexed pin whose function is selected by PORTCCFG.6<br>**PC6** is a bidirectional I/O port pin.<br>**GPIFADR6** is a GPIF address output pin. |
| 79 | 64 | – | – | – | PC7 or GPIFADR7 | I/O/Z | I (PC7) | Z (PC7) | Multiplexed pin whose function is selected by PORTCCFG.7<br>**PC7** is a bidirectional I/O port pin.<br>**GPIFADR7** is a GPIF address output pin. |

**Table 11. FX2LP Pin Descriptions**[13] (continued)

| 128 TQFP | 100 TQFP | 56 SSOP | 56 QFN | 56 VFBGA | Name | Type | Default | Reset[14] | Description |
|---|---|---|---|---|---|---|---|---|---|
| **PORT D** | | | | | | | | | |
| 102 | 80 | 52 | 45 | 8A | PD0 or FD[8] | I/O/Z | I (PD0) | Z (PD0) | Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[8]** is the bidirectional FIFO/GPIF data bus. |
| 103 | 81 | 53 | 46 | 7A | PD1 or FD[9] | I/O/Z | I (PD1) | Z (PD1) | Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[9]** is the bidirectional FIFO/GPIF data bus. |
| 104 | 82 | 54 | 47 | 6B | PD2 or FD[10] | I/O/Z | I (PD2) | Z (PD2) | Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[10]** is the bidirectional FIFO/GPIF data bus. |
| 105 | 83 | 55 | 48 | 6A | PD3 or FD[11] | I/O/Z | I (PD3) | Z (PD3) | Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[11]** is the bidirectional FIFO/GPIF data bus. |
| 121 | 95 | 56 | 49 | 3B | PD4 or FD[12] | I/O/Z | I (PD4) | Z (PD4) | Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[12]** is the bidirectional FIFO/GPIF data bus. |
| 122 | 96 | 1 | 50 | 3A | PD5 or FD[13] | I/O/Z | I (PD5) | Z (PD5) | Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[13]** is the bidirectional FIFO/GPIF data bus. |
| 123 | 97 | 2 | 51 | 3C | PD6 or FD[14] | I/O/Z | I (PD6) | Z (PD6) | Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[14]** is the bidirectional FIFO/GPIF data bus. |
| 124 | 98 | 3 | 52 | 2A | PD7 or FD[15] | I/O/Z | I (PD7) | Z (PD7) | Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[15]** is the bidirectional FIFO/GPIF data bus. |
| **Port E** | | | | | | | | | |
| 108 | 86 | – | – | – | PE0 or T0OUT | I/O/Z | I (PE0) | Z (PE0) | Multiplexed pin whose function is selected by the PORTECFG.0 bit. **PE0** is a bidirectional I/O port pin. **T0OUT** is an active-HIGH signal from 8051 Timer-counter0. T0OUT outputs a high level for one CLKOUT clock cycle when Timer0 overflows. If Timer0 is operated in Mode 3 (two separate timer/counters), T0OUT is active when the low byte timer/counter overflows. |
| 109 | 87 | – | – | – | PE1 or T1OUT | I/O/Z | I (PE1) | Z (PE1) | Multiplexed pin whose function is selected by the PORTECFG.1 bit. **PE1** is a bidirectional I/O port pin. **T1OUT** is an active HIGH signal from 8051 Timer-counter1. T1OUT outputs a high level for one CLKOUT clock cycle when Timer1 overflows. If Timer1 is operated in Mode 3 (two separate timer/counters), T1OUT is active when the low byte timer/counter overflows. |

**Table 11. FX2LP Pin Descriptions**[13] (continued)

| 128 TQFP | 100 TQFP | 56 SSOP | 56 QFN | 56 VFBGA | Name | Type | Default | Reset[14] | Description |
|---|---|---|---|---|---|---|---|---|---|
| 110 | 88 | – | – | – | PE2 or T2OUT | I/O/Z | I (PE2) | Z (PE2) | Multiplexed pin whose function is selected by the PORTECFG.2 bit.<br>**PE2** is a bidirectional I/O port pin.<br>**T2OUT** is the active HIGH output signal from 8051 Timer2. T2OUT is active (HIGH) for one clock cycle when Timer/Counter 2 overflows. |
| 111 | 89 | – | – | – | PE3 or RXD0OUT | I/O/Z | I (PE3) | Z (PE3) | Multiplexed pin whose function is selected by the PORTECFG.3 bit.<br>**PE3** is a bidirectional I/O port pin.<br>**RXD0OUT** is an active HIGH signal from 8051 UART0. If RXD0OUT is selected and UART0 is in Mode 0, this pin provides the output data for UART0 only when it is in sync mode. Otherwise it is a 1. |
| 112 | 90 | – | – | – | PE4 or RXD1OUT | I/O/Z | I (PE4) | Z (PE4) | Multiplexed pin whose function is selected by the PORTECFG.4 bit.<br>**PE4** is a bidirectional I/O port pin.<br>**RXD1OUT** is an active-HIGH output from 8051 UART1. When RXD1OUT is selected and UART1 is in Mode 0, this pin provides the output data for UART1 only when it is in sync mode. In Modes 1, 2, and 3, this pin is HIGH. |
| 113 | 91 | – | – | – | PE5 or INT6 | I/O/Z | I (PE5) | Z (PE5) | Multiplexed pin whose function is selected by the PORTECFG.5 bit.<br>**PE5** is a bidirectional I/O port pin.<br>**INT6** is the 8051 INT6 interrupt request input signal. The INT6 pin is edge-sensitive, active HIGH. |
| 114 | 92 | – | – | – | PE6 or T2EX | I/O/Z | I (PE6) | Z (PE6) | Multiplexed pin whose function is selected by the PORTECFG.6 bit.<br>**PE6** is a bidirectional I/O port pin.<br>**T2EX** is an active HIGH input signal to the 8051 Timer2. T2EX reloads timer 2 on its falling edge. T2EX is active only if the EXEN2 bit is set in T2CON. |
| 115 | 93 | – | – | – | PE7 or GPIFADR8 | I/O/Z | I (PE7) | Z (PE7) | Multiplexed pin whose function is selected by the PORTECFG.7 bit.<br>**PE7** is a bidirectional I/O port pin.<br>**GPIFADR8** is a GPIF address output pin. |
| 4 | 3 | 8 | 1 | 1A | RDY0 or SLRD | Input | N/A | N/A | Multiplexed pin whose function is selected by the following bits:<br>IFCONFIG[1..0].<br>**RDY0** is a GPIF input signal.<br>**SLRD** is the input-only read strobe with programmable polarity (FIFOPINPOLAR.3) for the slave FIFOs connected to FD[7..0] or FD[15..0]. |
| 5 | 4 | 9 | 2 | 1B | RDY1 or SLWR | Input | N/A | N/A | Multiplexed pin whose function is selected by the following bits:<br>IFCONFIG[1..0].<br>**RDY1** is a GPIF input signal.<br>**SLWR** is the input-only write strobe with programmable polarity (FIFOPINPOLAR.2) for the slave FIFOs connected to FD[7..0] or FD[15..0]. |
| 6 | 5 | – | – | – | RDY2 | Input | N/A | N/A | **RDY2** is a GPIF input signal. |

**Table 11. FX2LP Pin Descriptions**[13] (continued)

| 128 TQFP | 100 TQFP | 56 SSOP | 56 QFN | 56 VFBGA | Name | Type | Default | Reset[14] | Description |
|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | – | – | – | RDY3 | Input | N/A | N/A | **RDY3** is a GPIF input signal. |
| 8 | 7 | – | – | – | RDY4 | Input | N/A | N/A | **RDY4** is a GPIF input signal. |
| 9 | 8 | – | – | – | RDY5 | Input | N/A | N/A | **RDY5** is a GPIF input signal. |
| 69 | 54 | 36 | 29 | 7H | CTL0 or FLAGA | O/Z | H | L | Multiplexed pin whose function is selected by the following bits:<br>IFCONFIG[1..0].<br>**CTL0** is a GPIF control output.<br>**FLAGA** is a programmable slave-FIFO output status flag signal.<br>Defaults to programmable for the FIFO selected by the FIFOADR[1:0] pins. |
| 70 | 55 | 37 | 30 | 7G | CTL1 or FLAGB | O/Z | H | L | Multiplexed pin whose function is selected by the following bits:<br>IFCONFIG[1..0].<br>**CTL1** is a GPIF control output.<br>**FLAGB** is a programmable slave-FIFO output status flag signal.<br>Defaults to FULL for the FIFO selected by the FIFOADR[1:0] pins. |
| 71 | 56 | 38 | 31 | 8H | CTL2 or FLAGC | O/Z | H | L | Multiplexed pin whose function is selected by the following bits:<br>IFCONFIG[1..0].<br>**CTL2** is a GPIF control output.<br>**FLAGC** is a programmable slave-FIFO output status flag signal.<br>Defaults to EMPTY for the FIFO selected by the FIFOADR[1:0] pins. |
| 66 | 51 | – | – | – | CTL3 | O/Z | H | L | **CTL3** is a GPIF control output. |
| 67 | 52 | – | – | – | CTL4 | Output | H | L | **CTL4** is a GPIF control output. |
| 98 | 76 | – | – | – | CTL5 | Output | H | L | **CTL5** is a GPIF control output. |
| 32 | 26 | 20 | 13 | 2G | IFCLK on CY7C68013A and CY7C68014A<br>----------<br>PE0 on CY7C68015A and CY7C68016A | I/O/Z<br>----------<br>– I/O/Z | Z<br>----------<br>I | Z<br>----------<br>Z | Interface Clock, used for synchronously clocking data into or out of the slave FIFOs. IFCLK also serves as a timing reference for all slave FIFO control signals and GPIF. When internal clocking is used (IFCONFIG.7 = 1) the IFCLK pin can be configured to output 30/48 MHz by bits IFCONFIG.5 and IFCONFIG.6. IFCLK may be inverted, whether internally or externally sourced, by setting the bit IFCONFIG.4 =1.<br>----------<br>**PE0** is a bidirectional I/O port pin. |
| 28 | 22 | – | – | – | INT4 | Input | N/A | N/A | **INT4** is the 8051 INT4 interrupt request input signal. The INT4 pin is edge-sensitive, active HIGH. |
| 106 | 84 | – | – | – | INT5# | Input | N/A | N/A | **INT5#** is the 8051 INT5 interrupt request input signal. The INT5 pin is edge-sensitive, active LOW. |
| 31 | 25 | – | – | – | T2 | Input | N/A | N/A | **T2** is the active HIGH T2 input signal to 8051 Timer2, which provides the input to Timer2 when C/T2 = 1. When C/T2 = 0, Timer2 does not use this pin. |

**Table 11. FX2LP Pin Descriptions**[13] (continued)

| 128 TQFP | 100 TQFP | 56 SSOP | 56 QFN | 56 VFBGA | Name | Type | Default | Reset[14] | Description |
|---|---|---|---|---|---|---|---|---|---|
| 30 | 24 | – | – | – | T1 | Input | N/A | N/A | **T1** is the active HIGH T1 signal for 8051 Timer1, which provides the input to Timer1 when C/T1 is 1. When C/T1 is 0, Timer1 does not use this bit. |
| 29 | 23 | – | – | – | T0 | Input | N/A | N/A | **T0** is the active HIGH T0 signal for 8051 Timer0, which provides the input to Timer0 when C/T0 is 1. When C/T0 is 0, Timer0 does not use this bit. |
| 53 | 43 | – | – | – | RXD1 | Input | N/A | N/A | **RXD1**is an active HIGH input signal for 8051 UART1, which provides data to the UART in all modes. |
| 52 | 42 | – | – | – | TXD1 | Output | H | L | **TXD1**is an active HIGH output pin from 8051 UART1, which provides the output clock in sync mode, and the output data in async mode. |
| 51 | 41 | – | – | – | RXD0 | Input | N/A | N/A | **RXD0** is the active HIGH RXD0 input to 8051 UART0, which provides data to the UART in all modes. |
| 50 | 40 | – | – | – | TXD0 | Output | H | L | **TXD0** is the active HIGH TXD0 output from 8051 UART0, which provides the output clock in sync mode, and the output data in async mode. |
| 42 | | – | – | – | CS# | Output | H | H | **CS#** is the active LOW chip select for external memory. |
| 41 | 32 | – | – | – | WR# | Output | H | H | **WR#** is the active LOW write strobe output for external memory. |
| 40 | 31 | – | – | – | RD# | Output | H | H | **RD#** is the active LOW read strobe output for external memory. |
| 38 | | – | – | – | OE# | Output | H | H | **OE#** is the active LOW output enable for external memory. |
| | | | | | | | | | |
| 33 | 27 | 21 | 14 | 2H | Reserved | Input | N/A | N/A | **Reserved**. Connect to ground. |
| | | | | | | | | | |
| 101 | 79 | 51 | 44 | 7B | WAKEUP | Input | N/A | N/A | **USB Wakeup**. If the 8051 is in suspend, asserting this pin starts up the oscillator and interrupts the 8051 to enable it to exit the suspend mode. Holding WAKEUP asserted inhibits the EZ-USB chip from suspending. This pin has programmable polarity (WAKEUP.4). |
| 36 | 29 | 22 | 15 | 3F | SCL | OD | Z | Z (if booting is done) | **Clock** for the $I^2C$ interface. Connect to VCC with a 2.2-kΩ resistor, even if no $I^2C$ peripheral is attached. |
| 37 | 30 | 23 | 16 | 3G | SDA | OD | Z | Z (if booting is done) | **Data** for **$I^2C$ compatible interface**. Connect to VCC with a 2.2-kΩ resistor, **even if no $I^2C$ compatible peripheral is attached**. |
| | | | | | | | | | |
| 2 | 1 | 6 | 55 | 5A | VCC | Power | N/A | N/A | **VCC**. Connect to the 3.3-V power source. |
| 26 | 20 | 18 | 11 | 1G | VCC | Power | N/A | N/A | **VCC**. Connect to the 3.3-V power source. |
| 43 | 33 | 24 | 17 | 7E | VCC | Power | N/A | N/A | **VCC**. Connect to the 3.3-V power source. |
| 48 | 38 | – | – | – | VCC | Power | N/A | N/A | **VCC**. Connect to 3.3-V power source. |
| 64 | 49 | 34 | 27 | 8E | VCC | Power | N/A | N/A | **VCC**. Connect to the 3.3-V power source. |
| 68 | 53 | – | – | – | VCC | Power | N/A | N/A | **VCC**. Connect to the 3.3-V power source. |
| 81 | 66 | 39 | 32 | 5C | VCC | Power | N/A | N/A | **VCC**. Connect to the 3.3-V power source. |

**Table 11. FX2LP Pin Descriptions**[13] (continued)

| 128 TQFP | 100 TQFP | 56 SSOP | 56 QFN | 56 VFBGA | Name | Type | Default | Reset[14] | Description |
|---|---|---|---|---|---|---|---|---|---|
| 100 | 78 | 50 | 43 | 5B | VCC | Power | N/A | N/A | **VCC**. Connect to the 3.3-V power source. |
| 107 | 85 | – | – | – | VCC | Power | N/A | N/A | **VCC**. Connect to the 3.3-V power source. |
| 3 | 2 | 7 | 56 | 4B | GND | Ground | N/A | N/A | **Ground** |
| 27 | 21 | 19 | 12 | 1H | GND | Ground | N/A | N/A | **Ground** |
| 49 | 39 | – | – | – | GND | Ground | N/A | N/A | **Ground** |
| 58 | 48 | 33 | 26 | 7D | GND | Ground | N/A | N/A | **Ground** |
| 65 | 50 | 35 | 28 | 8D | GND | Ground | N/A | N/A | **Ground** |
| 80 | 65 | – | – | – | GND | Ground | N/A | N/A | **Ground** |
| 93 | 75 | 48 | 41 | 4C | GND | Ground | N/A | N/A | **Ground** |
| 116 | 94 | – | – | – | GND | Ground | N/A | N/A | **Ground** |
| 125 | 99 | 4 | 53 | 4A | GND | Ground | N/A | N/A | **Ground** |
| | | | | | | | | | |
| 14 | 13 | – | – | – | NC | N/A | N/A | N/A | **No Connect**. This pin must be left open. |
| 15 | 14 | – | – | – | NC | N/A | N/A | N/A | **No Connect**. This pin must be left open. |
| 16 | 15 | – | – | – | NC | N/A | N/A | N/A | **No Connect**. This pin must be left open. |

## Register Summary

FX2LP register bit definitions are described in the FX2LP TRM in greater detail.

### Table 12. FX2LP Register Summary

| Hex | Size | Name | Description | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Default | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | GPIF Waveform Memories | | | | | | | | | | | |
| E400 | 128 | WAVEDATA | GPIF Waveform Descriptor 0, 1, 2, 3 data | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| E480 | 128 | reserved | | | | | | | | | | | |
| | | GENERAL CONFIGURATION | | | | | | | | | | | |
| E50D | | GPCR2 | General Purpose Configuration Register 2 | reserved | reserved | reserved | FULL_SPEED_ONLY | reserved | reserved | reserved | reserved | 00000000 | R |
| E600 | 1 | CPUCS | CPU Control & Status | 0 | 0 | PORTCSTB | CLKSPD1 | CLKSPD0 | CLKINV | CLKOE | 8051RES | 00000010 | rrbbbbbr |
| E601 | 1 | IFCONFIG | Interface Configuration (Ports, GPIF, slave FIFOs) | IFCLKSRC | 3048MHZ | IFCLKOE | IFCLKPOL | ASYNC | GSTATE | IFCFG1 | IFCFG0 | 10000000 | RW |
| E602 | 1 | PINFLAGSAB[15] | Slave FIFO FLAGA and FLAGB Pin Configuration | FLAGB3 | FLAGB2 | FLAGB1 | FLAGB0 | FLAGA3 | FLAGA2 | FLAGA1 | FLAGA0 | 00000000 | RW |
| E603 | 1 | PINFLAGSCD[15] | Slave FIFO FLAGC and FLAGD Pin Configuration | FLAGD3 | FLAGD2 | FLAGD1 | FLAGD0 | FLAGC3 | FLAGC2 | FLAGC1 | FLAGC0 | 00000000 | RW |
| E604 | 1 | FIFORESET[15] | Restore FIFOS to default state | NAKALL | 0 | 0 | 0 | EP3 | EP2 | EP1 | EP0 | xxxxxxxx | W |
| E605 | 1 | BREAKPT | Breakpoint Control | 0 | 0 | 0 | 0 | BREAK | BPPULSE | BPEN | 0 | 00000000 | rrrrbbbr |
| E606 | 1 | BPADDRH | Breakpoint Address H | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | xxxxxxxx | RW |
| E607 | 1 | BPADDRL | Breakpoint Address L | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | xxxxxxxx | RW |
| E608 | 1 | UART230 | 230 Kbaud internally generated ref. clock | 0 | 0 | 0 | 0 | 0 | 0 | 230UART1 | 230UART0 | 00000000 | rrrrrrbb |
| E609 | 1 | FIFOPINPOLAR[15] | Slave FIFO Interface pins polarity | 0 | 0 | PKTEND | SLOE | SLRD | SLWR | EF | FF | 00000000 | rrbbbbbb |
| E60A | 1 | REVID | Chip Revision | rv7 | rv6 | rv5 | rv4 | rv3 | rv2 | rv1 | rv0 | RevA 00000001 | R |
| E60B | 1 | REVCTL[15] | Chip Revision Control | 0 | 0 | 0 | 0 | 0 | 0 | dyn_out | enh_pkt | 00000000 | rrrrrrbb |
| | | UDMA | | | | | | | | | | | |
| E60C | 1 | GPIFHOLDAMOUNT | MSTB Hold Time (for UDMA) | 0 | 0 | 0 | 0 | 0 | 0 | HOLDTIME1 | HOLDTIME0 | 00000000 | rrrrrrbb |
| | 3 | reserved | | | | | | | | | | | |
| | | ENDPOINT CONFIGURATION | | | | | | | | | | | |
| E610 | 1 | EP1OUTCFG | Endpoint 1-OUT Configuration | VALID | 0 | TYPE1 | TYPE0 | 0 | 0 | 0 | 0 | 10100000 | brbbrrrr |
| E611 | 1 | EP1INCFG | Endpoint 1-IN Configuration | VALID | 0 | TYPE1 | TYPE0 | 0 | 0 | 0 | 0 | 10100000 | brbbrrrr |
| E612 | 1 | EP2CFG | Endpoint 2 Configuration | VALID | DIR | TYPE1 | TYPE0 | SIZE | 0 | BUF1 | BUF0 | 10100010 | bbbbbrbb |
| E613 | 1 | EP4CFG | Endpoint 4 Configuration | VALID | DIR | TYPE1 | TYPE0 | 0 | 0 | 0 | 0 | 10100000 | bbbbrrrr |
| E614 | 1 | EP6CFG | Endpoint 6 Configuration | VALID | DIR | TYPE1 | TYPE0 | SIZE | 0 | BUF1 | BUF0 | 11100010 | bbbbbrbb |
| E615 | 1 | EP8CFG | Endpoint 8 Configuration | VALID | DIR | TYPE1 | TYPE0 | 0 | 0 | 0 | 0 | 11100000 | bbbbrrrr |
| | 2 | reserved | | | | | | | | | | | |
| E618 | 1 | EP2FIFOCFG[15] | Endpoint 2 / slave FIFO configuration | 0 | INFM1 | OEP1 | AUTOOUT | AUTOIN | ZEROLENIN | 0 | WORDWIDE | 00000101 | rbbbbbrb |
| E619 | 1 | EP4FIFOCFG[15] | Endpoint 4 / slave FIFO configuration | 0 | INFM1 | OEP1 | AUTOOUT | AUTOIN | ZEROLENIN | 0 | WORDWIDE | 00000101 | rbbbbbrb |
| E61A | 1 | EP6FIFOCFG[15] | Endpoint 6 / slave FIFO configuration | 0 | INFM1 | OEP1 | AUTOOUT | AUTOIN | ZEROLENIN | 0 | WORDWIDE | 00000101 | rbbbbbrb |
| E61B | 1 | EP8FIFOCFG[15] | Endpoint 8 / slave FIFO configuration | 0 | INFM1 | OEP1 | AUTOOUT | AUTOIN | ZEROLENIN | 0 | WORDWIDE | 00000101 | rbbbbbrb |
| E61C | 4 | reserved | | | | | | | | | | | |
| E620 | 1 | EP2AUTOINLENH[15] | Endpoint 2 AUTOIN Packet Length H | 0 | 0 | 0 | 0 | 0 | PL10 | PL9 | PL8 | 00000010 | rrrrrbbb |
| E621 | 1 | EP2AUTOINLENL[15] | Endpoint 2 AUTOIN Packet Length L | PL7 | PL6 | PL5 | PL4 | PL3 | PL2 | PL1 | PL0 | 00000000 | RW |
| E622 | 1 | EP4AUTOINLENH[15] | Endpoint 4 AUTOIN Packet Length H | 0 | 0 | 0 | 0 | 0 | 0 | PL9 | PL8 | 00000010 | rrrrrrbb |
| E623 | 1 | EP4AUTOINLENL[15] | Endpoint 4 AUTOIN Packet Length L | PL7 | PL6 | PL5 | PL4 | PL3 | PL2 | PL1 | PL0 | 00000000 | RW |
| E624 | 1 | EP6AUTOINLENH[15] | Endpoint 6 AUTOIN Packet Length H | 0 | 0 | 0 | 0 | 0 | PL10 | PL9 | PL8 | 00000010 | rrrrrbbb |
| E625 | 1 | EP6AUTOINLENL[15] | Endpoint 6 AUTOIN Packet Length L | PL7 | PL6 | PL5 | PL4 | PL3 | PL2 | PL1 | PL0 | 00000000 | RW |
| E626 | 1 | EP8AUTOINLENH[15] | Endpoint 8 AUTOIN Packet Length H | 0 | 0 | 0 | 0 | 0 | 0 | PL9 | PL8 | 00000010 | rrrrrrbb |
| E627 | 1 | EP8AUTOINLENL[15] | Endpoint 8 AUTOIN Packet Length L | PL7 | PL6 | PL5 | PL4 | PL3 | PL2 | PL1 | PL0 | 00000000 | RW |
| E628 | 1 | ECCCFG | ECC Configuration | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ECCM | 00000000 | rrrrrrrb |
| E629 | 1 | ECCRESET | ECC Reset | x | x | x | x | x | x | x | x | 00000000 | W |
| E62A | 1 | ECC1B0 | ECC1 Byte 0 Address | LINE15 | LINE14 | LINE13 | LINE12 | LINE11 | LINE10 | LINE9 | LINE8 | 00000000 | R |

**Note**

15. Read and writes to these registers may require synchronization delay; see Technical Reference Manual for “Synchronization Delay.”

**Table 12. FX2LP Register Summary** (continued)

| Hex | Size | Name | Description | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Default | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E62B | 1 | ECC1B1 | ECC1 Byte 1 Address | LINE7 | LINE6 | LINE5 | LINE4 | LINE3 | LINE2 | LINE1 | LINE0 | 00000000 | R |
| E62C | 1 | ECC1B2 | ECC1 Byte 2 Address | COL5 | COL4 | COL3 | COL2 | COL1 | COL0 | LINE17 | LINE16 | 00000000 | R |
| E62D | 1 | ECC2B0 | ECC2 Byte 0 Address | LINE15 | LINE14 | LINE13 | LINE12 | LINE11 | LINE10 | LINE9 | LINE8 | 00000000 | R |
| E62E | 1 | ECC2B1 | ECC2 Byte 1 Address | LINE7 | LINE6 | LINE5 | LINE4 | LINE3 | LINE2 | LINE1 | LINE0 | 00000000 | R |
| E62F | 1 | ECC2B2 | ECC2 Byte 2 Address | COL5 | COL4 | COL3 | COL2 | COL1 | COL0 | 0 | 0 | 00000000 | R |
| E630 H.S. | 1 | EP2FIFOPFH[16] | Endpoint 2 / slave FIFO Programmable Flag H | DECIS | PKTSTAT | IN:PKTS[2] OUT:PFC12 | IN:PKTS[1] OUT:PFC11 | IN:PKTS[0] OUT:PFC10 | 0 | PFC9 | PFC8 | 10001000 | bbbbbrbb |
| E630 F.S. | 1 | EP2FIFOPFH[16] | Endpoint 2 / slave FIFO Programmable Flag H | DECIS | PKTSTAT | OUT:PFC12 | OUT:PFC11 | OUT:PFC10 | 0 | PFC9 | IN:PKTS[2] OUT:PFC8 | 10001000 | bbbbbrbb |
| E631 H.S. | 1 | EP2FIFOPFL[16] | Endpoint 2 / slave FIFO Programmable Flag L | PFC7 | PFC6 | PFC5 | PFC4 | PFC3 | PFC2 | PFC1 | PFC0 | 00000000 | RW |
| E631 F.S | 1 | EP2FIFOPFL[16] | Endpoint 2 / slave FIFO Programmable Flag L | IN:PKTS[1] OUT:PFC7 | IN:PKTS[0] OUT:PFC6 | PFC5 | PFC4 | PFC3 | PFC2 | PFC1 | PFC0 | 00000000 | RW |
| E632 H.S. | 1 | EP4FIFOPFH[16] | Endpoint 4 / slave FIFO Programmable Flag H | DECIS | PKTSTAT | 0 | IN: PKTS[1] OUT:PFC10 | IN: PKTS[0] OUT:PFC9 | 0 | 0 | PFC8 | 10001000 | bbrbbrrb |
| E632 F.S | 1 | EP4FIFOPFH[16] | Endpoint 4 / slave FIFO Programmable Flag H | DECIS | PKTSTAT | 0 | OUT:PFC10 | OUT:PFC9 | 0 | 0 | PFC8 | 10001000 | bbrbbrrb |
| E633 H.S. | 1 | EP4FIFOPFL[16] | Endpoint 4 / slave FIFO Programmable Flag L | PFC7 | PFC6 | PFC5 | PFC4 | PFC3 | PFC2 | PFC1 | PFC0 | 00000000 | RW |
| E633 F.S | 1 | EP4FIFOPFL[16] | Endpoint 4 / slave FIFO Programmable Flag L | IN: PKTS[1] OUT:PFC7 | IN: PKTS[0] OUT:PFC6 | PFC5 | PFC4 | PFC3 | PFC2 | PFC1 | PFC0 | 00000000 | RW |
| E634 H.S. | 1 | EP6FIFOPFH[16] | Endpoint 6 / slave FIFO Programmable Flag H | DECIS | PKTSTAT | IN:PKTS[2] OUT:PFC12 | IN:PKTS[1] OUT:PFC11 | IN:PKTS[0] OUT:PFC10 | 0 | PFC9 | PFC8 | 00001000 | bbbbbrbb |
| E634 F.S | 1 | EP6FIFOPFH[16] | Endpoint 6 / slave FIFO Programmable Flag H | DECIS | PKTSTAT | OUT:PFC12 | OUT:PFC11 | OUT:PFC10 | 0 | PFC9 | IN:PKTS[2] OUT:PFC8 | 00001000 | bbbbbrbb |
| E635 H.S. | 1 | EP6FIFOPFL[16] | Endpoint 6 / slave FIFO Programmable Flag L | PFC7 | PFC6 | PFC5 | PFC4 | PFC3 | PFC2 | PFC1 | PFC0 | 00000000 | RW |
| E635 F.S | 1 | EP6FIFOPFL[16] | Endpoint 6 / slave FIFO Programmable Flag L | IN:PKTS[1] OUT:PFC7 | IN:PKTS[0] OUT:PFC6 | PFC5 | PFC4 | PFC3 | PFC2 | PFC1 | PFC0 | 00000000 | RW |
| E636 H.S. | 1 | EP8FIFOPFH[16] | Endpoint 8 / slave FIFO Programmable Flag H | DECIS | PKTSTAT | 0 | IN: PKTS[1] OUT:PFC10 | IN: PKTS[0] OUT:PFC9 | 0 | 0 | PFC8 | 00001000 | bbrbbrrb |
| E636 F.S | 1 | EP8FIFOPFH[16] | Endpoint 8 / slave FIFO Programmable Flag H | DECIS | PKTSTAT | 0 | OUT:PFC10 | OUT:PFC9 | 0 | 0 | PFC8 | 00001000 | bbrbbrrb |
| E637 H.S. | 1 | EP8FIFOPFL[16] | Endpoint 8 / slave FIFO Programmable Flag L | PFC7 | PFC6 | PFC5 | PFC4 | PFC3 | PFC2 | PFC1 | PFC0 | 00000000 | RW |
| E637 F.S | 1 | EP8FIFOPFL[16] | Endpoint 8 / slave FIFO Programmable Flag L | IN: PKTS[1] OUT:PFC7 | IN: PKTS[0] OUT:PFC6 | PFC5 | PFC4 | PFC3 | PFC2 | PFC1 | PFC0 | 00000000 | RW |
| | 8 | reserved | | | | | | | | | | | |
| E640 | 1 | EP2ISOINPKTS | EP2 (if ISO) IN Packets per frame (1-3) | AADJ | 0 | 0 | 0 | 0 | 0 | INPPF1 | INPPF0 | 00000001 | brrrrrbb |
| E641 | 1 | EP4ISOINPKTS | EP4 (if ISO) IN Packets per frame (1-3) | AADJ | 0 | 0 | 0 | 0 | 0 | INPPF1 | INPPF0 | 00000001 | brrrrrrr |
| E642 | 1 | EP6ISOINPKTS | EP6 (if ISO) IN Packets per frame (1-3) | AADJ | 0 | 0 | 0 | 0 | 0 | INPPF1 | INPPF0 | 00000001 | brrrrrbb |
| E643 | 1 | EP8ISOINPKTS | EP8 (if ISO) IN Packets per frame (1-3) | AADJ | 0 | 0 | 0 | 0 | 0 | INPPF1 | INPPF0 | 00000001 | brrrrrrr |
| E644 | 4 | reserved | | | | | | | | | | | |
| E648 | 1 | INPKTEND[16] | Force IN Packet End | Skip | 0 | 0 | 0 | EP3 | EP2 | EP1 | EP0 | xxxxxxxx | W |
| E649 | 7 | OUTPKTEND[16] | Force OUT Packet End | Skip | 0 | 0 | 0 | EP3 | EP2 | EP1 | EP0 | xxxxxxxx | W |
| | | INTERRUPTS | | | | | | | | | | | |
| E650 | 1 | EP2FIFOIE[16] | Endpoint 2 slave FIFO Flag Interrupt Enable | 0 | 0 | 0 | 0 | EDGEPF | PF | EF | FF | 00000000 | RW |
| E651 | 1 | EP2FIFOIRQ[16,17] | Endpoint 2 slave FIFO Flag Interrupt Request | 0 | 0 | 0 | 0 | 0 | PF | EF | FF | 00000000 | rrrrrbbb |
| E652 | 1 | EP4FIFOIE[16] | Endpoint 4 slave FIFO Flag Interrupt Enable | 0 | 0 | 0 | 0 | EDGEPF | PF | EF | FF | 00000000 | RW |
| E653 | 1 | EP4FIFOIRQ[16,17] | Endpoint 4 slave FIFO Flag Interrupt Request | 0 | 0 | 0 | 0 | 0 | PF | EF | FF | 00000000 | rrrrrbbb |
| E654 | 1 | EP6FIFOIE[16] | Endpoint 6 slave FIFO Flag Interrupt Enable | 0 | 0 | 0 | 0 | EDGEPF | PF | EF | FF | 00000000 | RW |
| E655 | 1 | EP6FIFOIRQ[16,17] | Endpoint 6 slave FIFO Flag Interrupt Request | 0 | 0 | 0 | 0 | 0 | PF | EF | FF | 00000000 | rrrrrbbb |
| E656 | 1 | EP8FIFOIE[16] | Endpoint 8 slave FIFO Flag Interrupt Enable | 0 | 0 | 0 | 0 | EDGEPF | PF | EF | FF | 00000000 | RW |
| E657 | 1 | EP8FIFOIRQ[16,17] | Endpoint 8 slave FIFO Flag Interrupt Request | 0 | 0 | 0 | 0 | 0 | PF | EF | FF | 00000000 | rrrrrbbb |
| E658 | 1 | IBNIE | IN-BULK-NAK Interrupt Enable | 0 | 0 | EP8 | EP6 | EP4 | EP2 | EP1 | EP0 | 00000000 | RW |
| E659 | 1 | IBNIRQ[17] | IN-BULK-NAK interrupt Request | 0 | 0 | EP8 | EP6 | EP4 | EP2 | EP1 | EP0 | 00xxxxxx | rrbbbbbb |
| E65A | 1 | NAKIE | Endpoint Ping-NAK / IBN Interrupt Enable | EP8 | EP6 | EP4 | EP2 | EP1 | EP0 | 0 | IBN | 00000000 | RW |
| E65B | 1 | NAKIRQ[17] | Endpoint Ping-NAK / IBN Interrupt Request | EP8 | EP6 | EP4 | EP2 | EP1 | EP0 | 0 | IBN | xxxxxx0x | bbbbbbrb |
| E65C | 1 | USBIE | USB Int Enables | 0 | EP0ACK | HSGRANT | URES | SUSP | SUTOK | SOF | SUDAV | 00000000 | RW |

**Notes**

16. Read and writes to these registers may require synchronization delay; see Technical Reference Manual for “Synchronization Delay”.
17. The register can only be reset; it cannot be set.

**Table 12. FX2LP Register Summary** (continued)

| Hex | Size | Name | Description | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Default | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E65D | 1 | USBIRQ[18] | USB Interrupt Requests | 0 | EP0ACK | HSGRANT | URES | SUSP | SUTOK | SOF | SUDAV | 0xxxxxxx | rbbbbbbb |
| E65E | 1 | EPIE | Endpoint Interrupt Enables | EP8 | EP6 | EP4 | EP2 | EP1OUT | EP1IN | EP0OUT | EP0IN | 00000000 | RW |
| E65F | 1 | EPIRQ[18] | Endpoint Interrupt Requests | EP8 | EP6 | EP4 | EP2 | EP1OUT | EP1IN | EP0OUT | EP0IN | 0 | RW |
| E660 | 1 | GPIFIE[19] | GPIF Interrupt Enable | 0 | 0 | 0 | 0 | 0 | 0 | GPIFWF | GPIFDONE | 00000000 | RW |
| E661 | 1 | GPIFIRQ[19] | GPIF Interrupt Request | 0 | 0 | 0 | 0 | 0 | 0 | GPIFWF | GPIFDONE | 000000xx | RW |
| E662 | 1 | USBERRIE | USB Error Interrupt Enables | ISOEP8 | ISOEP6 | ISOEP4 | ISOEP2 | 0 | 0 | 0 | ERRLIMIT | 00000000 | RW |
| E663 | 1 | USBERRIRQ[18] | USB Error Interrupt Requests | ISOEP8 | ISOEP6 | ISOEP4 | ISOEP2 | 0 | 0 | 0 | ERRLIMIT | 0000000x | bbbbrrrb |
| E664 | 1 | ERRCNTLIM | USB Error counter and limit | EC3 | EC2 | EC1 | EC0 | LIMIT3 | LIMIT2 | LIMIT1 | LIMIT0 | xxxx0100 | rrrrbbbb |
| E665 | 1 | CLRERRCNT | Clear Error Counter EC3:0 | x | x | x | x | x | x | x | x | xxxxxxxx | W |
| E666 | 1 | INT2IVEC | Interrupt 2 (USB) Autovector | 0 | I2V4 | I2V3 | I2V2 | I2V1 | I2V0 | 0 | 0 | 00000000 | R |
| E667 | 1 | INT4IVEC | Interrupt 4 (slave FIFO & GPIF) Autovector | 1 | 0 | I4V3 | I4V2 | I4V1 | I4V0 | 0 | 0 | 10000000 | R |
| E668 | 1 | INTSET-UP | Interrupt 2&4 setup | 0 | 0 | 0 | 0 | AV2EN | 0 | INT4SRC | AV4EN | 00000000 | RW |
| E669 | 7 | reserved | | | | | | | | | | | |
| | | INPUT / OUTPUT | | | | | | | | | | | |
| E670 | 1 | PORTACFG | I/O PORTA Alternate Configuration | FLAGD | SLCS | 0 | 0 | 0 | 0 | INT1 | INT0 | 00000000 | RW |
| E671 | 1 | PORTCCFG | I/O PORTC Alternate Configuration | GPIFA7 | GPIFA6 | GPIFA5 | GPIFA4 | GPIFA3 | GPIFA2 | GPIFA1 | GPIFA0 | 00000000 | RW |
| E672 | 1 | PORTECFG | I/O PORTE Alternate Configuration | GPIFA8 | T2EX | INT6 | RXD1OUT | RXD0OUT | T2OUT | T1OUT | T0OUT | 00000000 | RW |
| E673 | 4 | reserved | | | | | | | | | | | |
| E677 | 1 | reserved | | | | | | | | | | | |
| E678 | 1 | $I^2CS$ | I²C Bus Control & Status | START | STOP | LASTRD | ID1 | ID0 | BERR | ACK | DONE | 000xx000 | bbbrrrrr |
| E679 | 1 | I2DAT | I²C Bus Data | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | xxxxxxxx | RW |
| E67A | 1 | $I^2CTL$ | I²C Bus Control | 0 | 0 | 0 | 0 | 0 | 0 | STOPIE | 400KHZ | 00000000 | RW |
| E67B | 1 | XAUTODAT1 | Autoptr1 MOVX access, when APTREN=1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| E67C | 1 | XAUTODAT2 | Autoptr2 MOVX access, when APTREN=1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| | | UDMA CRC | | | | | | | | | | | |
| E67D | 1 | UDMACRCH[19] | UDMA CRC MSB | CRC15 | CRC14 | CRC13 | CRC12 | CRC11 | CRC10 | CRC9 | CRC8 | 01001010 | RW |
| E67E | 1 | UDMACRCL[19] | UDMA CRC LSB | CRC7 | CRC6 | CRC5 | CRC4 | CRC3 | CRC2 | CRC1 | CRC0 | 10111010 | RW |
| E67F | 1 | UDMACRC-QUALIFIER | UDMA CRC Qualifier | QENABLE | 0 | 0 | 0 | QSTATE | QSIGNAL2 | QSIGNAL1 | QSIGNAL0 | 00000000 | brrrbbbb |
| | | USB CONTROL | | | | | | | | | | | |
| E680 | 1 | USBCS | USB Control & Status | HSM | 0 | 0 | 0 | DISCON | NOSYNSOF | RENUM | SIGRSUME | x0000000 | rrrrbbbb |
| E681 | 1 | SUSPEND | Put chip into suspend | x | x | x | x | x | x | x | x | xxxxxxxx | W |
| E682 | 1 | WAKEUPCS | Wakeup Control & Status | WU2 | WU | WU2POL | WUPOL | 0 | DPEN | WU2EN | WUEN | xx000101 | bbbbrbbb |
| E683 | 1 | TOGCTL | Toggle Control | Q | S | R | I/O | EP3 | EP2 | EP1 | EP0 | x0000000 | rrrbbbbb |
| E684 | 1 | USBFRAMEH | USB Frame count H | 0 | 0 | 0 | 0 | 0 | FC10 | FC9 | FC8 | 00000xxx | R |
| E685 | 1 | USBFRAMEL | USB Frame count L | FC7 | FC6 | FC5 | FC4 | FC3 | FC2 | FC1 | FC0 | xxxxxxxx | R |
| E686 | 1 | MICROFRAME | Microframe count, 0-7 | 0 | 0 | 0 | 0 | 0 | MF2 | MF1 | MF0 | 00000xxx | R |
| E687 | 1 | FNADDR | USB Function address | 0 | FA6 | FA5 | FA4 | FA3 | FA2 | FA1 | FA0 | 0xxxxxxx | R |
| E688 | 2 | reserved | | | | | | | | | | | |
| | | | | | | | | | | | | | |
| | | ENDPOINTS | | | | | | | | | | | |
| E68A | 1 | EP0BCH[19] | Endpoint 0 Byte Count H | (BC15) | (BC14) | (BC13) | (BC12) | (BC11) | (BC10) | (BC9) | (BC8) | xxxxxxxx | RW |
| E68B | 1 | EP0BCL[19] | Endpoint 0 Byte Count L | (BC7) | BC6 | BC5 | BC4 | BC3 | BC2 | BC1 | BC0 | xxxxxxxx | RW |
| E68C | 1 | reserved | | | | | | | | | | | |
| E68D | 1 | EP1OUTBC | Endpoint 1 OUT Byte Count | 0 | BC6 | BC5 | BC4 | BC3 | BC2 | BC1 | BC0 | 0xxxxxxx | RW |
| E68E | 1 | reserved | | | | | | | | | | | |
| E68F | 1 | EP1INBC | Endpoint 1 IN Byte Count | 0 | BC6 | BC5 | BC4 | BC3 | BC2 | BC1 | BC0 | 0xxxxxxx | RW |
| E690 | 1 | EP2BCH[19] | Endpoint 2 Byte Count H | 0 | 0 | 0 | 0 | 0 | BC10 | BC9 | BC8 | 00000xxx | RW |
| E691 | 1 | EP2BCL[19] | Endpoint 2 Byte Count L | BC7/SKIP | BC6 | BC5 | BC4 | BC3 | BC2 | BC1 | BC0 | xxxxxxxx | RW |
| E692 | 2 | reserved | | | | | | | | | | | |
| E694 | 1 | EP4BCH[19] | Endpoint 4 Byte Count H | 0 | 0 | 0 | 0 | 0 | 0 | BC9 | BC8 | 000000xx | RW |
| E695 | 1 | EP4BCL[19] | Endpoint 4 Byte Count L | BC7/SKIP | BC6 | BC5 | BC4 | BC3 | BC2 | BC1 | BC0 | xxxxxxxx | RW |
| E696 | 2 | reserved | | | | | | | | | | | |
| E698 | 1 | EP6BCH[19] | Endpoint 6 Byte Count H | 0 | 0 | 0 | 0 | 0 | BC10 | BC9 | BC8 | 00000xxx | RW |
| E699 | 1 | EP6BCL[19] | Endpoint 6 Byte Count L | BC7/SKIP | BC6 | BC5 | BC4 | BC3 | BC2 | BC1 | BC0 | xxxxxxxx | RW |

**Notes**
18. The register can only be reset; it cannot be set.
19. Read and writes to these registers may require synchronization delay; see Technical Reference Manual for “Synchronization Delay”.

**Table 12. FX2LP Register Summary** (continued)

| Hex | Size | Name | Description | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Default | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E69A | 2 | reserved | | | | | | | | | | | |
| E69C | 1 | EP8BCH[20] | Endpoint 8 Byte Count H | 0 | 0 | 0 | 0 | 0 | 0 | BC9 | BC8 | 000000xx | RW |
| E69D | 1 | EP8BCL[20] | Endpoint 8 Byte Count L | BC7/SKIP | BC6 | BC5 | BC4 | BC3 | BC2 | BC1 | BC0 | xxxxxxxx | RW |
| E69E | 2 | reserved | | | | | | | | | | | |
| E6A0 | 1 | EP0CS | Endpoint 0 Control and Status | HSNAK | 0 | 0 | 0 | 0 | 0 | BUSY | STALL | 10000000 | bbbbbbrb |
| E6A1 | 1 | EP1OUTCS | Endpoint 1 OUT Control and Status | 0 | 0 | 0 | 0 | 0 | 0 | BUSY | STALL | 00000000 | bbbbbbrb |
| E6A2 | 1 | EP1INCS | Endpoint 1 IN Control and Status | 0 | 0 | 0 | 0 | 0 | 0 | BUSY | STALL | 00000000 | bbbbbbrb |
| E6A3 | 1 | EP2CS | Endpoint 2 Control and Status | 0 | NPAK2 | NPAK1 | NPAK0 | FULL | EMPTY | 0 | STALL | 00101000 | rrrrrrrb |
| E6A4 | 1 | EP4CS | Endpoint 4 Control and Status | 0 | 0 | NPAK1 | NPAK0 | FULL | EMPTY | 0 | STALL | 00101000 | rrrrrrrb |
| E6A5 | 1 | EP6CS | Endpoint 6 Control and Status | 0 | NPAK2 | NPAK1 | NPAK0 | FULL | EMPTY | 0 | STALL | 00000100 | rrrrrrrb |
| E6A6 | 1 | EP8CS | Endpoint 8 Control and Status | 0 | 0 | NPAK1 | NPAK0 | FULL | EMPTY | 0 | STALL | 00000100 | rrrrrrrb |
| E6A7 | 1 | EP2FIFOFLGS | Endpoint 2 slave FIFO Flags | 0 | 0 | 0 | 0 | 0 | PF | EF | FF | 00000010 | R |
| E6A8 | 1 | EP4FIFOFLGS | Endpoint 4 slave FIFO Flags | 0 | 0 | 0 | 0 | 0 | PF | EF | FF | 00000010 | R |
| E6A9 | 1 | EP6FIFOFLGS | Endpoint 6 slave FIFO Flags | 0 | 0 | 0 | 0 | 0 | PF | EF | FF | 00000110 | R |
| E6AA | 1 | EP8FIFOFLGS | Endpoint 8 slave FIFO Flags | 0 | 0 | 0 | 0 | 0 | PF | EF | FF | 00000110 | R |
| E6AB | 1 | EP2FIFOBCH | Endpoint 2 slave FIFO total byte count H | 0 | 0 | 0 | BC12 | BC11 | BC10 | BC9 | BC8 | 00000000 | R |
| E6AC | 1 | EP2FIFOBCL | Endpoint 2 slave FIFO total byte count L | BC7 | BC6 | BC5 | BC4 | BC3 | BC2 | BC1 | BC0 | 00000000 | R |
| E6AD | 1 | EP4FIFOBCH | Endpoint 4 slave FIFO total byte count H | 0 | 0 | 0 | 0 | 0 | BC10 | BC9 | BC8 | 00000000 | R |
| E6AE | 1 | EP4FIFOBCL | Endpoint 4 slave FIFO total byte count L | BC7 | BC6 | BC5 | BC4 | BC3 | BC2 | BC1 | BC0 | 00000000 | R |
| E6AF | 1 | EP6FIFOBCH | Endpoint 6 slave FIFO total byte count H | 0 | 0 | 0 | 0 | BC11 | BC10 | BC9 | BC8 | 00000000 | R |
| E6B0 | 1 | EP6FIFOBCL | Endpoint 6 slave FIFO total byte count L | BC7 | BC6 | BC5 | BC4 | BC3 | BC2 | BC1 | BC0 | 00000000 | R |
| E6B1 | 1 | EP8FIFOBCH | Endpoint 8 slave FIFO total byte count H | 0 | 0 | 0 | 0 | 0 | BC10 | BC9 | BC8 | 00000000 | R |
| E6B2 | 1 | EP8FIFOBCL | Endpoint 8 slave FIFO total byte count L | BC7 | BC6 | BC5 | BC4 | BC3 | BC2 | BC1 | BC0 | 00000000 | R |
| E6B3 | 1 | SUDPTRH | Setup Data Pointer high address byte | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | xxxxxxxx | RW |
| E6B4 | 1 | SUDPTRL | Setup Data Pointer low address byte | A7 | A6 | A5 | A4 | A3 | A2 | A1 | 0 | xxxxxxx0 | bbbbbbbr |
| E6B5 | 1 | SUDPTRCTL | Setup Data Pointer Auto Mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SDPAUTO | 00000001 | RW |
| | 2 | reserved | | | | | | | | | | | |
| E6B8 | 8 | SET-UPDAT | 8 bytes of setup data | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | R |
| | | | SET-UPDAT[0] = bmRequestType | | | | | | | | | | |
| | | | SET-UPDAT[1] = bmRequest | | | | | | | | | | |
| | | | SET-UPDAT[2:3] = wValue | | | | | | | | | | |
| | | | SET-UPDAT[4:5] = wIndex | | | | | | | | | | |
| | | | SET-UPDAT[6:7] = wLength | | | | | | | | | | |
| | | GPIF | | | | | | | | | | | |
| E6C0 | 1 | GPIFWFSELECT | Waveform Selector | SINGLEWR1 | SINGLEWR0 | SINGLERD1 | SINGLERD0 | FIFOWR1 | FIFOWR0 | FIFORD1 | FIFORD0 | 11100100 | RW |
| E6C1 | 1 | GPIFIDLECS | GPIF Done, GPIF IDLE drive mode | DONE | 0 | 0 | 0 | 0 | 0 | 0 | IDLEDRV | 10000000 | RW |
| E6C2 | 1 | GPIFIDLECTL | Inactive Bus, CTL states | 0 | 0 | CTL5 | CTL4 | CTL3 | CTL2 | CTL1 | CTL0 | 11111111 | RW |
| E6C3 | 1 | GPIFCTLCFG | CTL Drive Type | TRICTL | 0 | CTL5 | CTL4 | CTL3 | CTL2 | CTL1 | CTL0 | 00000000 | RW |
| E6C4 | 1 | GPIFADRH[20] | GPIF Address H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | GPIFA8 | 00000000 | RW |
| E6C5 | 1 | GPIFADRL[20] | GPIF Address L | GPIFA7 | GPIFA6 | GPIFA5 | GPIFA4 | GPIFA3 | GPIFA2 | GPIFA1 | GPIFA0 | 00000000 | RW |
| | | FLOWSTATE | | | | | | | | | | | |
| E6C6 | 1 | FLOWSTATE | Flowstate Enable and Selector | FSE | 0 | 0 | 0 | 0 | FS2 | FS1 | FS0 | 00000000 | brrrrbbb |
| E6C7 | 1 | FLOWLOGIC | Flowstate Logic | LFUNC1 | LFUNC0 | TERMA2 | TERMA1 | TERMA0 | TERMB2 | TERMB1 | TERMB0 | 00000000 | RW |
| E6C8 | 1 | FLOWEQ0CTL | CTL-Pin States in Flowstate (when Logic = 0) | CTL0E3 | CTL0E2 | CTL0E1/ CTL5 | CTL0E0/ CTL4 | CTL3 | CTL2 | CTL1 | CTL0 | 00000000 | RW |

**Note**

20. Read and writes to these registers may require synchronization delay; see Technical Reference Manual for “Synchronization Delay”.

**Table 12. FX2LP Register Summary** (continued)

| Hex | Size | Name | Description | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Default | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E6C9 | 1 | FLOWEQ1CTL | CTL-Pin States in Flow-state (when Logic = 1) | CTL0E3 | CTL0E2 | CTL0E1/ CTL5 | CTL0E0/ CTL4 | CTL3 | CTL2 | CTL1 | CTL0 | 00000000 | RW |
| E6CA | 1 | FLOWHOLDOFF | Holdoff Configuration | HOPERIOD3 | HOPERIOD2 | HOPERIOD1 | HOPERIOD0 | HOSTATE | HOCTL2 | HOCTL1 | HOCTL0 | 00010010 | RW |
| E6CB | 1 | FLOWSTB | Flowstate Strobe Configuration | SLAVE | RDYASYNC | CTLTOGL | SUSTAIN | 0 | MSTB2 | MSTB1 | MSTB0 | 00100000 | RW |
| E6CC | 1 | FLOWSTBEDGE | Flowstate Rising/Falling Edge Configuration | 0 | 0 | 0 | 0 | 0 | 0 | FALLING | RISING | 00000001 | rrrrrrbb |
| E6CD | 1 | FLOWSTBPERIOD | Master-Strobe Half-Period | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000010 | RW |
| E6CE | 1 | GPIFTCB3[21] | GPIF Transaction Count Byte 3 | TC31 | TC30 | TC29 | TC28 | TC27 | TC26 | TC25 | TC24 | 00000000 | RW |
| E6CF | 1 | GPIFTCB2[21] | GPIF Transaction Count Byte 2 | TC23 | TC22 | TC21 | TC20 | TC19 | TC18 | TC17 | TC16 | 00000000 | RW |
| E6D0 | 1 | GPIFTCB1[21] | GPIF Transaction Count Byte 1 | TC15 | TC14 | TC13 | TC12 | TC11 | TC10 | TC9 | TC8 | 00000000 | RW |
| E6D1 | 1 | GPIFTCB0[21] | GPIF Transaction Count Byte 0 | TC7 | TC6 | TC5 | TC4 | TC3 | TC2 | TC1 | TC0 | 00000001 | RW |
| | 2 | reserved | | | | | | | | | | 00000000 | RW |
| | | reserved | | | | | | | | | | | |
| | | reserved | | | | | | | | | | | |
| E6D2 | 1 | EP2GPIFFLGSEL[21] | Endpoint 2 GPIF Flag select | 0 | 0 | 0 | 0 | 0 | 0 | FS1 | FS0 | 00000000 | RW |
| E6D3 | 1 | EP2GPIFPFSTOP | Endpoint 2 GPIF stop transaction on prog. flag | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FIFO2FLAG | 00000000 | RW |
| E6D4 | 1 | EP2GPIFTRIG[21] | Endpoint 2 GPIF Trigger | x | x | x | x | x | x | x | x | xxxxxxxx | W |
| | 3 | reserved | | | | | | | | | | | |
| | | reserved | | | | | | | | | | | |
| | | reserved | | | | | | | | | | | |
| E6DA | 1 | EP4GPIFFLGSEL[21] | Endpoint 4 GPIF Flag select | 0 | 0 | 0 | 0 | 0 | 0 | FS1 | FS0 | 00000000 | RW |
| E6DB | 1 | EP4GPIFPFSTOP | Endpoint 4 GPIF stop transaction on GPIF Flag | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FIFO4FLAG | 00000000 | RW |
| E6DC | 1 | EP4GPIFTRIG[21] | Endpoint 4 GPIF Trigger | x | x | x | x | x | x | x | x | xxxxxxxx | W |
| | 3 | reserved | | | | | | | | | | | |
| | | reserved | | | | | | | | | | | |
| | | reserved | | | | | | | | | | | |
| E6E2 | 1 | EP6GPIFFLGSEL[21] | Endpoint 6 GPIF Flag select | 0 | 0 | 0 | 0 | 0 | 0 | FS1 | FS0 | 00000000 | RW |
| E6E3 | 1 | EP6GPIFPFSTOP | Endpoint 6 GPIF stop transaction on prog. flag | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FIFO6FLAG | 00000000 | RW |
| E6E4 | 1 | EP6GPIFTRIG[21] | Endpoint 6 GPIF Trigger | x | x | x | x | x | x | x | x | xxxxxxxx | W |
| | 3 | reserved | | | | | | | | | | | |
| | | reserved | | | | | | | | | | | |
| | | reserved | | | | | | | | | | | |
| E6EA | 1 | EP8GPIFFLGSEL[21] | Endpoint 8 GPIF Flag select | 0 | 0 | 0 | 0 | 0 | 0 | FS1 | FS0 | 00000000 | RW |
| E6EB | 1 | EP8GPIFPFSTOP | Endpoint 8 GPIF stop transaction on prog. flag | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FIFO8FLAG | 00000000 | RW |
| E6EC | 1 | EP8GPIFTRIG[21] | Endpoint 8 GPIF Trigger | x | x | x | x | x | x | x | x | xxxxxxxx | W |
| | 3 | reserved | | | | | | | | | | | |
| E6F0 | 1 | XGPIFSGLDATH | GPIF Data H (16-bit mode only) | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | xxxxxxxx | RW |
| E6F1 | 1 | XGPIFSGLDATLX | Read/Write GPIF Data L & trigger transaction | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| E6F2 | 1 | XGPIFSGLDATLNOX | Read GPIF Data L, no transaction trigger | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | R |
| E6F3 | 1 | GPIFREADYCFG | Internal RDY, Sync/Async, RDY pin states | INTRDY | SAS | TCXRDY5 | 0 | 0 | 0 | 0 | 0 | 00000000 | bbbrrrrr |
| | | | | | | | | | | | | | |
| E6F4 | 1 | GPIFREADYSTAT | GPIF Ready Status | 0 | 0 | RDY5 | RDY4 | RDY3 | RDY2 | RDY1 | RDY0 | 00xxxxxx | R |
| E6F5 | 1 | GPIFABORT | Abort GPIF Waveforms | x | x | x | x | x | x | x | x | xxxxxxxx | W |
| E6F6 | 2 | reserved | | | | | | | | | | | |
| | | ENDPOINT BUFFERS | | | | | | | | | | | |
| E740 | 64 | EP0BUF | EP0-IN/-OUT buffer | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| E780 | 64 | EP10UTBUF | EP1-OUT buffer | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| E7C0 | 64 | EP1INBUF | EP1-IN buffer | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| E800 | 2048 | reserved | | | | | | | | | | | RW |
| F000 | 1024 | EP2FIFOBUF | 512/1024 byte EP 2 / slave FIFO buffer (IN or OUT) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| F400 | 512 | EP4FIFOBUF | 512 byte EP 4 / slave FIFO buffer (IN or OUT) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| F600 | 512 | reserved | | | | | | | | | | | |

**Note**
21. Read and writes to these registers may require synchronization delay; see Technical Reference Manual for “Synchronization Delay”.

**Table 12. FX2LP Register Summary** (continued)

| Hex | Size | Name | Description | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Default | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| F800 | 1024 | EP6FIFOBUF | 512/1024 byte EP 6 / slave FIFO buffer (IN or OUT) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| FC00 | 512 | EP8FIFOBUF | 512 byte EP 8 / slave FIFO buffer (IN or OUT) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| FE00 | 512 | reserved | | | | | | | | | | | |
| xxxx | | I²C Configuration Byte | | 0 | DISCON | 0 | 0 | 0 | 0 | 0 | 400KHZ | xxxxxxxx [22] | n/a |
| | | Special Function Registers (SFRs) | | | | | | | | | | | |
| 80 | 1 | IOA[23] | Port A (bit addressable) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| 81 | 1 | SP | Stack Pointer | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000111 | RW |
| 82 | 1 | DPL0 | Data Pointer 0 L | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | 00000000 | RW |
| 83 | 1 | DPH0 | Data Pointer 0 H | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | 00000000 | RW |
| 84 | 1 | DPL1[23] | Data Pointer 1 L | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | 00000000 | RW |
| 85 | 1 | DPH1[23] | Data Pointer 1 H | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | 00000000 | RW |
| 86 | 1 | DPS[23] | Data Pointer 0/1 select | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SEL | 00000000 | RW |
| 87 | 1 | PCON | Power Control | SMOD0 | x | 1 | 1 | x | x | x | IDLE | 00110000 | RW |
| 88 | 1 | TCON | Timer/Counter Control (bit addressable) | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 | 00000000 | RW |
| 89 | 1 | TMOD | Timer/Counter Mode Control | GATE | CT | M1 | M0 | GATE | CT | M1 | M0 | 00000000 | RW |
| 8A | 1 | TL0 | Timer 0 reload L | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| 8B | 1 | TL1 | Timer 1 reload L | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| 8C | 1 | TH0 | Timer 0 reload H | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | 00000000 | RW |
| 8D | 1 | TH1 | Timer 1 reload H | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | 00000000 | RW |
| 8E | 1 | CKCON[23] | Clock Control | x | x | T2M | T1M | T0M | MD2 | MD1 | MD0 | 00000001 | RW |
| 8F | 1 | reserved | | | | | | | | | | | |
| 90 | 1 | IOB[23] | Port B (bit addressable) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| 91 | 1 | EXIF[23] | External Interrupt Flag(s) | IE5 | IE4 | I²CINT | USBNT | 1 | 0 | 0 | 0 | 00001000 | RW |
| 92 | 1 | MPAGE[23] | Upper Addr Byte of MOVX using @R0 / @R1 | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | 00000000 | RW |
| 93 | 5 | reserved | | | | | | | | | | | |
| 98 | 1 | SCON0 | Serial Port 0 Control (bit addressable) | SM0_0 | SM1_0 | SM2_0 | REN_0 | TB8_0 | RB8_0 | TI_0 | RI_0 | 00000000 | RW |
| 99 | 1 | SBUF0 | Serial Port 0 Data Buffer | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| 9A | 1 | AUTOPTRH1[23] | Autopointer 1 Address H | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | 00000000 | RW |
| 9B | 1 | AUTOPTRL1[23] | Autopointer 1 Address L | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | 00000000 | RW |
| 9C | 1 | reserved | | | | | | | | | | | |
| 9D | 1 | AUTOPTRH2[23] | Autopointer 2 Address H | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | 00000000 | RW |
| 9E | 1 | AUTOPTRL2[23] | Autopointer 2 Address L | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | 00000000 | RW |
| 9F | 1 | reserved | | | | | | | | | | | |
| A0 | 1 | IOC[23] | Port C (bit addressable) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| A1 | 1 | INT2CLR[23] | Interrupt 2 clear | x | x | x | x | x | x | x | x | xxxxxxxx | W |
| A2 | 1 | INT4CLR[23] | Interrupt 4 clear | x | x | x | x | x | x | x | x | xxxxxxxx | W |
| A3 | 5 | reserved | | | | | | | | | | | |
| A8 | 1 | IE | Interrupt Enable (bit addressable) | EA | ES1 | ET2 | ES0 | ET1 | EX1 | ET0 | EX0 | 00000000 | RW |
| A9 | 1 | reserved | | | | | | | | | | | |
| AA | 1 | EP2468STAT[23] | Endpoint 2,4,6,8 status flags | EP8F | EP8E | EP6F | EP6E | EP4F | EP4E | EP2F | EP2E | 01011010 | R |
| AB | 1 | EP24FIFOFLGS [23] | Endpoint 2,4 slave FIFO status flags | 0 | EP4PF | EP4EF | EP4FF | 0 | EP2PF | EP2EF | EP2FF | 00100010 | R |
| AC | 1 | EP68FIFOFLGS [23] | Endpoint 6,8 slave FIFO status flags | 0 | EP8PF | EP8EF | EP8FF | 0 | EP6PF | EP6EF | EP6FF | 01100110 | R |
| AD | 2 | reserved | | | | | | | | | | | |
| AF | 1 | AUTOPTRSETUP[23] | Autopointer 1&2 setup | 0 | 0 | 0 | 0 | 0 | APTR2INC | APTR1INC | APTREN | 00000110 | RW |
| B0 | 1 | IOD[23] | Port D (bit addressable) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| B1 | 1 | IOE[23] | Port E (NOT bit addressable) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| B2 | 1 | OEA[23] | Port A Output Enable | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| B3 | 1 | OEB[23] | Port B Output Enable | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| B4 | 1 | OEC[23] | Port C Output Enable | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| B5 | 1 | OED[23] | Port D Output Enable | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| B6 | 1 | OEE[23] | Port E Output Enable | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| B7 | 1 | reserved | | | | | | | | | | | |
| B8 | 1 | IP | Interrupt Priority (bit addressable) | 1 | PS1 | PT2 | PS0 | PT1 | PX1 | PT0 | PX0 | 10000000 | RW |
| B9 | 1 | reserved | | | | | | | | | | | |

**Notes**
22. If no EEPROM is detected by the SIE then the default is 00000000.
23. SFRs not part of the standard 8051 architecture.

**Table 12. FX2LP Register Summary** (continued)

| Hex | Size | Name | Description | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Default | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BA | 1 | EP01STAT[24] | Endpoint 0&1 Status | 0 | 0 | 0 | 0 | 0 | EP1INBSY | EP1OUTBSY | EP0BSY | 00000000 | R |
| BB | 1 | GPIFTRIG[24, 25] | Endpoint 2,4,6,8 GPIF slave FIFO Trigger | DONE | 0 | 0 | 0 | 0 | RW | EP1 | EP0 | 10000xxx | brrrrbbb |
| BC | 1 | reserved | | | | | | | | | | | |
| BD | 1 | GPIFSGLDATH[24] | GPIF Data H (16-bit mode only) | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | xxxxxxxx | RW |
| BE | 1 | GPIFSGLDATLX[24] | GPIF Data L w/ Trigger | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| BF | 1 | GPIFSGLDATL-NOX[24] | GPIF Data L w/ No Trigger | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | R |
| C0 | 1 | SCON1[24] | Serial Port 1 Control (bit addressable) | SM0_1 | SM1_1 | SM2_1 | REN_1 | TB8_1 | RB8_1 | TI_1 | RI_1 | 00000000 | RW |
| C1 | 1 | SBUF1[24] | Serial Port 1 Data Buffer | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| C2 | 6 | reserved | | | | | | | | | | | |
| C8 | 1 | T2CON | Timer/Counter 2 Control (bit addressable) | TF2 | EXF2 | RCLK | TCLK | EXEN2 | TR2 | CT2 | CPRL2 | 00000000 | RW |
| C9 | 1 | reserved | | | | | | | | | | | |
| CA | 1 | RCAP2L | Capture for Timer 2, auto-reload, up-counter | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| CB | 1 | RCAP2H | Capture for Timer 2, auto-reload, up-counter | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| CC | 1 | TL2 | Timer 2 reload L | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| CD | 1 | TH2 | Timer 2 reload H | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | 00000000 | RW |
| CE | 2 | reserved | | | | | | | | | | | |
| D0 | 1 | PSW | Program Status Word (bit addressable) | CY | AC | F0 | RS1 | RS0 | OV | F1 | P | 00000000 | RW |
| D1 | 7 | reserved | | | | | | | | | | | |
| D8 | 1 | EICON[24] | External Interrupt Control | SMOD1 | 1 | ERESI | RESI | INT6 | 0 | 0 | 0 | 01000000 | RW |
| D9 | 7 | reserved | | | | | | | | | | | |
| E0 | 1 | ACC | Accumulator (bit addressable) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| E1 | 7 | reserved | | | | | | | | | | | |
| E8 | 1 | EIE[24] | External Interrupt Enable(s) | 1 | 1 | 1 | EX6 | EX5 | EX4 | EI²C | EUSB | 11100000 | RW |
| E9 | 7 | reserved | | | | | | | | | | | |
| F0 | 1 | B | B (bit addressable) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| F1 | 7 | reserved | | | | | | | | | | | |
| F8 | 1 | EIP[24] | External Interrupt Priority Control | 1 | 1 | 1 | PX6 | PX5 | PX4 | PI²C | PUSB | 11100000 | RW |
| F9 | 7 | reserved | | | | | | | | | | | |

R = all bits read-only
W = all bits write-only
r = read-only bit
w = write-only bit
b = both read/write bit

**Notes**
24. SFRs not part of the standard 8051 architecture.
25. Read and writes to these registers may require synchronization delay; see Technical Reference Manual for “Synchronization Delay”.

## Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power supplied (Commercial)..... 0 °C to +70 °C

Ambient temperature with power supplied (Industrial) ..... –40 °C to +105 °C

Supply voltage to ground potential .....–0.5 V to +4.0 V

DC input voltage to any input pin[26] ..... 5.25 V

DC voltage applied to outputs in high Z state ..... –0.5 V to $V_{CC}$ + 0.5 V

Power dissipation ..... 300 mW

Static discharge voltage .....>2000 V

Max output current, per I/O port ..... 10 mA

Max output current, all five I/O ports (128-pin and 100-pin packages) ..... 50 mA

## Operating Conditions

$T_A$ (ambient temperature under bias) Commercial ..... 0 °C to +70 °C

$T_A$ (ambient temperature under bias) Industrial ..... –40 °C to +105 °C

Supply voltage .....+3.00 V to +3.60 V

Ground voltage ..... 0 V

$F_{OSC}$ (oscillator or crystal frequency) .... 24 MHz ± 100 ppm, parallel resonant

## Thermal Characteristics

Maximum junction temperature ..... 125 °C

The following table displays the thermal characteristics of various packages:

**Table 13. Thermal Characteristics**

| Package | Ambient Temperature (°C) | $\theta_{Jc}$ Junction to Case Thermal Resistance (°C/W) | $\theta_{Ja}$ Junction to Ambient Thermal Resistance (°C/W) |
|---|---|---|---|
| 56 SSOP | 70 | 24.4 | 47.7 |
| 100 TQFP | 70 | 11.9 | 45.9 |
| 128 TQFP | 70 | 15.5 | 43.2 |
| 56 QFN | 70 | 10.6 | 25.2 |
| 56 VFBGA | 70 | 30.9 | 58.6 |

The junction temperature $\theta_j$, can be calculated using the following equation: $\theta_j = P^*\theta_{Ja} + \theta_a$

Where,

P = Power

$\theta_{Ja}$ = Junction to ambient temperature ($\theta_{Jc} + \theta_{Ca}$)

$\theta_a$ = Ambient temperature (70 °C)

The case temperature $\theta_c$, can be calculated using the following equation: $\theta_c = P^*\theta_{Ca} + \theta_a$

where,

P = Power

$\theta_{Ca}$ = Case to ambient temperature

$\theta_a$ = Ambient temperature (70 °C)

**Note**
26. Do not power I/O with the chip power OFF.

## DC Electrical Characteristics

**Table 14. DC Characteristics**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VCC | Supply voltage | – | 3.00 | 3.3 | 3.60 | V |
| VCC Ramp Up | 0 to 3.3 V | – | 200 | – | – | µs |
| $V_{IH}$ | Input HIGH voltage | – | 2 | – | 5.25 | V |
| $V_{IL}$ | Input LOW voltage | – | –0.5 | – | 0.8 | V |
| $V_{IH_X}$ | Crystal input HIGH voltage | – | 2 | – | 5.25 | V |
| $V_{IL_X}$ | Crystal input LOW voltage | – | –0.5 | – | 0.8 | V |
| $I_I$ | Input leakage current | $0 < V_{IN} < V_{CC}$ | – | – | ±10 | µA |
| $V_{OH}$ | Output voltage HIGH | $I_{OUT}$ = 4 mA | 2.4 | – | – | V |
| $V_{OL}$ | Output LOW voltage | $I_{OUT}$ = –4 mA | – | – | 0.4 | V |
| $I_{OH}$ | Output current HIGH | – | – | – | 4 | mA |
| $I_{OL}$ | Output current LOW | – | – | – | 4 | mA |
| $C_{IN}$ | Input pin capacitance | Except D+/D– | – | – | 10 | pF |
| | | D+/D– | – | – | 15 | pF |
| $I_{SUSP}$ | Suspend current CY7C68014/CY7C68016 | Connected | – | 300 | 380[27] | µA |
| | | Disconnected | – | 100 | 150[27] | µA |
| | Suspend current CY7C68013/CY7C68015 | Connected | – | 0.5 | 1.2[27] | mA |
| | | Disconnected | – | 0.3 | 1.0[27] | mA |
| $I_{CC}$ | Supply current | 8051 running, connected to USB HS | – | 50 | 85 | mA |
| | | 8051 running, connected to USB FS | – | 35 | 65 | mA |
| $T_{RESET}$ | Reset time after valid power | $V_{CC}$ min = 3.0 V | 5.0 | – | – | ms |
| | Pin reset after powered on | | 200 | – | – | µs |

### USB Transceiver

USB 2.0 compliant in Full Speed and Hi-Speed modes.

**Note**
27. Measured at Max $V_{CC}$, 25 °C.

## AC Electrical Characteristics

### USB Transceiver

USB 2.0 compliant in Full-Speed and Hi-Speed modes.

### Program Memory Read

**Figure 12. Program Memory Read Timing Diagram**

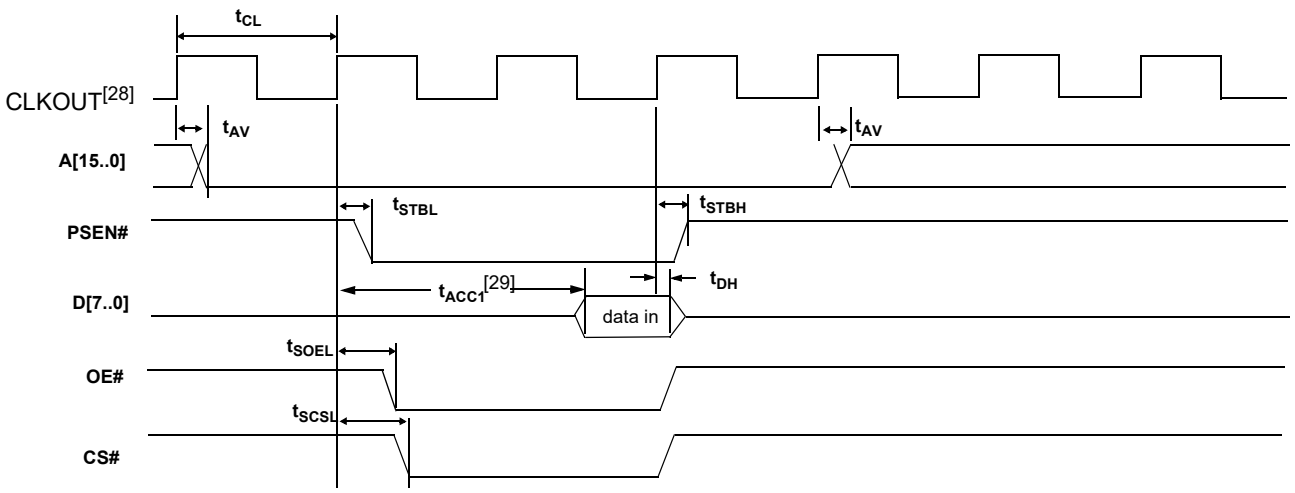



**Table 15. Program Memory Read Parameters**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{CL}$ | 1/CLKOUT frequency | – | 20.83 | – | ns | 48 MHz |
| | | – | 41.66 | – | ns | 24 MHz |
| | | – | 83.2 | – | ns | 12 MHz |
| $t_{AV}$ | Delay from clock to valid address | 0 | – | 10.7 | ns | – |
| $t_{STBL}$ | Clock to PSEN LOW | 0 | – | 8 | ns | – |
| $t_{STBH}$ | Clock to PSEN HIGH | 0 | – | 8 | ns | – |
| $t_{SOEL}$ | Clock to OE LOW | – | – | 11.1 | ns | – |
| $t_{SCSL}$ | Clock to CS LOW | – | – | 13 | ns | – |
| $t_{DSU}$ | Data setup to clock | 9.6 | – | – | ns | – |
| $t_{DH}$ | Data hold time | 0 | – | – | ns | – |

**Notes**
28. CLKOUT is shown with positive polarity.
29. $t_{ACC1}$ is computed from these parameters as follows:
$t_{ACC1}$(24 MHz) = 3*$t_{CL}$ – $t_{AV}$ – $t_{DSU}$ = 106 ns.
$t_{ACC1}$(48 MHz) = 3*$t_{CL}$ – $t_{AV}$ – $t_{DSU}$ = 43 ns.

## Data Memory Read[30]

**Figure 13. Data Memory Read Timing Diagram**

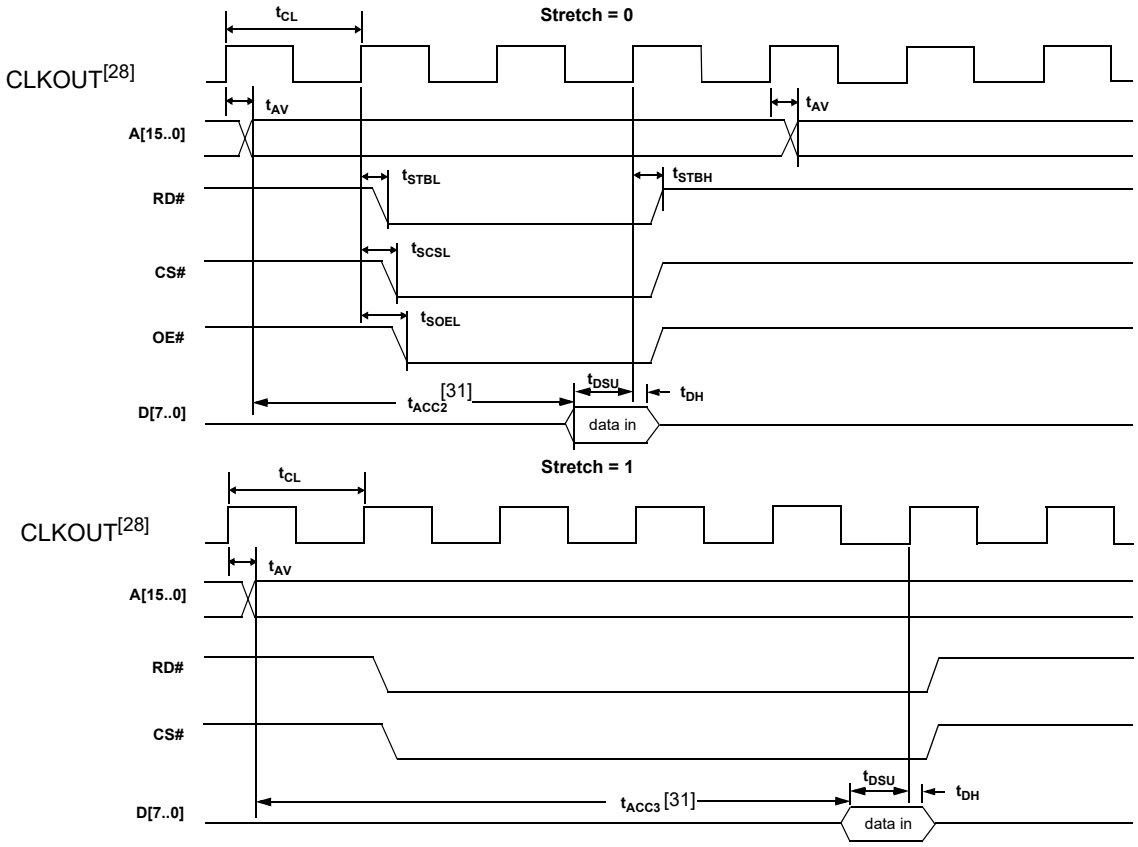



**Table 16. Data Memory Read Parameters**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{CL}$ | 1/CLKOUT frequency | – | 20.83 | – | ns | 48 MHz |
| | | – | 41.66 | – | ns | 24 MHz |
| | | – | 83.2 | – | ns | 12 MHz |
| $t_{AV}$ | Delay from clock to valid address | – | – | 10.7 | ns | – |
| $t_{STBL}$ | Clock to RD LOW | – | – | 11 | ns | – |
| $t_{STBH}$ | Clock to RD HIGH | – | – | 11 | ns | – |
| $t_{SCSL}$ | Clock to CS LOW | – | – | 13 | ns | – |
| $t_{SOEL}$ | Clock to OE LOW | – | – | 11.1 | ns | – |
| $t_{DSU}$ | Data setup to clock | 9.6 | – | – | ns | – |
| $t_{DH}$ | Data hold time | 0 | – | – | ns | – |

When using the AUTPOPTR1 or AUTOPTR2 to address external memory, the address of AUTOPTR1 is only active while either RD# or WR# is active. The address of AUTOPTR2 is active throughout the cycle and meets the address valid time for which is based on the stretch value.

**Notes**

30. The stretch memory cycle feature enables EZ-USB firmware to adjust the speed of data memory accesses not the program memory accesses. Details including typical strobe width timings can be found in the section 12.1.2 of the Technical Reference Manual. The address cycle width can be interpreted from these.
31. $t_{ACC2}$ and $t_{ACC3}$ are computed from these parameters as follows:
$t_{ACC2}$(24 MHz) = $3*t_{CL} – t_{AV} – t_{DSU}$ = 106 ns
$t_{ACC2}$(48 MHz) = $3*t_{CL} – t_{AV} – t_{DSU}$ = 43 ns
$t_{ACC3}$(24 MHz) = $5*t_{CL} – t_{AV} – t_{DSU}$ = 190 ns
$t_{ACC3}$(48 MHz) = $5*t_{CL} – t_{AV} – t_{DSU}$ = 86 ns.

## Data Memory Write[32]

**Figure 14. Data Memory Write Timing Diagram**

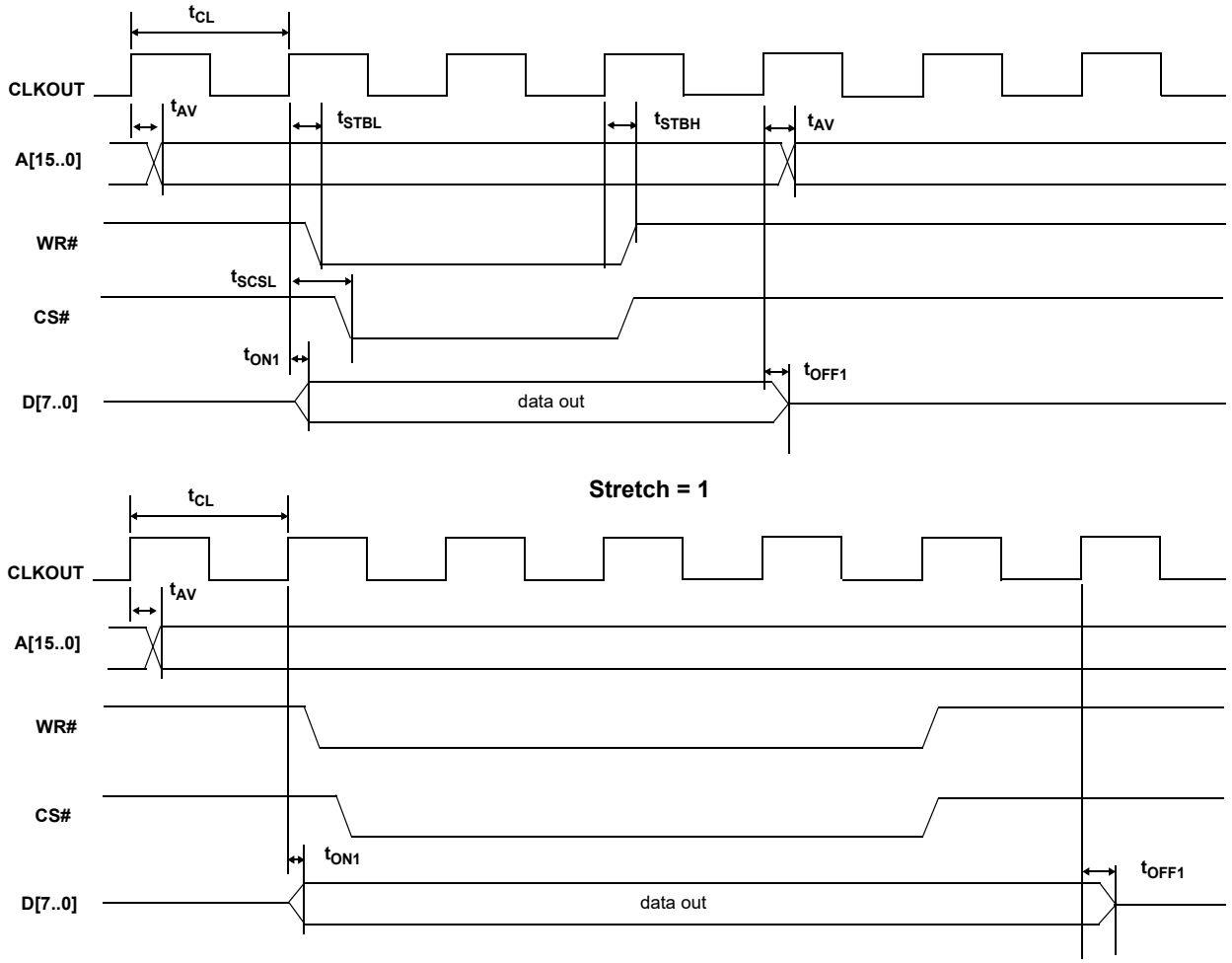



**Table 17. Data Memory Write Parameters**

| Parameter | Description | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $t_{AV}$ | Delay from clock to valid address | 0 | 10.7 | ns | – |
| $t_{STBL}$ | Clock to WR pulse LOW | 0 | 11.2 | ns | – |
| $t_{STBH}$ | Clock to WR pulse HIGH | 0 | 11.2 | ns | – |
| $t_{SCSL}$ | Clock to CS pulse LOW | – | 13.0 | ns | – |
| $t_{ON1}$ | Clock to data turn-on | 0 | 13.1 | ns | – |
| $t_{OFF1}$ | Clock to data hold time | 0 | 13.1 | ns | – |

When using the AUTPOPTR1 or AUTOPTR2 to address external memory, the address of AUTOPTR1 is only active while either RD# or WR# are active. The address of AUTOPTR2 is active throughout the cycle and meets the address valid time for which is based on the stretch value.

**Note**

32. The stretch memory cycle feature enables EZ-USB firmware to adjust the speed of data memory accesses not the program memory accesses. Details including typical strobe width timings can be found in the section 12.1.2 of the Technical Reference Manual. The address cycle width can be interpreted from these.

## PORTC Strobe Feature Timings

The RD# and WR# are present in the 100-pin version and the 128-pin package. In these 100-pin and 128-pin versions, an 8051 control bit can be set to pulse the RD# and WR# pins when the 8051 reads from or writes to PORTC. This feature is enabled by setting PORTCSTB bit in CPUCS register.

The RD# and WR# strobes are asserted for two CLKOUT cycles when PORTC is accessed.

The WR# strobe is asserted two clock cycles after PORTC is updated and is active for two clock cycles after that, as shown in Figure 16.

As for read, the value of PORTC three clock cycles before the assertion of RD# is the value that the 8051 reads in. The RD# is pulsed for two clock cycles after three clock cycles from the point when the 8051 has performed a read function on PORTC.

The RD# signal prompts the external logic to prepare the next data byte. Nothing gets sampled internally on assertion of the RD# signal itself; it is just a prefetch type signal to get the next data byte prepared. So, using it with that in mind easily meets the setup time to the next read.

The purpose of this pulsing of RD# is to allow the external peripheral to know that the 8051 is done reading PORTC and the data was latched into PORTC three CLKOUT cycles before asserting the RD# signal. After the RD# is pulsed, the external logic can update the data on PORTC.

Following is the timing diagram of the read and write strobing function on accessing PORTC. Refer to Data Memory Read[30] on page 44 and Data Memory Write[32] on page 45 for details on propagation delay of RD# and WR# signals.

**Figure 16. WR# Strobe Function when PORTC is Accessed by 8051**

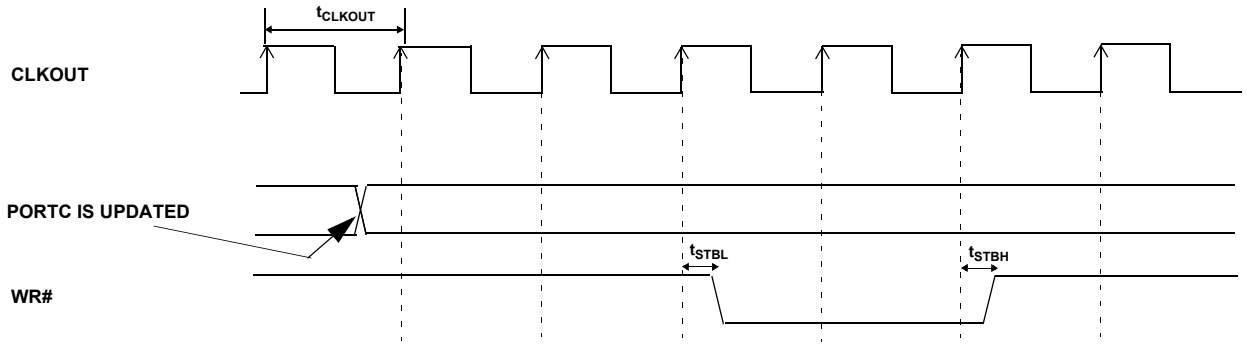
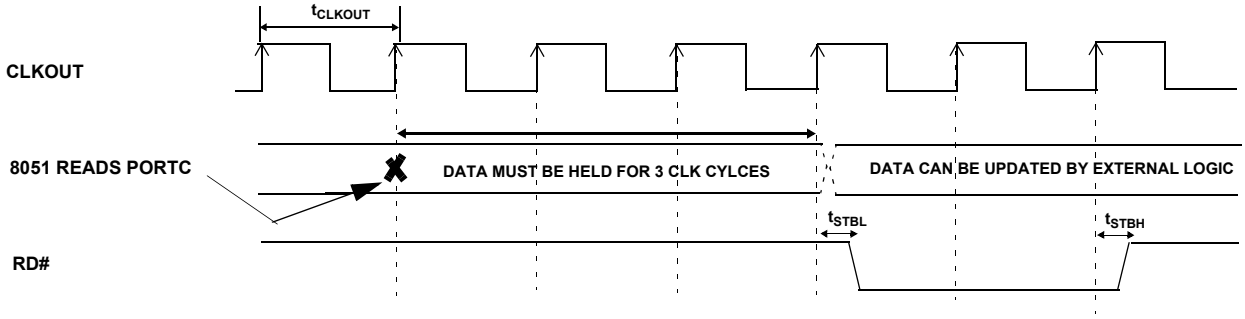



**Figure 17. RD# Strobe Function when PORTC is Accessed by 8051**



## GPIF Synchronous Signals

**Figure 18. GPIF Synchronous Signals Timing Diagram** [33]

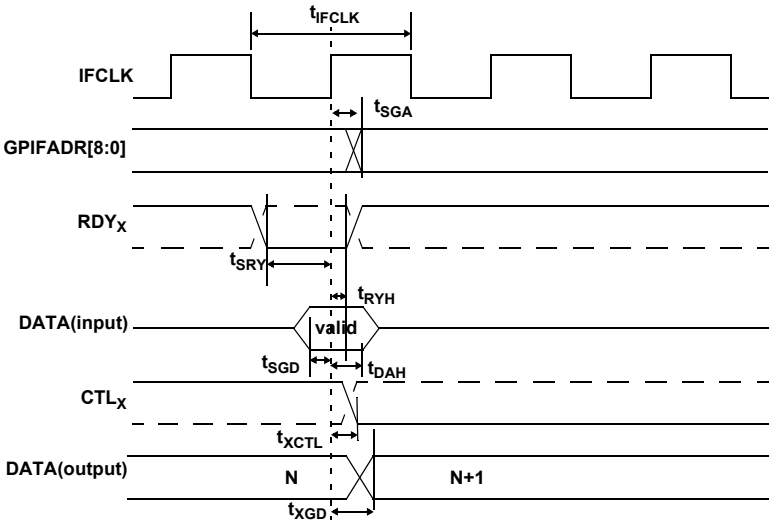



**Table 18. GPIF Synchronous Signals Parameters with Internally Sourced IFCLK**[33, 34]

| Parameter | Description | Min | Max | Typ | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $t_{IFCLK}$ | IFCLK Period | 20.83 | – | – | – | ns |
| $t_{SRY}$ | $RDY_X$ to clock setup time | 8.9 | – | – | – | ns |
| $t_{RYH}$ | $RDY_X$ Hold Time | 0 | – | – | – | ns |
| $t_{SGD}$ | GPIF data to clock setup time | 9.2 | – | – | – | ns |
| $t_{DAH}$ | GPIF data hold time | 0 | – | – | – | ns |
| $t_{SGA}$ | Clock to GPIF address propagation delay | – | 7.5 | – | – | ns |
| $t_{XGD}$ | Clock to GPIF data output propagation delay | – | 10 | – | – | ns |
| $t_{XCTL}$ | Clock to $CTL_X$ output propagation delay | – | 6.7 | – | – | ns |
| $t_{IFCLKR}$ | IFCLK rise time | – | – | – | 900 | ps |
| $t_{IFCLKF}$ | IFCLK fall time | – | – | – | 900 | ps |
| $t_{IFCLKOD}$ | IFCLK output duty cycle | – | – | 49 | 51 | % |
| $t_{IFCLKJ}$ | IFCLK jitter peak to peak | – | – | – | 300 | ps |

**Table 19. GPIF Synchronous Signals Parameters with Externally Sourced IFCLK**[34]

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{IFCLK}$ | IFCLK period[35] | 20.83 | 200 | ns |
| $t_{SRY}$ | $RDY_X$ to clock setup time | 2.9 | – | ns |
| $t_{RYH}$ | $RDY_X$ Hold Time | 3.7 | – | ns |
| $t_{SGD}$ | GPIF data to clock setup time | 3.2 | – | ns |
| $t_{DAH}$ | GPIF data hold time | 4.5 | – | ns |
| $t_{SGA}$ | Clock to GPIF address propagation delay | – | 11.5 | ns |
| $t_{XGD}$ | Clock to GPIF data output propagation delay | – | 15 | ns |
| $t_{XCTL}$ | Clock to $CTL_X$ output propagation delay | – | 10.7 | ns |

**Notes**
33. Dashed lines denote signals with programmable polarity.
34. GPIF asynchronous $RDY_x$ signals have a minimum setup time of 50 ns when using the internal 48-MHz IFCLK.
35. IFCLK must not exceed 48 MHz.

## Slave FIFO Synchronous Read

**Figure 19. Slave FIFO Synchronous Read Timing Diagram** [36]

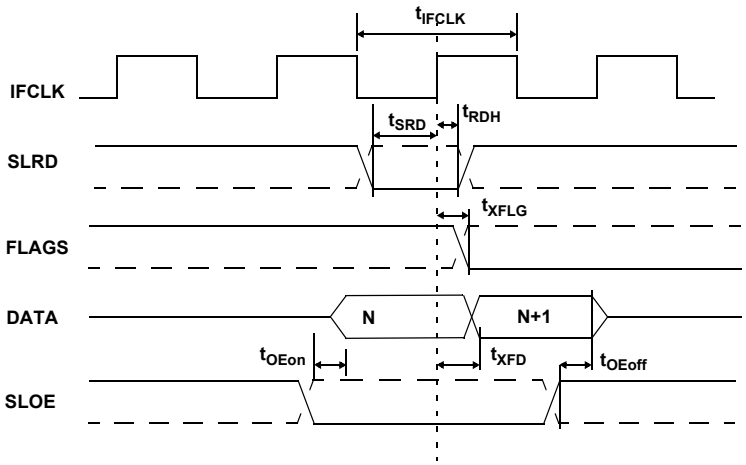



**Table 20. Slave FIFO Synchronous Read Parameters with Internally Sourced IFCLK**[37]

| Parameter | Description | Min | Max | Typ | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $t_{IFCLK}$ | IFCLK period | 20.83 | – | – | – | ns |
| $t_{SRD}$ | SLRD to clock setup time | 18.7 | – | – | – | ns |
| $t_{RDH}$ | Clock to SLRD hold time | 0 | – | – | – | ns |
| $t_{OEon}$ | SLOE turn on to FIFO data valid | – | 10.5 | – | – | ns |
| $t_{OEoff}$ | SLOE turn off to FIFO data hold | – | 10.5 | – | – | ns |
| $t_{XFLG}$ | Clock to FLAGS output propagation delay | – | 9.5 | – | – | ns |
| $t_{XFD}$ | Clock to FIFO data output propagation delay | – | 11 | – | – | ns |
| $t_{IFCLKR}$ | IFCLK rise time | – | – | – | 900 | ps |
| $t_{IFCLKF}$ | IFCLK fall time | – | – | – | 900 | ps |
| $t_{IFCLKOD}$ | IFCLK output duty cycle | – | – | 49 | 51 | % |
| $t_{IFCLKJ}$ | IFCLK jitter peak to peak | – | – | – | 300 | ps |

**Table 21. Slave FIFO Synchronous Read Parameters with Externally Sourced IFCLK**[37]

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{IFCLK}$ | IFCLK period | 20.83 | 200 | ns |
| $t_{SRD}$ | SLRD to clock setup time | 12.7 | – | ns |
| $t_{RDH}$ | Clock to SLRD hold time | 3.7 | – | ns |
| $t_{OEon}$ | SLOE turn on to FIFO data valid | – | 10.5 | ns |
| $t_{OEoff}$ | SLOE turn off to FIFO data hold | – | 10.5 | ns |
| $t_{XFLG}$ | Clock to FLAGS output propagation delay | – | 13.5 | ns |
| $t_{XFD}$ | Clock to FIFO data output propagation delay | – | 15 | ns |

**Notes**
36. Dashed lines denote signals with programmable polarity.
37. GPIF asynchronous $RDY_x$ signals have a minimum setup time of 50 ns when using the internal 48-MHz IFCLK.

## Slave FIFO Asynchronous Read

**Figure 20. Slave FIFO Asynchronous Read Timing Diagram** [38]

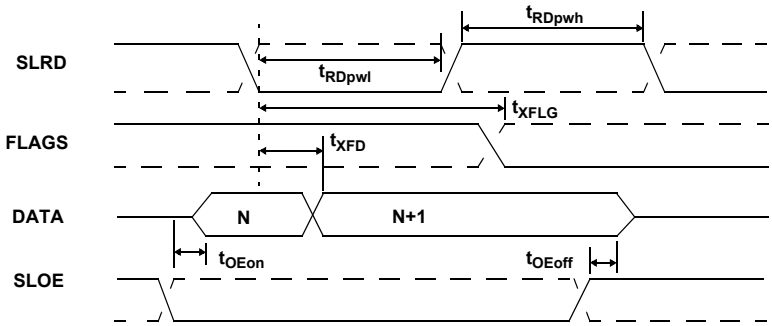



**Table 22. Slave FIFO Asynchronous Read Parameters**[39]

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{RDpwl}$ | SLRD pulse width LOW | 50 | – | ns |
| $t_{RDpwh}$ | SLRD pulse width HIGH | 50 | – | ns |
| $t_{XFLG}$ | SLRD to FLAGS output propagation delay | – | 70 | ns |
| $t_{XFD}$ | SLRD to FIFO data output propagation delay | – | 15 | ns |
| $t_{OEon}$ | SLOE turn-on to FIFO data valid | – | 10.5 | ns |
| $t_{OEoff}$ | SLOE turn-off to FIFO data hold | – | 10.5 | ns |

**Notes**
38. Dashed lines denote signals with programmable polarity.
39. Slave FIFO asynchronous parameter values use internal IFCLK setting at 48 MHz.

## Slave FIFO Synchronous Write

**Figure 21. Slave FIFO Synchronous Write Timing Diagram** [40]

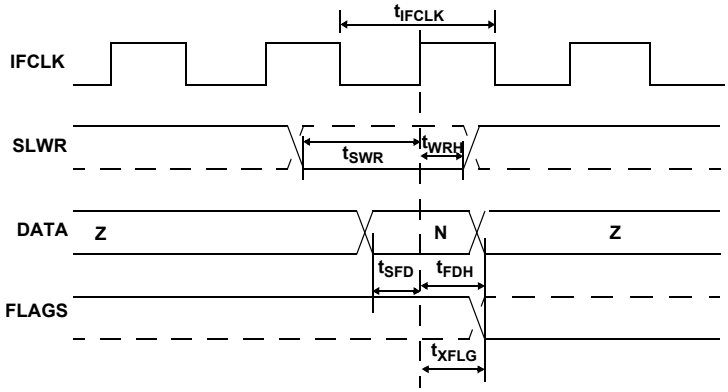



**Table 23. Slave FIFO Synchronous Write Parameters with Internally Sourced IFCLK**[41]

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{IFCLK}$ | IFCLK period | 20.83 | – | ns |
| $t_{SWR}$ | SLWR to clock setup time | 10.4 | – | ns |
| $t_{WRH}$ | Clock to SLWR hold time | 0 | – | ns |
| $t_{SFD}$ | FIFO data to clock setup time | 9.2 | – | ns |
| $t_{FDH}$ | Clock to FIFO data hold time | 0 | – | ns |
| $t_{XFLG}$ | Clock to FLAGS output propagation time | – | 9.5 | ns |

**Table 24. Slave FIFO Synchronous Write Parameters with Externally Sourced IFCLK**[41]

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{IFCLK}$ | IFCLK Period | 20.83 | 200 | ns |
| $t_{SWR}$ | SLWR to clock setup time | 12.1 | – | ns |
| $t_{WRH}$ | Clock to SLWR hold time | 3.6 | – | ns |
| $t_{SFD}$ | FIFO data to clock setup time | 3.2 | – | ns |
| $t_{FDH}$ | Clock to FIFO data hold time | 4.5 | – | ns |
| $t_{XFLG}$ | Clock to FLAGS output propagation time | – | 13.5 | ns |

**Notes**
40. Dashed lines denote signals with programmable polarity.
41. GPIF asynchronous $RDY_x$ signals have a minimum setup time of 50 ns when using the internal 48-MHz IFCLK.

## Slave FIFO Asynchronous Write

**Figure 22. Slave FIFO Asynchronous Write Timing Diagram** [42]

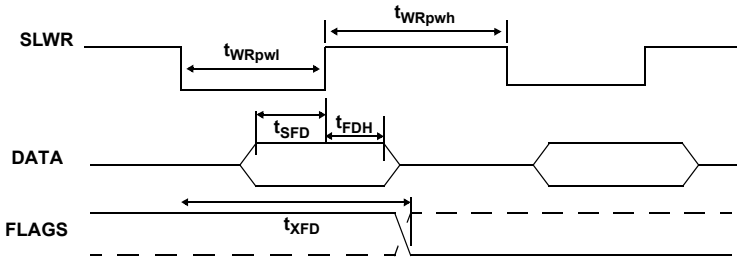



**Table 25. Slave FIFO Asynchronous Write Parameters with Internally Sourced IFCLK**[43]

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{WRpwl}$ | SLWR pulse LOW | 50 | – | ns |
| $t_{WRpwh}$ | SLWR pulse HIGH | 70 | – | ns |
| $t_{SFD}$ | SLWR to FIFO DATA setup time | 10 | – | ns |
| $t_{FDH}$ | FIFO DATA to SLWR hold time | 10 | – | ns |
| $t_{XFD}$ | SLWR to FLAGS output propagation delay | – | 70 | ns |

**Notes**
42. Dashed lines denote signals with programmable polarity.
43. Slave FIFO asynchronous parameter values use internal IFCLK setting at 48 MHz.

## Slave FIFO Synchronous Packet End Strobe

**Figure 23. Slave FIFO Synchronous Packet End Strobe Timing Diagram [44]**

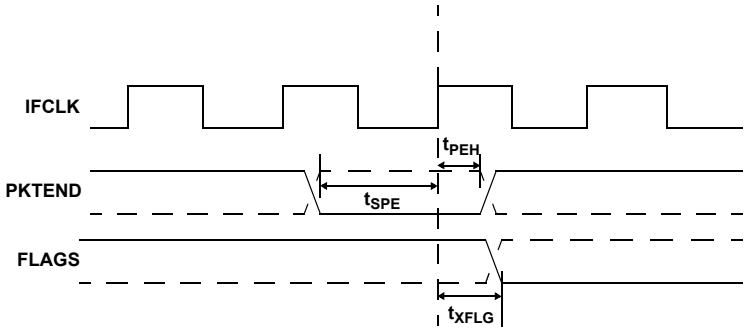



**Table 26. Slave FIFO Synchronous Packet End Strobe Parameters with Internally Sourced IFCLK[45]**

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{IFCLK}$ | IFCLK period | 20.83 | – | ns |
| $t_{SPE}$ | PKTEND to clock setup time | 14.6 | – | ns |
| $t_{PEH}$ | Clock to PKTEND hold time | 0 | – | ns |
| $t_{XFLG}$ | Clock to FLAGS output propagation delay | – | 9.5 | ns |

**Table 27. Slave FIFO Synchronous Packet End Strobe Parameters with Externally Sourced IFCLK[45]**

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{IFCLK}$ | IFCLK period | 20.83 | 200 | ns |
| $t_{SPE}$ | PKTEND to clock setup time | 8.6 | – | ns |
| $t_{PEH}$ | Clock to PKTEND hold time | 2.5 | – | ns |
| $t_{XFLG}$ | Clock to FLAGS output propagation delay | – | 13.5 | ns |

**Notes**
44. Dashed lines denote signals with programmable polarity.
45. GPIF asynchronous $RDY_x$ signals have a minimum setup time of 50 ns when using the internal 48-MHz IFCLK.

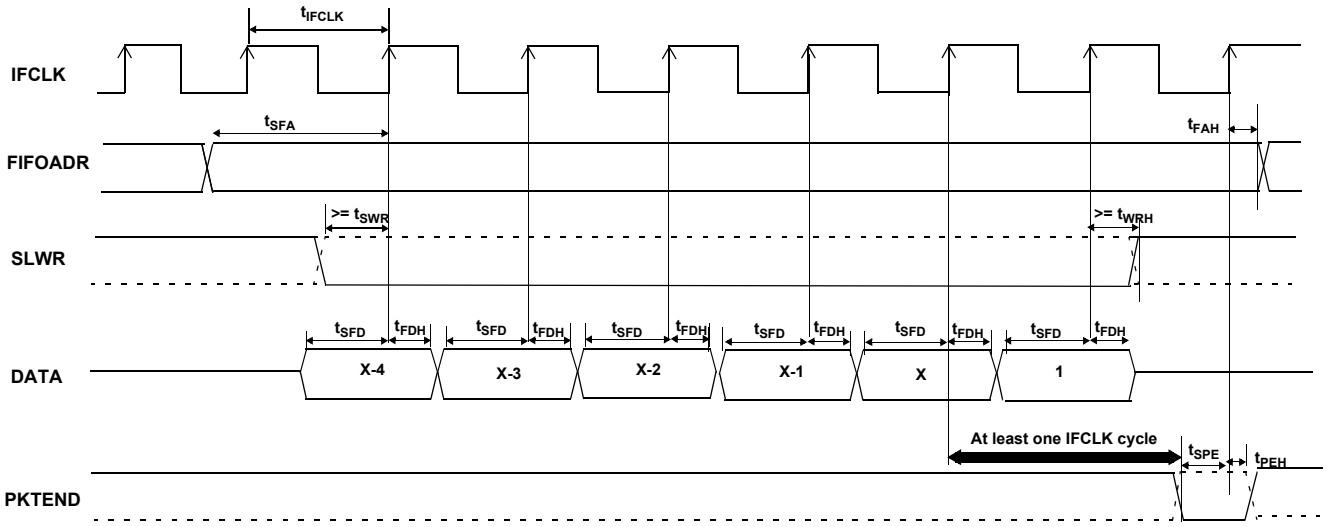
There is no specific timing requirement that should be met for asserting the PKTEND pin to asserting SLWR. PKTEND can be asserted with the last data value clocked into the FIFOs or thereafter. The setup time $t_{SPE}$ and the hold time $t_{PEH}$ must be met.

Although there are no specific timing requirements for PKTEND assertion, there is a specific corner-case condition that needs attention while using the PKTEND pin to commit a one byte or word packet. There is an additional timing requirement that needs to be met when the FIFO is configured to operate in auto mode and it is required to send two packets back to back: a full packet (full defined as the number of bytes in the FIFO meeting the level set in AUTOINLEN register) committed automatically followed by a short one byte or word packet committed manually using the PKTEND pin. In this scenario, the user must ensure to assert PKTEND, at least one clock cycle after the rising edge that caused the last byte or word to be clocked into the previous auto committed packet. Figure 24 shows this scenario. X is the value the AUTOINLEN register is set to when the IN endpoint is configured to be in auto mode.

Figure 24 shows a scenario where two packets are committed. The first packet gets committed automatically when the number of bytes in the FIFO reaches X (value set in AUTOINLEN register) and the second one byte/word short packet being committed manually using PKTEND.

Note that there is at least one IFCLK cycle timing between the assertion of PKTEND and clocking of the last byte of the previous packet (causing the packet to be committed automatically). Failing to adhere to this timing results in the FX2 failing to send the one byte or word short packet.

**Figure 24. Slave FIFO Synchronous Write Sequence and Timing Diagram**[46]




**Note**
46. Dashed lines denote signals with programmable polarity.

## Slave FIFO Asynchronous Packet End Strobe

**Figure 25. Slave FIFO Asynchronous Packet End Strobe Timing Diagram[47]**

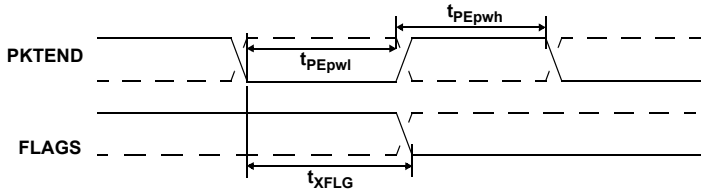



**Table 28. Slave FIFO Asynchronous Packet End Strobe Parameters[48]**

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{PEpwl}$ | PKTEND pulse width LOW | 50 | – | ns |
| $t_{PWpwh}$ | PKTEND pulse width HIGH | 50 | – | ns |
| $t_{XFLG}$ | PKTEND to FLAGS output propagation delay | – | 115 | ns |

## Slave FIFO Output Enable

**Figure 26. Slave FIFO Output Enable Timing Diagram[47]**

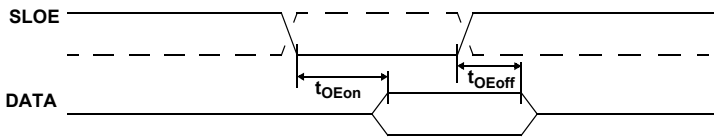



**Table 29. Slave FIFO Output Enable Parameters**

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{OEon}$ | SLOE assert to FIFO DATA output | – | 10.5 | ns |
| $t_{OEoff}$ | SLOE deassert to FIFO DATA hold | – | 10.5 | ns |

## Slave FIFO Address to Flags/Data

**Figure 27. Slave FIFO Address to Flags/Data Timing Diagram[47]**

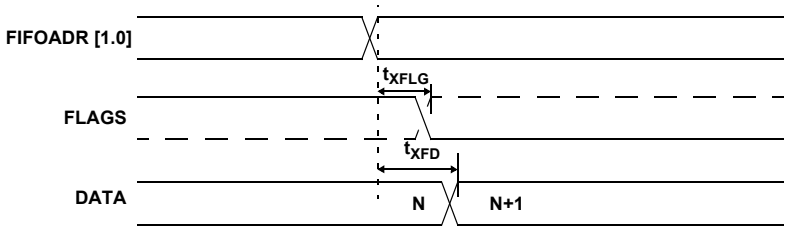



**Table 30. Slave FIFO Address to Flags/Data Parameters**

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{XFLG}$ | FIFOADR[1:0] to FLAGS output propagation delay | – | 10.7 | ns |
| $t_{XFD}$ | FIFOADR[1:0] to FIFODATA output propagation delay | – | 14.3 | ns |

**Notes**
47. Dashed lines denote signals with programmable polarity.
48. Slave FIFO asynchronous parameter values use internal IFCLK setting at 48 MHz.

## Slave FIFO Synchronous Address

**Figure 28. Slave FIFO Synchronous Address Timing Diagram[49]**

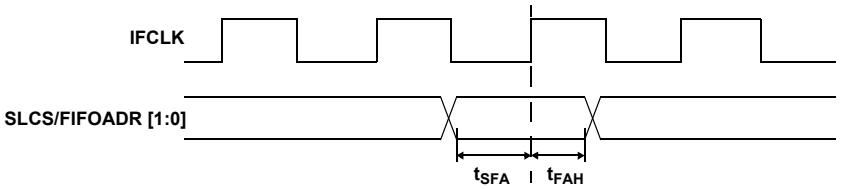



**Table 31. Slave FIFO Synchronous Address Parameters[50]**

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{IFCLK}$ | Interface clock period | 20.83 | 200 | ns |
| $t_{SFA}$ | FIFOADR[1:0] to clock setup time | 25 | – | ns |
| $t_{FAH}$ | Clock to FIFOADR[1:0] hold time | 10 | – | ns |

## Slave FIFO Asynchronous Address

**Figure 29. Slave FIFO Asynchronous Address Timing Diagram [49]**

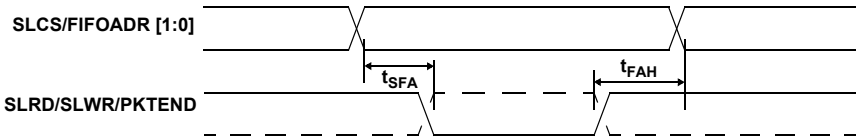



**Table 32. Slave FIFO Asynchronous Address Parameters[51]**

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{SFA}$ | FIFOADR[1:0] to SLRD/SLWR/PKTEND setup time | 10 | – | ns |
| $t_{FAH}$ | RD/WR/PKTEND to FIFOADR[1:0] hold time | 10 | – | ns |

**Notes**
49. Dashed lines denote signals with programmable polarity.
50. GPIF asynchronous $RDY_x$ signals have a minimum setup time of 50 ns when using the internal 48-MHz IFCLK.
51. Slave FIFO asynchronous parameter values use internal IFCLK setting at 48 MHz.

## Sequence Diagram

*Single and Burst Synchronous Read Example*

**Figure 30. Slave FIFO Synchronous Read Sequence and Timing Diagram**[52]

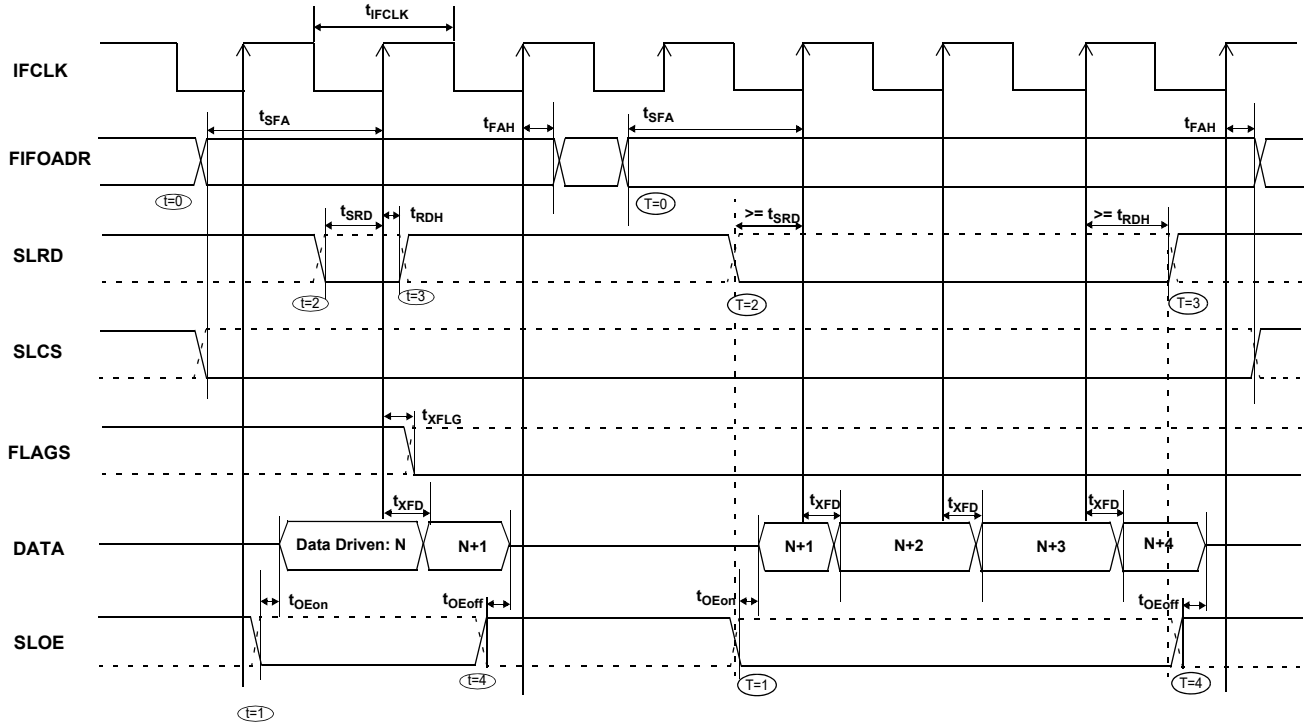



**Figure 31. Slave FIFO Synchronous Sequence of Events Diagram**

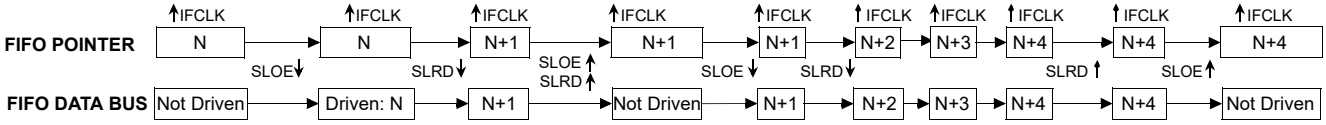



Figure 30 shows the timing relationship of the SLAVE FIFO signals during a synchronous FIFO read using IFCLK as the synchronizing clock. The diagram illustrates a single read followed by a burst read.

- At t = 0, the FIFO address is stable and the signal SLCS is asserted (SLCS may be tied LOW in some applications). Note that $t_{SFA}$ has a minimum of 25 ns. This means that when IFCLK is running at 48 MHz, the FIFO address setup time is more than one IFCLK cycle.
- At t = 1, SLOE is asserted. SLOE is an output enable only, whose sole function is to drive the data bus. The data that is driven on the bus is the data that the internal FIFO pointer is currently pointing to. In this example it is the first data value in the FIFO. **Note**: the data is prefetched and is driven on the bus when SLOE is asserted.
- At t = 2, SLRD is asserted. SLRD must meet the setup time of $t_{SRD}$ (time from asserting the SLRD signal to the rising edge of the IFCLK) and maintain a minimum hold time of $t_{RDH}$ (time from the IFCLK edge to the deassertion of the SLRD signal). If the SLCS signal is used, it must be asserted before SLRD is asserted (The SLCS and SLRD signals must both be asserted to start a valid read condition).
- The FIFO pointer is updated on the rising edge of the IFCLK, while SLRD is asserted. This starts the propagation of data from the newly addressed location to the data bus. After a propagation delay of $t_{XFD}$ (measured from the rising edge of IFCLK) the new data value is present. N is the first data value read from the FIFO. To have data on the FIFO data bus, SLOE MUST also be asserted.

The same sequence of events are shown for a burst read and are marked with the time indicators of T = 0 through 5.

**Note** For the burst mode, the SLRD and SLOE are left asserted during the entire duration of the read. In the burst read mode, when SLOE is asserted, data indexed by the FIFO pointer is on the data bus. During the first read cycle, on the rising edge of the clock, the FIFO pointer is updated and incremented to point to address N+1. For each subsequent rising edge of IFCLK, while the SLRD is asserted, the FIFO pointer is incremented and the next data value is placed on the data bus.

**Note**
52. Dashed lines denote signals with programmable polarity.

*Single and Burst Synchronous Write*

**Figure 32. Slave FIFO Synchronous Write Sequence and Timing Diagram**[53]

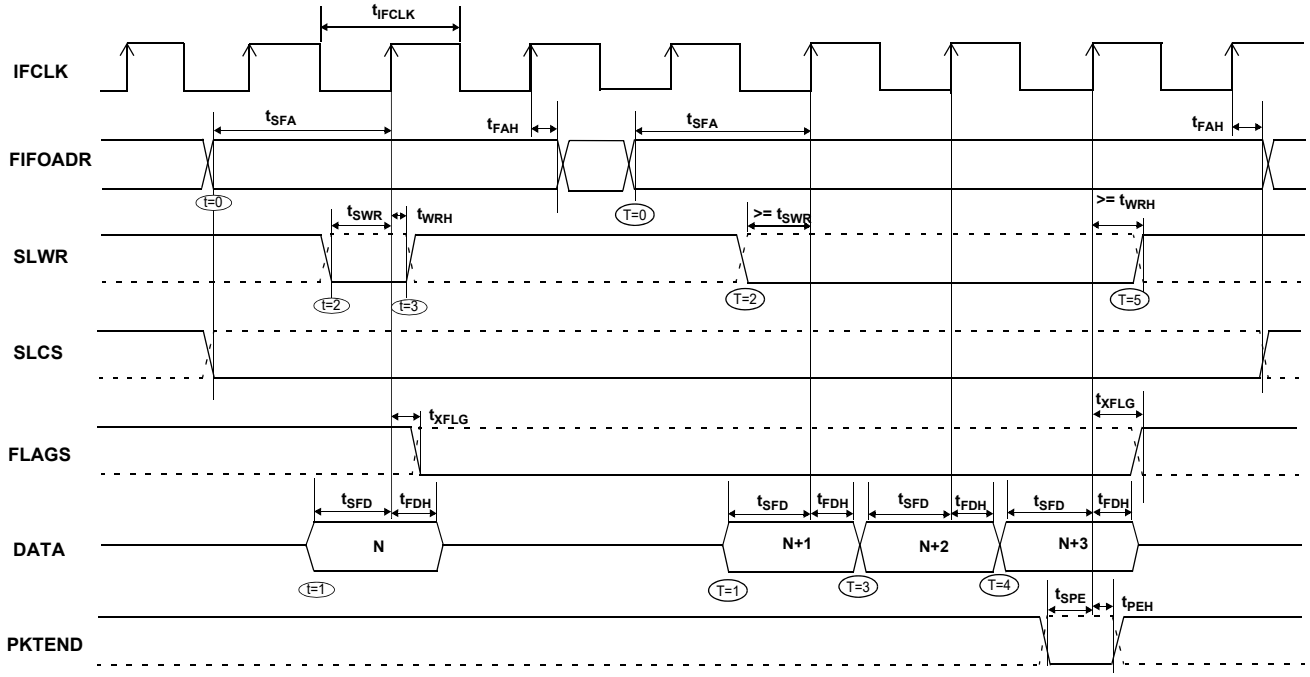



Figure 32 shows the timing relationship of the SLAVE FIFO signals during a synchronous write using IFCLK as the synchronizing clock. The diagram illustrates a single write followed by burst write of three bytes and committing all four bytes as a short packet using the PKTEND pin.

- At t = 0 the FIFO address is stable and the signal SLCS is asserted. (SLCS may be tied LOW in some applications) Note that $t_{SFA}$ has a minimum of 25 ns. This means when IFCLK is running at 48 MHz, the FIFO address setup time is more than one IFCLK cycle.
- At t = 1, the external master/peripheral must outputs the data value onto the data bus with a minimum set up time of $t_{SFD}$ before the rising edge of IFCLK.
- At t = 2, SLWR is asserted. The SLWR must meet the setup time of $t_{SWR}$ (time from asserting the SLWR signal to the rising edge of IFCLK) and maintain a minimum hold time of $t_{WRH}$ (time from the IFCLK edge to the deassertion of the SLWR signal). If the SLCS signal is used, it must be asserted with SLWR or before SLWR is asserted (The SLCS and SLWR signals must both be asserted to start a valid write condition).
- While the SLWR is asserted, data is written to the FIFO and on the rising edge of the IFCLK, the FIFO pointer is incremented. The FIFO flag is also updated after a delay of $t_{XFLG}$ from the rising edge of the clock.

The same sequence of events are also shown for a burst write and are marked with the time indicators of T = 0 through 5.

**Note** For the burst mode, SLWR and SLCS are left asserted for the entire duration of writing all the required data values. In this burst write mode, after the SLWR is asserted, the data on the FIFO data bus is written to the FIFO on every rising edge of IFCLK. The FIFO pointer is updated on each rising edge of IFCLK. In Figure 32, after the four bytes are written to the FIFO, SLWR is deasserted. The short 4 byte packet can be committed to the host by asserting the PKTEND signal.

There is no specific timing requirement that should be met for asserting PKTEND signal with regards to asserting the SLWR signal. PKTEND can be asserted with the last data value or thereafter. The only requirement is that the setup time $t_{SPE}$ and the hold time $t_{PEH}$ must be met. In the scenario of Figure 32, the number of data values committed includes the last value written to the FIFO. In this example, both the data value and the PKTEND signal are clocked on the same rising edge of IFCLK. PKTEND can also be asserted in subsequent clock cycles. The FIFOADDR lines should be held constant during the PKTEND assertion.

Although there are no specific timing requirement for the PKTEND assertion, there is a specific corner-case condition that needs attention while using the PKTEND to commit a one byte/word packet. Additional timing requirements exist when the FIFO is configured to operate in auto mode and it is desired to send two packets: a full packet ('full' defined as the number of bytes in the FIFO meeting the level set in the AUTOINLEN register) committed automatically followed by a short one byte or word packet committed manually using the PKTEND pin.

In this case, the external master must ensure to assert the PKTEND pin at least one clock cycle after the rising edge that caused the last byte or word that needs to be clocked into the previous auto committed packet (the packet with the number of bytes equal to what is set in the AUTOINLEN register). Refer to Figure 24 on page 53 for further details on this timing.

**Note**
53. Dashed lines denote signals with programmable polarity.

*Sequence Diagram of a Single and Burst Asynchronous Read*

**Figure 33. Slave FIFO Asynchronous Read Sequence and Timing Diagram[54]**

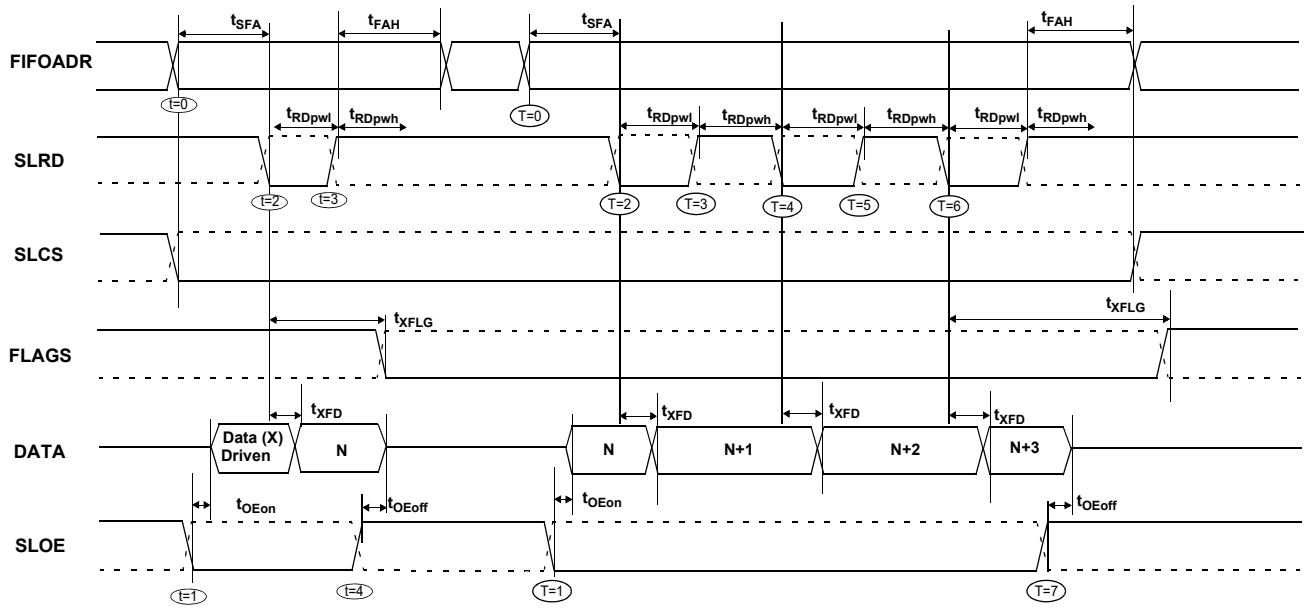



**Figure 34. Slave FIFO Asynchronous Read Sequence of Events Diagram**

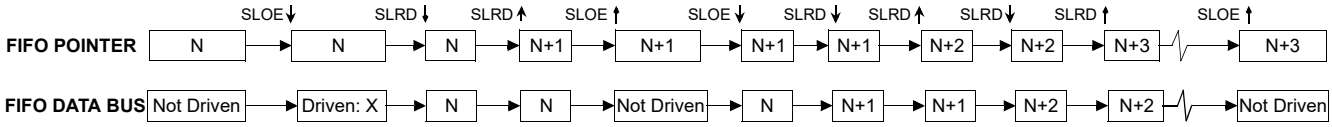



Figure 33 shows the timing relationship of the SLAVE FIFO signals during an asynchronous FIFO read. It shows a single read followed by a burst read.

- At t = 0, the FIFO address is stable and the SLCS signal is asserted.
- At t = 1, SLOE is asserted. This results in the data bus being driven. The data that is driven on to the bus is the previous data, the data that was in the FIFO from an earlier read cycle.
- At t = 2, SLRD is asserted. The SLRD must meet the minimum active pulse of $t_{RDpwl}$ and minimum de-active pulse width of $t_{RDpwh}$. If SLCS is used, then SLCS must be asserted before SLRD is asserted (The SLCS and SLRD signals must both be asserted to start a valid read condition.)
- The data that is driven, after asserting SLRD, is the updated data from the FIFO. This data is valid after a propagation delay of $t_{XFD}$ from the activating edge of SLRD. In Figure 33, data N is the first valid data read from the FIFO. For data to appear on the data bus during the read cycle (SLRD is asserted), SLOE must be in an asserted state. SLRD and SLOE can also be tied together.

The same sequence of events is also shown for a burst read marked with T = 0 through 5.

**Note** In the burst read mode, during SLOE is asserted, the data bus is in a driven state and outputs the previous data. After SLRD is asserted, the data from the FIFO is driven on the data bus (SLOE must also be asserted) and then the FIFO pointer is incremented.

**Note**
54. Dashed lines denote signals with programmable polarity.

*Sequence Diagram of a Single and Burst Asynchronous Write*

**Figure 35. Slave FIFO Asynchronous Write Sequence and Timing Diagram[55]**

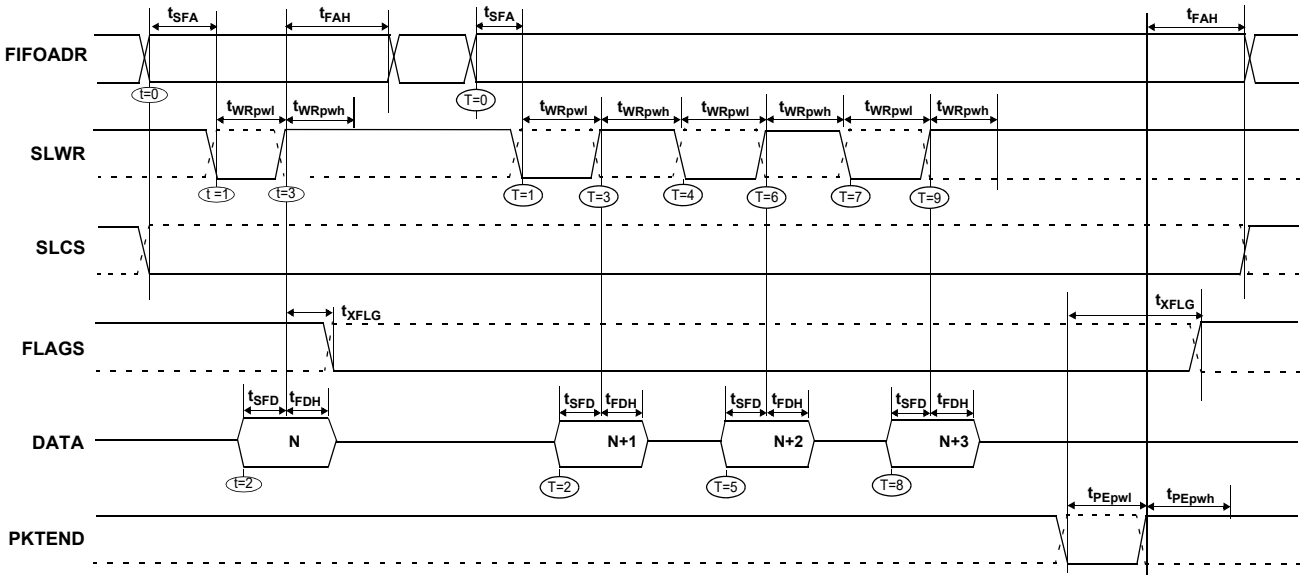



Figure 35 shows the timing relationship of the SLAVE FIFO write in an asynchronous mode. The diagram shows a single write followed by a burst write of 3 bytes and committing the 4byte short packet using PKTEND.

- At t = 0 the FIFO address is applied, ensuring that it meets the setup time of $t_{SFA}$. If SLCS is used, it must also be asserted (SLCS may be tied LOW in some applications).
- At t = 1 SLWR is asserted. SLWR must meet the minimum active pulse of $t_{WRpwl}$ and minimum de-active pulse width of $t_{WRpwh}$. If the SLCS is used, it must be asserted with SLWR or before SLWR is asserted.
- At t = 2, data must be present on the bus $t_{SFD}$ before the deasserting edge of SLWR.
- At t = 3, deasserting SLWR causes the data to be written from the data bus to the FIFO and then increments the FIFO pointer. The FIFO flag is also updated after $t_{XFLG}$ from the deasserting edge of SLWR.

The same sequence of events is shown for a burst write and is indicated by the timing marks of T = 0 through 5.

**Note** In the burst write mode, after SLWR is deasserted, the data is written to the FIFO and then the FIFO pointer is incremented to the next byte in the FIFO. The FIFO pointer is post incremented.

In Figure 35, after the four bytes are written to the FIFO and SLWR is deasserted, the short 4-byte packet can be committed to the host using PKTEND. The external device should be designed to not assert SLWR and the PKTEND signal at the same time. It should be designed to assert the PKTEND after SLWR is deasserted and met the minimum deasserted pulse width. The FIFOADDR lines have to held constant during the PKTEND assertion.

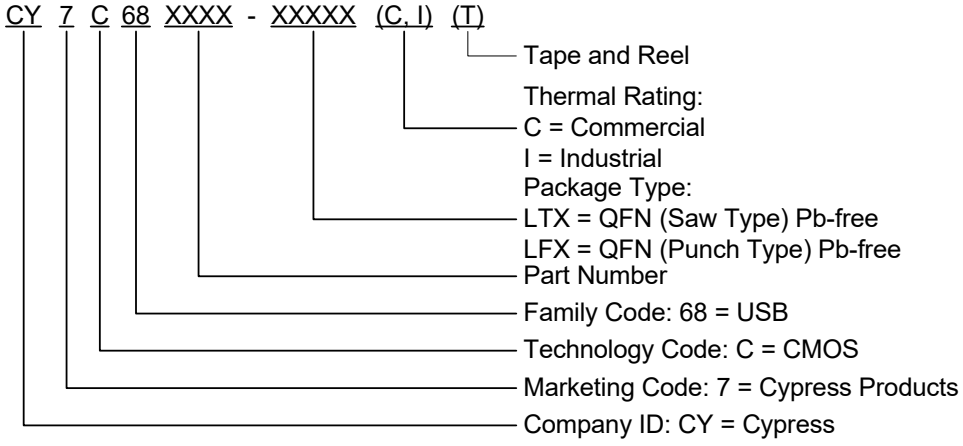
**Note**
55. Dashed lines denote signals with programmable polarity.

## Ordering Information

**Table 33. Ordering Information**

| Ordering Code | Package Type | RAM Size | # Prog I/Os | 8051 Address /Data Bus | Serial Debug[56] |
|---|---|---|---|---|---|
| **Ideal for Battery Powered Applications** | | | | | |
| CY7C68014A-128AXC | 128 TQFP – Pb-free | 16K | 40 | 16-/8-bit | Y |
| CY7C68014A-100AXC | 100 TQFP – Pb-free | 16K | 40 | – | Y |
| CY7C68014A-56PVXC | 56 SSOP – Pb-free | 16K | 24 | – | N |
| CY7C68014A-56LTXC | 56 QFN - Pb-free | 16K | 24 | – | N |
| CY7C68016A-56LTXC | 56 QFN - Pb-free | 16K | 26 | – | N |
| CY7C68016A-56LTXCT | 56 QFN - Pb-free | 16K | 26 | – | N |
| **Ideal for Non Battery Powered Applications** | | | | | |
| CY7C68013A-128AXC | 128 TQFP – Pb-free | 16K | 40 | 16-/8-bit | Y |
| CY7C68013A-128AXI | 128 TQFP – Pb-free (Industrial) | 16K | 40 | 16-/8-bit | Y |
| CY7C68013A-100AXC | 100 TQFP – Pb-free | 16K | 40 | – | Y |
| CY7C68013A-100AXI | 100 TQFP – Pb-free (Industrial) | 16K | 40 | – | Y |
| CY7C68013A-56PVXC | 56 SSOP – Pb-free | 16K | 24 | – | N |
| CY7C68013A-56PVXCT | 56 SSOP – Pb-free | 16K | 24 | – | N |
| CY7C68013A-56PVXI | 56 SSOP – Pb-free (Industrial) | 16K | 24 | – | N |
| CY7C68013A-56BAXC | 56 VFBGA – Pb-free | 16K | 24 | – | N |
| CY7C68013A-56BAXCT | 56 VFBGA – Pb-free | 16K | 24 | – | N |
| CY7C68013A-56LTXC | 56 QFN – Pb-free | 16K | 24 | – | N |
| CY7C68013A-56LTXCT | 56 QFN – Pb-free | 16K | 24 | – | N |
| CY7C68013A-56LTXI | 56 QFN – Pb-free (Industrial) | 16K | 24 | – | N |
| CY7C68015A-56LTXC | 56 QFN – Pb-free | 16K | 26 | – | N |
| **Development Tool Kit** | | | | | |
| CY3684 | EZ-USB FX2LP development kit | | | | |
| **Reference Design Kit** | | | | | |
| CY4611B | USB 2.0 to ATA/ATAPI reference design using EZ-USB FX2LP | | | | |

### Ordering Code Definitions




**Note**
56. As UART is not available in the 56-pin package of CY7C68013A, serial port debugging using Keil Monitor is not possible.

## Package Diagrams

The FX2LP is available in five packages:

- 56-pin SSOP
- 56-pin QFN
- 100-pin TQFP
- 128-pin TQFP
- 56-ball VFBGA

**Figure 36. 56-pin SSOP (300 Mils) Package Outline, 51-85062**

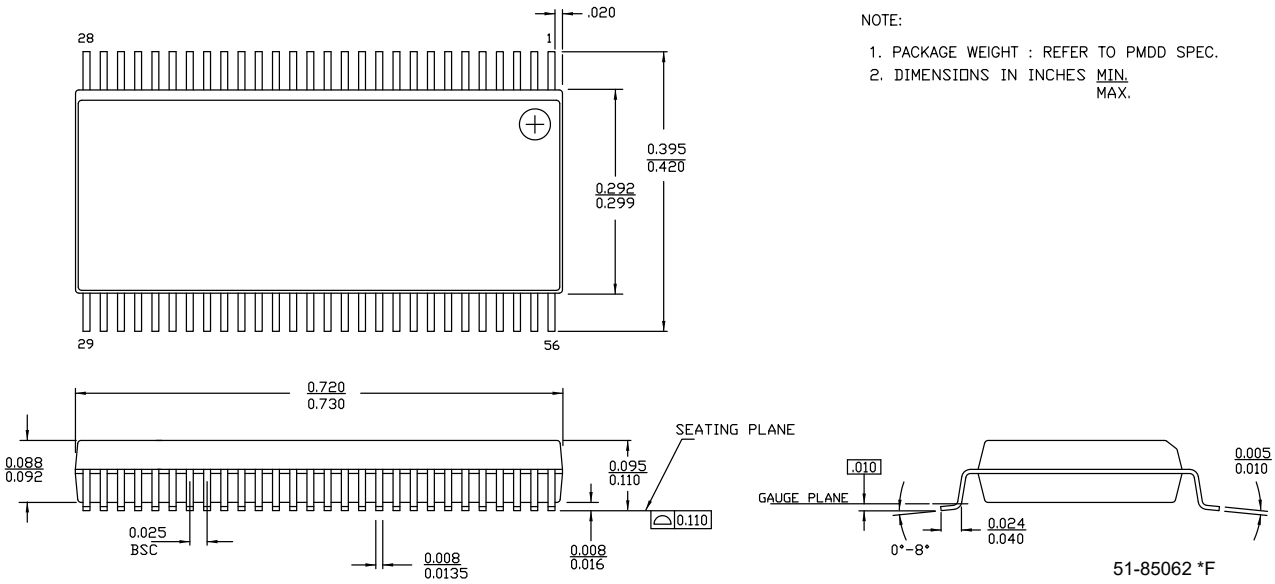


**Figure 37. 56-pin QFN ((8 × 8 × 1 mm) 4.5 × 5.2 E-Pad (Sawn)) Package Outline, 001-53450**

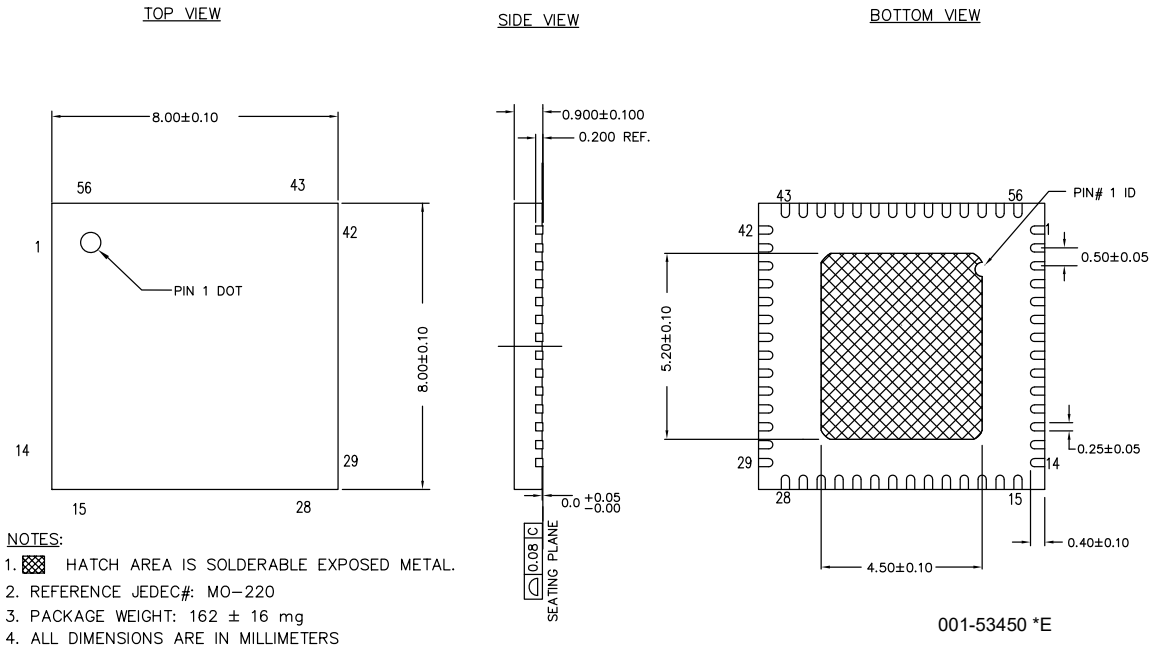
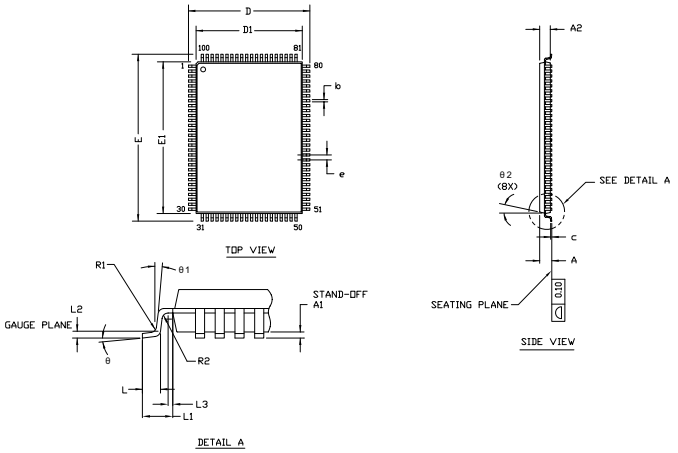



**Figure 38. 100-pin TQFP (14 × 20 × 1.4 mm) Package Outline, 51-85050**




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| D | 15.80 | 16.00 | 16.20 |
| D1 | 13.90 | 14.00 | 14.10 |
| E | 21.80 | 22.00 | 22.20 |
| E1 | 19.90 | 20.00 | 20.10 |
| R1 | 0.08 | — | 0.20 |
| R2 | 0.08 | — | 0.20 |
| θ | 0° | — | 7° |
| θ1 | 0° | — | — |
| θ2 | 11° | 12° | 13° |
| c | — | — | 0.20 |
| b | 0.22 | 0.30 | 0.38 |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF | | |
| L2 | 0.25 BSC | | |
| L3 | 0.20 | — | — |
| e | 0.65 TYP | | |

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH. MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE. BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
3. JEDEC SPECIFICATION NO. REF: MS-026.

51-85050 *G

**Figure 39. 128-pin TQFP (14 × 20 × 1.4 mm) Package Outline, 51-85101**

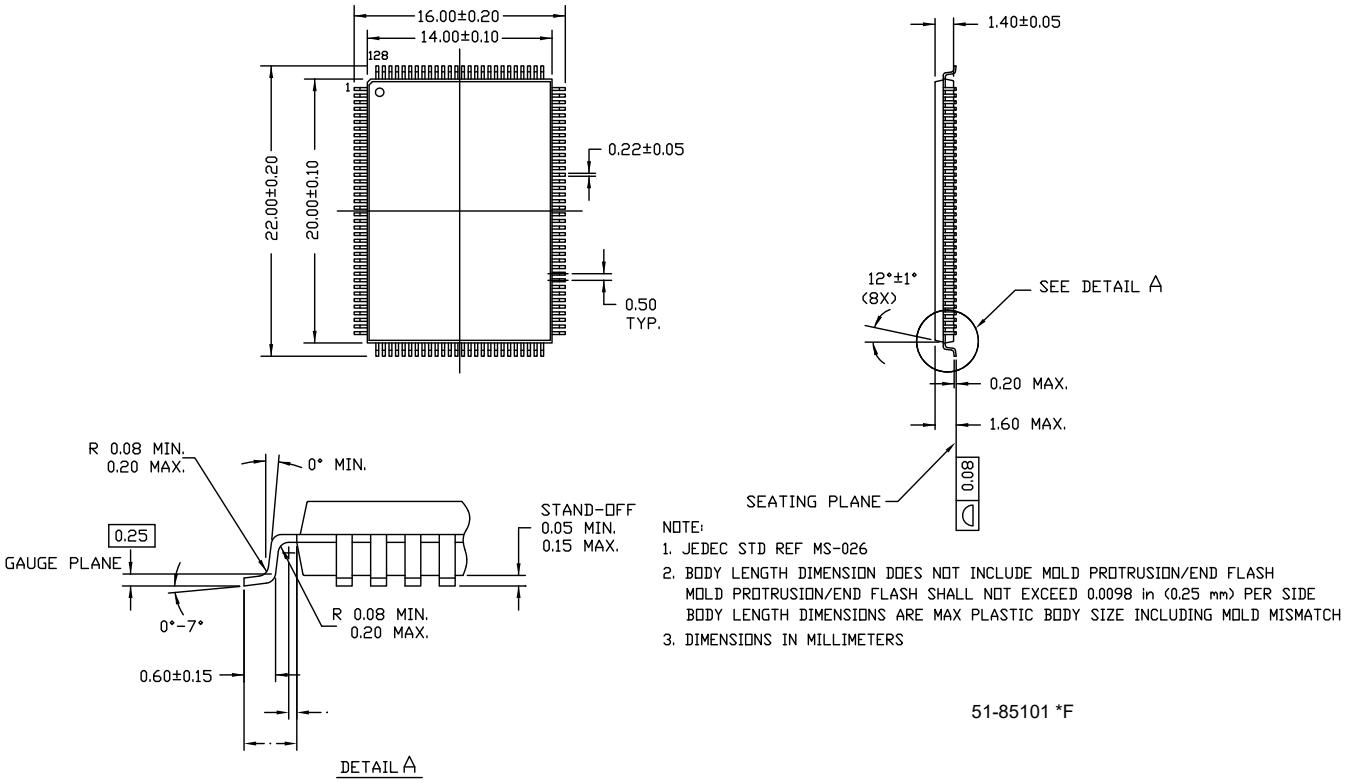
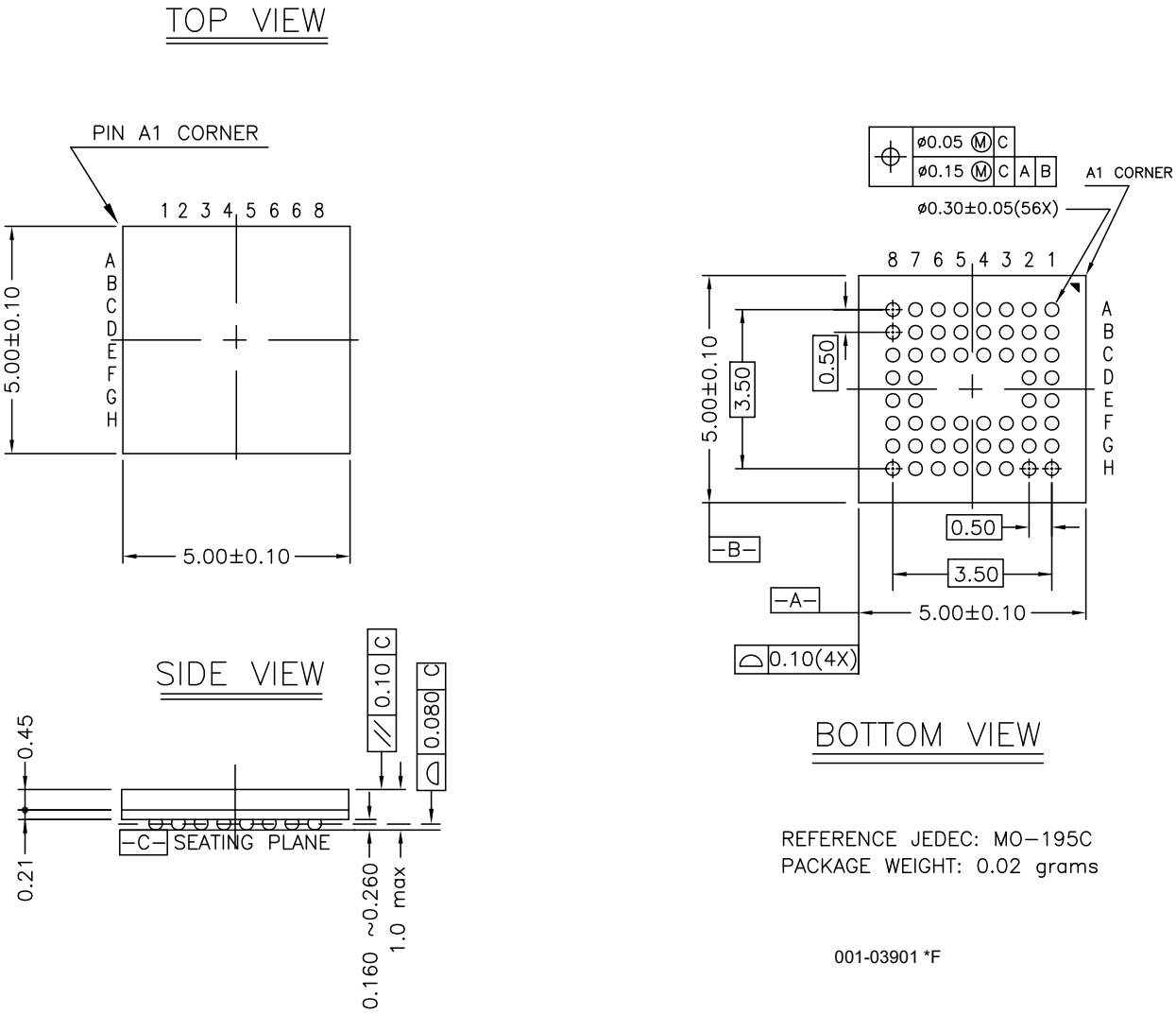


**Figure 40. 56-ball VFBGA (5 × 5 × 1.0 mm) 0.50 Pitch, 0.30 Ball Package Outline, 001-03901**



## PCB Layout Recommendations

Follow these recommendations to ensure reliable high-performance operation:[57]

- Four-layer, impedance-controlled boards are required to maintain signal quality.
- Specify impedance targets (ask your board vendor what they can achieve).
- To control impedance, maintain trace widths and trace spacing.
- Minimize stubs to minimize reflected signals.
- Connections between the USB connector shell and signal ground must be near the USB connector.
- Bypass and flyback caps on VBUS, near connector, are recommended.
- DPLUS and DMINUS trace lengths should be kept to within 2 mm of each other in length, with preferred length of 20 to 30 mm.
- Maintain a solid ground plane under the DPLUS and DMINUS traces. Do not allow the plane to split under these traces.
- Do not place vias on the DPLUS or DMINUS trace routing.
- Isolate the DPLUS and DMINUS traces from all other signal traces by no less than 10 mm.

**Note**

57. Source for recommendations: *EZ-USB FX2™PCB Design Recommendations*, http://www.cypress.com and *High Speed USB Platform Design Guidelines*, http://www.usb.org/developers/docs/hs_usb_pdg_r1_0.pdf.

## Quad Flat Package No Leads (QFN) Package Design Notes

Electrical contact of the part to the PCB is made by soldering the leads on the bottom surface of the package to the PCB. Therefore, special attention is required to the heat transfer area below the package to provide a good thermal bond to the circuit board. Design a copper (Cu) fill in the PCB as a thermal pad under the package. Heat is transferred from the FX2LP through the device's metal paddle on the bottom side of the package. Heat from here is conducted to the PCB at the thermal pad. It is then conducted from the thermal pad to the PCB inner ground plane by a 5 × 5 array of via. A via is a plated-through hole in the PCB with a finished diameter of 13 mil. The QFN's metal die paddle must be soldered to the PCB's thermal pad. Solder mask is placed on the board top side over each via to resist solder flow into the via. The mask on the top side also minimizes outgassing during the solder reflow process.

For further information on this package design, refer to application notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages. You can find this on Amkor's website http://www.amkor.com.

This application note provides detailed information about board mounting guidelines, soldering flow, rework process, etc.

Figure 41 shows a cross-sectional area underneath the package. The cross section is of only one via. The solder paste template should be designed to allow at least 50% solder coverage. The thickness of the solder paste template should be 5 mil. Use the No Clean type 3 solder paste for mounting the part. Nitrogen purge is recommended during reflow.

Figure 42 is a plot of the solder mask pattern and Figure 43 displays an X-Ray image of the assembly (darker areas indicate solder).

**Figure 41. Cross-section of the Area Underneath the QFN Package**

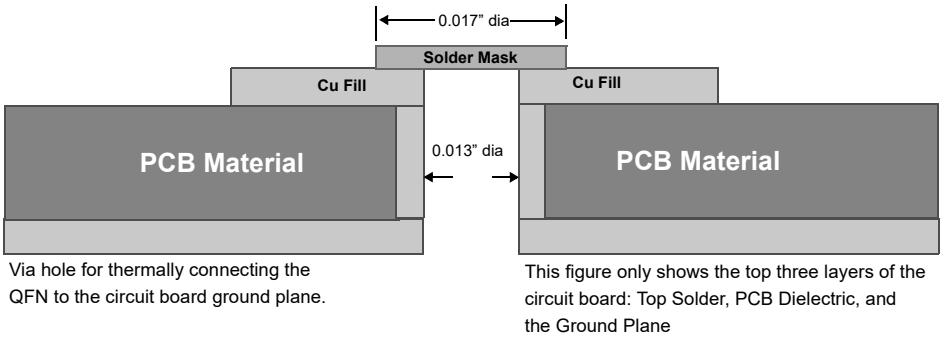



**Figure 42. Plot of the Solder Mask (White Area)**

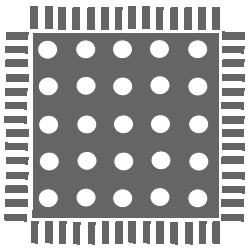
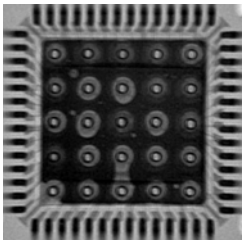


**Figure 43. X-ray Image of the Assembly**



## Acronyms

**Table 34. Acronyms Used in this Document**

| Acronym | Description |
|---|---|
| ASIC | application-specific integrated circuit |
| ATA | advanced technology attachment |
| DID | device identifier |
| DSL | digital service line |
| DSP | digital signal processor |
| ECC | error correction code |
| EEPROM | electrically erasable programmable read only memory |
| EPP | enhanced parallel port |
| FIFO | first in first out |
| GPIF | general programmable interface |
| GPIO | general purpose input output |
| I/O | input output |
| LAN | local area network |
| MPEG | moving picture experts group |
| PCMCIA | personal computer memory card international association |
| PID | product identifier |
| PLL | phase locked loop |
| QFN | quad flat no leads |
| RAM | random access memory |
| SIE | serial interface engine |
| SOF | start of frame |
| SSOP | super small outline package |
| TQFP | thin quad flat pack |
| USART | universal serial asynchronous receiver/transmitter |
| USB | universal serial bus |
| UTOPIA | universal test and operations physical-layer interface |
| VFBGA | very fine ball grid array |
| VID | vendor identifier |

## Document Conventions

### Units of Measure

**Table 35. Units of Measure**

| Symbol | Unit of Measure |
|---|---|
| kHz | kilohertz |
| mA | milliamperes |
| Mbps | megabits per second |
| MBPs | megabytes per second |
| MHz | megahertz |
| uA | microamperes |
| V | volts |

# Errata

This section describes the errata for the EZ-USB® FX2LP™ CY7C68013A/14A/15A/16A Rev. B silicon. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

## Part Numbers Affected

| Part Number | Package Type | Operating Range |
|---|---|---|
| CY7C68013A | All | Commercial |
| CY7C68014A | All | Commercial |
| CY7C68015A | All | Commercial |
| CY7C68016A | All | Commercial |

## CY7C68013A/14A/15A/16A Qualification Status

In production

## CY7C68013A/14A/15A/16A Errata Summary

This table defines the errata for available CY7C68013A/14A/15A/16A family devices. An “X” indicates that the errata pertain to the selected device.

| Items | CY7C68013A/14A/15A/16A | Silicon Revision | Fix Status |
|---|---|---|---|
| [1.]. Empty Flag Assertion | X | B | No silicon fix planned currently. Use the workaround. |

### 1. Empty Flag Assertion

**■ Problem Definition**

In Slave FIFO Asynchronous Word Wide mode, if a single word data is transferred from the USB host to EP2, configured as OUT Endpoint (EP) in the first transaction, then the Empty flag behaves incorrectly. This does not happen if the data size is more than one word in the first transaction.

**■ Parameters Affected**

NA

**■ Trigger Condition(S)**

In Slave FIFO Asynchronous Word Wide Mode, after firmware boot and initialization, EP2 OUT endpoint empty flag indicates the status as ‘Empty’. When data is received in EP2, the status changes to ‘Not-Empty’. However, if data transferred to EP2 is a single word, then asserting SLRD with FIFOADR pointing to any other endpoint changes ‘Not-Empty’ status to ‘Empty’ for EP2 even though there is a word data (or it is untouched). This is noticed only when the single word is sent as the first transaction and not if it follows a multi-word packet as the first transaction.

**■ Scope of Impact**

External interface does not see data available in EP2 OUT endpoint and can end up waiting for data to be read.

**■ Workaround**

One of the following workarounds can be used:

- Send a pulse signal to the SLWR pin, with FIFOADR pins pointing to an endpoint other than EP2, after firmware initialization and before or after transferring the data to EP2 from the host
- Set the length of the first data to EP2 to be more than a word
- Prioritize EP2 read from the Master for multiple OUT EPs and single word write to EP2
- Write to an IN EP, if any, from the Master before reading from other OUT EPs (other than EP2) from the Master.

**■ Fix Status**

There is no silicon fix planned for this currently; use the workarounds provided.

## Document History Page

| Document Title: CY7C68013A/CY7C68014A/CY7C68015A/CY7C68016A, EZ-USB® FX2LP™ USB Microcontroller High-Speed USB Peripheral Controller<br>Document Number: 38-08032 | | | |
|---|---|---|---|
| **Rev.** | **ECN No.** | **Submission Date** | **Description of Change** |
| ** | 124316 | 03/17/2003 | New data sheet (Advance Information). |
| *A | 128461 | 09/02/2003 | Updated Document Title to read as "CY7C68013A/CY7C68015A, EZ-USB FX2LP™ USB Microcontroller High-Speed USB Peripheral Controller".<br>Changed status from Advance Information to Final.<br>Added CY7C68015A part related information in all instances across the document.<br>Replaced $I^2C$-compatible with $I^2C$ in all instances across the document.<br>Updated Logic Block Diagram (Added ECC block and fixed errors).<br>Updated Functional Overview:<br>Updated 8051 Microprocessor:<br>Updated 8051 Clock Frequency:<br>Added Figure 1.<br>Updated Reset and Wakeup:<br>Updated Reset Pin:<br>Updated description; added Figure 2; and also added Table 5.<br>Updated Register Addresses:<br>Updated figure below the heading.<br>Updated Endpoint RAM:<br>Updated Endpoint Configurations (Hi-Speed Mode):<br>Updated Figure 5 (for clarity).<br>Added ECC Generation.<br>Updated $I^2C$ Controller:<br>Added "$I^2C$ Software Reset".<br>Updated Compatible with Previous Generation EZ-USB FX2:<br>Updated description; and also updated Table 9.<br>Added CY7C68013A/14A and CY7C68015A/16A Differences.<br>Updated Register Summary:<br>Updated Table 12.<br>Updated Package Diagrams:<br>spec 51-85144 – Changed revision from *B to *D.<br>Minor grammatical edits across the document. |
| *B | 130335 | 10/09/2003 | Changed status from Final to Preliminary. |
| *C | 131673 | 02/12/2004 | Updated Functional Overview:<br>Updated Reset and Wakeup:<br>Updated Reset Pin:<br>Updated description; added Note 6 and referred the same note at the end of sentence "If the crystal input pin is driven by a clock signal the internal PLL stabilizes in 200 µs after $V_{CC}$ has reached 3.0 Volts".<br>Updated Endpoint RAM:<br>Updated Endpoint Configurations (Hi-Speed Mode):<br>Updated description (Replaced column 9 with column 8 in last paragraph).<br>Updated ECC Generation:<br>Updated description.<br>Removed "ECC Features".<br>Updated ECC Implementation:<br>Updated description.<br>Updated Register Summary:<br>Updated Table 12. |

## Document History Page (continued)

| Document Title: CY7C68013A/CY7C68014A/CY7C68015A/CY7C68016A, EZ-USB® FX2LP™ USB Microcontroller High-Speed USB Peripheral Controller<br>Document Number: 38-08032 | | | |
|---|---|---|---|
| **Rev.** | **ECN No.** | **Submission Date** | **Description of Change** |
| *C (cont.) | 131673 | 02/12/2004 | Updated DC Electrical Characteristics:<br>Updated Table 14:<br>Added $V_{IH_X}$, $V_{IL_X}$ parameters and their corresponding details.<br>Updated USB Transceiver:<br>Replaced “certified” with “compliant”.<br>Updated AC Electrical Characteristics:<br>Updated USB Transceiver:<br>Replaced “certified” with “compliant”.<br>Updated Data Memory Write[32]:<br>Updated Figure 14.<br>Added Sequence Diagram.<br>Updated Ordering Information:<br>Updated Table 33:<br>Updated part numbers. |
| *D | 230713 | 06/09/2004 | Updated Ordering Information:<br>Updated Table 33:<br>Updated part numbers (Changed Lead free MPNs as per spec change in 28-00054). |
| *E | 242398 | 07/13/2004 | Minor Change:<br>Post to external web, |
| *F | 271169 | 10/07/2004 | Updated Features:<br>Added “USB 2.0–USB-IF high speed certified (TID # 40440111)”.<br>Added Features (CY7C68013A/14A only).<br>Added Features (CY7C68015A/16A only).<br>Updated Logic Block Diagram (Added USB 2.0 logo).<br>Updated Absolute Maximum Ratings:<br>Replaced TBD with values for “Power Dissipation”.<br>Updated DC Electrical Characteristics:<br>Updated Table 14:<br>Updated minimum and maximum values of $V_{CC}$ parameter.<br>Replaced TBD with values for $V_{IH_X}$, $V_{IL_X}$, $I_{SUSP}$, $I_{CC}$ parameters.<br>Updated AC Electrical Characteristics:<br>Updated Slave FIFO Asynchronous Packet End Strobe:<br>Updated Table 28:<br>Changed maximum value of $t_{XFLG}$ parameter from 70 ns to 115 ns.<br>Updated Ordering Information:<br>Updated Table 33:<br>Updated part numbers. |
| *G | 316313 | 02/04/2005 | Updated Document Title to read as<br>“CY7C68013A/CY7C68014A/CY7C68015A/CY7C68016A, EZ-USB FX2LP™ USB Micro-controller High-Speed USB Peripheral Controller”.<br>Changed status from Preliminary to Final.<br>Added CY7C68014A, CY7C68016A part related information in all instances across the document.<br>Updated DC Electrical Characteristics:<br>Updated Table 14:<br>Added $V_{CC}$ Ramp Up parameter and its corresponding details.<br>Updated AC Electrical Characteristics:<br>Updated Slave FIFO Synchronous Packet End Strobe:<br>Added description; and also added Figure 24.<br>Updated Ordering Information:<br>Updated Table 33:<br>Updated part numbers. |

## Document History Page (continued)

| Document Title: CY7C68013A/CY7C68014A/CY7C68015A/CY7C68016A, EZ-USB® FX2LP™ USB Microcontroller High-Speed USB Peripheral Controller<br>Document Number: 38-08032 | | | |
|---|---|---|---|
| **Rev.** | **ECN No.** | **Submission Date** | **Description of Change** |
| *H | 338901 | 04/18/2005 | Updated Register Summary:<br>Updated Table 12.<br>Updated AC Electrical Characteristics:<br>Updated Data Memory Read[30]:<br>Added description.<br>Updated Data Memory Write[32]:<br>Added description.<br>Updated Slave FIFO Synchronous Read:<br>Updated Table 20:<br>Replaced TBD with "–" under "Min" column corresponding to $t_{XFD}$ parameter.<br>Updated Ordering Information:<br>Updated Table 33:<br>Updated part numbers. |
| *I | 371097 | 06/09/2005 | Updated AC Electrical Characteristics:<br>Added PORTC Strobe Feature Timings. |
| *J | 397239 | 09/19/2005 | Added 56-pin VFBGA Package related information in all instances across the document.<br>Updated Register Summary:<br>Updated Table 12.<br>Updated DC Electrical Characteristics:<br>Updated Table 14:<br>Updated minimum and maximum values of $V_{CC}$ parameter.<br>Updated Ordering Information:<br>Updated Table 33:<br>Updated part numbers.<br>Updated Package Diagrams:<br>Added spec 001-03901 *B. |
| *K | 420505 | 02/09/2006 | Updated Pin Assignments:<br>Updated description (Replaced "four package types" with "five package types").<br>Updated Absolute Maximum Ratings:<br>Added "Ambient Temperature with Power Supplied (Industrial)" and its corresponding details.<br>Added Thermal Characteristics.<br>Updated AC Electrical Characteristics:<br>Updated Slave FIFO Asynchronous Write:<br>Updated Figure 22 (Remove SLCS).<br>Updated Sequence Diagram:<br>Updated Single and Burst Synchronous Write:<br>Updated description.<br>Updated Sequence Diagram of a Single and Burst Asynchronous Read:<br>Updated description.<br>Updated to new template. |
| *L | 2064406 | 02/04/2008 | Updated Features:<br>Replaced "TID # 40440111" with "TID # 40460272".<br>Updated Functional Overview:<br>Updated CY7C68013A/14A and CY7C68015A/16A Differences:<br>Updated Table 10 (Removed T0OUT and T1OUT in "CY7C68015A/CY7C68016A" column).<br>Updated AC Electrical Characteristics:<br>Updated Slave FIFO Synchronous Write:<br>Updated Table 23 (Updated minimum value of $t_{SWR}$ parameter).<br>Updated Package Diagrams:<br>spec 51-85144 – Changed revision from *D to *G. |

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| Document Title: CY7C68013A/CY7C68014A/CY7C68015A/CY7C68016A, EZ-USB® FX2LP™ USB Microcontroller High-Speed USB Peripheral Controller<br>Document Number: 38-08032 | | | |
|---|---|---|---|
| **Rev.** | **ECN No.** | **Submission Date** | **Description of Change** |
| *M | 2710327 | 05/22/2009 | Updated Operating Conditions:<br>Changed value of $F_{OSC}$ (oscillator or crystal frequency) from<br>“24 MHz ± 100 ppm, Parallel Resonant” to “24 MHz ± 10 ppm, Parallel Resonant”.<br>Updated Ordering Information:<br>Updated Table 33:<br>Updated part numbers.<br>Updated Package Diagrams:<br>Added spec 51-85187 *C. |
| *N | 2727334 | 07/01/2009 | Updated Package Diagrams:<br>spec 51-85187 – Changed revision from *C to *D.<br>Fixed Typo in Document History Page (Removed sentence on E-Pad size change from *F revision). |
| *O | 2756202 | 08/26/2009 | Updated Ordering Information:<br>Updated Table 33:<br>No change in part numbers.<br>Added a column “Serial Debug” and added details under the column.<br>Added Note 56 and referred the same note in “Serial Debug”. |
| *P | 2785207 | 10/12/2009 | Updated Ordering Information:<br>Updated Table 33:<br>No change in part numbers.<br>Updated details in “Package Type” column (Added information on Pb-free parts). |
| *Q | 2811890 | 11/20/2009 | Updated Ordering Information:<br>Updated Table 33:<br>Updated part numbers.<br>Updated details under “# Program I/Os” column for CY7C68016A-56LTXC and CY7C68016A-56LTXCT MPNs. |
| *R | 2896281 | 03/19/2010 | Updated Ordering Information:<br>Updated Table 33:<br>Updated part numbers.<br>Updated Package Diagrams:<br>spec 51-85062 – Changed revision from *C to *D.<br>spec 51-85144 – Changed revision from *G to *H.<br>spec 51-85187 – Changed revision from *D to *E.<br>spec 51-85050 – Changed revision from *B to *C.<br>spec 51-85101 – Changed revision from *C to *D.<br>Updated to new template. |
| *S | 3035980 | 09/22/2010 | Updated Operating Conditions:<br>Changed value of $F_{OSC}$ (oscillator or crystal frequency) from<br>“24 MHz ± 10 ppm, Parallel Resonant” to “24 MHz ± 100 ppm, Parallel Resonant”.<br>Updated Ordering Information:<br>Updated Table 33:<br>No change in part numbers.<br>Added Ordering Code Definitions.<br>Added Acronyms and Units of Measure.<br>Updated to new template. |

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| Document Title: CY7C68013A/CY7C68014A/CY7C68015A/CY7C68016A, EZ-USB® FX2LP™ USB Microcontroller High-Speed USB Peripheral Controller<br>Document Number: 38-08032 | | | |
|---|---|---|---|
| **Rev.** | **ECN No.** | **Submission Date** | **Description of Change** |
| *T | 3161410 | 02/03/2011 | Updated Package Diagrams:<br>Removed spec 51-85144 *H.<br>Added spec 001-12921 *A.<br>Removed spec 51-85187 *E.<br>Added spec 001-53450 *B.<br>spec 51-85050 – Changed revision from *C to *D.<br>spec 51-85101 – Changed revision from *D to *E.<br>Completing Sunset Review. |
| *U | 3195232 | 03/14/2011 | Updated table numbering.<br>Updated Thermal Characteristics:<br>Updated Table 13 (Removed column “θCa Case to Ambient Temperature (°C/W)”).<br>Updated AC Electrical Characteristics:<br>Updated GPIF Synchronous Signals:<br>Updated Table 18 (Added a column “Typ” and added values in that column).<br>Updated Slave FIFO Synchronous Read:<br>Updated Table 20 (Added a column “Typ” and added values in that column).<br>Updated Package Diagrams:<br>spec 001-12921 – Changed revision from *A to *B.<br>spec 001-03901 – Changed revision from *C to *D. |
| *V | 3512313 | 02/01/2012 | Updated Ordering Information:<br>Updated Table 33:<br>Updated part numbers.<br>Updated Package Diagrams:<br>spec 51-85062 – Changed revision from *D to *E.<br>Removed spec 001-12921 *B.<br>spec 001-03901 – Changed revision from *D to *E.<br>Completing Sunset Review. |
| *W | 3998554 | 07/19/2013 | Added Errata footnote (Note 5).<br>Updated Functional Overview:<br>Updated Interrupt System:<br>Updated FIFO/GPIF Interrupt (INT4):<br>Added Note 5 and referred the same note in “Endpoint 2 empty flag” in Table 4.<br>Updated Package Diagrams:<br>spec 51-85062 – Changed revision from *E to *F.<br>spec 001-53450 – Changed revision from *B to *C.<br>Added Errata.<br>Updated to new template. |
| *X | 4617527 | 01/15/2015 | Added More Information.<br>Updated Pin Assignments:<br>Updated CY7C68013A/15A Pin Descriptions:<br>Updated Table 11 (Added a column “Reset” and added details in that column).<br>Updated AC Electrical Characteristics:<br>Updated Data Memory Read[30]:<br>Added Note 30 and referred the same note in heading.<br>Updated Figure 13.<br>Updated Data Memory Write[32]:<br>Added Note 30 and referred the same note in heading.<br>Updated Package Diagrams:<br>spec 001-53450 – Changed revision from *C to *D.<br>spec 51-85050 – Changed revision from *D to *E.<br>spec 51-85101 – Changed revision from *E to *F.<br>Updated to new template.<br>Completing Sunset Review. |

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| Document Title: CY7C68013A/CY7C68014A/CY7C68015A/CY7C68016A, EZ-USB® FX2LP™ USB Microcontroller High-Speed USB Peripheral Controller<br>Document Number: 38-08032 | | | |
|---|---|---|---|
| **Rev.** | **ECN No.** | **Submission Date** | **Description of Change** |
| *Y | 5317277 | 06/28/2016 | Updated to new template. |
| *Z | 5713641 | 04/26/2017 | Updated Package Diagrams:<br>spec 51-85050 – Changed revision from *E to *G.<br>Updated to new template. |
| AA | 5930426 | 11/09/2017 | Updated AC Electrical Characteristics:<br>Updated GPIF Synchronous Signals:<br>Updated Table 18.<br>Updated Table 19. |
| AB | 6403695 | 12/06/2018 | Updated Features:<br>Added Note 1 and referred the note at the end in “Integrated $I^2C$ controller; runs at 100 or 400 kHz”.<br>Updated Functional Overview:<br>Updated $I^2C$ Bus:<br>Added Note 3 and referred the note at the end in “FX2LP supports the $I^2C$ bus as a master only at 100/400 kHz”.<br>Updated Thermal Characteristics:<br>Added “Maximum junction temperature” and its corresponding details.<br>Updated Package Diagrams:<br>spec 001-53450 – Changed revision from *D to *E.<br>Updated to new template.<br>Completing Sunset Review. |
| AC | 6637530 | 07/26/2019 | Updated to new template. |

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