

54191/DM54191/DM74191 Synchronous Up/Down 4-Bit Binary Counter with Mode Control

General Description

This circuit is a synchronous, reversible, up/down counter. The 191 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

This counter is fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

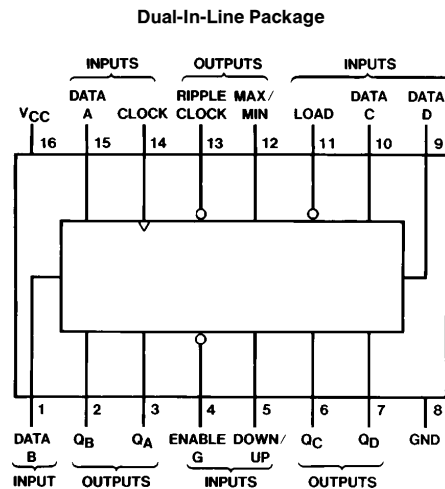
The clock, down/up, and load inputs are buffered to lower the drive requirement; which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Features

- Single down/up count control line
- Count enable control input
- Ripple clock output for cascading
- Asynchronously presettable with load control
- Parallel outputs
- Cascadable for n-bit applications
- Alternate Military/Aerospace device (54191) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram



TL/F/6562-1

54191/DM54191/DM74191 Synchronous Up/Down 4-Bit Binary Counter with Mode Control

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the “Electrical Characteristics” table are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	DM54191			DM74191			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.8			0.8	V
I _{OH}	High Level Output Current			−0.8			−0.8	mA
I _{OL}	Low Level Output Current			16			16	mA
f _{CLK}	Clock Frequency (Note 4)	0		20	0		20	MHz
t _W	Pulse Width (Note 4)	Clock	25		25			ns
		Load	35		35			
t _{SU}	Data Setup Time (Note 4)	28			28			ns
t _H	Hold Time (Note 4)	0			0			ns
t _{REL}	Load Release Time (Note 4)	30			30			ns
T _A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = −12 mA			−1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IL} = Max, V _{IH} = Min	2.4	3.4		V
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IH} = Min, V _{IL} = Max		0.2	0.4	V
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 5.5V			1	mA
I _{IH}	High Level Input Current	V _{CC} = Max V _I = 2.4V	Enable		120	μA
			Others		40	
I _{IL}	Low Level Input Current	V _{CC} = Max V _I = 0.4V	Enable		−4.8	mA
			Others		−1.6	
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	DM54	−20	−65	mA
			DM74	−18	−65	
I _{CC}	Supply Current	V _{CC} = Max (Note 3)	DM54	65	99	mA
			DM74	65	105	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

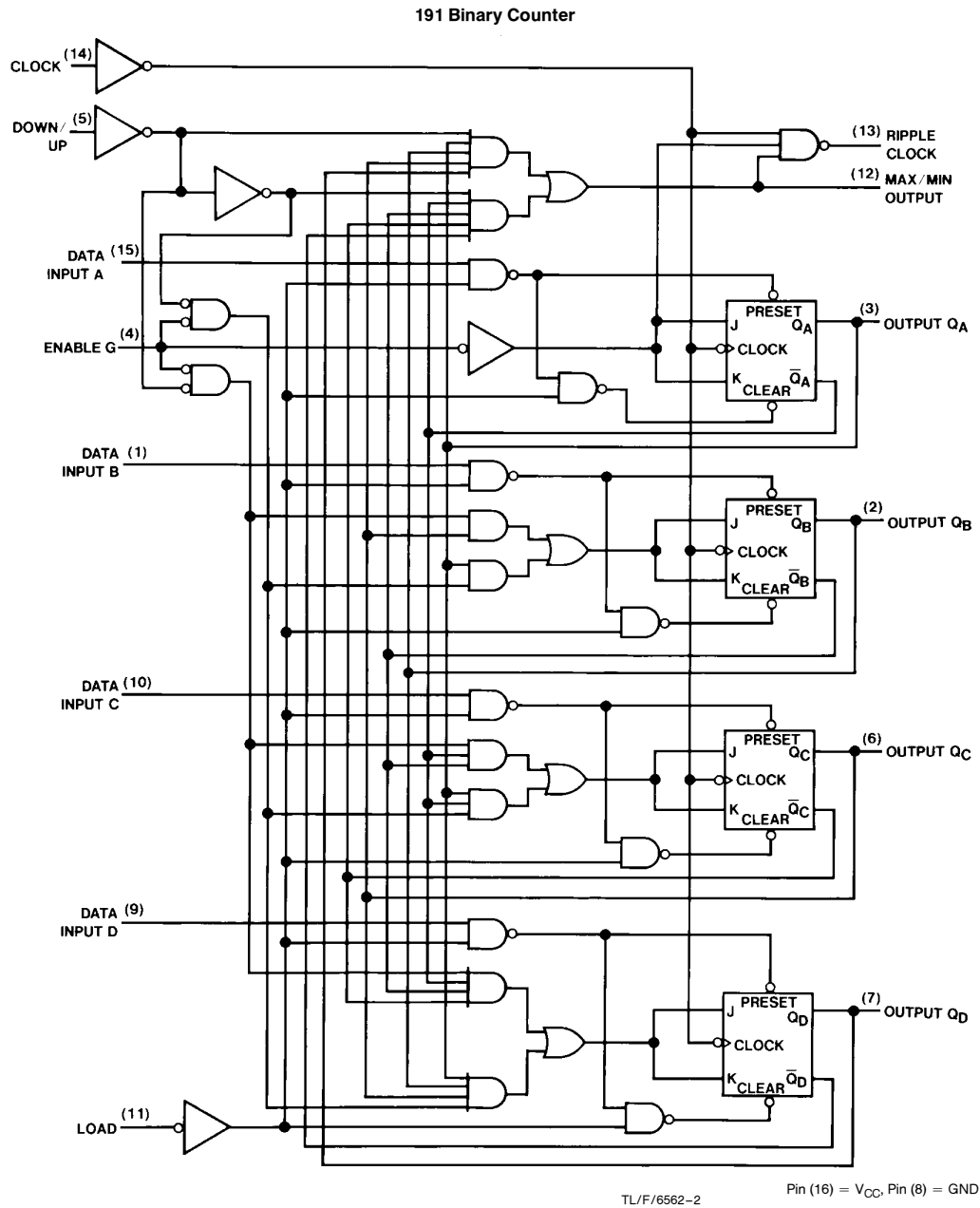
Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega, C_L = 15 pF$		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Load to Any Q		33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Load to Any Q		70	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Any Q		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Any Q		70	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		36	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Max/Min		42	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Max/Min		52	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Down/Up to Ripple Carry		45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Down/Up to Ripple Carry		45	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Down/Up to Max/Min		33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Down/Up to Max/Min		33	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable G to Ripple Carry		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable G to Ripple Carry		24	ns

Logic Diagram



191 Decade Counter

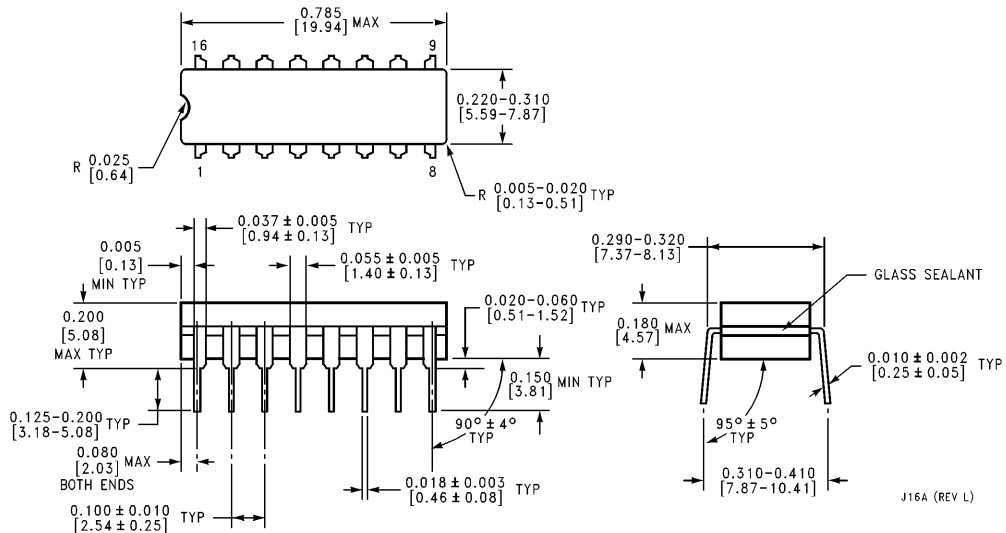
Typical Load, Count, and Inhibit Sequences

The diagram illustrates the timing relationships for the 191 Decade Counter. Key signals and their states during the sequences are as follows:

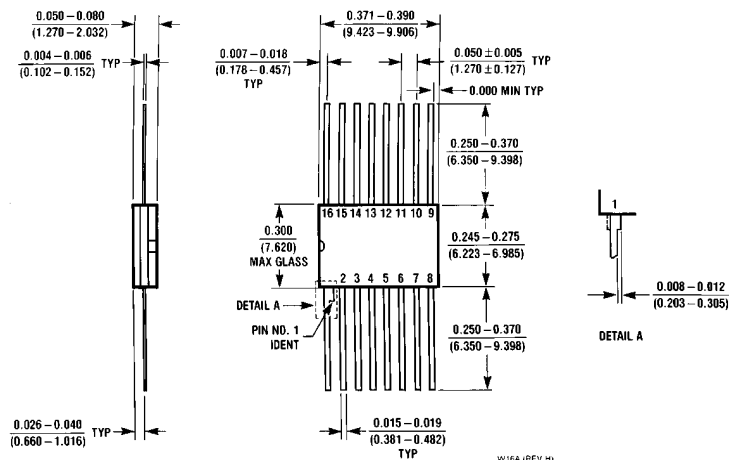
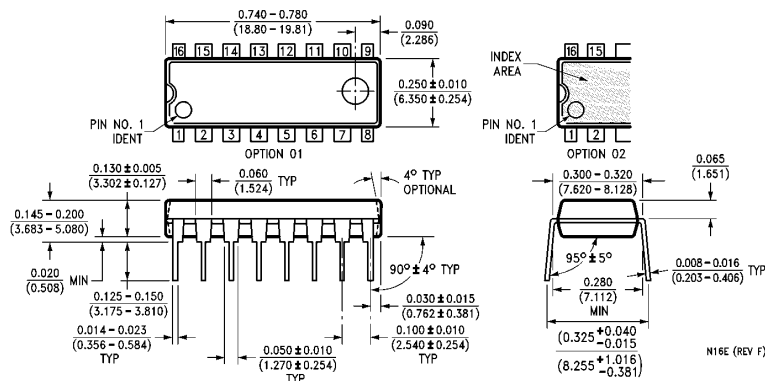
- LOAD:** Active-low pulse.
- DATA INPUTS (A, B, C, D):** Set to 13 (A=H, B=L, C=H, D=H) during the load operation.
- CLOCK:** Square wave providing the counting clock.
- DOWN/UP:** Low for count-up, high for count-down.
- ENABLE:** Low for counting, high for inhibit.
- QA, QB, QC, QD:** Counter outputs.
- MAX/MIN:** Output indicating the count limit.
- RIPPLE CLOCK:** Output for cascading counters.

The sequence shown is: **LOAD** (13) → **COUNT UP** (14, 15, 0, 1, 2) → **INHIBIT** (2, 2, 1, 0) → **COUNT DOWN** (15, 14, 13).

Physical Dimensions inches (millimeters)



5

Physical Dimensions inches (millimeters) (Continued)**LIFE SUPPORT POLICY**

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