SPC564A70B4, SPC564A70L7

32-bit Power Architecture® based MCU for automotive powertrain applications

Datasheet – preliminary data

Features

- 150 MHz e200z4 Power Architecture® core
  - Variable length instruction encoding (VLE)
  - Superscalar architecture with 2 execution units
  - Up to 2 integer or floating point instructions per cycle
  - Up to 4 multiply and accumulate operations per cycle
- Memory organization
  - 2 MB on-chip flash memory with ECC and read-while-write (RWW)
  - 128 KB on-chip SRAM with standby functionality (32 KB) and ECC
  - 8 KB instruction cache (with line locking), configurable as 2- or 4-way
  - 14 + 3 KB eTPU code and data RAM
  - 4 × 4 crossbar switch (XBAR)
  - 24-entry MMU
- Fail Safe Protection
  - 16-entry Memory Protection Unit (MPU)
  - CRC unit with 3 submodules
  - Junction temperature sensor
- Interrupt
  - Configurable interrupt controller (INTC) with non-maskable interrupt (NMI)
  - 64-channel eDMA
- Serial channels
  - 3 eSCI modules
  - 3 DSPI modules (2 of which support downstream Micro Second Channel [MSC])
  - 3 FlexCAN modules with 64 message buffers each


PBGA324 (23 mm x 23 mm)


LQFP176 (24 mm x 24 mm)

  - 1 FlexRay module (V2.1) up to 10 Mbit/s w/dual or single channel, 128 message objects, ECC
- 1 eMIOS (24 unified channels)
- 1 eTPU2 (second generation eTPU)
  - 32 standard channels
  - 1 reaction module (6 channels with 3 outputs per channel)
- 2 enhanced queued analog-to-digital converters (eQADCs)
  - Forty 12-bit input channels
  - 688 ns minimum conversion time
- On-chip CAN/SCI Bootstrap loader with Boot Assist Module (BAM)
- Nexus: Class 3+ for core; Class 1 for eTPU
- JTAG (5-pin)
- Development Trigger Semaphore (DTS)
- Clock generation
  - On-chip 4–40 MHz main oscillator
  - On-chip FMPLL (frequency-modulated phase-locked loop)
- Up to 112 general purpose I/O lines
- Power reduction modes: slow, stop, and standby
- Flexible supply scheme
  - 5 V single supply with external ballast
  - Multiple external supply: 5 V, 3.3 V , and 1.2 V
- Designed for LQFP176, LBGA208, PBGA324

Table 1. Device summary

Memory Flash size	Part number		
	Package LQFP176	Package LBGA208	Package PBGA324
2MB	SPC564A70L7	-	SPC564A70B4

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1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the SPC564A70 series of microcontroller units (MCUs). It also describes the device features and highlights important electrical and physical characteristics. For functional characteristics, refer to the device reference manual.

1.2 Description

This microcontroller is a 32-bit system-on-chip (SoC) device intended for use in mid-range engine control and automotive transmission control applications.

It is compatible with devices in ST's SPC56xx family and offers performance and capability above that of the SPC563M devices.

The microcontroller's e200z4 host processor core is built on the Power Architecture technology and designed specifically for embedded applications. In addition to the Power Architecture technology, this core supports instructions for digital signal processing (DSP).

The device has two levels of memory hierarchy consisting of 8 KB of instruction cache, backed by a 128 KB on-chip SRAM and a 2 MB internal flash memory.

For development, the device includes a calibration bus that is accessible only when using the STMicroelectronics calibration tool.

1.3 Device feature summary

Table 2 summarizes the SPC564A70 features and compares them to those of the SPC564A80.

Table 2. SPC564A70 device feature summary

Feature		SPC564A70	SPC564A80
Process		90 nm	
Core		e200z4	
	SIMD	Yes	
	VLE	Yes	
	Cache	8 KB instruction	
	Non-Maskable Interrupt (NMI)	NMI and Critical Interrupt	
	MMU	24-entry	
	MPU	16-entry	
	Crossbar switch	4 × 4	5 × 4
	Core performance	0–150 MHz	
Windowing software watchdog		Yes	

Table 2. SPC564A70 device feature summary (continued)

Feature		SPC564A70	SPC564A80
Core Nexus		Class 3+	
SRAM		128 KB	192 KB
Flash		2 MB	4 MB
Flash fetch accelerator		4 × 128-bit	4 × 256-bit
External bus		None	16-bit (incl. 32-bit muxed)
Calibration bus		16-bit (incl. 32-bit muxed)	
DMA		64 channels	
DMA Nexus		None	
Serial		3	
	eSCI_A	Yes (MSC uplink)	
	eSCI_B	Yes (MSC uplink)	
	eSCI_C	Yes	
CAN		3	
	CAN_A	64 message buffers	
	CAN_B	64 message buffers	
	CAN_C	64 message buffers	
SPI		3	
	Micro Second Channel (MSC) bus downlink	Yes	
	DSPI_A	No	
	DSPI_B	Yes (with LVDS)	
	DSPI_C	Yes (with LVDS)	
	DSPI_D	Yes	
FlexRay		Yes	
System timers		5 PIT channels 4 STM channels 1 Software Watchdog	
eMIOS		24 channels	
eTPU		32-channel eTPU2	
	Code memory	14 KB	
	Data memory	3 KB	
	Reaction module	6 channels	
Interrupt controller		485 channels(1)	
ADC		40 channels	

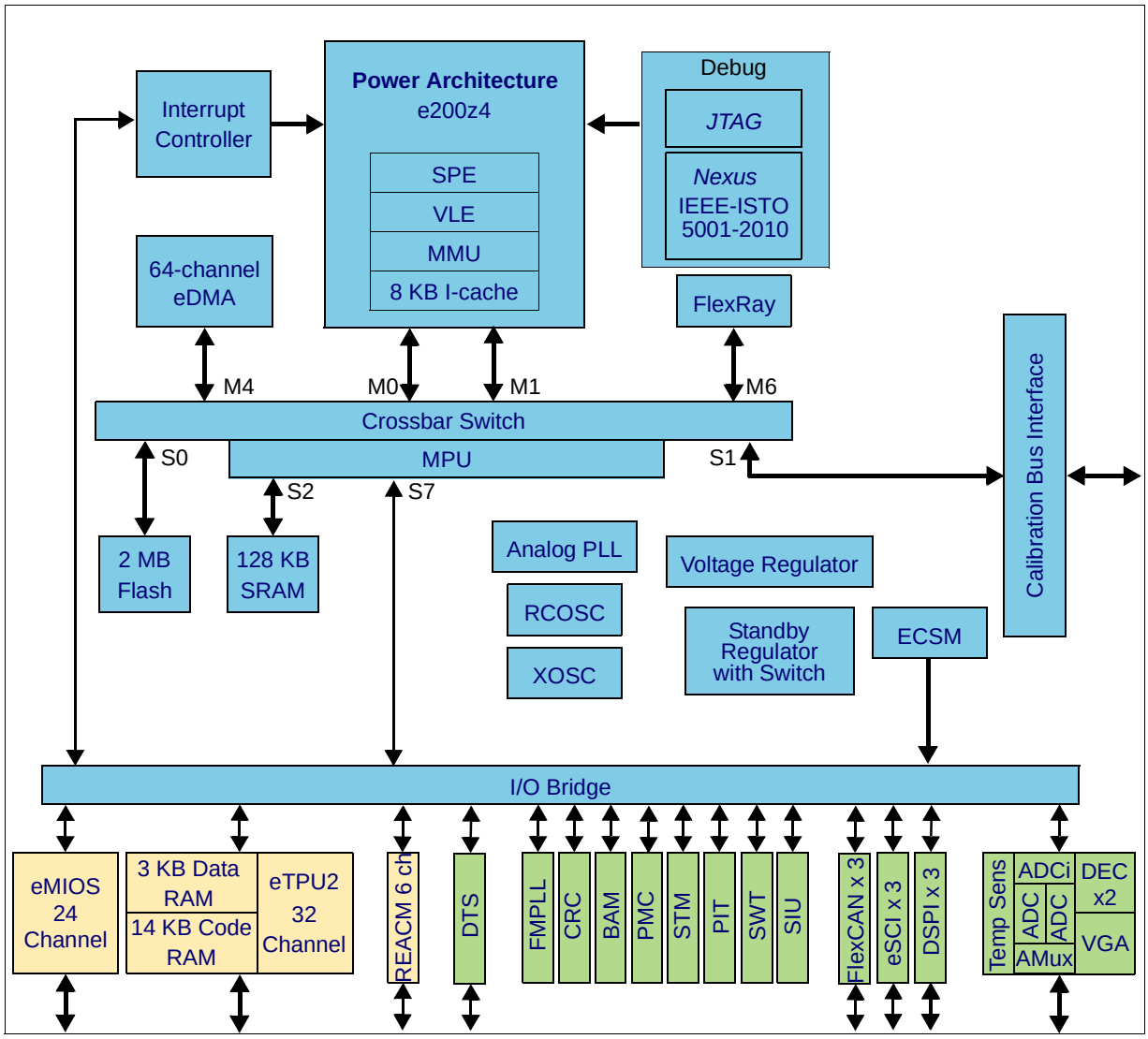
Table 2. SPC564A70 device feature summary (continued)

Feature		SPC564A70	SPC564A80
	ADC_0	Yes	
	ADC_1	Yes	
	Temperature sensor	Yes	
	Variable gain amplifier	Yes	
	Decimation filter	2	
	Sensor diagnostics	Yes	
CRC		Yes	
FMPLL		Yes	
VRC		Yes	
Supplies		5 V, 3.3 V(2)	
Low-power modes		Stop mode Slow mode	
Packages		LQFP176(3) PBGA324 496-pin CSP(4)	LQFP176(3) PBGA324 Known Good Die (KGD) 496-pin CSP(4)

1. 197 interrupt vectors are reserved.
2. 5 V single supply only for LQFP176
3. Pinout compatible with STMicroelectronics' SPC563M64 devices
4. For ST calibration tool only

1.4 Block diagram

Figure 1 shows a top-level block diagram of the SPC564A70 series.



LEGEND

ADC	– Analog to Digital Converter	**JTAG**	– IEEE 1149.1 Test Controller
ADCi	– ADC interface	**MMU**	– Memory Management Unit
AMux	– Analog Multiplexer	**MPU**	– Memory Protection Unit
BAM	– Boot Assist Module	**PMC**	– Power Management Controller
CRC	– Cyclic Redundancy Check unit	**PIT**	– Periodic Interrupt Timer
DEC	– Decimation Filter	**RCOSC**	– Low-speed RC Oscillator
DTS	– Development Trigger Semaphore	**REACM**	– Reaction Module
DSPI	– Deserial/Serial Peripheral Interface	**SIU**	– System Integration Unit
ECSM	– Error Correction Status Module	**SPE**	– Signal Processing Extension
eDMA	– Enhanced Direct Memory Access	**SRAM**	– Static RAM
eMIOS	– Enhanced Modular Input Output System	**STM**	– System Timer Module
eSCI	– Enhanced Serial Communications Interface	**SWT**	– Software Watchdog Timer
eTPU2	– Second gen. Enhanced Time Processing Unit	**VGA**	– Variable Gain Amplifier
FlexCAN	– Controller Area Network	**VLE**	– Variable Length (instruction) Encoding
FMPLL	– Frequency-Modulated Phase-Locked Loop	**XOSC**	– XTAL Oscillator

Figure 1. SPC564A70 series block diagram

Table 3 summarizes the functions of the blocks present on the SPC564A70 series microcontrollers.

Table 3. SPC564A70 series block summary

Block	Function
Boot assist module (BAM)	Block of read-only memory containing executable code that searches for user-supplied boot code and, if none is found, executes the BAM boot code resident in device ROM
Calibration bus interface	Transfers data across the crossbar switch to/from peripherals attached to the calibration tool connector
Controller area network (FlexCAN)	Supports the standard CAN communications protocol
Crossbar switch (XBAR)	Internal busmaster
Cyclic redundancy check (CRC)	CRC checksum generator
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
e200z4 core	Executes programs and interrupt handlers
Enhanced direct memory access (eDMA)	Performs complex data movements with minimal intervention from the core.
Enhanced modular input-output system (eMIOS)	Provides the functionality to generate or measure events
Enhanced queued analog-to-digital converter (eQADC)	Provides accurate and fast conversions for a wide range of applications
Enhanced serial communication interface (eSCI)	Provides asynchronous serial communication capability with peripheral devices and other microcontroller units
Enhanced time processor unit (eTPU2)	Second-generation co-processor processes real-time input events, performs output waveform generation, and accesses shared data without host intervention
Error Correction Status Module (ECSM)	The Error Correction Status Module supports a number of miscellaneous control functions for the platform, and includes registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
Flash memory	Provides storage for program code, constants, and variables
FlexRay	Provides high-speed distributed control for advanced automotive applications
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
Memory protection unit (MPU)	Provides hardware access control for all memory references generated
Nexus port controller (NPC)	Provides real-time development support capabilities in compliance with the IEEE-ISTO 5001-2010 standard
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers

Table 3. SPC564A70 series block summary (continued)

Block	Function
Reaction Module (REACM)	Works in conjunction with the eQADC and eTPU2 to increase system performance by removing the CPU from the current control loop.
System Integration Unit (SIU)	Controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation.
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System timers	Includes periodic interrupt timer with real-time interrupt; output compare timer and system watchdog timer
System watchdog timer (SWT)	Provides protection from runaway code
Temperature sensor	Provides the temperature of the device as an analog value

- 150 MHz e200z4 Power Architecture® core
  - Variable length instruction encoding (VLE)
  - Superscalar architecture with 2 execution units
  - Up to 2 integer or floating point instructions per cycle
  - Up to 4 multiply and accumulate operations per cycle
- Memory organization
  - 2 MB on-chip flash memory with ECC and read-while-write (RWW)
  - 128 KB on-chip SRAM with standby functionality (32 KB) and ECC
  - 8 KB instruction cache (with line locking), configurable as 2- or 4-way
  - 14 + 3 KB eTPU code and data RAM
  - 4 × 4 crossbar switch (XBAR)
  - 24-entry MMU
- Fail Safe Protection
  - 16-entry Memory Protection Unit (MPU)
  - CRC unit with 3 submodules
  - Junction temperature sensor
- Interrupt
  - Configurable interrupt controller (INTC) with non-maskable interrupt (NMI)
  - 64-channel eDMA
- Serial channels
  - 3 eSCI modules
  - 3 DSPI modules (2 of which support downstream Micro Second Channel [MSC])
  - 3 FlexCAN modules with 64 message buffers each
  - 1 FlexRay module (V2.1) up to 10 Mbit/s w/dual or single channel, 128 message objects, ECC
- 1 eMIOS
  - 24 unified channels
- 1 eTPU2 (second generation eTPU)
  - 32 standard channels

  - 1 reaction module (6 channels with 3 outputs per channel)
- 2 enhanced queued analog-to-digital converters (eQADCs)
  - Forty 12-bit input channels (multiplexed on 2 ADCs); expandable to 56 channels with external multiplexers
  - 6 command queues
  - Trigger and DMA support
  - 688 ns minimum conversion time
- On-chip CAN/SCI Bootstrap loader with Boot Assist Module (BAM)
- Nexus: Class 3+ for core; Class 1 for eTPU
- JTAG (5-pin)
- Development Trigger Semaphore (DTS)
  - EVTO pin for communication with external tool
- Clock generation
  - On-chip 4–40 MHz main oscillator
  - On-chip FMPLL (frequency-modulated phase-locked loop)
- Up to 112 general purpose I/O lines
  - Individually programmable as input, output or special function
  - Programmable threshold (hysteresis)
- Power reduction modes: slow, stop, and standby
- Flexible supply scheme
  - 5 V single supply with external ballast
  - Multiple external supply: 5 V, 3.3 V, and 1.2 V

1.5 Feature details

1.5.1 e200z4 core

SPC564A70 devices have a high performance e200z4 core processor:

- 32-bit Power Architecture technology programmer's model
- Variable Length Encoding (VLE) enhancements
- Dual issue, 32-bit Power Architecture technology compliant CPU
- 8 KB, 2/4-way set associative instruction cache
- Thirty-two 64-bit general purpose registers (GPRs)
- Memory Management Unit (MMU) with 24-entry fully-associative translation look-aside buffer (TLB)
- Harvard Architecture: Separate instruction bus and load/store bus
- Vectored interrupt support
- Non-maskable interrupt input
- Critical Interrupt input
- New 'Wait for Interrupt' instruction, to be used with new low power modes
- Reservation instructions for implementing read-modify-write accesses
- Signal processing extension (SPE) APU
- Single Precision Floating point (scalar and vector)
- Nexus Class 3+ debug
- Process ID manipulation for the MMU using an external tool
- In-order execution and retirement
- Precise exception handling
- Branch processing unit
  - Dedicated branch address calculation adder
  - Branch target prefetching using 8-entry BTB
- Supports independent instruction and data accesses to different memory subsystems, such as SRAM and flash memory via independent Instruction and Data BIUs
- Load/store unit
  - 2-cycle load latency
  - Fully pipelined
  - Big and Little endian support
  - Misaligned access support
- Signal Processing Extension (SPE1.1) APU supporting SIMD fixed-point operations using the 64-bit General Purpose Register file
- Embedded Floating-Point (EFP2) APU supporting scalar and vector SIMD single-precision floating-point operations, using the 64-bit General Purpose Register file
- Power management
  - Low power design – extensive clock gating
  - Power saving modes: wait
  - Dynamic power management of execution units, cache and MMU
- Testability

  - Synthesizeable, MuxD scan design
  - ABIST/MBIST for arrays
  - Built-in Parallel Signature Unit
- Calibration support allowing an external tool to modify address mapping

1.5.2 Crossbar switch (XBAR)

The XBAR multiport crossbar switch supports simultaneous connections between four master ports and four slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows three concurrent transactions to occur from the master ports to any slave port but each master must access a different slave. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters are treated with equal priority and are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access. The crossbar provides the following features:

- 4 master ports
  - CPU instruction bus
  - CPU data bus
  - eDMA
  - FlexRay
- 4 slave ports
  - Flash
  - Calibration bus interface
  - SRAM
  - Peripheral bridge
- 32-bit internal address, 64-bit internal data paths

1.5.3 Enhanced direct memory access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 64 programmable channels, with minimal intervention from the host processor. The hardware micro-architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation minimizes overall block size. The eDMA module provides the following features:

- All data movement via dual-address transfers: read from source, write to destination
- Programmable source and destination addresses, transfer size, plus support for enhanced addressing modes
- Transfer control descriptor organized to support two-deep, nested transfer operations
- An inner data transfer loop defined by a “minor” byte transfer count
- An outer data transfer loop defined by a “major” iteration count

- Channel activation via one of three methods:
  - Explicit software initiation
  - Initiation via a channel-to-channel linking mechanism for continuous transfers
  - Peripheral-paced hardware requests (one per channel)
- Support for fixed-priority and round-robin channel arbitration
- Channel completion reported via optional interrupt requests
- 1 interrupt per channel, optionally asserted at completion of major iteration count
- Error termination interrupts optionally enabled
- Support for scatter/gather DMA processing
- Ability to suspend channel transfers by a higher priority channel

1.5.4 Interrupt controller (INTC)

The INTC provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource cannot preempt each other.

The INTC provides the following features:

- 9-bit vector addresses
- Unique vector for each interrupt request source
- Hardware connection to processor or read from register
- Each interrupt source can assigned a specific priority by software
- Preemptive prioritized interrupt requests to processor
- ISR at a higher priority preempts executing ISRs or tasks at lower priorities
- Automatic pushing or popping of preempted priority to or from a LIFO
- Ability to modify the ISR or task priority to implement the priority ceiling protocol for accessing shared resources
- Low latency—3 clocks from receipt of interrupt request from peripheral to interrupt request to processor

This device also includes a non-maskable interrupt (NMI) pin that bypasses the INTC and multiplexing logic.

1.5.5 Memory protection unit (MPU)

The Memory Protection Unit (MPU) provides hardware access control for all memory references generated in a device. Using preprogrammed region descriptors, which define memory spaces and their associated access rights, the MPU concurrently monitors all

system bus transactions and evaluates the appropriateness of each transfer. Memory references with sufficient access control rights are allowed to complete; references that are not mapped to any region descriptor or have insufficient rights are terminated with a protection error response.

The MPU has these major features:

- Support for 16 memory region descriptors, each 128 bits in size
  - Specification of start and end addresses provide granularity for region sizes from 32 bytes to 4 GB
  - MPU is invalid at reset, thus no access restrictions are enforced
  - 2 types of access control definitions: processor core bus master supports the traditional {read, write, execute} permissions with independent definitions for supervisor and user mode accesses; the remaining non-core bus masters (eDMA, FlexRay) support {read, write} attributes
  - Automatic hardware maintenance of the region descriptor valid bit removes issues associated with maintaining a coherent image of the descriptor
  - Alternate memory view of the access control word for each descriptor provides an efficient mechanism to dynamically alter the access rights of a descriptor only
  - For overlapping region descriptors, priority is given to permission granting over access denying as this approach provides more flexibility to system software
- Support for two XBAR slave port connections (SRAM and PBRIDGE)
  - For each connected XBAR slave port (SRAM and PBRIDGE), MPU hardware monitors every port access using the preprogrammed memory region descriptors
  - An access protection error is detected if a memory reference does not hit in any memory region or the reference is flagged as illegal in all memory regions where it does hit. In the event of an access error, the XBAR reference is terminated with an error response and the MPU inhibits the bus cycle being sent to the targeted slave device
  - 64-bit error registers, one for each XBAR slave port, capture the last faulting address, attributes, and detail information

1.5.6 Frequency-modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 40 MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable. The PLL has the following major features:

- Input clock frequency from 4 MHz to 40 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- 3 modes of operation
  - Bypass mode with PLL off
  - Bypass mode with PLL running (default mode out of reset)
  - PLL normal mode
- Each of the 3 modes may be run with a crystal oscillator or an external clock reference

- Programmable frequency modulation
  - Modulation enabled/disabled through software
  - Triangle wave modulation up to 100 kHz modulation frequency
  - Programmable modulation depth (0% to 2% modulation depth)
  - Programmable modulation frequency dependent on reference frequency
- Lock detect circuitry reports when the PLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
- Clock Quality Module
  - Detects the quality of the crystal clock and causes interrupt request or system reset if error is detected
  - Detects the quality of the PLL output clock; if error detected, causes system reset or switches system clock to crystal clock and causes interrupt request
- Programmable interrupt request or system reset on loss of lock
- Self-clocked mode (SCM) operation

1.5.7 System integration unit (SIU)

The SPC564A70 SIU controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU. The reset controller performs reset monitoring of internal and external reset sources, and drives the RSTOUT pin. Communication between the SIU and the e200z4 CPU core is via the crossbar switch. The SIU provides the following features:

- System configuration
  - MCU reset configuration via external pins
  - Pad configuration control for each pad
  - Pad configuration control for virtual I/O via DSPI serialization
- System reset monitoring and generation
  - Power-on reset support
  - Reset status register provides last reset source to software
  - Glitch detection on reset input
  - Software controlled reset assertion
- External interrupt
  - Rising or falling edge event detection
  - Programmable digital filter for glitch rejection
  - Critical Interrupt request
  - Non-Maskable Interrupt request
- GPIO
  - Centralized control of I/O and bus pins
  - Virtual GPIO via DSPI serialization (requires external deserialization device)
  - Dedicated input and output registers for setting each GPIO and Virtual GPIO pin

- Internal multiplexing
  - Allows serial and parallel chaining of DSPIs
  - Allows flexible selection of eQADC trigger inputs
  - Allows selection of interrupt requests between external pins and DSPI
  - From a set of eTPU output channels, allows selection of source signals for decimation filter integrators

1.5.8 Flash memory

The SPC564A70 provides 2 MB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used to store instructions or data, or both. The flash module includes a Fetch Accelerator that optimizes the performance of the flash array to match the CPU architecture. The flash module interfaces the system bus to a dedicated flash memory array controller. For CPU 'loads', DMA transfers and CPU instruction fetch, it supports a 64-bit data bus width at the system bus port, and 128-bit read data interfaces to flash memory. The module contains a prefetch controller which prefetches sequential lines of data from the flash array into the buffers. Prefetch buffer hits allow no-wait responses.

The flash memory provides the following features:

- Supports a 64-bit data bus for instruction fetch, CPU loads and DMA access. Byte, halfword, word and doubleword reads are supported. Only aligned word and doubleword writes are supported.
- Fetch Accelerator
  - Architected to optimize the performance of the flash
  - Configurable read buffering and line prefetch support
  - 4-entry 128-bit wide line read buffer
  - Prefetch controller
- Hardware and software configurable read and write access protections on a per-master basis
- Interface to the flash array controller pipelined with a depth of one, allowing overlapped accesses to proceed in parallel for pipelined flash array designs
- Configurable access timing usable in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (0–31 additional cycles) usable for emulation of other memory types
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page size of 128 bits (4 words)
- ECC with single-bit correction, double-bit detection
- Program page size of 128 bits (4 words) to accelerate programming
- ECC single-bit error corrections are visible to software
- Minimum program size is 2 consecutive 32-bit words, aligned on a 0-modulo-8 byte address, due to ECC
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Shadow information stored in non-volatile shadow block
- Independent program/erase of the shadow block

1.5.9 Static random access memory (SRAM)

The SRAM provides 128 KB of general purpose system SRAM. The first 32 KB block of the SRAM is powered by its own power supply pin only during standby operation.

The SRAM controller includes these features:

- 128 KB data RAM implemented as eight 16 KB (2048 × 78 bits) blocks
- Each 16 KB block has 2 rows repairable (RAMs with internal repair feature)
- Supports read/write accesses mapped to the SRAM memory from any master
- 32 KB block powered by separate supply for standby operation
- Byte, halfword, word and doubleword addressable
- ECC performs single bit correction, double bit detection

1.5.10 Boot assist module (BAM)

The BAM is a block of read-only memory that is programmed once by ST and is identical for all SPC564A70 MCUs. The BAM program is executed every time the MCU is powered on or reset in normal mode. The BAM supports different modes of booting. They are:

- Booting from internal flash memory
- Serial boot loading (boot code is downloaded into RAM via eSCI or the FlexCAN and then executed)

The BAM also reads the reset configuration half word (RCHW) from internal flash memory and configures the SPC564A70 hardware accordingly. The BAM provides the following features:

- Sets up MMU to cover all resources and mapping of all physical addresses to logical addresses with minimum address translation
- Sets up MMU to allow user boot code to execute as either Power Architecture technology code (default) or as VLE code
- Location and detection of user boot code
- Automatic switch to serial boot mode if internal flash is blank or invalid
- Supports user programmable 64-bit password protection for serial boot mode
- Supports serial bootloading via FlexCAN bus and eSCI using standard protocol
- Supports serial bootloading via FlexCAN bus and eSCI with auto baud rate sensing
- Supports serial bootloading of either Power Architecture technology code (default) or VLE code
- Supports booting from calibration bus interface
- Supports censorship protection for internal flash memory
- Provides an option to enable the core watchdog timer
- Provides an option to disable the system watchdog timer

1.5.11 Enhanced modular input/output system (eMIOS)

The eMIOS timer module provides the capability to generate or measure events in hardware.

The eMIOS module features include:

- Twenty-four 24-bit wide channels
- 3 channels' internal timebases sharable between channels
- 1 timebase from eTPU2 can be imported and used by the channels
- Global enable feature for all eMIOS and eTPU timebases
- Dedicated pin for each channel (not available on all package types)
- Each channel (0–23) supports the following functions:
  - General Purpose Input/Output (GPIO)
  - Single Action Input Capture (SAIC)
  - Single Action Output Compare (SAOC)
  - Output Pulse Width Modulation Buffered (OPWMB)
  - Input Period Measurement (IPM)
  - Input Pulse Width Measurement (IPWM)
  - Double Action Output Compare (DOAC)
  - Modulus Counter Buffered (MCB)
  - Output Pulse Width & Frequency Modulation Buffered (OPWFMB)
- Each channel has its own pin (not available on all package types)

1.5.12 Second generation enhanced time processing unit (eTPU2)

The eTPU2 is an enhanced co-processor designed for timing control. Operating in parallel with the host CPU, the eTPU2 processes instructions and real-time input events, performs output waveform generation, and accesses shared data without host intervention. Consequently, for each timer event, the host CPU setup and service times are minimized or eliminated. A powerful timer subsystem is formed by combining the eTPU2 with its own instruction and data RAM. High-level assembler/compiler and documentation allows customers to develop their own functions on the eTPU2.

SPC564A70 devices feature the second generation of the eTPU, called eTPU2. Enhancements of the eTPU2 over the standard eTPU include:

- The Timer Counter (TCR1), channel logic and digital filters (both channel and the external timer clock input [TCRCLK]) now have an option to run at full system clock speed or system clock / 2.
- Channels support unordered transitions: transition 2 can now be detected before transition 1. Related to this enhancement, the transition detection latches (TDL1 and TDL2) can now be independently negated by microcode.
- A new User Programmable Channel Mode has been added: the blocking, enabling, service request and capture characteristics of this channel mode can be programmed via microcode.
- Microinstructions now provide an option to issue Interrupt and Data Transfer requests selected by channel. They can also be requested simultaneously at the same instruction.
- Channel Flags 0 and 1 can now be tested for branching, in addition to selecting the entry point.
- Channel digital filters can be bypassed.

The eTPU2 includes these distinctive features:

- 32 channels; each channel associated with one input and one output signal
  - Enhanced input digital filters on the input pins for improved noise immunity
  - Identical, orthogonal channels: each channel can perform any time function. Each time function can be assigned to more than one channel at a given time, so each signal can have any functionality.
  - Each channel has an event mechanism which supports single and double action functionality in various combinations. It includes two 24-bit capture registers, two 24-bit match registers, 24-bit greater-equal and equal-only comparators.
  - Input and output signal states visible from the host
- 2 independent 24-bit time bases for channel synchronization:
  - First time base clocked by system clock with programmable prescale division from 2 to 512 (in steps of 2), or by output of second time base prescaler
  - Second time base counter can work as a continuous angle counter, enabling angle based applications to match angle instead of time
  - Both time bases can be exported to the eMIOS timer module
  - Both time bases visible from the host
- Event-triggered microengine:
  - Fixed-length instruction execution in two-system-clock microcycle
  - 14 KB of code memory (SCM)
  - 3 KB of parameter (data) RAM (SPRAM)
  - Parallel execution of data memory, ALU, channel control and flow control sub-instructions in selected combinations
  - 32-bit microengine registers and 24-bit wide ALU, with 1 microcycle addition and subtraction, absolute value, bitwise logical operations on 24-bit, 16-bit, or byte operands, single-bit manipulation, shift operations, sign extension and conditional execution
  - Additional 24-bit Multiply/MAC/Divide unit which supports all signed/unsigned Multiply/MAC combinations, and unsigned 24-bit divide. The MAC/Divide unit works in parallel with the regular microcode commands.
- Resource sharing features support channel use of common channel registers, memory and microengine time:
  - Hardware scheduler works as a “task management” unit, dispatching event service routines by predefined, host-configured priority
  - Automatic channel context switch when a “task switch” occurs, that is, one function thread ends and another begins to service a request from other channel: channel-specific registers, flags and parameter base address are automatically loaded for the next serviced channel
  - SPRAM shared between host CPU and eTPU2, supporting communication either between channels and host or inter-channel
  - Hardware implementation of 4 semaphores support coherent parameter sharing between both eTPU engines
  - Dual-parameter coherency hardware support allows atomic access to 2 parameters by host

- Test and development support features:
  - Nexus Class 1 debug, supporting single-step execution, arbitrary microinstruction execution, hardware breakpoints and watchpoints on several conditions
  - Software breakpoints
  - SCM continuous signature-check built-in self test MISC (multiple input signature calculator), runs concurrently with eTPU2 normal operation

1.5.13 Reaction module (REACM)

The REACM provides the ability to modulate output signals to manage closed loop control without CPU assistance. It works in conjunction with the eQADC and eTPU2 to increase system performance by removing the CPU from the current control loop.

The REACM has the following features:

- 6 reaction channels with peak and hold control blocks
- Each channel output is a bus of 3 signals, providing ability to control 3 inputs.
- Each channel can implement a peak and hold waveform, making it possible to implement up to six independent peak and hold control channels

Target applications include solenoid control for direct injection systems and valve control in automatic transmissions.

1.5.14 Enhanced queued analog-to-digital converter (eQADC)

The eQADC block provides accurate and fast conversions for a wide range of applications. The eQADC provides a parallel interface to two on-chip analog-to-digital converters (ADC), and a single master to single slave serial interface to an off-chip external device. Both on-chip ADCs have access to all the analog channels.

The eQADC prioritizes and transfers commands from six command conversion command ‘queues’ to the on-chip ADCs or to the external device. The block can also receive data from the on-chip ADCs or from an off-chip external device into the six result queues, in parallel, independently of the command queues. The six command queues are prioritized with Queue_0 having the highest priority and Queue_5 the lowest. Queue_0 also has the added ability to bypass all buffering and queuing and abort a currently running conversion on either ADC and start a Queue_0 conversion. This means that Queue_0 will always have a deterministic time from trigger to start of conversion, irrespective of what tasks the ADCs were performing when the trigger occurred. The eQADC supports software and external hardware triggers from other blocks to initiate transfers of commands from the queues to the on-chip ADCs or to the external device. It also monitors the fullness of command queues and result queues, and accordingly generates DMA or interrupt requests to control data movement between the queues and the system memory, which is external to the eQADC.

The ADCs also support features designed to allow the direct connection of high impedance acoustic sensors that might be used in a system for detecting engine knock. These features include differential inputs; integrated variable gain amplifiers for increasing the dynamic range; programmable pull-up and pull-down resistors for biasing and sensor diagnostics.

The eQADC also integrates a programmable decimation filter capable of taking in ADC conversion results at a high rate, passing them through a hardware low pass filter, then down-sampling the output of the filter and feeding the lower sample rate results to the result FIFOs. This allows the ADCs to sample the sensor at a rate high enough to avoid aliasing of

out-of-band noise; while providing a reduced sample rate output to minimize the amount DSP processing bandwidth required to fully process the digitized waveform.

The eQADC provides the following features:

- Dual on-chip ADCs
  - 2 × 12-bit ADC resolution
  - Programmable resolution for increased conversion speed (12-bit, 10-bit, 8-bit)
    12-bit conversion time – 938 ns (1 M sample/s)
    10-bit conversion time – 813 ns (1.2 M sample/s)
    8-bit conversion time – 688 ns (1.4M sample/s)
  - Up to 10-bit accuracy at 500K sample/s and 8-bit accuracy at 1M sample/s
  - Differential conversions
  - Single-ended signal range from 0 to 5 V
  - Sample times of 2 (default), 8, 64, or 128 ADC clock cycles
  - Provides time stamp information when requested
  - Allows time stamp information relative to eTPU clock sources, such as an angle clock
  - Parallel interface to eQADC command FIFOs (CFIFOs) and result FIFOs (RFIFOs)
  - Supports both right-justified unsigned and signed formats for conversion results
- 40 single-ended input channels, expandable to 56 channels with external multiplexers (supports 4 external 8-to-1 muxes)
- 8 channels can be used as 4 pairs of differential analog input channels
- Differential channels include variable gain amplifier for improved dynamic range (×1, ×2, ×4)
- Differential channels include programmable pull-up and pull-down resistors for biasing and sensor diagnostics (200 kΩ, 100 kΩ, 5 kΩ)
- Additional internal channels for monitoring voltages (such as core voltage, I/O voltage, LVI voltages, etc.) inside the device
- An internal bandgap reference to allow absolute voltage measurements
- Silicon die temperature sensor
  - Provides temperature of silicon as an analog value
  - Read using an internal ADC analog channel
  - May be read with either ADC
- 2 decimation filters
  - Programmable decimation factor (1 to 16)
  - Selectable IIR or FIR filter
  - Up to 4th order IIR or 8th order FIR
  - Programmable coefficients
  - Saturated or non-saturated modes
  - Programmable Rounding (Convergent; Two’s Complement; Truncated)

  - Prefill mode to precondition the filter before the sample window opens
  - Supports Multiple Cascading Decimation Filters to implement more complex filter designs
  - Optional Absolute Integrators on the output of Decimation Filters
- Full duplex synchronous serial interface (SSI) to an external device
  - Free-running clock for use by an external device
  - Supports a 26-bit message length
- Priority based queues
  - Supports 6 queues with fixed priority. When commands of distinct queues are bound for the same ADC, the higher priority queue is always served first
  - Queue_0 can bypass all prioritization, buffering and abort current conversions to start a Queue_0 conversion a deterministic time after the queue trigger
  - Supports software and hardware trigger modes to arm a particular queue
  - Generates interrupt when command coherency is not achieved
- External hardware triggers
  - Supports rising edge, falling edge, high level and low level triggers
  - Supports configurable digital filter

1.5.15 Deserial serial peripheral interface (DSPI)

The DSPI block provides a synchronous serial interface for communication between the SPC564A70 MCU and external devices. The DSPI supports pin count reduction through serialization and deserialization of eTPU and eMIOS channels and memory-mapped registers. The channels and register content are transmitted using a SPI-like protocol. This SPI-like protocol is completely configurable for baud rate, polarity and phase, frame length, chip select assertion, etc. Each bit in the frame may be configured to serialize either eTPU channels, eMIOS channels or GPIO signals. The DSPI can be configured to serialize data to an external device that implements the Microsecond Bus protocol. There are three identical DSPI blocks on the SPC564A70 MCU. The DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) to improve high speed operation.

DSPI module features include:

- Selectable LVDS pads working at 40 MHz for SOUT and SCK pins for DSPI_B and DSPI_C
- Support for downstream Micro Second Channel (MSC) with Timed Serial Bus (TSB) configuration on DSPI_B and DSPI_C
- 3 sources of serialized data: eTPU_A, eMIOS output channels, and memory-mapped register in the DSPI
- 4 destinations for deserialized data: eTPU_A and eMIOS input channels, SIU external Interrupt input request, memory-mapped register in the DSPI
- 32-bit DSI and TSB modes require 32 PCR registers, 32 GPO and GPI registers in the SIU to select either GPIO, eTPU or eMIOS bits for serialization
- The DSPI module can generate and check parity in a serial frame

1.5.16 Enhanced serial communications interface (eSCI)

Three eSCI modules provide asynchronous serial communications with peripheral devices and other MCUs, and include support to interface to Local Interconnect Network (LIN) slave devices. Each eSCI block provides the following features:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit data format
- Programmable 12-bit or 13-bit data format for Timed Serial Bus (TSB) configuration to support the Microsecond bus standard
- Automatic parity generation
- LIN support
  - Compatible with LIN slaves from revisions 1.x and 2.0 of the LIN standard
  - Autonomous transmission of entire frames
  - Configurable to support all revisions of the LIN standard
  - Automatic parity bit generation
  - Double stop bit after bit error
  - 10- or 13-bit break support
- Separately enabled transmitter and receiver
- Programmable transmitter output parity
- 2 receiver wake-up methods:
  - Idle line wake-up
  - Address mark wake-up
- Interrupt-driven operation with flags
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection
- DMA support for both transmit and receive data
  - Global error bit stored with receive data in system RAM to allow post processing of errors

1.5.17 Controller area network (FlexCAN)

The SPC564A70 MCU includes three FlexCAN blocks. The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. Each FlexCAN module contains 64 message buffers.

The FlexCAN modules provide the following features:

- Full Implementation of the CAN protocol specification, Version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames

  - Zero to eight bytes data length
  - Programmable bit rate up to 1 Mbit/s
- Content-related addressing
- 64 message buffers of 0 to 8 bytes data length
- Individual Rx Mask Register per message buffer
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Includes 1088 bytes of embedded memory for message buffer storage
- Includes 256-byte memory for storing individual Rx mask registers
- Full-featured Rx FIFO with storage capacity for 6 frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against 8 extended, 16 standard or 32 partial (8 bits) IDs, with individual masking capability
- Selectable backwards compatibility with previous FlexCAN versions
- Programmable clock source to the CAN Protocol Interface, either system clock or oscillator clock
- Listen only mode capability
- Programmable loop-back mode supporting self-test operation
- 3 programmable Mask Registers
- Programmable transmit-first scheme: lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Warning interrupts when the Rx and Tx Error Counters reach 96
- Independent of the transmission medium (an external transceiver is assumed)
- Multi-master concept
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Low power mode, with programmable wakeup on bus activity

1.5.18 FlexRay

The SPC564A70 includes one dual-channel FlexRay module that implements the FlexRay Communications System Protocol Specification, Version 2.1 Rev A. Features include:

- Single channel support
- FlexRay bus data rates of 10 Mbit/s, 8 Mbit/s, 5 Mbit/s, and 2.5 Mbit/s supported
- 128 message buffers, each configurable as:
  - Receive message buffer
  - Single-buffered transmit message buffer
  - Double-buffered transmit message buffer (combines two single-buffered message buffers)
- 2 independent receive FIFOs
  - 1 receive FIFO per channel
  - Up to 255 entries for each FIFO
- ECC support

1.5.19 System timers

The system timers include two distinct types of system timer:

- Periodic interrupts/triggers using the Periodic Interrupt Timer (PIT)
- Operating system task monitors using the System Timer Module (STM)

Periodic interrupt timer (PIT)

The PIT provides five independent timer channels, capable of producing periodic interrupts and periodic triggers. The PIT has no external input or output pins and is intended to provide system ‘tick’ signals to the operating system, as well as periodic triggers for eQADC queues. Of the five channels in the PIT, four are clocked by the system clock and one is clocked by the crystal clock. This one channel is also referred to as Real-Time Interrupt (RTI) and is used to wake up the device from low power stop mode.

The following features are implemented in the PIT:

- 5 independent timer channels
- Each channel includes 32-bit wide down counter with automatic reload
- 4 channels clocked from system clock
- 1 channel clocked from crystal clock (wake-up timer)
- Wake-up timer remains active when System STOP mode is entered; used to restart system clock after predefined time-out period
- Each channel optionally able to generate an interrupt request or a trigger event (to trigger eQADC queues) when timer reaches zero

System timer module (STM)

The STM is designed to implement the software task monitor as defined by AUTOSAR[(a)]. It consists of a single 32-bit counter, clocked by the system clock, and four independent timer

a. AUTOSAR: AUTomotive Open System ARchitecture (see www.autosar.org)

comparators. These comparators produce a CPU interrupt when the timer exceeds the programmed value.

The following features are implemented in the STM:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.5.20 Software watchdog timer (SWT)

The SWT is a second watchdog module to complement the standard Power Architecture watchdog integrated in the CPU core. The SWT is a 32-bit modulus counter, clocked by the system clock or the crystal clock, that can provide a system reset or interrupt request when the correct software key is not written within the required time window.

The following features are implemented:

- 32-bit modulus counter
- Clocked by system clock or crystal clock
- Optional programmable watchdog window mode
- Can optionally cause system reset or interrupt request on timeout
- Reset by writing a software key to memory mapped register
- Enabled out of reset
- Configuration is protected by a software key or a write-once register

1.5.21 Cyclic redundancy check (CRC) module

The CRC computing unit is dedicated to the computation of CRC off-loading the CPU. The CRC module features:

- Support for CRC-16-CCITT (*x*25 protocol):
  - $x^{16} + x^{12} + x^5 + 1$
- Support for CRC-32 (Ethernet protocol):
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Zero wait states for each write/read operations to the CRC_CFG and CRC_INP registers at the maximum frequency

1.5.22 Error correction status module (ECSM)

The ECSM provides a myriad of miscellaneous control functions regarding program-visible information about the platform configuration and revision levels, a reset status register, a software watchdog timer, wakeup control for exiting sleep modes, and information on platform memory errors reported by error-correcting codes and/or generic access error information for certain processor cores.

The Error Correction Status Module supports a number of miscellaneous control functions for the platform. The ECSM includes these features:

- Registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
- For test purposes, optional registers to specify the generation of double-bit memory errors are enabled on the SPC564A70.

The sources of the ECC errors are:

- Flash memory
- SRAM
- Peripheral RAM (FlexRay, CAN, eTPU2 parameter RAM)

1.5.23 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access privilege level per peripheral (per master: read access enable; write access enable)
- Write buffering for peripherals
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

1.5.24 Calibration bus interface

The calibration bus interface controls data transfer across the crossbar switch to/from memories or peripherals attached to the calibration tool connector in the calibration address space. The calibration bus interface is only available in the calibration tool.

Features include:

- 3.3 V ± 10% I/O (3.0 V to 3.6 V)
- Memory controller supports various memory types
- 16-bit data bus, up to 22-bit address bus
- Pin muxing supports 32-bit muxed bus
- Selectable drive strength
- Configurable bus speed modes
- Bus monitor
- Configurable wait states

1.5.25 Power management controller (PMC)

The PMC contains circuitry to generate the internal 3.3 V supply and to control the regulation of 1.2 V supply with an external NPN ballast transistor. It also contains low voltage inhibit (LVI) and power-on reset (POR) circuits for the 1.2 V supply, the 3.3 V supply, the 3.3 V/5 V supply of the closest I/O segment (VDDEH1), and the 5 V supply of the regulators (VDDREG).

1.5.26 Nexus port controller (NPC)

The NPC block provides real-time Nexus Class3+ development support capabilities for the SPC564A70 Power Architecture technology-based MCU in compliance with the IEEE-ISTO 5001-2010 standard. MDO port widths of 4 pins and 12 pins are available in all packages.

1.5.27 JTAG controller (JTAGC)

The JTAG controller (JTAGC) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001 standard. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE 1149.1-2001 standard and supports the following features:

- IEEE 1149.1-2001 Test Access Port (TAP) interface 4 pins (TDI, TMS, TCK, and TDO)
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD, HIGHZ, CLAMP
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC
  - ACCESS_AUX_TAP_ONCE
  - ACCESS_AUX_TAP_eTPU
  - ACCESS_CENSOR
- 3 test data registers to support JTAG Boundary Scan mode
  - Bypass register
  - Boundary scan register
  - Device identification register
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- Censorship Inhibit Register
  - 64-bit Censorship password register
  - If the external tool writes a 64-bit password that matches the Serial Boot password stored in the internal flash shadow row, Censorship is disabled until the next system reset.

1.5.28 Development trigger semaphore (DTS)

SPC564A70 devices include a system development feature, the Development Trigger Semaphore (DTS) module, that enables user software to signal to an external tool—by driving a persistent (affected only by reset or an external tool) signal on an external device pin—that data is available. The DTS includes a register of semaphores (32-bits) and an identification register.

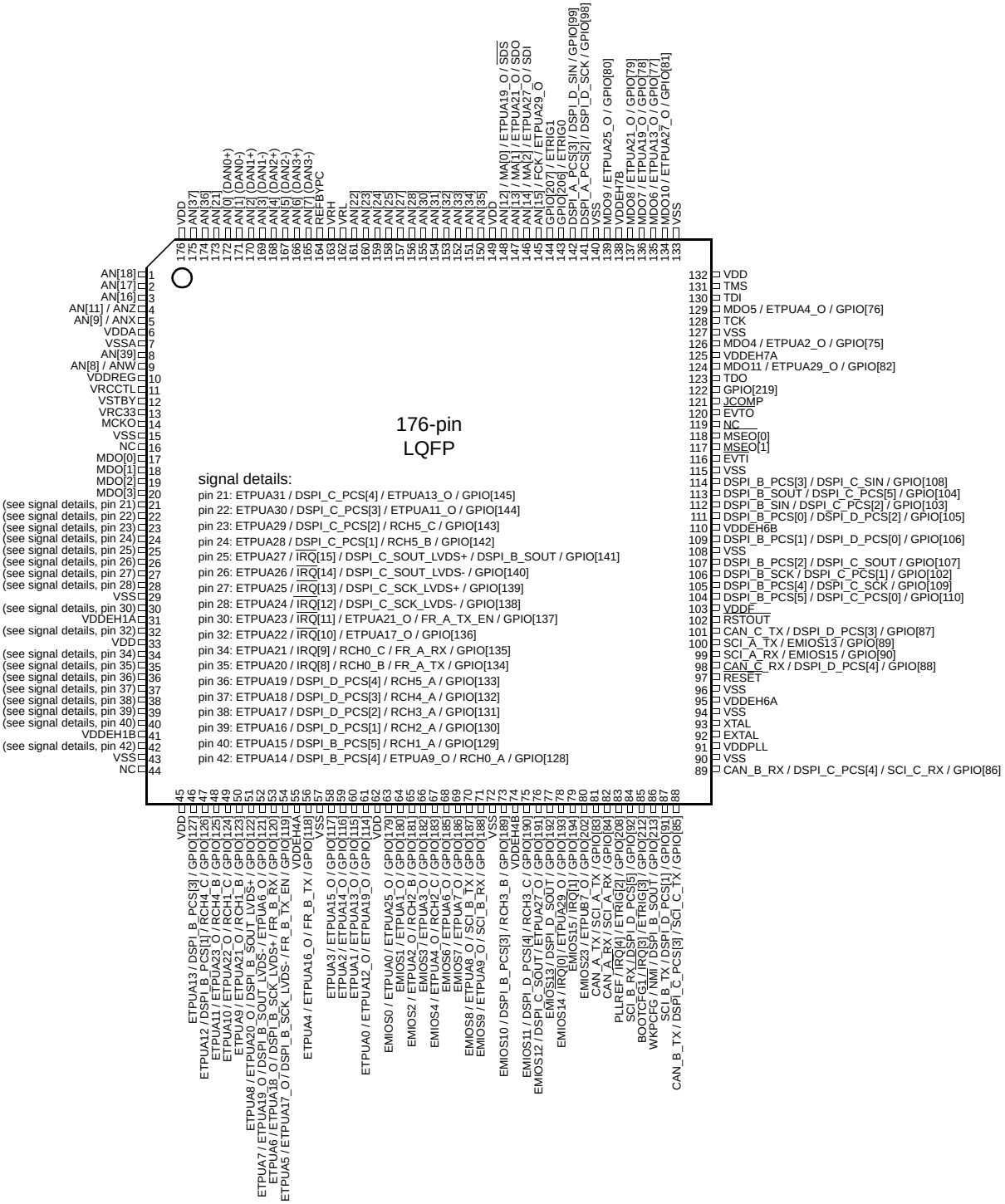
There are a variety of ways this module can be used, including as a component of an external real-time data acquisition system.

2 Pinout and signal description

This section contains the pinouts for all production packages for the SPC564A70 device. For pin signal descriptions, please refer to *Table 4*

Note: Any pins labeled “NC” are to be left unconnected. Any connection to an external circuit or voltage may cause unpredictable device behavior or damage.

2.1 LQFP176 pinout



Note: Pin 96 (VSS) should be tied low.

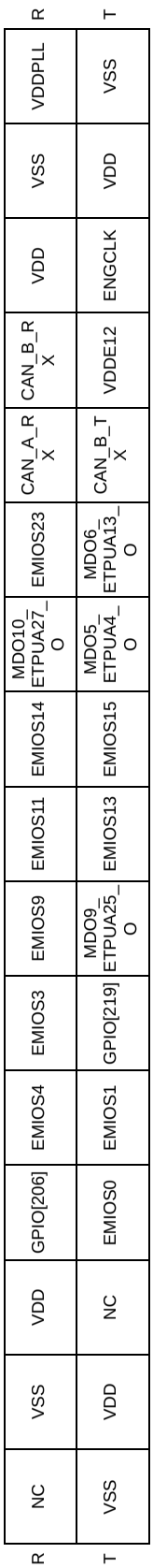
Figure 2. 176-pin LQFP pinout (top view)

2.2 LBGA208 ballmap[b]

Figure 3. 208-pin LBGA package ballmap (viewed from above)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	AN9	AN11	VDDA1	VSSA1	AN1	AN5	VRH	VRL	AN27	VSSA0	AN12-SDS	MDO2	MDO0	VRC33	VSS	A
B	VDD	VSS	AN8	AN21	AN0	AN4	REFBYPC	AN22	AN25	AN28	VDDA0	AN13-SDO	MDO3	MDO1	VSS	VDD	B
C	VSTBY	VDD	VSS	AN17	AN34	AN16	AN3	AN7	AN23	AN32	AN33	AN14-SDI	AN15-FCK	VSS	MSEO0	TCK	C
D	VRC33	AN39	VDD	VSS	AN18	AN2	AN6	AN24	AN30	AN31	AN35	VDDEH7	VSS	TMS	EVTO	NC	D
E	ETPUA30	ETPUA31	AN37	VDD									NC	TDI	EVTI	MSEO1	E
F	ETPUA28	ETPUA29	ETPUA26	AN36									VDDEH6AB	TDO	MCKO	JCOMP	F
G	ETPUA24	ETPUA27	ETPUA25	ETPUA21			VSS	VSS	VSS	VSS			DSPI_B_SOUT	DSPI_B_PCS[3]	DSPI_B_SIN	DSPI_B_PCS[0]	G
H	ETPUA23	ETPUA22	ETPUA17	ETPUA18			VSS	VSS	VSS	VSS			GPIO[99]	DSPI_B_PCS[4]	DSPI_B_PCS[2]	DSPI_B_PCS[1]	H
J	ETPUA20	ETPUA19	ETPUA14	ETPUA13			VSS	VSS	VSS	VSS			DSPI_B_PCS[5]	SCI_A_TX	GPIO[98]	DSPI_B_SCK	J
K	ETPUA16	ETPUA15	ETPUA7	VDDEH1AB			VSS	VSS	VSS	VSS			CAN_C_TX	SCI_A_RX	RSTOUT	VDDREG	K
L	ETPUA12	ETPUA11	ETPUA6	TCRCLKA									SCI_B_TX	CAN_C_RX	WKPCFG	RESET	L
M	ETPUA10	ETPUA9	ETPUA1	ETPUA5									SCI_B_RX	PLLREF	BOOTCFG1	VSS	M
N	ETPUA8	ETPUA4	ETPUA0	VSS	VDD	VRC33	EMIOS2	EMIOS10	VDDEH4AB	EMIOS12	MDO7_ETPUA19_O	VRC33	VSS	VRCCTL	NC	EXTAL	N
P	ETPUA3	ETPUA2	VSS	VDD	GPIO[207]	NC	EMIOS6	EMIOS8	MDO11_ETPUA29_O	MDO4_ETPUA2_O	MDO8_ETPUA21_O	CAN_A_TX	VDD	VSS	NC	XTAL	P

b. LBGA208 is available upon specific request. Please contact your ST sales office for details.


R
T
NC
VSS
VDD
VSS
R
T
VSS
VDD
NC
EMIOS0
EMIOS1
GPIO[219]
ETPUA25_O
EMIOS15
EMIOS13
ETPUA4_O
ETPUA13_O
CAN_B_TX
VDDE12
ENGCLK
VDD
VDDPLL
VSS
VDD
GPIO[206]
EMIOS4
EMIOS3
MDO9_
EMIOS9
EMIOS11
EMIOS14
MDO10_
EMIOS23
CAN_A_RX
CAN_B_RX
VDD
VSS
R
T

2.3 PBGA324 ballmap

	1	2	3	4	5	6	7	8	9	10	11
A	VSS	VDD	VSTBY	AN37	AN11	VDDA	VSSA	AN1	AN5	VRH	VRL
B	VRC33	VSS	VDD	AN36	AN39	AN19	AN16	AN0	AN4	REFBYPC	AN23
C	ETPUA30	ETPUA31	VSS	VDD	AN38	AN17	AN20	AN21	AN3	AN7	AN22
D	ETPUA28	ETPUA29	ETPUA26	VSS	VDD	AN8	AN9	AN10	AN18	AN2	AN6
E	ETPUA24	ETPUA27	ETPUA25	ETPUA21							
F	ETPUA23	ETPUA22	ETPUA17	ETPUA18							
G	ETPUA20	ETPUA19	ETPUA14	ETPUA13							
H	ETPUA16	ETPUA15	ETPUA10	VDDEH1AB							
J	ETPUA12	ETPUA11	ETPUA6	ETPUA9					VSS	VSS	VSS
K	ETPUA8	ETPUA7	ETPUA2	ETPUA5					VSS	VSS	VSS
L	ETPUA4	ETPUA3	ETPUA0	ETPUA1					VSS	VSS	VSS

Figure 4. 324-pin PBGA package ballmap (northwest, viewed from above)

M	NC	TCRCLKA	NC	NC					NC	NC	VSS
N	NC	NC	NC	NC					VSS	VSS	NC
P	GPIO[12]	GPIO[13]	NC	VRC33					VSS	VSS	NC
R	GPIO[14]	GPIO[15]	VDDE-EH	NC							
T	GPIO[16]	GPIO[17]	NC	NC							
U	NC	NC	NC	NC							
V	NC	NC	NC	NC							
W	NC	VDDE-EH	NC	VSS	VDD	NC	VRC33	NC	NC	NC	NC
Y	NC	NC	VSS	VDD	NC	NC	NC	NC	GPIO[207]	NC	NC
AA	NC	VSS	VDD	NC	NC	NC	GPIO[206]	NC	NC	NC	EMIOS3
AB	VSS	VDD	NC	NC	NC	NC	NC	NC	NC	EMIOS0	EMIOS1
	1	2	3	4	5	6	7	8	9	10	11

Figure 5. 324-pin PBGA package ballmap (southwest, viewed from above)

12	13	14	15	16	17	18	19	20	21	22	
AN27	AN28	AN35	VSSA	AN12_SDS	MDO11_ ETPUA29_O	MDO10_ ETPUA27_O	MDO8_ ETPUA21_O	VDD	VRC33	VSS	A
AN26	AN31	AN32	VSSA	AN13_SDO	MDO9_ ETPUA25_O	MDO7_ ETPUA19_O	MDO4_ ETPUA2_O	MDO0	VSS	NC2	B
AN25	AN30	AN33	VDDA	AN14_SDI	MDO5_ ETPUA4_O	MDO2	MDO1	VSS	NC2	VDD	C
AN24	AN29	AN34	VDDEH7	AN15_FCK	MDO6_ ETPUA13_O	MDO3	VSS	NC2	TCK	TDI	D
							NC2	TMS	TDO	NC	E
							NC2	JCOMP	EVTI	EVTO	F
							RDY	MCKO	MSEO0	MSEO1	G
							VDDEH6AB	GPIO[203]	GPIO[204]	DSPI_B_SIN	H
VSS	VSS	NC2					DSPI_B_ SOUT	DSPI_B_ PCS[3]	DSPI_B_ PCS[0]	DSPI_B_ PCS[1]	J
VSS	VSS	VSS					GPIO[99]	DSPI_B_ PCS[4]	DSPI_B_SCK	DSPI_B_ PCS[2]	K
VSS	VSS	VSS					DSPI_B_ PCS[5]	DSPI_A_ SOUT	DSPI_A_SIN	DSPI_A_SCK	L

Figure 6. 324-pin PBGA package ballmap (northeast, viewed from above)

VSS	VSS	VSS					DSPI_A_ PCS[1]	DSPI_A_ PCS[0]	GPIO[98]	VDDREG	M
VSS	VSS	VSS					DSPI_A_ PCS[4]	SCI_A_TX	DSPI_A_ PCS[5]	NC	N
VSS	VSS	VSS					CAN_C_TX	SCI_A_RX	RSTOUT	RSTCFG	P
							WKPCFG	CAN_C_RX	SCI_B_TX	RESET	R
							SCI_B_RX	BOOTCFG1	VSS	VSS	T
							VDDEH6AB	PLLCFG1	BOOTCFG0	EXTAL	U
							VDD	VRCCTL	PLLREF	XTAL	V
EMIOS2	EMIOS8	VDDEH4AB	EMIOS12	EMIOS21	VDDE12	SCI_C_TX	VSS	VDD	NC	VDDPLL	W
EMIOS6	EMIOS10	EMIOS15	EMIOS17	EMIOS22	CAN_A_TX	VDDE12	SCI_C_RX	VSS	VDD	VRC33	Y
EMIOS5	EMIOS9	EMIOS13	EMIOS16	EMIOS19	EMIOS23	CAN_A_RX	VDDE12	CLKOUT	VSS	VDD	AA
EMIOS4	EMIOS7	EMIOS11	EMIOS14	EMIOS18	EMIOS20	CAN_B_TX	CAN_B_RX	VDDE12	ENGCLK	VSS	AB
12	13	14	15	16	17	18	19	20	21	22	

Figure 7. 324-pin PBGA package ballmap (southeast, viewed from above)

2.4 Signal summary

Table 4. SPC564A70 signal properties

Name[1]	Function[2]	P / A / G[3]	PCR PA field (4)	PCR (5)	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
GPIO											
FR_A_TX GPIO[12]	FlexRay transmit data channel A GPIO	A1 G	010 000	12	O I/O	VDDE-EH / Medium	— / Up	— / Up	—	—	P1
FR_A_TX_EN GPIO[13]	FlexRay ch. A tx data enable GPIO	A1 G	010 000	13	O I/O	VDDE-EH / Medium	— / Up	— / Up	—	—	P2
FR_A_RX GPIO[14]	FlexRay receive data ch. A GPIO	A1 G	010 000	14	I I/O	VDDE-EH / Medium	— / Up	— / Up	—	—	R1
FR_B_TX GPIO[15]	FlexRay transmit data ch. B GPIO	A1 G	010 000	15	O I/O	VDDE-EH / Medium	— / Up	— / Up	—	—	R2
FR_B_TX_EN GPIO[16]	FlexRay tx data enable for ch. B GPIO	A1 G	010 000	16	O I/O	VDDE-EH / Medium	— / Up	— / Up	—	—	T1
FR_B_RX GPIO[17]	FlexRay receive data channel B GPIO	A1 G	010 000	17	I I/O	VDDE-EH / Medium	— / Up	— / Up	—	—	T2
GPIO[206] ETRIG0	GPIO / eQADC Trigger Input	G	00	206	I/O[10]	VDDEH7 / Slow[11]	— / Up	— / Up	143	R4	AA7
GPIO[207] ETRIG1	GPIO / eQADC Trigger Input	G	00	207	I/O[10]	VDDEH7 / Slow	— / Up	— / Up	144	P5	Y9
GPIO[219]	GPIO	G	000	219 (12)	I/O	VDDEH7 / MultV	— / Up	— / Up	122	T6	—
Reset / Configuration											
$\overline{\text{RESET}}$	External Reset Input	P	—	—	I	VDDEH6 / Slow	$\overline{\text{RESET}}$ / Up	$\overline{\text{RESET}}$ / Up	97	L16	R22
$\overline{\text{RSTOUT}}$	External Reset Output	P	01	230	O	VDDEH6 / Slow	$\overline{\text{RSTOUT}}$ / Down	$\overline{\text{RSTOUT}}$ / Down	102	K15	P21
PLLREF IRQ[4] ETRIG2 GPIO[208]	FMPLL Mode Selection External Interrupt Request eQADC Trigger Input GPIO	P A1 A2 G	001 010 100 000	208	I I I I/O	VDDEH6 / Slow	— / Up	PLLREF / Up	83	M14	V21

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
PLLCFG1[13] IRQ[5] DSPI_D_SOUT GPIO[209]	— External interrupt request DSPI D data output GPIO	— A1 A2 G	— 010 100 000	209	— I O I/O	VDDEH6 / Medium	— / Up	— / Up	—	—	U20
RSTCFG GPIO[210]	RSTCFG GPIO	P G	01 00	210	I I/O	VDDEH6 / Slow	— / Down	—	—	—	P22
BOOTCFG[0] IRQ[2] GPIO[211]	Boot Config. Input External Interrupt Request GPIO	P A1 G	01 10 00	211	I I I/O	VDDEH6 / Slow	— / Down	BOOTCFG[0] / Down	—	—	U21
BOOTCFG[1] IRQ[3] ETRIG3 GPIO[212]	Boot Config. Input External Interrupt Request eQADC Trigger Input GPIO	P A1 A2 G	001 010 100 000	212	I I I I/O	VDDEH6 / Slow	— / Down	BOOTCFG[1] / Down	85	M15	T20
WKPCFG $\overline{\text{NMI}}$ DSPI_B_SOUT GPIO[213]	Weak Pull Config. Input Non-Maskable Interrupt DSPI B data output GPIO	P A1 A2 G	001 010 100 000	213	I I O I/O	VDDEH6 / Medium	— / Up	WKPCFG / Up	86	L15	R19
Calibration Bus											
CAL_CS0	Calibration chip select	P	01	336	O	VDDE12 / Fast		— / —	—	—	—
CAL_CS2 CAL_ADDR[10] CAL_WE[2]/BE[2]	Calibration chip select Calibration address bus Calibration write/byte enable	P A1 A2	001 010 100	338	O I/O O	VDDE12 / Fast		— / —	—	—	—
CAL_CS3 CAL_ADDR[11] CAL_$\overline{\text{WE}}$[3]/$\overline{\text{BE}}$[3]	Calibration chip select Calibration address bus Calibration write/byte enable	P A1 A2	001 010 100	339	O I/O O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[12] CAL_$\overline{\text{WE}}$[2]/$\overline{\text{BE}}$[2]	Calibration address bus Calibration write/byte enable	P A1	01 10	340	I/O O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[13] CAL_$\overline{\text{WE}}$[3]/$\overline{\text{BE}}$[3]	Calibration address bus Calibration write/byte enable	P A1	01 10	340	I/O O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[14] CAL_DATA[31]	Calibration address bus Calibration data bus	P A1	01 10	340	I/O I/O	VDDE12 / Fast		— / —	—	—	—

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
CAL_ADDR[15] CAL_ALE	Calibration address bus Calibration address latch enable	P A1	01 10	340	I/O O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[16] CAL_DATA[16]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[17] CAL_DATA[17]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[18] CAL_DATA[18]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[19] CAL_DATA[19]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[20] CAL_DATA[20]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[21] CAL_DATA[21]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[22] CAL_DATA[22]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[23] CAL_DATA[23]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[24] CAL_DATA[24]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[25] CAL_DATA[25]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[26] CAL_DATA[26]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[27] CAL_DATA[27]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[28] CAL_DATA[28]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[29] CAL_DATA[29]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[30] CAL_DATA[30]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
CAL_DATA[0]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[1]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[2]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[3]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[4]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[5]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[6]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[7]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[8]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[9]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[10]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[11]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[12]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[13]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[14]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—
CAL_DATA[15]	Calibration data bus	P	01	341	I/O	VDDE12 / Fast	— / Up	— / Up	—	—	—

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
CAL_RD_WR	Calibration data bus	P	01	342	O	VDDE12 / Fast		— / —	—	—	—
CAL_WE[0]	Calibration write enable	P	01	342	O	VDDE12 / Fast		— / —	—	—	—
CAL_WE[1]	Calibration write enable	P	01	342	O	VDDE12 / Fast		— / —	—	—	—
CAL_OE	Calibration output enable	P	01	342	O	VDDE12 / Fast		— / —	—	—	—
CAL_TS CAL_ALE	Calibration transfer start Address Latch Enable	P A1	01 10	343	O O	VDDE12 / Fast		— / —	—	—	—
CAL_MDO[4]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[4] / —	—	—	—
CAL_MDO[5]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[5] / —	—	—	—
CAL_MDO[6]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[6] / —	—	—	—
CAL_MDO[7]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[7] / —	—	—	—
CAL_MDO[8]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[8] / —	—	—	—
CAL_MDO[9]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[9] / —	—	—	—
CAL_MDO[10]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[10] / —	—	—	—
CAL_MDO[11]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[11] / —	—	—	—
NEXUS[14]											
$\overline{\text{EVTI}}$	Nexus event in	P	01	231	I	VDDEH7 / MultiV	— / Up	$\overline{\text{EVTI}}$ / Up	116	E15	F21
$\overline{\text{EVTO}}$[15]	Nexus event out	P	01	227	O	VDDEH7 / MultiV	ABR/Up	$\overline{\text{EVTO}}$ / —	120	D15	F22

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
MCKO	Nexus message clock out	P	—	219[12]	O	VRC33 / Fast	—	MCKO / —	14	F15	G20
MDO[0]	Nexus message data out	P	01	220	O	VRC33 / Fast	—	MDO[0] / —	17	A14	B20
MDO[1]	Nexus message data out	P	01	221	O	VRC33 / Fast	—	MDO[1] / —	18	B14	C19
MDO[2]	Nexus message data out	P	01	222	O	VRC33 / Fast	—	MDO[2] / —	19	A13	C18
MDO[3]	Nexus message data out	P	01	223	O	VRC33 / Fast	—	MDO[3] / —	20	B13	D18
MDO[4] ETPUA2_O GPIO[75]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	75	O O I/O	VDDEH7 / MultiV	—	— / —	126	P10	B19
MDO[5] ETPUA4_O GPIO[76]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	76	O O I/O	VDDEH7 / MultiV	—	— / —	129	T10	C17
MDO[6] ETPUA13_O GPIO[77]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	77	O O I/O	VDDEH7 / MultiV	—	— / —	135	T11	D17
MDO[7] ETPUA19_O GPIO[78]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	78	O O I/O	VDDEH7 / MultiV	—	— / —	136	N11	B18
MDO[8] ETPUA21_O GPIO[79]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	79	O O I/O	VDDEH7 / MultiV	—	— / —	137	P11	A19
MDO[9] ETPUA25_O PIO[80]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	80	O O I/O	VDDEH7 / MultiV	—	— / —	139	T7	B17
MDO[10] ETPUA27_O GPIO[81]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	81	O O I/O	VDDEH7 / MultiV	—	— / —	134	R10	A18
MDO[11] ETPUA29_O GPIO[82]	Nexus message data out eTPU A channel (output only) GPIO[82]	P A1 G	01 10 00	82	O O I/O	VDDEH7 / MultiV	—	— / —	124	P9	A17

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
MSEO[0]	Nexus message start/end out	P	01	224	O	VDDEH7 / MultiV	—	$\overline{\text{MSEO[0]}}$ / —	118	C15	G21
MSEO[1]	Nexus message start/end out	P	01	225	O	VDDEH7 / MultiV	—	$\overline{\text{MSEO[1]}}$ / —	117	E16	G22
RDY	Nexus ready output	P	01	226	O	VDDEH7 / MultiV	—	—	—	—	G19
JTAG											
TCK	JTAG test clock input	P	01	—	I	VDDEH7 / MultiV	TCK / Down	TCK / Down	128	C16	D21
TDI	JTAG test data input	P	01	232	I	VDDEH7 / MultiV	TDI / Up	TDI / Up	130	E14	D22
TDO	JTAG test data output	P	01	228	O	VDDEH7 / MultiV	TDO / Up	TDO / Up	123	F14	E21
TMS	JTAG test mode select input	P	01	—	I	VDDEH7 / MultiV	TMS / Up	TMS / Up	131	D14	E20
JCOMP	JTAG TAP controller enable	P	01	—	I	VDDEH7 / MultiV	JCOMP / Down	JCOMP / Down	121	F16	F20
FlexCAN											
CAN_A_TX SCI_A_TX GPIO[83]	FlexCAN A transmit eSCI A transmit GPIO	P A1 G	01 10 00	83	O O I/O	VDDEH6 / Slow	— / Up	— / Up	81	P12	Y17
CAN_A_RX SCI_A_RX GPIO[84]	FlexCAN A receive eSCI A receive GPIO	P A1 G	01 10 00	84	I I I/O	VDDEH6 / Slow	— / Up	— / Up	82	R12	AA18
CAN_B_TX DSPI_C_PCS[3] SCI_C_TX GPIO[85]	FlexCAN B transmit DSPI C peripheral chip select eSCI C transmit GPIO	P A1 A2 G	001 010 100 000	85	O O O I/O	VDDEH6 / Slow	— / Up	— / Up	88	T12	AB18
CAN_B_RX DSPI_C_PCS[4] SCI_C_RX GPIO[86]	FlexCAN B receive DSPI C peripheral chip select eSCI C receive GPIO	P A1 A2 G	001 010 100 000	86	I O I I/O	VDDEH6 / Slow	— / Up	— / Up	89	R13	AB19

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
CAN_C_TX DSPI_D_PCS[3] GPIO[87]	FlexCAN C transmit DSPI D peripheral chip select GPIO	P A1 G	01 10 00	87	O O I/O	VDDEH6 / Medium	— / Up	— / Up	101	K13	P19
CAN_C_RX DSPI_D_PCS[4] GPIO[88]	FlexCAN C receive DSPI D peripheral chip select GPIO	P A1 G	01 10 00	88	I O I/O	VDDEH6 / Slow	— / Up	— / Up	98	L14	R20
eSCI											
SCI_A_TX EMIOS13[16] GPIO[89]	eSCI A transmit eMIOS channel GPIO	P A1 G	01 10 00	89	O O I/O	VDDEH6 / Medium	— / Up	— / Up	100	J14	N20
SCI_A_RX EMIOS15[16] GPIO[90]	eSCI A receive eMIOS channel GPIO	P A1 G	01 10 00	90	I O I/O	VDDEH6 / Medium	— / Up	— / Up	99	K14	P20
SCI_B_TX DSPI_D_PCS[1] GPIO[91]	eSCI B transmit DSPI D peripheral chip select GPIO	P A1 G	01 10 00	91	O O I/O	VDDEH6 / Medium	— / Up	— / Up	87	L13	R21
SCI_B_RX DSPI_D_PCS[5] GPIO[92]	eSCI B receive DSPI D peripheral chip select GPIO	P A1 G	01 10 00	92	I O I/O	VDDEH6 / Medium	— / Up	— / Up	84	M13	T19
SCI_C_TX GPIO[244]	eSCI C transmit GPIO	P G	01 00	244	O I/O	VDDEH6 / Medium	— / Up	— / Up	—	—	W18
SCI_C_RX GPIO[245]	eSCI C receive GPIO	P G	01 00	245	I I/O	VDDEH6 / Medium	— / Up	— / Up	—	—	Y19
DSPI											
DSPI_A_SCK[17] DSPI_C_PCS[1] GPIO[93]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	93	— O I/O	VDDEH7 / Medium	— / Up	— / Up	—	—	L22
DSPI_A_SIN[17] DSPI_C_PCS[2] GPIO[94]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	94	— O I/O	VDDEH7 / Medium	— / Up	— / Up	—	—	L21
DSPI_A_SOUT[17] DSPI_C_PCS[5] GPIO[95]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	95	— O I/O	VDDEH7 / Medium	— / Up	— / Up	—	—	L20

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
DSPI_A_PCS[0][17] DSPI_D_PCS[2] GPIO[96]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	96	— O I/O	VDDEH7 / Medium	— / Up	— / Up	—	—	M20
DSPI_A_PCS[1][17] DSPI_B_PCS[2] GPIO[97]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	97	— O I/O	VDDEH7 / Medium	— / Up	— / Up	—	—	M19
DSPI_A_PCS[2][17] DSPI_D_SCK GPIO[98]	— SPI clock pin for DSPI module GPIO	— A1 G	— 10 00	98	— I/O I/O	VDDEH7 / Medium	— / Up	— / Up	141	J15	M21
DSPI_A_PCS[3][17] DSPI_D_SIN GPIO[99]	— DSPI D data input GPIO	— A1 G	— 10 00	99	— I I/O	VDDEH7 / Medium	— / Up	— / Up	142	H13	K19
DSPI_A_PCS[4][17] DSPI_D_SOUT GPIO[100]	— DSPI D data output GPIO	— A1 G	— 10 00	100	— O I/O	VDDEH7 / Medium	— / Up	— / Up	—	—	N19
DSPI_A_PCS[5][17] DSPI_B_PCS[3] GPIO[101]	— DSPI B peripheral chip select GPIO	— A1 G	— 10 00	101	— O I/O	VDDEH7 / Medium	— / Up	— / Up	—	—	N21
DSPI_B_SCK DSPI_C_PCS[1] GPIO[102]	SPI clock pin for DSPI module DSPI B peripheral chip select GPIO	P A1 G	01 10 00	102	I/O O I/O	VDDEH6 / Medium	— / Up	— / Up	106	J16	K21
DSPI_B_SIN DSPI_C_PCS[2] GPIO[103]	DSPI B data input DSPI C peripheral chip select GPIO	P A1 G	01 10 00	103	I O I/O	VDDEH6 / Medium	— / Up	— / Up	112	G15	H22
DSPI_B_SOUT DSPI_C_PCS[5] GPIO[104]	DSPI B data output DSPI C peripheral chip select GPIO	P A1 G	01 10 00	104	O O I/O	VDDEH6 / Medium	— / Up	— / Up	113	G13	J19
DSPI_B_PCS[0] DSPI_D_PCS[2] GPIO[105]	DSPI B peripheral chip select DSPI D peripheral chip select GPIO	P A1 G	01 10 00	105	I/O O I/O	VDDEH6 / Medium	— / Up	— / Up	111	G16	J21
DSPI_B_PCS[1] DSPI_D_PCS[0] GPIO[106]	DSPI B peripheral chip select DSPI D peripheral chip select GPIO	P A1 G	01 10 00	106	O I/O I/O	VDDEH6 / Medium	— / Up	— / Up	109	H16	J22

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
DSPI_B_PCS[2] DSPI_C_SOUT GPIO[107]	DSPI B peripheral chip select DSPI C data output GPIO	P A1 G	01 10 00	107	O O I/O	VDDEH6 / Medium	— / Up	— / Up	107	H15	K22
DSPI_B_PCS[3] DSPI_C_SIN GPIO[108]	DSPI B peripheral chip select DSPI C data input GPIO	P A1 G	01 10 00	108	O I I/O	VDDEH6 / Medium	— / Up	— / Up	114	G14	J20
DSPI_B_PCS[4] DSPI_C_SCK GPIO[109]	DSPI B peripheral chip select SPI clock pin for DSPI module GPIO	P A1 G	01 10 00	109	O I/O I/O	VDDEH6 / Medium	— / Up	— / Up	105	H14	K20
DSPI_B_PCS[5] DSPI_C_PCS[0] GPIO[110]	DSPI B peripheral chip select DSPI C peripheral chip select GPIO	P A1 G	01 10 00	110	O I/O I/O	VDDEH6 / Medium	— / Up	— / Up	104	J13	L19
eQADC											
AN0 DAN0+	Single Ended Analog Input Positive Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[0] / —	172	B5	B8
AN1 DAN0–	Single Ended Analog Input Negative Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[1] / —	171	A6	A8
AN2 DAN1+	Single Ended Analog Input Positive Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[2] / —	170	D6	D10
AN3 DAN1–	Single Ended Analog Input Negative Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[3] / —	169	C7	C9
AN4 DAN2+	Single Ended Analog Input Positive Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[4] / —	168	B6	B9
AN5 DAN2–	Single Ended Analog Input Negative Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[5] / —	167	A7	A9
AN6 DAN3+	Single Ended Analog Input Positive Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[6] / —	166	D7	D11

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
AN7 DAN3–	Single Ended Analog Input Negative Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[7] / —	165	C8	C10
AN8 ANW	Single-ended Analog Input Multiplexed Analog Input	P	01	—	I	VDDA / Analog	I / —	AN[8] / —	9	B3	D6
AN9 ANX	Single-ended Analog Input External Multiplexed Analog Input	P	01	—	I	VDDA / Analog	I / —	AN[9] / —	5	A2	D7
AN10 ANY	Single-ended Analog Input Multiplexed Analog Input	P	01	—	I	VDDA / Analog	I / —	AN[10] / —	—	—	D8
AN11 ANZ	Single-ended Analog Input Multiplexed Analog Input	P	01	—	I	VDDA / Analog	I / —	AN[11] / —	4	A3	A5
AN12 - SDS MA0 ETPUA19_O $\overline{SDS}$	Single-ended Analog Input MUX Address 0 eTPU A channel (output only) eQADC Serial Data Select	P A1 A2 G	001 010 100 000	215	I O O I/O	VDDEH7 / Medium	I / —	AN[12] / —	148	A12	A16
AN13 - SDO MA1 ETPUA21_O SDO	Single-ended Analog Input MUX Address 1 eTPU A channel (output only) eQADC Serial Data Out	P A1 A2 G	001 010 100 000	216	I O O O	VDDEH7 / Medium	I / —	AN[13] / —	147	B12	B16
AN14 - SDI MA2 ETPUA27_O SDI	Single-ended Analog Input MUX Address 2 eTPU A channel (output only) eQADC Serial Data In	P A1 A2 G	001 010 100 000	217	I O O I	VDDEH7 / Medium	I / —	AN[14] / —	146	C12	C16
AN15 - FCK FCK ETPUA29_O	Single-ended Analog Input eQADC Free Running Clock eTPU A channel (output only)	P A1 A2	001 010 100	218	I O O	VDDEH7 / Medium	I / —	AN[15] / —	145	C13	D16
AN16	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[16] / —	3	C6	B7
AN17	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[17] / —	2	C4	C6
AN18	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[18] / —	1	D5	D9
AN19	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[19] / —	—	—	B6

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
AN20	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[20] / —	—	—	C7
AN21	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[21] / —	173	B4	C8
AN22	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[22] / —	161	B8	C11
AN23	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[23] / —	160	C9	B11
AN24	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[24] / —	159	D8	D12
AN25	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[25] / —	158	B9	C12
AN26	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[26] / —	—	—	B12
AN27	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[27] / —	157	A10	A12
AN28	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[28] / —	156	B10	A13
AN29	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[29] / —	—	—	D13
AN30	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[30] / —	155	D9	C13
AN31	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[31] / —	154	D10	B13
AN32	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[32] / —	153	C10	B14
AN33	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[33] / —	152	C11	C14
AN34	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[34] / —	151	C5	D14
AN35	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[35] / —	150	D11	A14

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
AN36	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[36] / —	174	F4	B4
AN37	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[37] / —	175	E3	A4
AN38	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[38] / —	—	—	C5
AN39	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[39] / —	8	D2	B5
VRH	Voltage Reference High	P	—	—	I	VDDA / —	I / —	—	163	A8	A10
VRL	Voltage Reference Low	P	—	—	I	VDDA / —	I / —	—	162	A9	A11
REFBYBC	Reference Bypass Capacitor Input	P	—	—	I	VDDA / Analog	I / —	—	164	B7	B10
eTPU2											
TCRCLKA IRQ[7] GPIO[113]	eTPU A TCR clock External interrupt request GPIO	P A1 G	01 10 00	113	I I I/O	VDDEH4 / Slow	— / Up	— / Up	—	L4	M2
ETPUA0 ETPUA12_O ETPUA19_O GPIO[114]	eTPU A channel eTPU A channel (output only) eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	114	I/O O O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	61	N3	L3
ETPUA1 ETPUA13_O GPIO[115]	eTPU A channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	115	I/O O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	60	M3	L4
ETPUA2 ETPUA14_O GPIO[116]	eTPU A channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	116	I/O O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	59	P2	K3
ETPUA3 ETPUA15_O GPIO[117]	eTPU A channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	117	I/O O I/O	VDDEH4 / Slow	— / WKPCFG	GPIO / WKPCFG	58	P1	L2

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
ETPUA4 ETPUA16_O — FR_B_TX GPIO[118]	eTPU A channel eTPU A channel (output only) — FlexRay transmit data channel B GPIO	P A1 A2 A3 G	0001 0010 — 1000 0000	118	I/O O — O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	56	N2	L1
ETPUA5 ETPUA17_O DSPI_B_SCK_LVDS– FR_B_TX_EN GPIO[119]	eTPU A channel eTPU A channel (output only) LVDS negative DSPI clock FlexRay tx data enable for ch. B GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	119	I/O O O O I/O	VDDEH4 / Slow + LVDS	— / WKPCFG	— / WKPCFG	54	M4	K4
ETPUA6 ETPUA18_O DSPI_B_SCK_LVDS+ FR_B_RX GPIO[120]	eTPU A channel eTPU A channel (output only) LVDS positive DSPI clock FlexRay receive data channel B GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	120	I/O O O I I/O	VDDEH4 / Medium + LVDS	— / WKPCFG	— / WKPCFG	53	L3	J3
ETPUA7 ETPUA19_O DSPI_B_SOUT_LVDS– ETPUA6_O GPIO[121]	eTPU A channel eTPU A channel (output only) LVDS negative DSPI data out eTPU A channel (output only) GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	121	I/O O O O I/O	VDDEH4 / Slow + LVDS	— / WKPCFG	— / WKPCFG	52	K3	K2
ETPUA8 ETPUA20_O DSPI_B_SOUT_LVDS+ GPIO[122]	eTPU A channel eTPU A channel (output only) LVDS positive DSPI data out GPIO	P A1 A2 G	001 010 100 000	122	I/O O O I/O	VDDEH4 / Slow + LVDS	— / WKPCFG	— / WKPCFG	51	N1	K1
ETPUA9 ETPUA21_O RCH1_B GPIO[123]	eTPU A channel eTPU A channel (output only) Reaction channel 1B GPIO	P A1 A2 G	001 010 100 000	123	I/O O O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	50	M2	J4
ETPUA10 ETPUA22_O RCH1_C GPIO[124]	eTPU A channel eTPU A channel (output only) Reaction channel 1C GPIO	P A1 A2 G	001 010 100 000	124	I/O O O I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	49	M1	H3
ETPUA11 ETPUA23_O RCH4_B GPIO[125]	eTPU A channel eTPU A channel (output only) Reaction channel 4B GPIO	P A1 A2 G	001 010 100 000	125	I/O O O I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	48	L2	J2

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
ETPUA12 DSPI_B_PCS[1] RCH4_C GPIO[126]	eTPU A channel DSPI B peripheral chip select Reaction channel 4C GPIO	P A1 A2 G	001 010 100 000	126	I/O O O I/O	VDDEH1 / Medium	— / WKPCFG	— / WKPCFG	47	L1	J1
ETPUA13 DSPI_B_PCS[3] GPIO[127]	eTPU A channel DSPI B peripheral chip select GPIO	P A1 G	01 10 00	127	I/O O I/O	VDDEH1 / Medium	— / WKPCFG	— / WKPCFG	46	J4	G4
ETPUA14 DSPI_B_PCS[4] ETPUA9_O RCH0_A GPIO[128]	eTPU A channel DSPI B peripheral chip select eTPU A channel (output only) Reaction channel 0A GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	128	I/O O O O I/O	VDDEH1 / Medium	— / WKPCFG	— / WKPCFG	42	J3	G3
ETPUA15 DSPI_B_PCS[5] RCH1_A GPIO[129]	eTPU A channel DSPI B peripheral chip select Reaction channel 1A GPIO	P A1 A2 G	001 010 100 000	129	I/O O O I/O	VDDEH1 / Medium	— / WKPCFG	— / WKPCFG	40	K2	H2
ETPUA16 DSPI_D_PCS[1] RCH2_A GPIO[130]	eTPU A channel DSPI D peripheral chip select Reaction channel 2A GPIO	P A1 A2 G	001 010 100 000	130	I/O O O I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	39	K1	H1
ETPUA17 DSPI_D_PCS[2] RCH3_A GPIO[131]	eTPU A channel DSPI D peripheral chip select Reaction channel 3A GPIO	P A1 A2 G	001 010 100 000	131	I/O O O I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	38	H3	F3
ETPUA18 DSPI_D_PCS[3] RCH4_A GPIO[132]	eTPU A channel DSPI D peripheral chip select Reaction channel 4A GPIO	P A1 A2 G	001 010 100 000	132	I/O O O I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	37	H4	F4
ETPUA19 DSPI_D_PCS[4] RCH5_A GPIO[133]	eTPU A channel DSPI D peripheral chip select Reaction channel 5A GPIO	P A1 A2 G	001 010 100 000	133	I/O O O I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	36	J2	G2

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
ETPUA20 IRQ[8] RCH0_B FR_A_TX GPIO[134]	eTPU A channel External interrupt request Reaction channel 0B FlexRay transmit data channel A GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	134	I/O I O O I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	35	J1	G1
ETPUA21 IRQ[9] RCH0_C FR_A_RX GPIO[135]	eTPU A channel External interrupt request Reaction channel 0C FlexRay receive channel A GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	135	I/O I O I I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	34	G4	E4
ETPUA22 IRQ[10] ETPUA17_O GPIO[136]	eTPU A channel External interrupt request eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	136	I/O I O I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	32	H2	F2
ETPUA23 IRQ[11] ETPUA21_O FR_A_TX_EN GPIO[137]	eTPU A channel External interrupt request eTPU A channel (output only) FlexRay ch. A transmit enable GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	137	I/O I O O I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	30	H1	F1
ETPUA24 IRQ[12] DSPI_C_SCK_LVDS– GPIO[138]	eTPU A channel External interrupt request LVDS negative DSPI clock GPIO	P A1 A2 G	001 010 100 000	138	I/O I O I/O	VDDEH1 / Slow + LVDS	— / WKPCFG	— / WKPCFG	28	G1	E1
ETPUA25 IRQ[13] DSPI_C_SCK_LVDS+ GPIO[139]	eTPU A channel External interrupt request LVDS positive DSPI clock GPIO	P A1 A2 G	001 010 100 000	139	I/O I O I/O	VDDEH1 / Medium + LVDS	— / WKPCFG	— / WKPCFG	27	G3	E3
ETPUA26 IRQ[14] DSPI_C_SOUT_LVDS– GPIO[140]	eTPU A channel External interrupt request LVDS negative DSPI data out GPIO	P A1 A2 G	001 010 100 000	140	I/O I O I/O	VDDEH1 / Slow + LVDS	— / WKPCFG	— / WKPCFG	26	F3	D3
ETPUA27 IRQ[15] DSPI_C_SOUT_LVDS+ DSPI_B_SOUT GPIO[141]	eTPU A channel External interrupt request LVDS positive DSPI data out DSPI B data output GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	141	I/O I O O I/O	VDDEH1 / Slow + LVDS	— / WKPCFG	— / WKPCFG	25	G2	E2

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
ETPUA28 DSPI_C_PCS[1] RCH5_B GPIO[142]	eTPU A channel DSPI C peripheral chip select Reaction channel 5B GPIO	P A1 A2 G	001 010 100 000	142	I/O O O I/O	VDDEH1 / Medium	— / WKPCFG	— / WKPCFG	24	F1	D1
ETPUA29 DSPI_C_PCS[2] RCH5_C GPIO[143]	eTPU A channel DSPI C peripheral chip select Reaction channel 5C GPIO	P A1 A2 G	001 010 100 000	143	I/O O O I/O	VDDEH1 / Medium	— / WKPCFG	— / WKPCFG	23	F2	D2
ETPUA30 DSPI_C_PCS[3] ETPUA11_O GPIO[144]	eTPU A channel DSPI C peripheral chip select eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	144	I/O O O I/O	VDDEH1 / Medium	— / WKPCFG	— / WKPCFG	22	E1	C1
ETPUA31 DSPI_C_PCS[4] ETPUA13_O GPIO[145]	eTPU A channel DSPI C peripheral chip select eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	145	I/O O O I/O	VDDEH1 / Medium	— / WKPCFG	— / WKPCFG	21	E2	C2
eMIOS											
EMIOS0 ETPUA0_O ETPUA25_O GPIO[179]	eMIOS channel eTPU A channel (output only) eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	179	I/O O O I/O	VDDEH4 / Slow	— / Up	— / Up	63	T4	AB10
EMIOS1 ETPUA1_O GPIO[180]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	180	I/O O I/O	VDDEH4 / Slow	— / Up	— / Up	64	T5	AB11
EMIOS2 ETPUA2_O RCH2_B GPIO[181]	eMIOS channel eTPU A channel (output only) Reaction channel 2B GPIO	P A1 A2 G	001 010 100 000	181	I/O O O I/O	VDDEH4 / Slow	— / Up	— / Up	65	N7	W12
EMIOS3 ETPUA3_O GPIO[182]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	182	I/O O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	66	R6	AA11
EMIOS4 ETPUA4_O RCH2_C GPIO[183]	eMIOS channel eTPU A channel (output only) Reaction channel 2C GPIO	P A1 A2 G	001 010 100 000	183	I/O O O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	67	R5	AB12

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
EMIOS5 ETPUA5_O GPIO[184]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	184	I/O O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	—	—	AA12
EMIOS6 ETPUA6_O GPIO[185]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	185	I/O O I/O	VDDEH4 / Slow	— / Down	— / Down	68	P7	Y12
EMIOS7 ETPUA7_O GPIO[186]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	186	I/O O I/O	VDDEH4 / Slow	— / Down	— / Down	69	—	AB13
EMIOS8 ETPUA8_O SCI_B_TX GPIO[187]	eMIOS channel eTPU A channel (output only) eSCI B transmit GPIO	P A1 A2 G	001 010 100 000	187	I/O O O I/O	VDDEH4 / Slow	— / Up	— / Up	70	P8	W13
EMIOS9 ETPUA9_O SCI_B_RX GPIO[188]	eMIOS channel eTPU A channel (output only) eSCI B receive GPIO	P A1 A2 G	001 010 100 000	188	I/O O I I/O	VDDEH4 / Slow	— / Up	— / Up	71	R7	AA13
EMIOS10 DSPI_D_PCS[3] RCH3_B GPIO[189]	eMIOS channel DSPI D peripheral chip select Reaction channel 3B GPIO	P A1 A2 G	001 010 100 000	189	I/O O O I/O	VDDEH4 / Medium	— / WKPCFG	— / WKPCFG	73	N8	Y13
EMIOS11 DSPI_D_PCS[4] RCH3_C GPIO[190]	eMIOS channel DSPI D peripheral chip select Reaction channel 3C GPIO	P A1 A2 G	001 010 100 000	190	I/O O O I/O	VDDEH4 / Medium	— / WKPCFG	— / WKPCFG	75	R8	AB14
EMIOS12 DSPI_C_SOUT ETPUA27_O GPIO[191]	eMIOS channel DSPI C data output eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	191	I/O O O I/O	VDDEH4 / Medium	— / WKPCFG	— / WKPCFG	76	N10	W15
EMIOS13 DSPI_D_SOUT GPIO[192]	eMIOS channel DSPI D data output GPIO	P A1 G	01 10 00	192	I/O O I/O	VDDEH4 / Medium	— / WKPCFG	— / WKPCFG	77	T8	AA14

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
EMIOS14 IRQ[0] ETPUA29_O GPIO[193]	eMIOS channel External interrupt request eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	193	I/O I O I/O	VDDEH4 / Slow	— / Down	— / Down	78	R9	AB15
EMIOS15 IRQ[1] GPIO[194]	eMIOS channel External interrupt request GPIO	P A1 G	01 10 00	194	I/O I I/O	VDDEH4 / Slow	— / Down	— / Down	79	T9	Y14
EMIOS16 GPIO[195]	eMIOS channel GPIO	P G	01 00	195	I/O I/O	VDDEH4 / Slow	— / Up	— / Up	—	—	AA15
EMIOS17 GPIO[196]	eMIOS channel GPIO	P G	01 00	196	I/O I/O	VDDEH4 / Slow	— / Up	— / Up	—	—	Y15
EMIOS18 GPIO[197]	eMIOS channel GPIO	P G	01 00	197	I/O I/O	VDDEH4 / Slow	— / Up	— / Up	—	—	AB16
EMIOS19 GPIO[198]	eMIOS channel GPIO	P G	01 00	198	I/O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	—	—	AA16
EMIOS20 GPIO[199]	eMIOS channel GPIO	P G	01 00	199	I/O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	—	—	AB17
EMIOS21 GPIO[200]	eMIOS channel GPIO	P G	01 00	200	I/O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	—	—	W16
EMIOS22 GPIO[201]	eMIOS channel GPIO	P G	01 00	201	I/O I/O	VDDEH4 / Slow	— / Down	— / Down	—	—	Y16
EMIOS23 GPIO[202]	eMIOS channel GPIO	P G	01 00	202	I/O I/O	VDDEH4 / Slow	— / Down	— / Down	80	R11	AA17
EMIOS14[16] GPIO[203]	eMIOS channel GPIO	P G	01 00	203	O I/O	VDDEH7 / Slow	— / Down	— / Down	—	—	H20
EMIOS15[16] GPIO[204]	eMIOS channel GPIO	P G	01 00	204	O I/O	VDDEH7 / Slow	— / Down	— / Down	—	—	H21
Clock Synthesizer											
XTAL	Crystal oscillator output	P	01	—	O	VDDEH6 / Analog	—	—	93	P16	V22
EXTAL	Crystal oscillator input	P	01	—	I	VDDEH6 / Analog	—	—	92	N16	U22

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
CLKOUT	System clock output	P	01	229	O	VDDE12 / Fast	—	CLKOUT	—	—	AA20
ENGCLK	Engineering clock output	P	01	214	O	VDDE12 / Fast	—	ENGCLK	—	T14	AB21
Power / Ground											
VDDREG	Voltage regulator supply	—		—	I	5 V	I / —	VDDREG	10	K16	M22
VRCCTL	Voltage regulator control output	—		—	O	—	O / —	VRCCTL	11	N14	V20
VRC33[18]	Internal regulator output	—		—	O	3.3 V	I/O / —	VRC33	13	A15, D1, N6, N12	A21, B1, P4, W7, Y22
	Input for external 3.3 V supply	—		—	I	3.3 V					
VDDA	eQADC high reference voltage	—		—	I	5 V	I / —	VDDA	6	A4, B11	A6, C15
VSSA	eQADC ground/low reference voltage	—		—	I	—	I / —	VSSA	7	A5, A11	A7, A15, B15
VDDPLL	FMPLL supply voltage	—		—	I	1.2 V	I / —	VDDPLL	91	R16	W22
VSTBY	Power supply for standby RAM	—		—	I	0.9 V – 6 V	I / —	VSTBY	12	C1	A3
VDD	Core supply for input or decoupling	—		—	I	1.2 V	I / —	VDD	33, 45, 62, 103, 132, 149, 176	B1, B16, C2, D3, E4, N5, P4, P13, R3, R14, T2, T15	A2, A20, B3, C4, C22, D5, V19, W5, W20, Y4, Y21, AA3, AA22, AB2
VDDE12	External supply input for calibration bus interfaces	—		—	I	3.0 V – 3.6 V	I / —	VDDE12	—	—	—
VDDE5	External supply input for ENGCLK and CLKOUT	—		—	I	3.0 V – 3.6 V	I / —	VDDE5	—	T13	W17, Y18, AA19, AB20
VDDE-EH	External supply for EBI interfaces	—		—	I	3.0 V – 5.0 V	I / —	VDDE-EH	—	—	R3, W2
VDDEH1A[19]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH1A[19]	31	—	—
VDDEH1B[19]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH1B[19]	41	—	—

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
VDDEH1AB[19]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH1AB[19]	—	K4	H4
VDDEH4[20]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH4[20]	—	—	—
VDDEH4A[20]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH4A[20]	55	—	—
VDDEH4B[20]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH4B[20]	74	—	—
VDDEH4AB[20]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH4AB[20]	—	N9	W14
VDDEH6[21]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH6[21]	—	—	—
VDDEH6A[21]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH6A[21]	95	—	—
VDDEH6B[21]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH6B[21]	110	—	—
VDDEH6AB[21]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH6AB[21]	—	F13	H19, U19
VDDEH7[22]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH7	—	D12	D15
VDDEH7A[22]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH7A	125	—	—
VDDEH7B[22]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH7B	138	—	—
VSS	Ground	—		—	I	—	I / —	VSS	15, 29, 43, 57, 72, 90, 94, 96, 108, 115, 127, 133, 140	A1, A16, B2, B15, C3, C14, D4, D13, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M16, N4, N13, P3, P14, R2, R15, T1, T16	A1, A22, B2, B21, C3, C20, D4, D19, J9, J10, J11, J12, J13, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M11, M12, M13, M14, N9, N10, N12, N13, N14, P9, P10, P12, P13, P14, T21, T22, W4, W19, Y3, Y20, AA2, AA21, AB1, AB22

1. The suffix "_O" identifies an output-only eTPU channel
2. For each pin in the table, each line in the Function column is a separate function of the pin. For all I/O pins the selection of primary pin function or GPIO is done in the SIU except where explicitly noted. See the Signal details table for a description of each signal.
3. The P/A/G column indicates the position a signal occupies in the muxing order for a pin—Primary, Alternate 1, Alternate 2, Alternate 3, or GPIO. S setting the PA field value in the appropriate PCR register in the SIU module. The PA field values are as follows: P - 0b0001, A1 - 0b0010, A2 - 0b0 0b0000. Depending on the register, the PA field size can vary in length. For PA fields having fewer than four bits, remove the appropriate number these values.
4. The Pad Configuration Register (PCR) PA field is used by software to select pin function.
5. Values in the PCR column refer to registers in the System Integration Unit (SIU). The actual register name is "SIU_PCR" suffixed by the PCR num PCR[190] refers to the SIU register named SIU_PCR190.
6. The VDDE and VDDEH supply inputs are broken into segments. Each segment of slow I/O pins (VDDEH) may have a separate supply in the 3.3 V 10%/+5%). Each segment of fast I/O (VDDE) may have a separate supply in the 1.8 V to 3.3 V range (+/– 10%).
7. See *Table 5* for details on pad types.
8. The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance. Terminology is (weak pull up enabled), Down (weak pull down enabled), Low (output driven low), High (output driven high). A dash for the function in this column input and output buffer are turned off. The signal name to the left or right of the slash indicates the pin is enabled.
9. LBGA208 is available upon specific request. Please contact your ST sales office for details.
10. When used as ETRIG, this pin must be configured as an input. For GPIO it can be configured either as an input or output.
11. Maximum frequency is 50 kHz
12. PCR219 controls two different pins: MCKO and GPIO[219]. Please refer to Pad Configuration Register 219 section in SIU chapter of device refere
13. On LQFP176 and LBGA208 packages, this pin is tied low internally.
14. These pins are selected by asserting JCOMP and configuring the NPC. SIU values have no effect on the function of this pin once enabled.
15. The BAM uses this pin to select if auto baud rate is on or off.
16. Output only
17. This signal name is used to support legacy naming.
18. Do not use VRC33 to drive external circuits.
19. VDDEH1A, VDDEH1B and VDDEH1AB are shorted together in all production packages. The separation of the signal names is present to support they should be considered as the same signal in this document.
20. VDDEH4, VDDEH4A, VDDEH4B and VDDEH4AB are shorted together in all production packages. The separation of the signal names is present to however they should be considered as the same signal in this document.
21. VDDEH6, VDDEH6A, VDDEH6B and VDDEH6AB are shorted together in all production packages. The separation of the signal names is present to however they should be considered as the same signal in this document.
22. VDDEH7, VDDEH7A and VDDE7B are shorted together in all production packages. The separation of the signal names is present to support legac should be considered as the same signal in this document.

Table 5. Pad types

Pad Type	Name	I/O Voltage Range
Slow	pad_ssr_hv	3.0V - 5.5 V
Medium	pad_msr_hv	3.0 V - 5.5 V
Fast	pad_fc	3.0 V - 3.6 V
MultiV(1),(2)	pad_multv_hv	3.0 V - 5.5 V (high swing mode) 3.0 V - 3.6 V (low swing mode)
Analog	pad_ae_hv	0.0 - 5.5 V
LVDS	pad_lo_lv	—

1. Multivoltage pads are automatically configured in low swing mode when a JTAG or Nexus function is selected, otherwise they are high swing.
2. VDDEH7 supply cannot be below 4.5 V when in low-swing mode.

2.5 Signal details

Table 6. Signal details

Signal	Module or function	Description
CLKOUT	Clock Generation	SPC564A70 clock output for the calibration bus interface
ENGCLK	Clock Generation	Clock for external ASIC devices
EXTAL	Clock Generation	Input pin for an external crystal oscillator or an external clock source based on the value driven on the PLLREF pin at reset
PLLREF	Clock Generation Reset/Configuration	PLLREF is used to select whether the oscillator operates in xtal mode or external reference mode from reset. PLLREF = 0 selects external reference mode. On the PBGA324 package, PLLREF is bonded to the ball used for PLLCFG[0] for compatibility with previous devices. For the 176-pin QFP and 208-ball BGA packages: 0: External reference clock is selected 1: XTAL oscillator mode is selected For the 324-ball BGA package: If RSTCFG is 0: 0: External reference clock is selected 1: XTAL oscillator mode is selected If RSTCFG is 1, XTAL oscillator mode is selected.
XTAL	Clock Generation	Crystal oscillator input
DSPI_B_SCK_LVDS– DSPI_B_SCK_LVDS+	DSPI	LVDS pair used for DSPI_B TSB mode transmission
DSPI_B_SOUT_LVDS– DSPI_B_SOUT_LVDS+	DSPI	LVDS pair used for DSPI_B TSB mode transmission

Table 6. Signal details (continued)

Signal	Module or function	Description
DSPI_C_SCK_LVDS– DSPI_C_SCK_LVDS+	DSPI	LVDS pair used for DSPI_C TSB mode transmission
DSPI_C_SOUT_LVDS– DSPI_C_SOUT_LVDS+	DSPI	LVDS pair used for DSPI_C TSB mode transmission
DSPI_B_PCS[0] DSPI_C_PCS[0] DSPI_D_PCS[0]	DSPI_B – DSPI_D	Peripheral chip select when device is in master mode—slave select when used in slave mode
DSPI_B_PCS[1:5] DSPI_C_PCS[1:5] DSPI_D_PCS[1:5]	DSPI_B – DSPI_D	Peripheral chip select when device is in master mode—not used in slave mode
DSPI_B_SCK DSPI_C_SCK DSPI_D_SCK	DSPI_B – DSPI_D	DSPI clock—output when device is in master mode; input when in slave mode
DSPI_B_SIN DSPI_C_SIN DSPI_D_SIN	DSPI_B – DSPI_D	DSPI data in
DSPI_B_SOUT DSPI_C_SOUT DSPI_D_SOUT	DSPI_B – DSPI_D	DSPI data out
eMIOS[0:23]	eMIOS	eMIOS I/O channels
AN[0:39]	eQADC	Single-ended analog inputs for analog-to-digital converter
AN[0:7]/DAN+	eQADC	Differential analog input pair for analog-to-digital converter with pull-up/pull-down functionality
AN[0:7]/DAN–	eQADC	Differential analog input pair for analog-to-digital converter with pull-up/pull-down functionality
FCK	eQADC	eQADC free running clock for eQADC SSI
MA[0:2]	eQADC	These three control bits are output to enable the selection for an external Analog Mux for expansion channels.
REFBYPC	eQADC	Bypass capacitor input
SDI	eQADC	Serial data in
SDO	eQADC	Serial data out
SDS	eQADC	Serial data select
VRH	eQADC	Voltage reference high input
VRL	eQADC	Voltage reference low input
SCI_A_RX SCI_B_RX SCI_C_RX	eSCI_A – eSCI_C	eSCI receive
SCI_A_TX SCI_B_TX SCI_C_TX	eSCI_A – eSCI_C	eSCI transmit

Table 6. Signal details (continued)

Signal	Module or function	Description
ETPU_A[0:31]	eTPU	eTPU I/O channel
RCH0_[A:C] RCH1_[A:C] RCH2_[A:C] RCH3_[A:C] RCH4_[A:C] RCH5_[A:C]	eTPU2 Reaction Module	eTPU2 reaction channels. Used to control external actuators, e.g., solenoid control for direct injection systems and valve control in automatic transmissions
TCRCLKA	eTPU2	Input clock for TCR time base
CAN_A_TX CAN_B_TX CAN_C_TX	FlexCAN_A – FlexCAN_C	FlexCAN transmit
CAN_A_RX CAN_B_RX CAN_C_RX	FlexCAN_A – FlexCAN_C	FlexCAN receive
FR_A_RX FR_B_RX	FlexRay	FlexRay receive (Channels A, B)
FR_A_TX_EN FR_B_TX_EN	FlexRay	FlexRay transmit enable (Channels A, B)
FR_A_TX FR_B_TX	FlexRay	FlexRay transmit (Channels A, B)
JCOMP	JTAG	Enables the JTAG TAP controller
TCK	JTAG	Clock input for the on-chip test logic
TDI	JTAG	Serial test instruction and data input for the on-chip test logic
TDO	JTAG	Serial test data output for the on-chip test logic
TMS	JTAG	Controls test mode operations for the on-chip test logic
$\overline{\text{EVTI}}$	Nexus	$\overline{\text{EVTI}}$ is an input that is read on the negation of $\overline{\text{RESET}}$ to enable or disable the Nexus Debug port. After reset, the $\overline{\text{EVTI}}$ pin is used to initiate program synchronization messages or generate a breakpoint.
$\overline{\text{EVTO}}$	Nexus	Output that provides timing to a development tool for a single watchpoint or breakpoint occurrence
MCKO	Nexus	MCKO is a free running clock output to the development tools which is used for timing of the MDO and $\overline{\text{MSEO}}$ signals.
MDO[0:11]	Nexus	Trace message output to development tools. This pin also indicates the status of the crystal oscillator clock following a power-on reset, when MDO[0] is driven high until the crystal oscillator clock achieves stability and is then negated.
$\overline{\text{MSEO}}$[0:1]	Nexus	Output pin—Indicates the start or end of the variable length message on the MDO pins

Table 6. Signal details (continued)

Signal	Module or function	Description
RDY	Nexus	Nexus Ready Output (RDY)—Indicates to the development tools that data is ready to be read from or written to the Nexus read/write access registers.
BOOTCFG[0:1]	SIU – Configuration	Two BOOTCFG signals are implemented in SPC564A70 MCUs. The BAM program uses the BOOTCFG0 bit to determine where to read the reset configuration word, and whether to initiate a FlexCAN or eSCI boot. The BOOTCFG1 pin is sampled during the assertion of the RSTOUT signal, and the value is used to update the RSR and the BAM boot mode. See reference manual section “Reset Configuration Half Word (RCHW)” for details on the RCHW. The table “Boot Modes” in reference manual section “BAM Program Operation” defines the boot modes specified by the BOOTCFG1 pin. The following values are for BOOTCFG[0:1}: 00: Boot from internal flash memory 01: FlexCAN/eSCI boot 10: Boot from external memory using calibration bus 11: Reserved Note: For the 176-pin QFP and 208-ball BGA packages BOOTCFG[0] is always 0 since the EBI interface is not available.
WKPCFG	SIU – Configuration	The WKPCFG pin is applied at the assertion of the internal reset signal (assertion of $\overline{\text{RSTOUT}}$), and is sampled four clock cycles before the negation of the $\overline{\text{RSTOUT}}$ pin. The value is used to configure whether the eTPU and eMIOS pins are connected to internal weak pull up or weak pull down devices after reset. The value latched on the WKPCFG pin at reset is stored in the Reset Status Register (RSR), and is updated for all reset sources except the Debug Port Reset and Software External Reset. 0:Weak pulldown applied to eTPU and eMIOS pins at reset 1:Weak pullup applied to eTPU and eMIOS pins at reset
ETRIG[2:3]	SIU – eQADC Triggers	External signal eTRIGx triggers eQADC CFIFOx
GPIO[206] ETRIG0 (Input)	SIU – eQADC Triggers	External signal eTRIGx triggers eQADC CFIFOx
GPIO[207] ETRIG1 (Input)	SIU – eQADC Triggers	External signal eTRIGx triggers eQADC CFIFOx

Table 6. Signal details (continued)

Signal	Module or function	Description
IRQ[0:5] IRQ[7:15]	SIU – External Interrupts	The IRQ[0:15] pins connect to the SIU IRQ inputs. IMUX Select Register 1 is used to select the IRQ[0:15] pins as inputs to the IRQs. See reference manual section “External IRQ Input Select Register (SIU_EIISR)” for more information.
NMI	SIU – External Interrupts	Non-Maskable Interrupt
GPIO[12:17] GPIO[75:110] GPIO[113:145] GPIO[179:204] GPIO[206:213] GPIO[219] GPIO[244:245]	SIU – GPIO	Configurable general purpose I/O pins. Each GPIO input and output is separately controlled by an 8-bit input (GPDI) or output (GPDO) register. Additionally, each GPIO pin is configured using a dedicated SIU_PCR register. The GPIO pins are generally multiplexed with other I/O pin functions. See the following reference manual sections for more information: – “Pad Configuration Registers (SIU_PCR)” – “GPIO Pin Data Output Registers (SIU_GPDO0_3 – SIU_GPDO412_413)” – “GPIO Pin Data Input Registers (SIU_GPDI0_3 – SIU_GPDI_232)”
$\overline{\text{RESET}}$	SIU – Reset	The $\overline{\text{RESET}}$ pin is an active low input. The $\overline{\text{RESET}}$ pin is asserted by an external device during a power-on or external reset. The internal reset signal asserts only if the $\overline{\text{RESET}}$ pin asserts for 10 clock cycles. Assertion of the $\overline{\text{RESET}}$ pin while the device is in reset causes the reset cycle to start over. The $\overline{\text{RESET}}$ pin has a glitch detector which detects spikes greater than two clock cycles in duration that fall below the switch point of the input buffer logic of the VDDEH input pins. The switch point lies between the maximum VIL and minimum VIH specifications for the VDDEH input pins.
RSTCFG	SIU – Reset	Used to enable or disable the PLLREF and the BOOTCFG[0:1] configuration signals. 0:Get configuration information from BOOTCFG[0:1] and PLLREF 1:Use default configuration of booting from internal flash with crystal clock source For the 176-pin QFP and 208-ball BGA packages RSTCFG is always 0, so PLLREF and BOOTCFG signals are used.

Table 6. Signal details (continued)

Signal	Module or function	Description
$\overline{\text{RSTOUT}}$	SIU – Reset	The $\overline{\text{RSTOUT}}$ pin is an active low output that uses a push/pull configuration. The $\overline{\text{RSTOUT}}$ pin is driven to the low state by the MCU for all internal and external reset sources. There is a delay between initiation of the reset and the assertion of the $\overline{\text{RSTOUT}}$ pin. See reference manual section “RSTOUT” for details.

Table 7. Power/ground segmentation

Power segment	Voltage	I/O pins powered by segment
VDDE5	3.0 V – 3.6 V	DATA[0:15], CLKOUT, ENGCLK
VDDE12	3.0 V – 3.6 V	CAL_CS0, CAL_CS2, CAL_CS3, CAL_ADDR[12:30], CAL_DATA[0:15], CAL_RD_WR, CAL_WE0, CAL_WE1, CAL_OE, CAL_TS
VDDE-EH	3.0 V – 5.5 V	FR_A_TX, FR_A_TX_EN, FR_A_RX, FR_B_TX, FR_B_TX_EN, FR_B_RX
VDDEH1	3.3 V – 5.5 V	ETPUA[10:31]
VDDEH4	3.3 V – 5.5 V	EMIOS[0:23], TCRCLKA, ETPUA[0:9]
VDDEH6	3.3 V – 5.5 V	$\overline{\text{RESET}}$, $\overline{\text{RSTOUT}}$, PLLREF, PLLCFG1, RSTCFG, BOOTCFG0, BOOTCFG1, WKPCFG, CAN_A_TX, CAN_A_RX, CAN_B_TX, CAN_B_RX, CAN_C_TX, CAN_C_RX, SCI_A_TX, SCI_A_RX, SCI_B_TX, SCI_B_RX, SCI_C_TX, SCI_C_RX, DSPI_B_SCK, DSPI_B_SIN, DSPI_B_SOUT, DSPI_B_PCS[0:5], EXTAL, XTAL
VDDEH7	3.3 V – 5.5 V	EMIOS14, EMIOS15, GPIO[98:99], GPIO[203:204], GPIO[206], GPIO[207], GPIO[219], EVTI, EVTO, MDO[4:11], MSEO0, MSEO1, RDY, TCK, TDI, TDO, TMS, JCOMP, DSPI_A_SCK, DSPI_A_SIN, DSPI_A_SOUT, DSPI_A_PCS[0:1], DSPI_A_PCS[4:5], AN12-SDS, AN13-SDO, AN14-SDI, AN15-FCK
VDDA	5.0 V	AN[0:11], AN[16:39], VRH, VRL, REFBYBC
VRC33	3.3 V	MCKO, MDO[0:3]
Other power segments		
VDDREG	5.0 V	—
VRCCTL	—	—
VDDPLL	1.2 V	—
VSTBY	0.9 V – 6.0 V	—
VSS	—	—

3 Electrical characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the SPC564A70 series of MCUs.

The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

3.1 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 8* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.2 Maximum ratings

Table 9. Absolute maximum ratings(1)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{DD}	SR	1.2 V core supply voltage(2)		–0.3	1.32	V
V_{FLASH}	SR	Flash core voltage(3)(4)		–0.3	3.6	V
V_{STBY}	SR	SRAM standby voltage(5)		–0.3	6.0	V
V_{DDPLL}	SR	Clock synthesizer voltage(3)		–0.3	1.32	V
V_{RC33}	SR	Voltage regulator control input voltage(4)		–0.3	3.6	V
V_{DDA}	SR	Analog supply voltage(5)	Reference to V_{SSA}	–0.3	5.5	V
V_{DDE}	SR	I/O supply voltage(4)(6)		–0.3	3.6	V
V_{DDEH}	SR	I/O supply voltage(5)(7)		–0.3	5.5	V
V_{IN}	SR	DC input voltage(8)	V_{DDEH} powered I/O pads	–1.0[10]	V_{DDEH} + 0.3 V(9)	V
			V_{DDE} powered I/O pads	–1.0[14]	V_{DDE} + 0.3 V(10)	
			V_{DDA} powered I/O pads	–1.0	5.5	
V_{DDREG}	SR	Voltage regulator supply voltage		–0.3	5.5	V
V_{RH}	SR	Analog reference high voltage	Reference to VRL	–0.3	5.5	V
$V_{SS} – V_{SSA}$	SR	V_{SS} differential voltage		–0.1	0.1	V
$V_{RH} – V_{RL}$	SR	V_{REF} differential voltage		–0.3	5.5	V
$V_{RL} – V_{SSA}$	SR	V_{RL} to V_{SSA} differential voltage		–0.3	0.3	V
$V_{SSPLL} – V_{SS}$	SR	V_{SSPLL} to V_{SS} differential voltage		–0.1	0.1	V
I_{MAXD}	SR	Maximum DC digital input current(11)	Per pin, applies to all digital pins	–3	3	mA
I_{MAXA}	SR	Maximum DC analog input current(12)	Per pin, applies to all analog pins	—	5(13)	mA
T_J	SR	Maximum operating temperature range — die junction temperature		–40.0	150.0	°C
T_{STG}	SR	Storage temperature range		–55	150	°C
T_{SDR}	SR	Maximum solder temperature(14)		—	260	°C
MSL	SR	Moisture sensitivity level(15)		—	3	—

1. Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Allowed 2 V for 10 hours cumulative time, remaining time at 1.2 V + 10%
3. The V_{FLASH} supply is connected to V_{RC33} in the package substrate. This specification applies to calibration package devices only.
4. Allowed 5.3 V for 10 hours cumulative time, remaining time at 3.3 V + 10%
5. Allowed 5.9 V for 10 hours cumulative time, remaining time at 5 V + 10%

6. All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE}, or V_{DDEH}.
7. Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met.
8. AC signal overshoot and undershoot of up to 2.0 V of the input voltages is permitted for an accumulative duration of 60 hours over the complete lifetime of the device (injection current not limited for this duration).
9. Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDEH} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDEH} is within the operating voltage specifications.
10. Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within the operating voltage specifications.
11. Total injection current for all pins (including both digital and analog) must not exceed 25 mA.
12. Total injection current for all analog input pins must not exceed 15 mA.
13. Lifetime operation at these specification limits is not guaranteed.
14. Solder profile per IPC/JEDEC J-STD-020D
15. Moisture sensitivity per JEDEC test method A112

3.3 Thermal characteristics

Table 10. Thermal characteristics for 176-pin LQFP(1)

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection(2)	Single-layer board – 1s	38	°C/W
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection(2)	Four-layer board – 2s2p	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-moving-air, ambient(2)	at 200 ft./min., single-layer board – 1s	30	°C/W
	CC	D		at 200 ft./min., four-layer board – 2s2p	25	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board(3)		20	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-case(4)		5	°C/W
Ψ_{JT}	CC	D	Junction-to-package top, natural convection(5)		2	°C/W

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 11. Thermal characteristics for 208-pin LBGA(1)(2)

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection(3)	Single layer board – 1s(4)	39	°C/W
	CC	D		Four layer board – 2s2p(5)	24	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-moving-air, ambient(3)	at 200 ft./min., single-layer board – 1s(5)	31	°C/W
	CC	D		at 200 ft./min., four-layer board – 2s2p	20	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board(6)	Four-layer board – 2s2p	13	°C/W
$R_{\theta JC}$	CC	D	Junction-to-case(7)		6	°C/W
Ψ_{JT}	CC	D	Junction-to-package top natural convection(8)		2	°C/W

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. LBGA208 is available upon specific request. Please contact your ST sales office for details.
3. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
4. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal
5. Per JEDEC JESD51-6 with the board horizontal
6. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
7. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
8. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 12. Thermal characteristics for 324-pin PBGA(1)

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection(2)	Single-layer board – 1s	31	°C/W
	CC	D		Four-layer board – 2s2p	23	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-moving-air, ambient(2)	at 200 ft./min., single-layer board – 1s	23	°C/W
	CC	D		at 200 ft./min., four-layer board – 2s2p	17	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board(3)		11	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-case(4)		7	°C/W
Ψ_{JT}	CC	D	Junction-to-package top, natural convection(5)		2	°C/W

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.3.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from *Equation 1*:

Equation 1 $T_J = T_A + (R_{\theta JA} * P_D)$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components that are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed-box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using *Equation 2*:

Equation 2 $T_J = T_B + (R_{\theta JB} * P_D)$

where:

T_B = board temperature for the package perimeter (°C)

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8S

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, an acceptable value for the junction temperature is predictable. Ensure the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

Equation 3 $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using *Equation 4*:

Equation 4 $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

References:

- Semiconductor Equipment and Materials International
  3081 Zanker Road
  San Jose, CA 95134
  USA
  Phone (+1) 408-943-6900
- MIL-SPEC and EIA/JESD (JEDEC) specifications available from Global Engineering Documents (phone (+1) 800-854-7179 or (+1) 303-397-7956)
- JEDEC specifications available on the Web at www.jedec.org
- C.E. Triplett and B. Joiner, “*An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module*,” Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
- G. Kromann, S. Shidore, and S. Addison, “*Thermal Modeling of a PBGA for Air-Cooled Applications*”, Electronic Packaging and Production, pp. 53-58, March 1998.
- B. Joiner and V. Adams, “*Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling*,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

3.4 EMI (electromagnetic interference) characteristics

Table 13. EMI testing specifications(1)

Symbol	Parameter	Conditions	f_{OSC}/f_{BUS}	Frequency	Level (max)	Unit
V_{RE_TEM}	Radiated emissions, electric field	V_{DD} = 5.25 V; T_A = +25 °C 150 kHz–30 MHz — RBW 9 kHz, step size 5 kHz 30 MHz–1 GHz — RBW 120 kHz, step size 80 kHz	16 MHz crystal 40 MHz bus No PLL frequency modulation	150 kHz–50 MHz	20	dBµV
				50–150 MHz	20	
				150–500 MHz	26	
				500–1000 MHz	26	
				IEC Level	K	—
				SAE Level	3	—
			16 MHz crystal 40 MHz bus ±2% PLL frequency modulation	150 kHz–50 MHz	13	dBµV
				50–150 MHz	13	
				150–500 MHz	11	
				500–1000 MHz	13	
				IEC Level	L	—
				SAE Level	2	—

1. EMI testing and I/O port waveforms per standard IEC 61967-2.

3.5 Electrostatic discharge (ESD) characteristics

Table 14. ESD ratings(1)(2)

Symbol		Parameter	Conditions	Value	Unit
—	SR	ESD for Human Body Model (HBM)	—	2000	V
R1	SR	HBM circuit description	—	1500	Ω
C	SR		—	100	pF
—	SR	ESD for Field Induced Charge Model (FDCM)	All pins	500	V
			Corner pins	750	
—	SR	Number of pulses per pin	Positive pulses (HBM)	1	—
			Negative pulses (HBM)	1	—
—	SR	Number of pulses	—	1	—

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature.”

3.6 Power management control (PMC) and power on reset (POR) electrical specifications

Table 15. PMC operating conditions and external regulators supply voltage

ID	Name		C	Parameter	Value			Unit
					Min	Typ	Max	
1	T_J	SR	—	Junction temperature	–40	27	150	°C
2	V_{DDREG}	SR	—	PMC 5 V supply voltage VDDREG	4.75	5	5.25	V
3	V_{DD}	CC	C	Core supply voltage 1.2 V VDD when external regulator is used without disabling the internal regulator (PMC unit turned on, LVI monitor active)(1)	1.26 (2)	1.3	1.32	V
3a	—	CC	C	Core supply voltage 1.2 V VDD when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	1.14	1.2	1.32	V
4	I_{VDD}	CC	C	Voltage regulator core supply maximum required DC output current	400	—	—	mA
5	V_{DD33}	CC	C	Regulated 3.3 V supply voltage when external regulator is used without disabling the internal regulator (PMC unit turned-on, internal 3.3V regulator enabled, LVI monitor active)(3)	3.3	3.45	3.6	V
5a	—	CC	C	Regulated 3.3 V supply voltage when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	3	3.3	3.6	V
6	—	CC	C	Voltage regulator 3.3 V supply maximum required DC output current	80	—	—	mA

1. An internal regulator controller can be used to regulate the core supply.
2. The minimum supply required for the part to exit reset and enter in normal run mode is 1.28 V.
3. An internal regulator can be used to regulate the 3.3 V supply.

Table 16. PMC electrical characteristics

ID	Name		C	Parameter	Value			Unit
					Min	Typ	Max	
1	V_{BG}	CC	C	Nominal bandgap voltage reference	—	1.219	—	V
1a	—	CC	C	Untrimmed bandgap reference voltage	V_{BG} – 7%	V_{BG}	V_{BG} + 6%	V
1b	—	CC	C	Trimmed bandgap reference voltage (5 V, 27 °C)	V_{BG} – 10mV	V_{BG}	V_{BG} + 10mV	V
1c	—	CC	C	Bandgap reference temperature variation	—	100	—	ppm/°C
1d	—	CC	C	Bandgap reference supply voltage variation	—	3000	—	ppm/V
2	V_{DD}	CC	C	Nominal V_{DD} core supply internal regulator target DC output voltage(1)	—	1.28	—	V
2a	—	CC	C	Nominal V_{DD} core supply internal regulator target DC output voltage variation at power-on reset	V_{DD} – 6%	V_{DD}	V_{DD} + 10%	V
2b	—	CC	C	Nominal V_{DD} core supply internal regulator target DC output voltage variation after power-on reset	V_{DD} – 10%(2)	V_{DD}	V_{DD} + 3%	V

Table 16. PMC electrical characteristics (continued)

ID	Name		C	Parameter	Value			Unit
					Min	Typ	Max	
2c	—	CC	C	Trimming step V_{DD}	—	20	—	mV
2d	I_{VRCCTL}	CC	C	Voltage regulator controller for core supply maximum DC output current	20	—	—	mA
3	Lvi1p2	CC	C	Nominal LVI for rising core supply(3)	—	1.160	—	V
3a	—	CC	C	Variation of LVI for rising core supply at power-on reset(4)	1.120	1.200	1.280	V
3b	—	CC	C	Variation of LVI for rising core supply after power-on reset(4)	Lvi1p2 – 3%	Lvi1p2	Lvi1p2 + 3%	V
3c	—	CC	C	Trimming step LVI core supply	—	20	—	mV
3d	Lvi1p2_h	CC	C	LVI core supply hysteresis	—	40	—	mV
4	Por1.2V_r	CC	C	POR 1.2 V rising	—	0.709	—	V
4a	—	CC	C	POR 1.2 V rising variation	Por1.2V_r – 35%	Por1.2V_r	Por1.2V_r + 35%	V
4b	Por1.2V_f	CC	C	POR 1.2 V falling	—	0.638	—	V
4c	—	CC	C	POR 1.2 V falling variation	Por1.2V_f – 35%	Por1.2V_f	Por1.2V_f + 35%	V
5	V_{DD33}	CC	C	Nominal 3.3 V supply internal regulator DC output voltage	—	3.39	—	V
5a	—	CC	C	Nominal 3.3 V supply internal regulator DC output voltage variation at power-on reset	V_{DD33} – 8.5%	V_{DD33}	V_{DD33} + 7%	V
5b	—	CC	C	Nominal 3.3 V supply internal regulator DC output voltage variation after power-on reset(5)	V_{DD33} – 7.5%	V_{DD33}	V_{DD33} + 7%	V
5c	—	CC	C	Voltage regulator 3.3 V output impedance at maximum DC load	—	—	2	Ω
5d	Idd3p3	CC	C	Voltage regulator 3.3 V maximum DC output current	80	—	—	mA
5e	Vdd33 ILim	CC	C	Voltage regulator 3.3 V DC current limit	—	130	—	mA
6	Lvi3p3	CC	C	Nominal LVI for rising 3.3 V supply(6)	—	3.090	—	V
6a	—	CC	C	Variation of LVI for rising 3.3 V supply at power-on reset(7)	Lvi3p3 – 6%	Lvi3p3	Lvi3p3 + 6%	V
6b	—	CC	C	Variation of LVI for rising 3.3 V supply after power-on reset(7)	Lvi3p3 – 3%	Lvi3p3	Lvi3p3 + 3%	V
6c	—	CC	C	Trimming step LVI 3.3 V	—	20	—	mV
6d	Lvi3p3_h	CC	C	LVI 3.3 V hysteresis	—	60	—	mV
7	Por3.3V_r	CC	C	Nominal POR for rising 3.3 V supply(8)	—	2.07	—	V
7a	—	CC	C	Variation of POR for rising 3.3 V supply	Por3.3V_r – 35%	Por3.3V_r	Por3.3V_r + 35%	V

Table 16. PMC electrical characteristics (continued)

ID	Name		C	Parameter	Value			Unit
					Min	Typ	Max	
7b	Por3.3V_f	CC	C	Nominal POR for falling 3.3 V supply	—	1.95	—	V
7c	—	CC	C	Variation of POR for falling 3.3 V supply	Por3.3V_f – 35%	Por3.3V_f	Por3.3V_f + 35%	V
8	Lvi5p0	CC	C	Nominal LVI for rising 5 V VDDREG supply	—	4.290	—	V
8a	—	CC	C	Variation of LVI for rising 5 V VDDREG supply at power-on reset	Lvi5p0 – 6%	Lvi5p0	Lvi5p0 + 6%	V
8b	—	CC	C	Variation of LVI for rising 5 V VDDREG supply power-on reset	Lvi5p0 – 3%	Lvi5p0	Lvi5p0 + 3%	V
8c	—	CC	C	Trimming step LVI 5 V	—	20	—	mV
8d	Lvi5p0_h	CC	C	LVI 5 V hysteresis	—	60	—	mV
9	Por5V_r	CC	C	Nominal POR for rising 5 V VDDREG supply	—	2.67	—	V
9a	—	CC	C	Variation of POR for rising 5 V VDDREG supply	Por5V_r – 35%	Por5V_r	Por5V_r + 35%	V
9b	Por5V_f	CC	C	Nominal POR for falling 5 V VDDREG supply	—	2.47	—	V
9c	—	CC	C	Variation of POR for falling 5 V VDDREG supply	Por5V_f – 35%	Por5V_f	Por5V_f + 35%	V

1. Using external ballast transistor.
2. Min range is extended to 10% since Lvi1p2 is reprogrammed from 1.2 V to 1.16 V after power-on reset.
3. LVI for falling supply is calculated as LVI rising – LVI hysteresis.
4. Lvi1p2 tracks DC target variation of internal V_{DD} regulator. Minimum and maximum Lvi1p2 correspond to minimum and maximum V_{DD} DC target respectively.
5. With internal load up to Idd3p3
6. The Lvi3p3 specs are also valid for the V_{DDEH} LVI
7. Lvi3p3 tracks DC target variation of internal V_{DD33} regulator. Minimum and maximum Lvi3p3 correspond to minimum and maximum V_{DD33} DC target respectively.
8. The 3.3V POR specs are also valid for the V_{DDEH} POR

3.6.1 Regulator example

In designs where the SPC564A70 microcontroller's internal regulators are used, a ballast is required for generation of the 1.2 V internal supply. No ballast is required when an external 1.2 V supply is used.

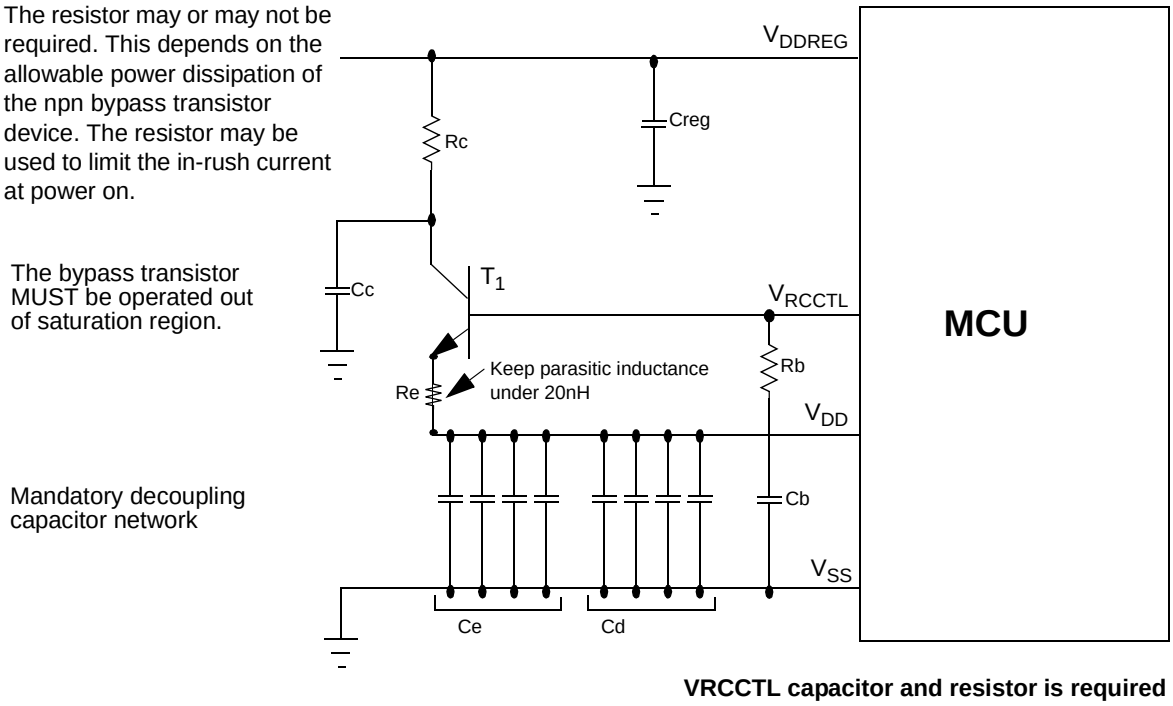


Figure 8. Core voltage regulator controller external components preferred configuration

Table 17. SPC564A70 External network specification

External Network Parameter	Min	Typ	Max	Comment
T1	—	—	—	NJD2873 or BCP68 only
Cb	1.1 µF	2.2µF	2.97µF	X7R,-50%/+35%
Ce	3*2.35µF+5µF	3*4.7µF+10µF	3*6.35µF+13.5µF	X7R, -50%/+35%
Equivalent ESR of Ce capacitors	5mΩ	—	50mΩ	—
Cd	4*50nF	4*100nF	4*135nF	X7R, -50%/+35%
Rb	9Ω	10Ω	11Ω	+/-10%
Re	0.252Ω	0.280Ω	0.308Ω	+/-10%
Creg	—	10µF	—	It depends on external Vreg.
Cc	5µF	10µF	13.5µF	X7R, -50%/+35%
Rc	1.1Ω	—	5.6Ω	May or may not be required. It depends on the allowable power dissipation of T1.

3.6.2 Recommended power transistors

The following NPN transistors are recommended for use with the on-chip voltage regulator controller: ON Semiconductor™ BCP68T1 or NJD2873 as well as Philips Semiconductor™ BCP68. The collector of the external transistor is preferably connected to the same voltage supply source as the output stage of the regulator.

Table 18. Transistor recommended operating characteristics

Symbol	Parameter	Value	Unit
h_{FE} (β)	DC current gain (Beta)	60–550	—
P_D	Absolute minimum power dissipation	>1.0 (1.5 preferred)	W
I_{CMaxDC}	Minimum peak collector current	1.0	A
VCE_{SAT}	Collector-to-emitter saturation voltage	200–600(1)	mV
V_{BE}	Base-to-emitter voltage	0.4–1.0	V

1. Adjust resistor at bipolar transistor collector for 3.3 V/5.0 V to avoid VCE < VCE_{SAT}

3.7 Power up/down sequencing

There is no power sequencing required among power sources during power up and power down, in order to operate within specification.

Although there are no power up/down sequencing requirements to prevent issues such as latch-up or excessive current spikes, the state of the I/O pins during power up/down varies according to *Table 19* for all pins with pad type fast, and *Table 20* for all pins with pad type medium, slow, and multi-voltage.

Table 19. Power sequence pin states—Fast type pads

V_{DDE}	V_{RC33}	V_{DD}	Pin state
Low	X	X	Low
V_{DDE}	Low	X	High
V_{DDE}	V_{RC33}	Low	High impedance
V_{DDE}	V_{RC33}	V_{DD}	Functional

Table 20. Power sequence pin states—Medium, slow and multi-voltage type pads

V_{DDEH}	V_{DD}	Pin state
Low	X	Low
V_{DDEH}	Low	High impedance
V_{DDEH}	V_{DD}	Functional

3.8 DC electrical specifications

Table 21. DC electrical specifications(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{DD}	SR	P	Core supply voltage	—	1.14	—	1.32	V
V_{DDE}	SR	P	I/O supply voltage	—	3.0	—	3.6	V
V_{DDEH}	SR	P	I/O supply voltage	—	3.0	—	5.25	V
V_{DDE-EH}	SR	P	I/O supply voltage	—	3.0	—	5.25	V
V_{RC33}	SR	P	3.3 V regulated voltage(2)	—	3.0	—	3.6	V
V_{DDA}	SR	P	Analog supply voltage	—	4.75(3)	—	5.25	V
V_{INDC}	SR	C	Analog input voltage	—	V_{SSA} – 0.3	—	V_{DDA} + 0.3	V
$V_{SS} – V_{SSA}$	SR	D	V_{SS} differential voltage	—	–100	—	100	mV
V_{RL}	SR	D	Analog reference low voltage	—	V_{SSA}	—	V_{SSA} + 0.1	V
$V_{RL} – V_{SSA}$	SR	D	V_{RL} differential voltage	—	–100	—	100	mV
V_{RH}	SR	D	Analog reference high voltage	—	V_{DDA} – 0.1	—	V_{DDA}	V
$V_{RH} – V_{RL}$	SR	P	V_{REF} differential voltage	—	4.75	—	5.25	V
V_{DDF}	SR	P	Flash operating voltage(4)	—	1.14	—	1.32	V
V_{FLASH}(5)	SR	P	Flash read voltage	—	3.0	—	3.6	V
V_{STBY}	SR	C	SRAM standby voltage	Unregulated mode	0.95	—	1.2	V
				Regulated mode	2.0	—	5.5	
V_{DDREG}	SR	P	Voltage regulator supply voltage(6)	—	4.75	—	5.25	V
V_{DDPLL}	SR	P	Clock synthesizer operating voltage	—	1.14	—	1.32	V
$V_{SSPLL} – V_{SS}$	SR	D	V_{SSPLL} to V_{SS} differential voltage	—	–100	—	100	mV
V_{IL_S}	SR	P	Slow/medium I/O input low voltage	Hysteresis enabled	V_{SS} – 0.3	—	0.35 * V_{DDEH}	V
		P		Hysteresis disabled	V_{SS} – 0.3	—	0.40 * V_{DDEH}	
V_{IL_F}	SR	P	Fast I/O input low voltage	Hysteresis enabled	V_{SS} – 0.3	—	0.35 * V_{DDE}	V
		P		Hysteresis disabled	V_{SS} – 0.3	—	0.40 * V_{DDE}	
V_{IL_LS}	SR	P	Multi-voltage I/O pad input low voltage in Low-swing-mode(7)(8)(9)(10)	Hysteresis enabled	V_{SS} – 0.3	—	0.8	V
		P		Hysteresis disabled	V_{SS} – 0.3	—	0.9	
V_{IL_HS}	SR	P	Multi-voltage pad I/O input low voltage in high-swing-mode	Hysteresis enabled	V_{SS} – 0.3	—	0.35 V_{DDEH}	V
		P		Hysteresis disabled	V_{SS} – 0.3	—	0.4 V_{DDEH}	

Table 21. DC electrical specifications(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IH_S}	SR	P	Slow/medium pad I/O input high voltage	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH} + 0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH} + 0.3	
V_{IH_F}	SR	P	Fast I/O input high voltage	Hysteresis enabled	0.65 V_{DDE}	—	V_{DDE} + 0.3	V
		P		Hysteresis disabled	0.58 V_{DDE}	—	V_{DDE} + 0.3	
V_{IH_LS}	SR	P	Multi-voltage pad I/O input high voltage in low-swing-mode(7)(8)(9)(10)	Hysteresis enabled	2.5	—	V_{DDE} + 0.3	V
		P		Hysteresis disabled	2.2	—	V_{DDE} + 0.3	
V_{IH_HS}	SR	P	Multi-voltage I/O input high voltage in high-swing-mode	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH} + 0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH} + 0.3	
V_{OL_S}	CC	P	Slow/medium pad I/O output low voltage(11)	—	—	—	0.2 * V_{DDEH}	V
V_{OL_F}	CC	P	Fast I/O output low voltage(11)	—	—	—	0.2 * V_{DDE}	V
V_{OL_LS}	CC	P	Multi-voltage pad I/O output low voltage in low-swing mode(7)(8)(9)(10)(11)	—	—	—	0.6	V
V_{OL_HS}	CC	P	Multi-voltage pad I/O output low voltage in high-swing mode(11)	—	—	—	0.2 V_{DDEH}	V
V_{OH_S}	CC	P	Slow/medium I/O output high voltage(11)	—	0.8 V_{DDEH}	—	—	V
V_{OH_F}	CC	P	Fast pad I/O output high voltage(11)	—	0.8 V_{DDE}	—	—	V
V_{OH_LS}	CC	P	Multi-voltage pad I/O output high voltage in low-swing mode(7)(8)(9)(10)(11)	—	2.3	3.1	3.7	V
V_{OH_HS}	CC	P	Multi-voltage pad I/O output high voltage in high-swing mode(11)	—	0.8 V_{DDEH}	—	—	V
V_{HYS_S}	CC	P	Slow/medium/multi-voltage I/O input hysteresis	—	0.1 * V_{DDEH}	—	—	V
V_{HYS_F}	CC	P	Fast I/O input hysteresis	—	0.1 * V_{DDE}	—	—	V
V_{HYS_LS}	CC	C	Low-swing-mode multi-voltage I/O input hysteresis	Hysteresis enabled	0.25	—	—	v

Table 21. DC electrical specifications(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$I_{DD}+I_{DDPLL}$	CC	P	Operating current 1.2 V supplies	V_{DD} @1.32 V @ 80 MHz	—	—	300	mA
		P		V_{DD} @ 1.32 V @ 120 MHz	—	—	360	mA
		P		V_{DD} @ 1.32 V @ 150 MHz	—	—	400	mA
I_{DDSTBY}	CC	T	Operating current 0.95-1.2 V	V_{STBY} at 55 °C	—	35	100	µA
		T	Operating current 2–5.5 V	V_{STBY} at 55 °C	—	45	110	µA
$I_{DDSTBY27}$	CC	P	Operating current 0.95-1.2 V	V_{STBY} 27 °C	—	25	90	µA
		P	Operating current 2-5.5 V	V_{STBY} 27 °C	—	35	100	µA
$I_{DDSTBY150}$	CC	P	Operating current 0.95-1.2 V	V_{STBY} 150 °C	—	790	2000	µA
		P	Operating current 2–5.5 V	V_{STBY} at 150 °C	—	760	2000	µA
I_{DDSLOW} I_{DDSTOP}	CC	C	V_{DD} low-power mode operating current @ 1.32 V	Slow mode(12)	—	—	191	mA
		C		Stop mode(13)	—	—	190	
I_{DD33}	CC	P	Operating current 3.3 V supplies	V_{RC33}(2)	—	—	60	mA
I_{DDA} I_{REF} I_{DDREG}	CC	P	Operating current 5.0 V supplies	V_{DDA}	—	—	30.0	mA
		P		Analog reference supply current (transient)	—	—	1.0	
		P		V_{DDREG}	—	—	70(14)	
I_{DDH1} I_{DDH4} I_{DDH6} I_{DDH7} I_{DD7} I_{DDH9} I_{DD12}	CC	P	Operating current V_{DDE}(15) supplies	V_{DDEH1}	—	—	See note (15)	mA
		P		V_{DDEH4}	—	—		
		P		V_{DDEH6}	—	—		
		P		V_{DDEH7}	—	—		
		P		V_{DDE7}	—	—		
		P		V_{DDEH9}	—	—		
		P		V_{DDE12}	—	—		
I_{ACT_S}	CC	P	Slow/medium I/O weak pull-up/down current16	3.0 V–3.6 V	15	—	95	µA
		P		4.75 V–5.25 V	35	—	200	

Table 21. DC electrical specifications(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{ACT_F}	CC	P	Fast I/O weak pull-up/down current(16)	1.62 V–1.98 V	36	—	120	µA
		P		2.25 V–2.75 V	34	—	139	
		P		3.0 V–3.6 V	42	—	158	
$I_{ACT\_MV\_PU}$	CC	C	Multi-voltage pad weak pull-up current	V_{DDE} = 3.0 – 3.6 V(7), multi-voltage, high swing mode only	10	—	75	µA
		C		4.75 V–5.25 V	25	—	175	
$I_{ACT\_MV\_PD}$	CC	C	Multi-voltage pad weak pull-down current	V_{DDE} = 3.0 – 3.6 V(7), multi-voltage, all process corners, high swing mode only	10	—	60	µA
		C		4.75 V–5.25 V	25	—	200	
I_{INACT_D}	CC	P	I/O input leakage current(17)	—	–2.5	—	2.5	µA
I_{IC}	SR	T	DC injection current (per pin)	—	–1.0	—	1.0	mA
I_{INACT_A}	SR	P	Analog input current, channel off, AN[0:7](18)	—	–250	—	250	nA
		P	Analog input current, channel off, all other analog pins18	—	–150	—	150	
C_L	CC	D	Load capacitance (fast I/O)(19)	DSC(PCR[8:9]) = 0b00	—	—	10	pF
		D		DSC(PCR[8:9]) = 0b01	—	—	20	
		D		DSC(PCR[8:9]) = 0b10	—	—	30	
		D		DSC(PCR[8:9]) = 0b11	—	—	50	
C_{IN}	CC	D	Input capacitance (digital pins)	—	—	—	7	pF
C_{IN_A}	CC	D	Input capacitance (analog pins)	—	—	—	10	pF
C_{IN_M}	CC	D	Input capacitance (digital and analog pins(20))	—	—	—	12	pF
$R_{PUPD200K}$	SR	C	Weak pull-up/down resistance(21), 200 kΩ option	—	130	—	280	kΩ

Table 21. DC electrical specifications(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$R_{PUPD100K}$	SR	C	Weak pull-up/down resistance(21), 100 kΩ option	—	65	—	140	kΩ
R_{PUPD5K}	SR	C	Weak pull-up/down resistance(21), 5 kΩ option	5 V ± 10% supply	1.4	—	5.2	kΩ
		C		3.3 V ± 10% supply	1.7	—	7.7	
R_{PUPD5K}	SR	C	Weak Pull-Up/Down Resistance(21), 5 kΩ Option	5 V ± 5% supply	1.4	—	7.5	kΩ
$R_{PUPDMTCH}$	CC	C	Pull-up/Down Resistance matching ratios (100K/200K)	Pull-up and pull-down resistances both enabled and settings are equal.	–2.5	—	2.5	%
T_A (T_L to T_H)	SR	P	Operating temperature range - ambient (packaged)	—	–40.0	—	125.0	°C
—	SR	D	Slew rate on power supply pins	—	—	—	25	V/ms

1. These specifications are design targets and subject to change per device characterization.
2. These specifications apply when V_{RC33} is supplied externally, after disabling the internal regulator (V_{DDREG} = 0).
3. ADC is functional with 4 V ≤ V_{DDA} ≤ 4.75 V but with derated accuracy. This means the ADC will continue to function at full speed with no undesirable behavior, but the accuracy will be degraded.
4. The V_{DDF} supply is connected to V_{DD} in the package substrate. This specification applies to calibration package devices only.
5. V_{FLASH} is available in the calibration package only.
6. Regulator is functional, with derated performance, with supply voltage down to 4.0 V
7. Multi-voltage power supply cannot be below 4.5 V when in low-swing mode
8. The slew rate (SRC) setting must be 0b11 when in low-swing mode.
9. While in low-swing mode there are no restrictions in transitioning to high-swing mode.
10. Pin in low-swing mode can accept a 5 V input
11. All V_{OL}/V_{OH} values 100% tested with ± 2 mA load except where otherwise noted
12. Bypass mode, system clock @ 1 MHz (using system clock divider), PLL shut down, CPU running simple executive code, 4 x ADC conversion every 10 ms, 2 x PWM channels @ 1 kHz, all other modules stopped.
13. Bypass mode, system clock @ 1 MHz (using system clock divider), CPU stopped, PIT running, all other modules stopped
14. If 1.2V and 3.3V internal regulators are on,then iddreg=70mA

    If supply is external that is 3.3V internal regulator is off, then iddreg=15mA
15. Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. See *Table 22* for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.
16. Absolute value of current, measured at V_{IL} and V_{IH}
17. Weak pull-up/down inactive. Measured at V_{DDE} = 3.6 V and V_{DDEH} = 5.25 V. Applies to all digital pad types.
18. Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 °C, in the ambient temperature range of 50 to 125 °C. Applies to analog pads.
19. Applies to CLKOUT, external bus pins, and Nexus pins

20. Applies to the FCK, SDI, SDO, and SDS pins
21. This programmable option applies only to eQADC differential input channels and is used for biasing and sensor diagnostics.

3.9 I/O pad current specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from *Table 22* based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in *Table 22*.

Table 22. I/O pad average I_{DDE} specifications(1)

Pad type	Symbol		C	Period (ns)	Load(2) (pF)	V_{DDE} (V)	Drive/Slew rate select	I_{DDE} Avg (mA)(3)	I_{DDE} RMS (mA)
Slow	$I_{DRV\_SSR\_HV}$	CC	D	37	50	5.25	11	9	—
		CC	D	130	50	5.25	01	2.5	—
		CC	D	650	50	5.25	00	0.5	—
		CC	D	840	200	5.25	00	1.5	—
Medium	$I_{DRV\_MSR\_HV}$	CC	D	24	50	5.25	11	14	—
		CC	D	62	50	5.25	01	5.3	—
		CC	D	317	50	5.25	00	1.1	—
		CC	D	425	200	5.25	00	3	—

Table 22. I/O pad average I_{DDE} specifications(1) (continued)

Pad type	Symbol	C		Period (ns)	Load(2) (pF)	V_{DDE} (V)	Drive/Slew rate select	I_{DDE} Avg (mA)(3)	I_{DDE} RMS (mA)
Fast	I_{DRV_FC}	CC	D	10	50	3.6	11	22.7	68.3
		CC	D	10	30	3.6	10	12.1	41.1
		CC	D	10	20	3.6	01	8.3	27.7
		CC	D	10	10	3.6	00	4.44	14.3
		CC	D	10	50	1.98	11	12.5	31
		CC	D	10	30	1.98	10	7.3	18.6
		CC	D	10	20	1.98	01	5.42	12.6
		CC	D	10	10	1.98	00	2.84	6.4
MultiV (High swing mode)	$I_{DRV\_MULTV\_HV}$	CC	D	20	50	5.25	11	9	—
		CC	D	30	50	5.25	01	6.1	—
		CC	D	117	50	5.25	00	2.3	—
		CC	D	212	200	5.25	00	5.8	—
MultiV (Low swing mode)	$I_{DRV\_MULTV\_HV}$	CC	D	30	30	5.25	11	3.4	—

1. Numbers from simulations at best case process, 150 °C
2. All loads are lumped.
3. Average current is for pad configured as output only

3.9.1 I/O pad V_{RC33} current specifications

The power consumption of the V_{RC33} supply is dependent on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{RC33} currents for all I/O segments. The output pin V_{RC33} current can be calculated from *Table 23* based on the voltage, frequency, and load on all fast pins. The input pin V_{RC33} current can be calculated from *Table 23* based on the voltage, frequency, and load on all medium pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in *Table 23*.

Table 23. I/O pad V_{RC33} average I_{DDE} specifications(1)

Pad type	Symbol		C	Period (ns)	Load(2) (pF)	Drive select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
Slow	$I_{DRV\_SSR\_HV}$	CC	D	100	50	11	0.8	235.7
		CC	D	200	50	01	0.04	87.4
		CC	D	800	50	00	0.06	47.4
		CC	D	800	200	00	0.009	47
Medium	$I_{DRV\_MSR\_HV}$	CC	D	40	50	11	2.75	258
		CC	D	100	50	01	0.11	76.5
		CC	D	500	50	00	0.02	56.2
		CC	D	500	200	00	0.01	56.2
MultiV(3) (High swing mode)	$I_{DRV\_MULTV\_HV}$	CC	D	20	50	11	33.4	35.4
		CC	D	30	50	01	33.4	34.8
		CC	D	117	50	00	33.4	33.8
		CC	D	212	200	00	33.4	33.7
MultiV(4) (Low swing mode)	$I_{DRV\_MULTV\_HV}$	CC	D	30	30	11	33.4	33.7

1. These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.
2. All loads are lumped.
3. Average current is for pad configured as output only
4. In low swing mode, multi-voltage pads must operate in highest slew rate setting, ipp_sre0 = 1, ipp_sre1 = 1.

Table 24. V_{RC33} pad average DC current(1)

Pad type	Symbol		C	Period (ns)	Load(2) (pF)	V_{RC33} (V)	V_{DDE} (V)	Drive select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
Fast	I_{DRV_FC}	CC	D	10	50	3.6	3.6	11	2.35	6.12
		CC	D	10	30	3.6	3.6	10	1.75	4.3
		CC	D	10	20	3.6	3.6	01	1.41	3.43
		CC	D	10	10	3.6	3.6	00	1.06	2.9
		CC	D	10	50	3.6	1.98	11	1.75	4.56
		CC	D	10	30	3.6	1.98	10	1.32	3.44
		CC	D	10	20	3.6	1.98	01	1.14	2.95
		CC	D	10	10	3.6	1.98	00	0.95	2.62

1. These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.
2. All loads are lumped.

3.9.2 LVDS pad specifications

LVDS pads are implemented to support the MSC (Microsecond Channel) protocol which is an enhanced feature of the DSPI module. The LVDS pads are compliant with LVDS specifications and support data rates up to 50 MHz.

Table 25. DSPI LVDS pad specification

Symbol	C		Parameter	Condition	Value			Unit
					Min	Typ	Max	
Data rate								
$f_{LVDSCLK}$	CC	D	Data frequency	—	—	50	—	MHz
Driver specifications								
V_{OD}	CC	P	Differential output voltage	SRC = 0b00 or 0b11	150	—	400	mV
	CC	P		SRC = 0b01	90	—	320	
	CC	P		SRC = 0b10	160	—	480	
V_{OC}	CC	P	Common mode voltage (LVDS), VOS	—	1.06	1.2	1.39	V
T_R/T_F	CC	D	Rise/Fall time	—	—	2	—	ns
T_{PLH}	CC	D	Propagation delay (Low to High)	—	—	4	—	ns
T_{PHL}	CC	D	Propagation delay (High to Low)	—	—	4	—	ns
t_{PDSYNC}	CC	D	Delay (H/L), sync mode	—	—	4	—	ns
T_{DZ}	CC	D	Delay, Z to Normal (High/Low)	—	—	500	—	ns
T_{SKEW}	CC	D	Differential skew Itphla-tplhbI or Itplhb-tphlaI	—	—	—	0.5	ns
Termination								
	CC	D	Transmission line (differential Zo)	—	95	100	105	W
	CC	D	Temperature	—	–40	—	150	°C

3.10 Oscillator and PLLMRFM electrical characteristics

Table 26. PLLMRFM electrical specifications(1)

(V_{DDPLL} = 1.08 V to 3.6 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H)

Symbol	C		Parameter	Conditions	Value		Unit
					Min	Max	
$f_{ref\_crystal}$	C	P	PLL reference frequency range(2)	Crystal reference	4	40	MHz
f_{ref_ext}	C	P		External reference	4	80	
f_{pll_in}	C	D	Phase detector input frequency range (after pre-divider)	—	4	16	MHz

Table 26. PLLMRFM electrical specifications[1]

(V_{DDPLL} = 1.08 V to 3.6 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H) (continued)

Symbol		C	Parameter		Conditions	Value		Unit
						Min	Max	
f_{vco}	CC	D	VCO frequency range		—	256	512	MHz
f_{sys}	CC	T	On-chip PLL frequency[2]		—	16	150	MHz
f_{sys}	CC	T	System frequency in bypass mode[3]		Crystal reference	4	40	MHz
		T			External reference	0	80	
t_{CYC}	CC	D	System clock period		—	—	1 / f_{sys}	ns
f_{LORL} f_{LORH}	CC	D	Loss of reference frequency window[4]		Lower limit	1.6	3.7	MHz
		D			Upper limit	24	56	
f_{SCM}	CC	P	Self-clocked mode frequency[5][6]		—	1.2	72.25	MHz
C_{JITTER}	CC	C	CLKOUT period jitter[7][8][9][10]	Peak-to-peak (clock edge to clock edge)	f_{SYS} maximum	–5	5	% f_{CLKOUT}
		C		Long-term jitter (avg. over 2 ms interval)		–6	6	ns
t_{cst}	CC	T	Crystal start-up time[11][12]		—	—	10	ms
V_{IHEXT}	CC	D	EXTAL input high voltage		Crystal mode[13]	Vxtal + 0.4	—	V
		T			External reference[13][14]	V_{RC33}/2 + 0.4	V_{RC33}	
V_{ILEXT}	CC	D	EXTAL input low voltage		Crystal mode[13]	—	Vxtal – 0.4	V
		T			External reference[13][14]	0	V_{RC33}/2 – 0.4	
—	CC	T	XTAL load capacitance		—	5	30	pF
—	CC	C	XTAL load capacitance[11]		4 MHz	5	30	pF
					8 MHz	5	26	
					12 MHz	5	23	
					16 MHz	5	19	
					20 MHz	5	16	
					40 MHz	5	8	
t_{lpll}	CC	P	PLL lock time[11][15]		—	—	200	µs
t_{dc}	CC	D	Duty cycle of reference		—	40	60	%

Table 26. PLLMRFM electrical specifications(1)

(V_{DDPLL} = 1.08 V to 3.6 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{LCK}	CC	D	Frequency LOCK range	—	–6	6	% f_{sys}
f_{UL}	CC	D	Frequency un-LOCK range	—	–18	18	% f_{sys}
f_{CS}	CC	D	Modulation depth	Center spread	±0.25	±4.0	% f_{sys}
f_{DS}		D		Down spread	–0.5	–8.0	
f_{MOD}	CC	D	Modulation frequency(16)	—	—	100	kHz

1. All values given are initial design targets and subject to change.
2. Considering operation with PLL not bypassed
3. All internal registers retain data at 0 Hz.
4. “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.
5. Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.
6. f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.
7. This value is determined by the crystal manufacturer and board design.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.
9. Proper PC board layout procedures must be followed to achieve specifications.
10. Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).
11. This value is determined by the crystal manufacturer and board design. For 4 MHz to 40 MHz crystals specified for this PLL, load capacitors should not exceed these limits.
12. Proper PC board layout procedures must be followed to achieve specifications.
13. This parameter is guaranteed by design rather than 100% tested.
14. V_{IHEXT} cannot exceed V_{RC33} in external reference mode.
15. This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
16. Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

3.11 Temperature sensor electrical characteristics

Table 27. Temperature sensor electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
—	CC	C	Temperature monitoring range		–40	—	150	°C

Table 27. Temperature sensor electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
—	CC	C	Sensitivity		—	6.3	—	mV/°C
—	CC	C	Accuracy	T_J = –40 to 150 °C	–10	—	10	°C

3.12 eQADC electrical characteristics

Table 28. eQADC conversion specifications (operating)

Symbol		C	Parameter	Value		Unit
				min	max	
f_{ADCLK}	SR	—	ADC clock (ADCLK) frequency	2	16	MHz
CC	CC	D	Conversion cycles	2+13	128+14	ADCLK cycles
T_{SR}	CC	C	Stop mode recovery time(1)	—	10	µs
f_{ADCLK}	SR	—	ADC clock (ADCLK) frequency	2	16	mV

1. Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions.Delay from power up to full accuracy = 8 ms.

Table 29. eQADC single ended conversion specifications (operating)

Symbol		C	Parameter	Value		Unit
				min	max	
OFFNC	CC	C	Offset error without calibration	0	160	Counts
OFFWC	CC	C	Offset error with calibration	–4	4	Counts
GAINNC	CC	C	Full scale gain error without calibration	–160	0	Counts
GAINWC	CC	C	Full scale gain error with calibration	–4	4	Counts
I_{INJ}	CC	T	Disruptive input injection current (1), (2), (3), (4)	–3	3	mA
E_{INJ}	CC	T	Incremental error due to injection current(5),(6)	–4	4	Counts
TUE8	CC	C	Total unadjusted error (TUE) at 8 MHz	–4	4(6)	Counts
TUE16	CC	C	Total unadjusted error at 16 MHz	–8	8	Counts

1. Below disruptive current conditions, the channel being stressed has conversion values of 0x3FF for analog inputs greater then V_{RH} and 0x0 for values less then V_{RL}. Other channels are not affected by non-disruptive conditions.
2. Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.
3. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA} + 0.5$ V and $V_{NEGCLAMP} = – 0.3$ V, then use the larger of the calculated values.
4. Condition applies to two adjacent pins at injection limits.

5. Performance expected with production silicon.
6. All channels have same 10 kΩ < Rs < 100 kΩ; Channel under test has Rs=10 kΩ; I_{INJ}=I_{INJMAX},I_{INJMIN}

Table 30. eQADC differential ended conversion specifications (operating)

Symbol		C	Parameter		Value		Unit
					min	max	
GAINVGA1 (1)	CC	–	Variable gain amplifier accuracy (gain=1)(2)				
	CC	C	INL	8 MHz ADC	–4	4	Counts (3)
	CC	C		16 MHz ADC	–8	8	Counts
	CC	C	DNL	8 MHz ADC	–3(4)	3(4)	Counts
	CC	C		16 MHz ADC	–3(4)	3(4)	Counts
GAINVGA2 (1)	CC	–	Variable gain amplifier accuracy (gain=2)(2)				
	CC	D	INL	8 MHz ADC	–5	5	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–3	3	Counts
	CC	D		16 MHz ADC	–3	3	Counts
GAINVGA4 (1)	CC	–	Variable gain amplifier accuracy (gain=4)(2)				
	CC	D	INL	8 MHz ADC	–7	7	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–4	4	Counts
	CC	D		16 MHz ADC	–4	4	Counts

Table 30. eQADC differential ended conversion specifications (operating) (continued)

Symbol		C	Parameter		Value		Unit
					min	max	
$DIFF_{max}$	CC	C	Maximum differential voltage (DANx+ - DANx-) or (DANx- - DANx+)(5)	PREGAIN set to 1X setting	—	(VRH - VRL)/2	V
$DIFF_{max2}$	CC	C		PREGAIN set to 2X setting	—	(VRH - VRL)/4	V
$DIFF_{max4}$	CC	C		PREGAIN set to 4X setting	—	(VRH - VRL)/8	V
$DIFF_{cmv}$	CC	C	Differential input Common mode voltage (DANx- + DANx+)/2(5)	—	$(V_{RH} + V_{RL})/2$ - 5%	$(V_{RH} + V_{RL})/2$ + 5%	V

1. Applies only to differential channels.
2. Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed by as indicated.
3. At $V_{RH} – V_{RL}$ = 5.12 V, one LSB = 1.25 mV.
4. Guaranteed 10-bit mono tonicity.
5. Voltages between VRL and VRH will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

3.13 Configuring SRAM wait states

Use the SWSC field in the ECSM_MUDCR register to specify an additional wait state for the device SRAM. By default, no wait state is added.

Table 31. Cutoff frequency for additional SRAM wait state

(1)	SWSC Value
98	0
153	1

1. Max frequencies including 2% PLL FM.

Please see the device reference manual for details.

3.14 Platform flash controller electrical characteristics

Table 32. APC, RWSC, WWSC settings vs. frequency of operation(1)

Max. Flash Operating Frequency (MHz)(2)	APC(3)	RWSC(3)	WWSC
20 MHz	0b000	0b000	0b01
61 MHz	0b001	0b001	0b01
90 MHz	0b010	0b010	0b01
123 MHz	0b011	0b011	0b01
153 MHz	0b100	0b100	0b01

1. APC, RWSC and WWSC are fields in the flash memory BIUCR register used to specify wait states for address pipelining and read/write accesses. Illegal combinations exist—all entries must be taken from the same row.
2. Max frequencies including 2% PLL FM.
3. APC must be equal to RWSC.

3.15 Flash memory electrical characteristics

Table 33. Flash program and erase specifications(1)

#	Symbol		C	Parameter	Value				Unit
					Min	Typ	Initial max(2)	Max(3)	
1	$T_{dwprogram}$	CC	C	Double Word (64 bits) Program Time	—	30	—	500	µs
2	$T_{pprogram}$	CC	C	Page Program Time(4)	—	40	160	500	µs
3	$T_{16kpperase}$	CC	C	16 KB Block Pre-program and Erase Time	—	—	1000	5000	ms
5	$T_{64kpperase}$	CC	C	64 KB Block Pre-program and Erase Time	—	—	1800	5000	ms
6	$T_{128kpperase}$	CC	C	128 KB Block Pre-program and Erase Time	—	—	2600	7500	ms
7	$T_{256kpperase}$	CC	C	256 KB Block Pre-program and Erase Time	—	—	5200	15000	ms
8	T_{psrt}	SR	—	Program suspend request rate(5)	100	—	—	—	µs
9	T_{esrt}	SR	—	Erase suspend request rate (6)	10				ms

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: ≤ 100 program/erase cycles, 25 °C, typical supply voltage, 80 MHz minimum system frequency.
3. The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4. Page size is 128 bits (4 words)
5. Time between program suspend resume and the next program suspend request.
6. Time between erase suspend resume and the next erase suspend request.

Table 34. Flash EEPROM module life

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Typ	
P/E	CC	D	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 KB blocks over the operating temperature range (T_J)	—	100000	—	cycles
P/E	CC	D	Number of program/erase cycles per block for 128 KB and 256 KB blocks over the operating temperature range (T_J)	—	1000	100000	cycles
Retention	CC	D	Minimum data retention at 85 °C	Blocks with 0 – 1000 P/E cycles	20	—	years
		D		Blocks with 10000 P/E cycles	10	—	
		D		Blocks with 100000 P/E cycles	5	—	

3.16 AC specifications

3.16.1 Pad AC specifications

Table 35. Pad AC specifications (V_{DDE} = 4.75 V)(1)

Name		C	Output delay (ns)(2)(3) Low-to-High / High-to-Low		Rise/Fall edge (ns)(3)(4)		Drive load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB, LSB
Medium(5)(6)(7)	CC	D	4.6/3.7	12/12	2.2/2.2	12/12	50	11(8)
	—							10(9)
	CC	D	12/13	28/34	5.6/6	15/15	50	01
	CC	D	69/71	152/165	34/35	74/74	50	00
Slow(7)(10)	CC	D	7.3/5.7	19/18	4.4/4.3	20/20	50	11(8)
	—							10(9)
	CC	D	26/27	61/69	13/13	34/34	50	01
	CC	D	137/142	320/330	72/74	164/164	50	00
MultiV(11) (High Swing Mode)	CC	D	4.1/3.6	10.3/8.9	3.28/2.98	8/8	50	11(8)
	—							10(9)
	CC	D	8.38/6.11	16/12.9	5.48/4.81	11/11	50	01
	CC	D	61.7/10.4	92.2/24.3	42.0/12.2	63/63	50	00
MultiV (Low Swing Mode)	CC	D	2.31/2.34	7.62/6.33	1.26/1.67	6.5/4.4	30	11(8)
Fast(12)	—							
Standalone input buffer(13)	CC	D	0.5/0.5	1.9/1.9	0.3/0.3	±1.5/1.5	0.5	—

1. These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.75 V to 5.25 V, $T_A = T_L$ to T_H.
2. This parameter is supplied for reference and is not guaranteed by design and not tested.
3. Delay and rise/fall are measured to 20% or 80% of the respective signal.
4. This parameter is guaranteed by characterization before qualification rather than 100% tested.
5. In high swing mode, high/low swing pad V_{OL} and V_{OH} values are the same as those of the slew controlled output pads.
6. Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pull-up/pull-down.
7. Output delay is shown in *Figure 9* and *Figure 10*. Add a maximum of one system clock to the output delay for delay with respect to system clock.

8. Can be used on the tester
9. This drive select value is not supported. If selected, it will be approximately equal to 11.
10. Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pull-up/pull-down.
11. Selectable high/low swing I/O pad with selectable slew in high swing mode only
12. Fast pads are 3.3 V pads.
13. Also has weak pull-up/pull-down.

Table 36. Pad AC specifications (V_{DDE} = 3.0 V)(1)

Pad type		C	Output delay (ns)(2)(3) Low-to-High / High-to-Low		Rise/Fall edge (ns)(3)(4)		Drive load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Medium(5)(6)(7)	CC	D	5.8/4.4	18/17	2.7/2.1	10/10	50	11(8)
	CC	D	16/13	46/49	11.2/8.6	34/34	200	
	—							10(9)
	CC	D	14/16	37/45	6.5/6.7	19/19	50	01
	CC	D	27/27	69/82	15/13	43/43	200	
	CC	D	83/86	200/210	38/38	86/86	50	00
	CC	D	113/109	270/285	53/46	120/120	200	
Slow(7)(10)	CC	D	9.2/6.9	27/28	5.5/4.1	20/20	50	11
	CC	D	30/23	81/87	21/16	63/63	200	
	—							10(9)
	CC	D	31/31	80/90	15.4/15.4	42/42	50	01
	CC	D	58/52	144/155	32/26	82/85	200	
	CC	D	162/168	415/415	80/82	190/190	50	00
	CC	D	216/205	533/540	106/95	250/250	200	
MultiV(7)(11) (High Swing Mode)	CC	D	—	3.7/3.1	—	10/10	30	11(8)
	CC	D	—	46/49	—	42/42	200	
	—							10(9)
	CC	D	—	32	—	15/15	50	01
	CC	D	—	72	—	46/46	200	
	CC	D	—	210	—	100/100	50	00
	CC	D	—	295	—	134/134	200	
MultiV (Low Swing Mode)	Not a valid operational mode							

Table 36. Pad AC specifications (V_{DDE} = 3.0 V)(1) (continued)

Pad type		C	Output delay (ns)(2)(3) Low-to-High / High-to-Low		Rise/Fall edge (ns)(3)(4)		Drive load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Fast	CC	D	—	2.5/2.5	—	1.2/1.2	10	00
	CC	D	—	2.5/2.5	—	1.2/1.2	20	01
	CC	D	—	2.5/2.5	—	1.2/1.2	30	10
	CC	D	—	2.5/2.5	—	1.2/1.2	50	11(8)
Standalone input buffer(12)	CC	D	0.5/0.5	3/3	0.4/0.4	±1.5/1.5	0.5	—

1. These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.14 V to 1.32 V, V_{DDE} = 3 V to 3.6 V, V_{DDEH} = 3 V to 3.6 V, $T_A = T_L$ to T_H.
2. This parameter is supplied for reference and is not guaranteed by design and not tested.
3. Delay and rise/fall are measured to 20% or 80% of the respective signal.
4. This parameter is guaranteed by characterization before qualification rather than 100% tested.
5. In high swing mode, high/low swing pad V_{OL} and V_{OH} values are the same as those of the slew controlled output pads.
6. Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pull-up/pull-down.
7. Output delay is shown in *Figure 9* and *Figure 10*. Add a maximum of one system clock to the output delay for delay with respect to system clock.
8. Can be used on the tester.
9. This drive select value is not supported. If selected, it will be approximately equal to 11.
10. Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pull-up/pull-down.
11. Selectable high/low swing I/O pad with selectable slew in high swing mode only.
12. Also has weak pull-up/pull-down.

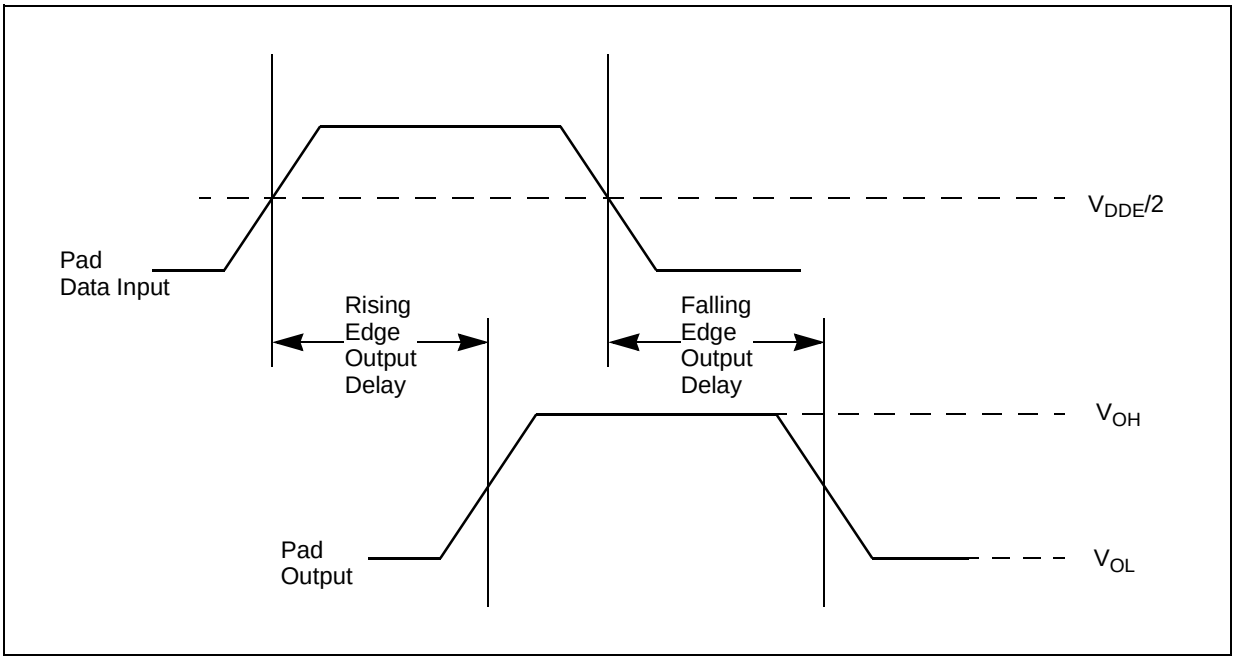


Figure 9. Pad output delay—Fast pads

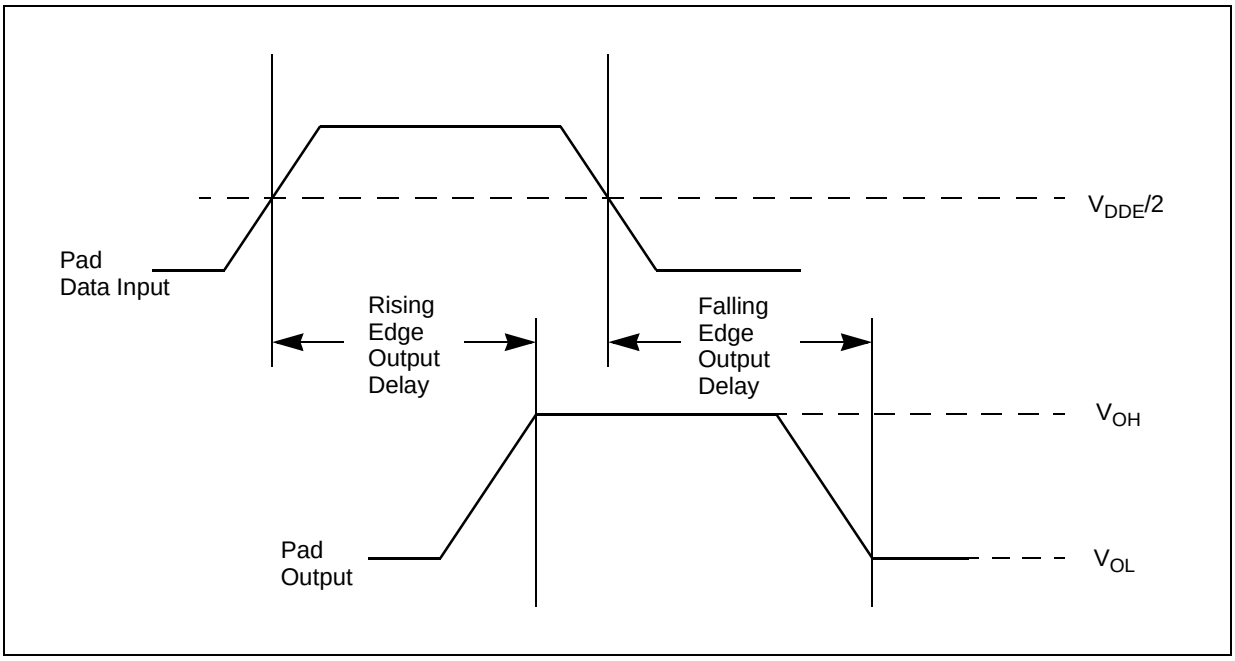


Figure 10. Pad output delay—Slew rate controlled fast, medium, and slow pads

3.17 AC timing

3.17.1 Reset and configuration pin timing

Table 37. Reset and configuration pin timing(1)

#	Symbol	Characteristic	Value		Unit
			Min	Max	
1	t_{RPW}	$\overline{\text{RESET}}$ Pulse Width	10	—	t_{CYC}
2	t_{GPW}	$\overline{\text{RESET}}$ Glitch Detect Pulse Width	2	—	t_{CYC}
3	t_{RCSU}	PLLREF, BOOTCFG, WKPCFG Setup Time to $\overline{\text{RSTOUT}}$ Valid	10	—	t_{CYC}
4	t_{RCH}	PLLREF, BOOTCFG, WKPCFG Hold Time to $\overline{\text{RSTOUT}}$ Valid	0	—	t_{CYC}

1. Reset timing specified at: V_{DDEH} = 3.0 V to 5.25 V, V_{DD} = 1.14 V to 1.32 V, $T_A = T_L$ to T_H.

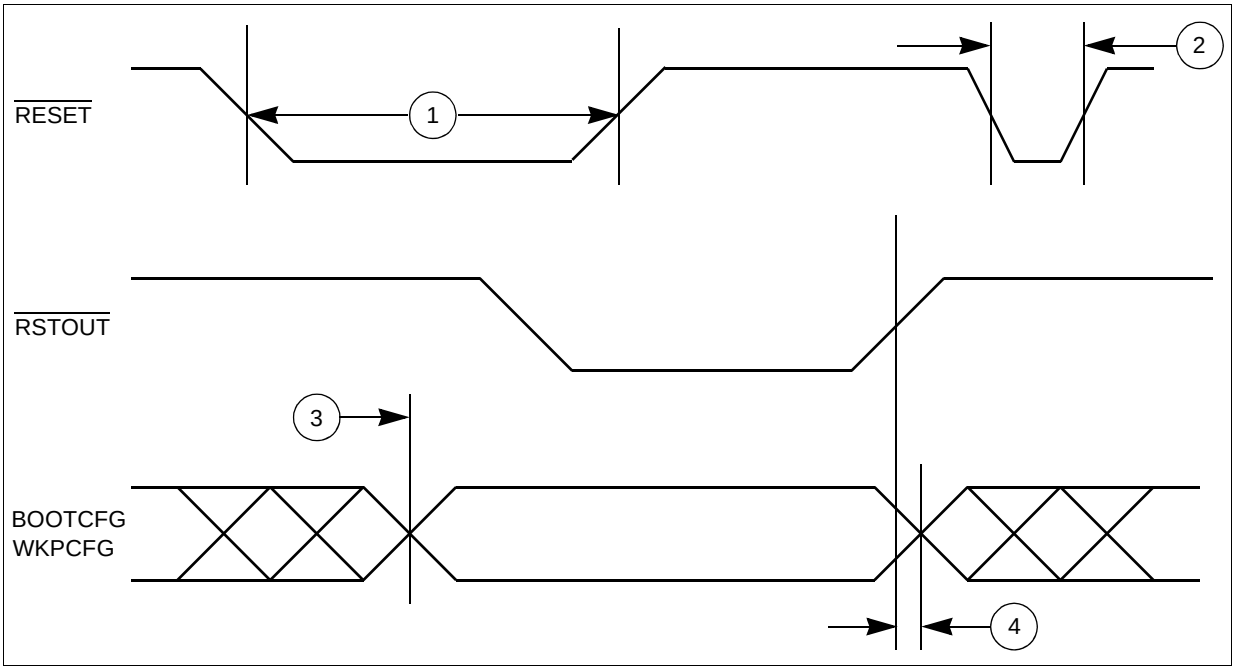


Figure 11. Reset and configuration pin timing

3.17.2 IEEE 1149.1 interface timing

Table 38. JTAG pin AC electrical characteristics(1)

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
1	t_{JCYC}	CC	D	TCK Cycle Time	100	—	ns

Table 38. JTAG pin AC electrical characteristics[1] (continued)

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
2	t_{JDC}	CC	D	TCK Clock Pulse Width	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK Rise and Fall Times (40%–70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI Data Setup Time	10	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI Data Hold Time	25	—	ns
6	t_{TDOV}	CC	D	TCK Low to TDO Data Valid	—	22[2]	ns
7	t_{TDOI}	CC	D	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	CC	D	TCK Low to TDO High Impedance	—	22	ns
9	t_{JCMPPW}	CC	D	JCOMP Assertion Time	100	—	ns
10	t_{JCMPS}	CC	D	JCOMP Setup Time to TCK Low	40	—	ns
11	t_{BSDV}	CC	D	TCK Falling Edge to Output Valid	—	50	ns
12	t_{BSDVZ}	CC	D	TCK Falling Edge to Output Valid out of High Impedance	—	50	ns
13	t_{BSDHZ}	CC	D	TCK Falling Edge to Output High Impedance	—	50	ns
14	t_{BSDST}	CC	D	Boundary Scan Input Valid to TCK Rising Edge	25[3]	—	ns
15	t_{BSDHT}	CC	D	TCK Rising Edge to Boundary Scan Input Invalid	25[3]	—	ns

1. JTAG timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.75 V to 5.25 V with multi-voltage pads programmed to Low-Swing mode, $T_A = T_L$ to T_H, C_L = 30 pF, SRC = 0b11. These specifications apply to JTAG boundary scan only. See *Table 39* for functional specifications.
2. Pad delay is 8–10 ns. Remainder includes TCK pad delay, clock tree delay logic delay and TDO output pad delay.
3. For 20 MHz TCK.

Note: The Nexus/JTAG Read/Write Access Control/Status Register (RWCS) write (to begin a read access) or the write to the Read/Write Access Data Register (RWD) (to begin a write access) does not actually begin its action until 1 JTAG clock (TCK) after leaving the JTAG Update-DR state. This prevents the access from being performed and therefore will not signal its completion via the READY (RDY) output unless the JTAG controller receives an additional TCK. In addition, EVTI is not latched into the device unless there are clock transitions on TCK.

The tool/debugger must provide at least one TCK clock for the $\overline{EVTI}$ signal to be recognized by the MCU. When using the RDY signal to indicate the end of a Nexus read/write access, ensure that TCK continues to run for at least one TCK after leaving the Update-DR state. This can be just a TCK with TMS low while in the Run-Test/Idle state or by continuing with the next Nexus/JTAG command. Expect the effect of $\overline{EVTI}$ and RDY to be delayed by edges of TCK.

RDY is not available in all device packages.

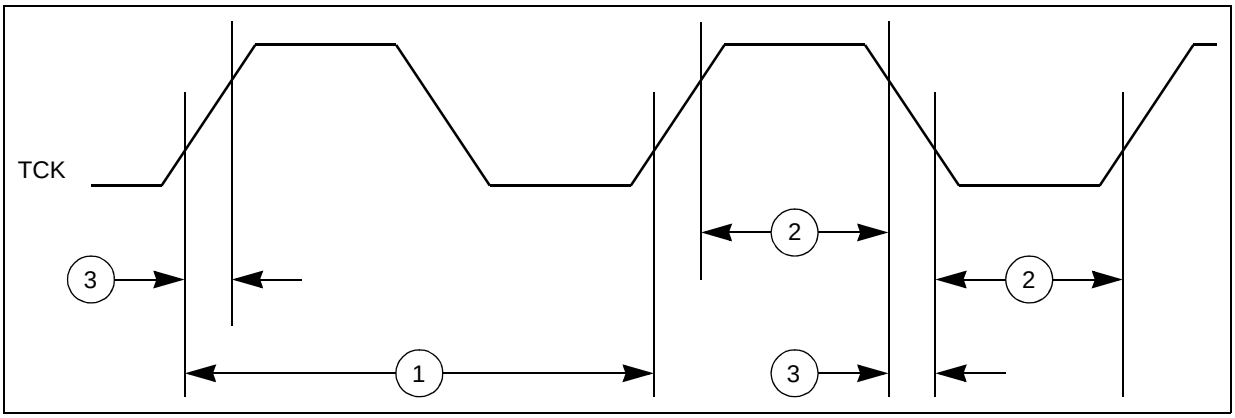


Figure 12. JTAG test clock input timing

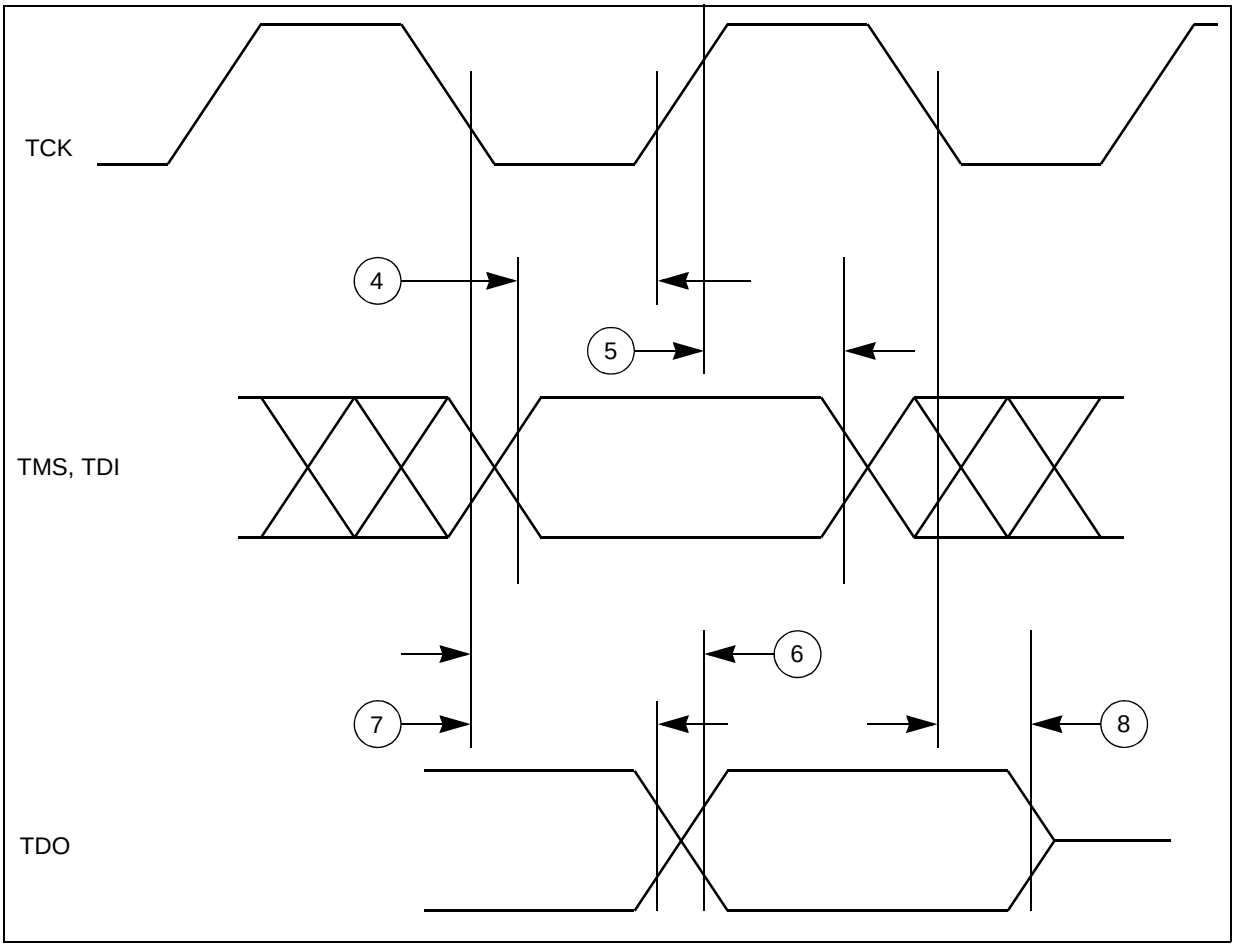


Figure 13. JTAG test access port timing

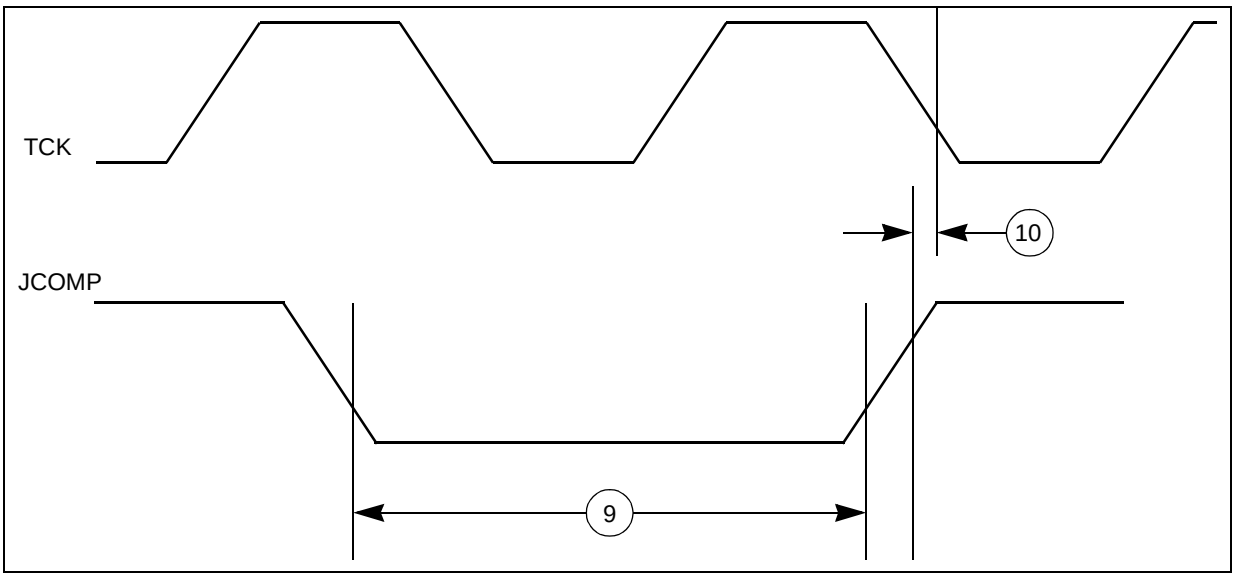


Figure 14. JTAG JCOMP timing

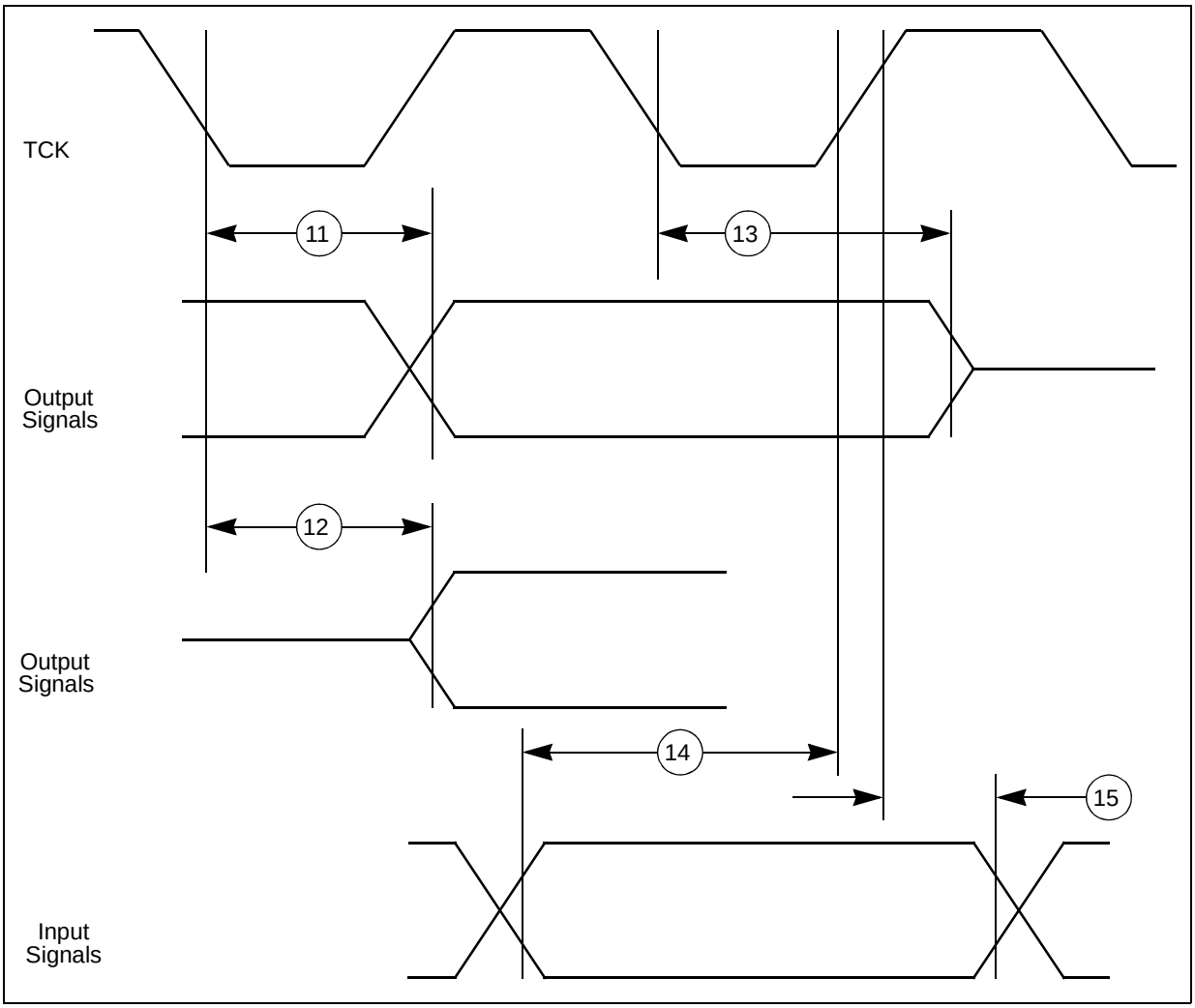


Figure 15. JTAG boundary scan timing

3.17.3 Nexus timing

Table 39. Nexus debug port timing(1)

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
1	t_{MCYC}	CC	D	MCKO Cycle Time	2(2)(3)	8	t_{CYC}
1a	t_{MCYC}	CC	D	Absolute Minimum MCKO Cycle Time	25(4)	—	ns
2	t_{MDC}	CC	D	MCKO Duty Cycle	40	60	%
3	t_{MDOV}	CC	D	MCKO Low to MDO Data Valid(5)	–0.1	0.35	t_{MCYC}
4	t_{MSEOV}	CC	D	MCKO Low to $\overline{\text{MSEO}}$ Data Valid(5)	–0.1	0.35	t_{MCYC}
6	t_{EVTOV}	CC	D	MCKO Low to $\overline{\text{EVTO}}$ Data Valid(5)	–0.1	0.35	t_{MCYC}
7	t_{EVTIPW}	CC	D	$\overline{\text{EVTI}}$ Pulse Width	4.0	—	t_{TCYC}

Table 39. Nexus debug port timing[1] (continued)

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
8	t_{EVTOPW}	CC	D	$\overline{EVTO}$ Pulse Width	1	—	t_{MCYC}
9	t_{TCYC}	CC	D	TCK Cycle Time	4[6],[7]	—	t_{CYC}
9a	t_{TCYC}	CC	D	Absolute Minimum TCK Cycle Time	100[8]	—	ns
10	t_{TDC}	CC	D	TCK Duty Cycle	40	60	%
11	t_{NTDIS}	CC	D	TDI Data Setup Time	10	—	ns
12	t_{NTDIH}	CC	D	TDI Data Hold Time	25	—	ns
13	t_{NTMSS}	CC	D	TMS Data Setup Time	10	—	ns
14	t_{NTMSH}	CC	D	TMS Data Hold Time	25	—	ns
15	—	CC	D	TDO propagation delay from falling edge of TCK	—	19.5	ns
16	—	CC	D	TDO hold time wrt TCK falling edge (minimum TDO propagation delay)	5.25	—	ns

1. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.75 V to 5.25 V with multi-voltage pads programmed to Low-Swing mode, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.
2. Achieving the absolute minimum MCKO cycle time may require setting the MCKO divider to more than its minimum setting (NPC_PCR[MCKO_DIV] depending on the actual system frequency being used.
3. This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum MCKO period specification.
4. This may require setting the MCO divider to more than its minimum setting (NPC_PCR[MCKO_DIV]) depending on the actual system frequency being used.
5. MDO, $\overline{MSEO}$, and $\overline{EVTO}$ data is held valid until next MCKO low cycle.
6. Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.
7. This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.
8. This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.

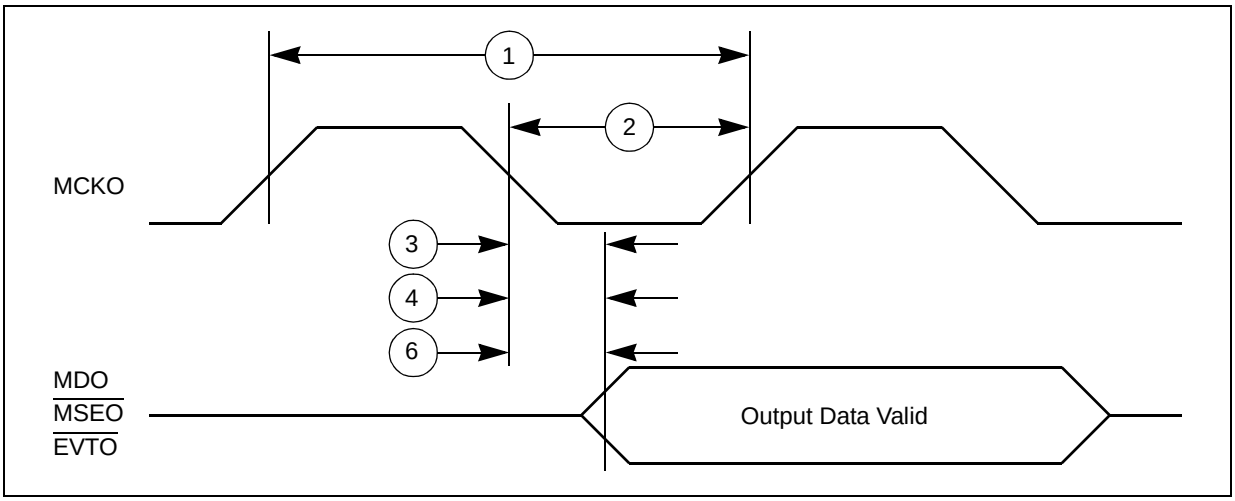


Figure 16. Nexus output timing

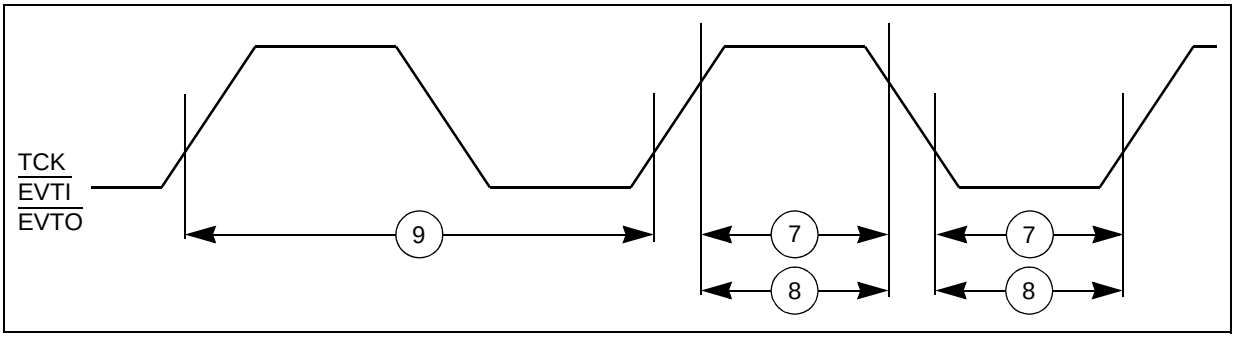


Figure 17. Nexus event trigger and test clock timings

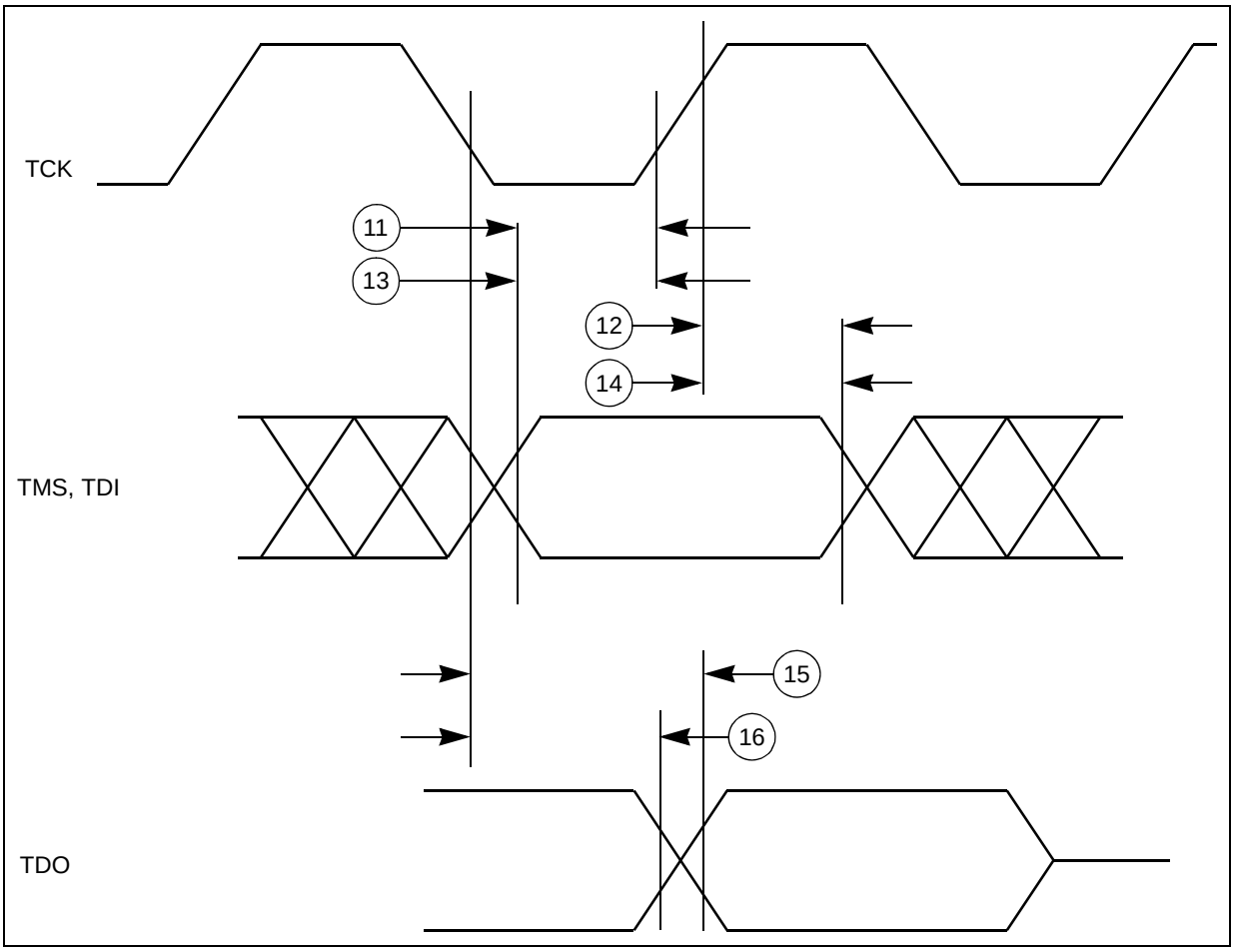


Figure 18. Nexus TDI, TMS, TDO timing

Table 40. Nexus debug port operating frequency

Package	Nexus Width	Nexus Routing	Nexus Pin Usage			Max. Operating Frequency
			MDO[0:3]	MDO[4:11]	CAL_MDO[4:11]	
LQFP176 BGA208 BGA324	Reduced port mode(1)	Route to MDO(2)	Nexus Data Out [0:3]	GPIO	GPIO	40 MHz(3)
	Full port mode(4)	Route to MDO(2)	Nexus Data Out [0:3]	Nexus Data Out [4:11]	GPIO	40 MHz(5),(6)
CSP496	Reduced port mode(1)	Route to MDO(2)	Nexus Data Out [0:3]	GPIO	GPIO	40 MHz(3)
	Full port mode(4)	Route to MDO(2)	Nexus Data Out [0:3]	Nexus Data Out [4:11]	GPIO	40 MHz(5),(6)
		Route to CAL_MDO(7)	Cal Nexus Data Out [0:3]	GPIO	Cal Nexus Data Out [4:11]	40 MHz(3)

1. NPC_PCR[FPM] = 0
2. NPC_PCR[NEXCFG] = 0
3. The Nexus AUX port runs up to 40 MHz. Set NPC_PCR[MCKO_DIV] to divide-by-two if the system frequency is greater than 40 MHz.
4. NPC_PCR[FPM] = 1
5. Set the NPC_PCR[MCKO_DIV] to divide by two if the system frequency is between 40 MHz and 80 MHz inclusive. Set the NPC_PCR[MCKO_DIV] to divide by four if the system frequency is greater than 80 MHz.
6. Pad restrictions limit the Maximum Operation Frequency in these configurations
7. NPC_PCR[NEXCFG] = 1

3.17.4 Calibration bus interface timing

Table 41. Calibration bus interface maximum operating frequency

Port width	Multiplexed mode	Pin usage			Max. operating frequency
		CAL_ADDR[12:15]	CAL_ADDR[16:30]	CAL_DATA[0:15]	
16-bit	Yes	GPIO	GPIO	CAL_ADDR[12:30] CAL_DATA[0:15]	66 MHz(1)
16-bit	No	CAL_ADDR[12:15]	CAL_ADDR[16:30]	CAL_DATA[0:15]	66 MHz(1)
32-bit	Yes	CAL_WE/BE[2:3] CAL_DATA[31]	CAL_ADDR[16:30] CAL_DATA[16:30]	CAL_ADDR[0:15] CAL_DATA[0:15]	66 MHz(1)

1. Set SIU_ECCR[EBDF] to either divide by two or divide by four if the system frequency is greater than 66 MHz.

Table 42. Calibration bus operation timing(1)

#	Symbol		C	Characteristic	66 MHz(2)		Unit
					Min	Max	
1	T_C	CC	P	CLKOUT period(3)	15.2	—	ns
2	t_{CDC}	CC	T	CLKOUT duty cycle	45%	55%	T_C
3	t_{CRT}	CC	T	CLKOUT rise time	—	(4)	ns
4	t_{CFT}	CC	T	CLKOUT fall time	—	4	ns
5	t_{COH}	CC	P	CLKOUT Posedge to Output Signal Invalid or High Z (Hold Time) CAL_ADDR[12:30] CAL_CS[0], CAL_CS[2:3] CAL_DATA[0:15] CAL_OE CAL_RD_$\overline{WR}$ CAL_TS CAL_$\overline{WE}$[0:3]/$\overline{BE}$[0:3]	1.3	—	ns
6	t_{COV}	CC	P	CLKOUT Posedge to Output Signal Valid (Output Delay) CAL_ADDR[12:30] CAL_CS[0], CAL_CS[2:3] CAL_DATA[0:15] CAL_OE CAL_RD_$\overline{WR}$ CAL_TS CAL_$\overline{WE}$[0:3]/$\overline{BE}$[0:3]	—	9	ns
7	t_{CIS}	CC	P	Input Signal Valid to CLKOUT Posedge (Setup Time) DATA[0:31]	6.0	—	ns

Table 42. Calibration bus operation timing(1) (continued)

#	Symbol		C	Characteristic	66 MHz(2)		Unit
					Min	Max	
8	t_{CIH}	CC	P	CLKOUT Posedge to Input Signal Invalid (Hold Time) DATA[0:31]	1.0	—	ns
9	t_{APW}	CC	P	ALE Pulse Width(5)	6.5	—	ns
10	t_{AAI}	CC	P	ALE Negated to Address Invalid(5)	1.5(6)	—	ns

1. Calibration bus timing specified at f_{SYS} = 150 MHz and 100 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDE} = 3 V to 3.6 V (unless stated otherwise), $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.
2. The calibration bus is limited to half the speed of the internal bus. The maximum calibration bus frequency is 66 MHz. The bus division factor should be set accordingly based on the internal frequency being used.
3. Signals are measured at 50% V_{DDE}
4. Refer to fast pad timing in *Table 35* and *Table 36* (different values for 1.8 V vs. 3.3 V).
5. Measured at 50% of ALE
6. When CAL_TS pad is used for CAL_ALE function the hold time is 1 ns instead of 1.5 ns.

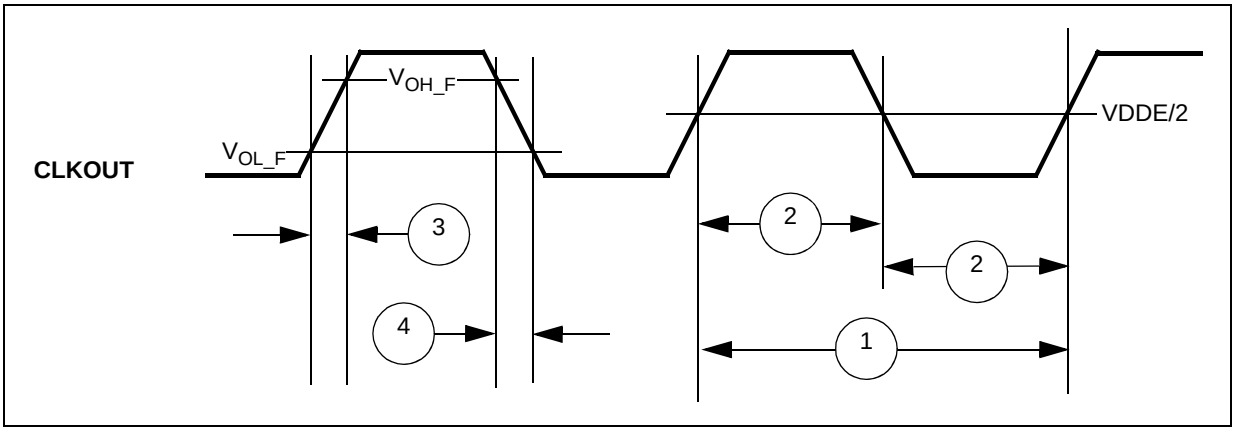


Figure 19. CLKOUT timing

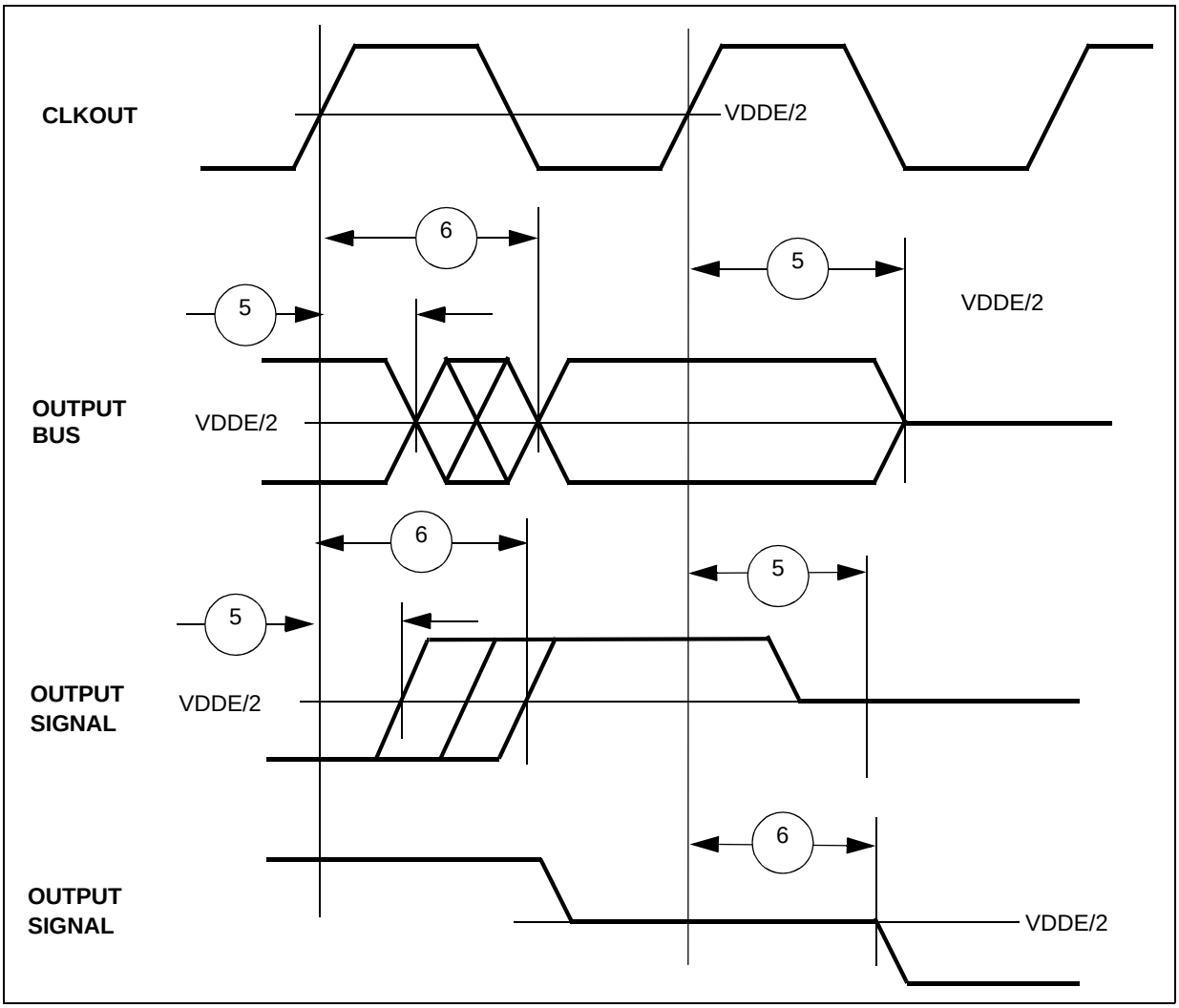


Figure 20. Synchronous output timing

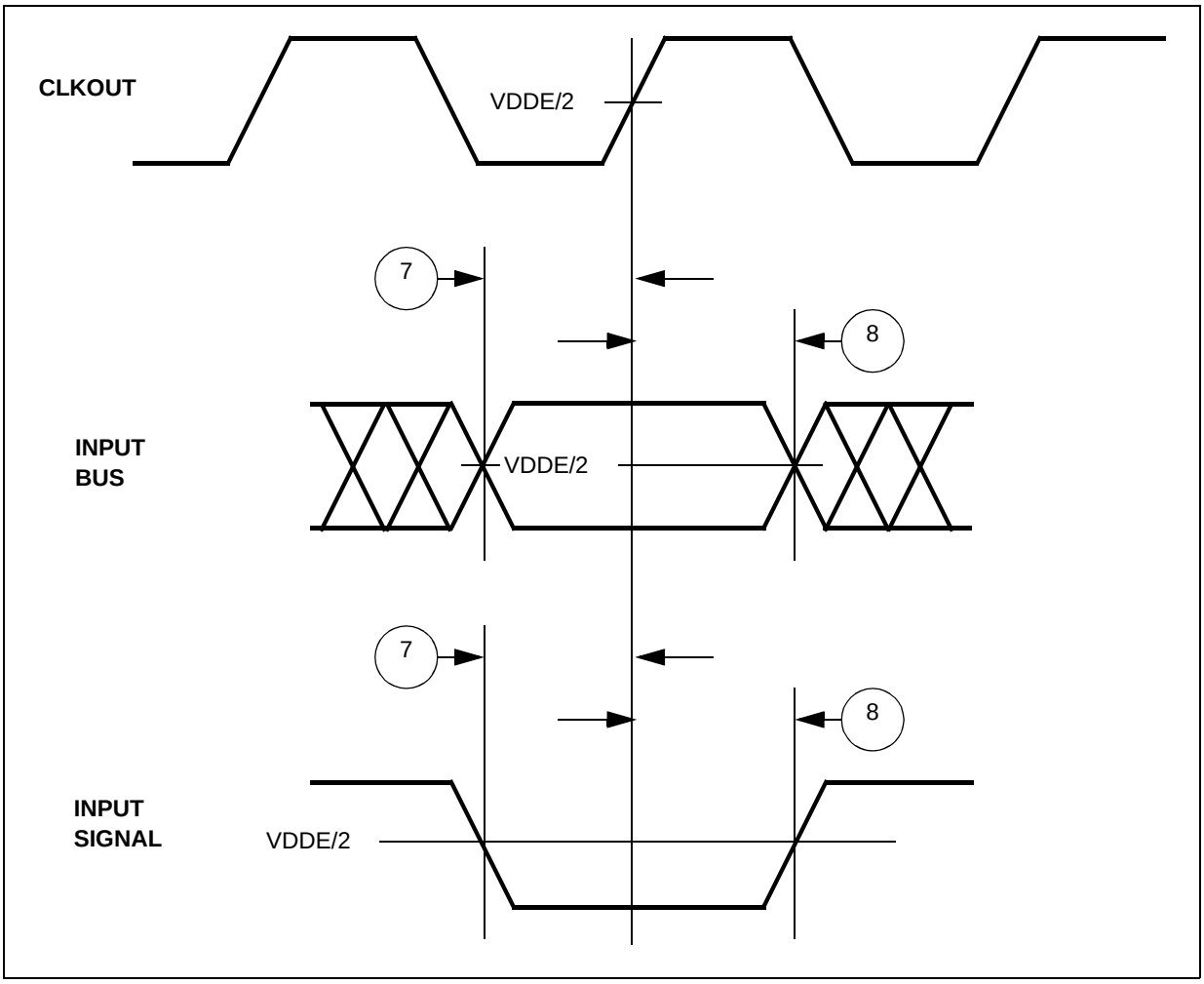


Figure 21. Synchronous input timing

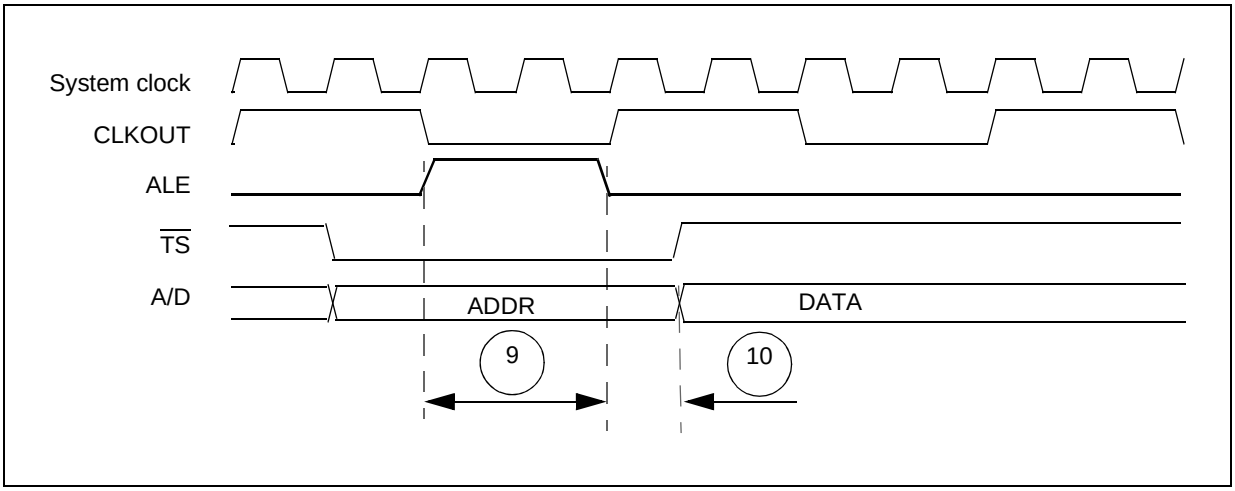


Figure 22. ALE signal timing

3.17.5 External interrupt timing (IRQ pin)

Table 43. External interrupt timing(1)

#	Symbol	Characteristic	Value		Unit
			Min	Max	
1	t_{IPWL}	IRQ Pulse Width Low	3	—	t_{CYC}
2	t_{IPWH}	IRQ Pulse Width High	3	—	t_{CYC}
3	t_{ICYC}	IRQ Edge to Edge Time(2)	6	—	t_{CYC}

1. IRQ timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 3.0 V to 5.25 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.
2. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

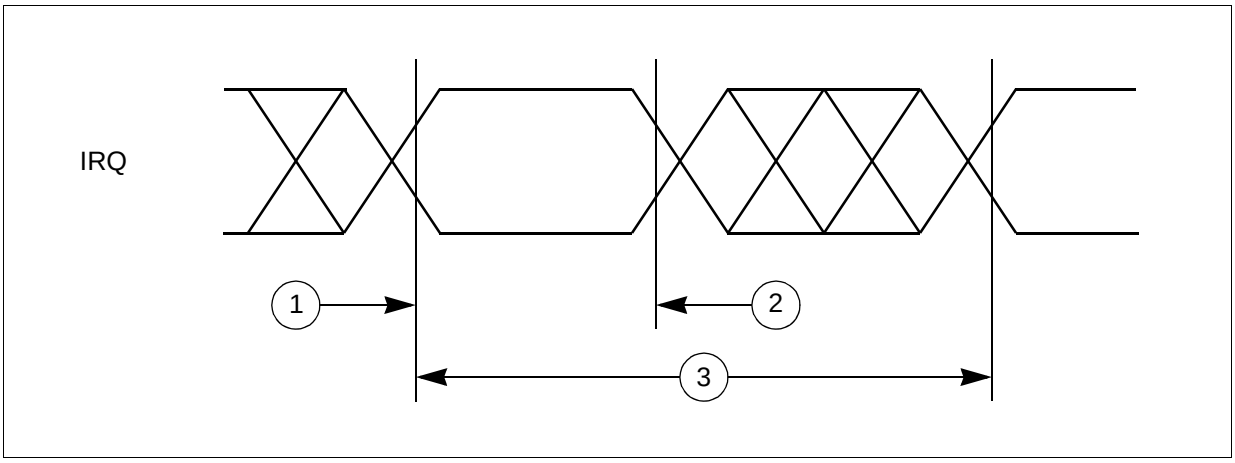


Figure 23. External interrupt timing

3.17.6 eTPU timing

Table 44. eTPU timing(1)

#	Symbol	Characteristic	Value		Unit
			Min	Max	
1	t_{ICPW}	eTPU Input Channel Pulse Width	4	—	t_{CYC}
2	t_{OCPW}	eTPU Output Channel Pulse Width(2)	2	—	t_{CYC}

1. eTPU timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 3.0 V to 5.25 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.
2. This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

3.17.7 eMIOS timing

Table 45. eMIOS timing(1)

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
1	t_{MIPW}	CC	D	eMIOS Input Pulse Width	4	—	t_{CYC}
2	t_{MOPW}	CC	D	eMIOS Output Pulse Width	1	—	t_{CYC}

1. eMIOS timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.75 V to 5.25 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.

3.17.8 DSPI timing

DSPI channel frequency support for the SPC564A70 MCU is shown in *Table 46*. Timing specifications are in *Table 47*.

Table 46. DSPI channel frequency support

System clock (MHz)	DSPI Use Mode	Maximum usable frequency (MHz)	Notes
150	LVDS	37.5	Use sysclock /4 divide ratio
	Non-LVDS	18.75	Use sysclock /8 divide ratio
120	LVDS	40	Use sysclock /3 divide ratio. Gives 33/66 duty cycle. Use DSPI configuration DBR = 0b1 (double baud rate), BR = 0b0000 (scaler value 2) and PBR = 0b01 (prescaler value 3).
	Non-LVDS	20	Use sysclock /6 divide ratio
80	LVDS	40	Use sysclock /2 divide ratio
	Non-LVDS	20	Use sysclock /4 divide ratio

Table 47. DSPI timing(1)(2)

#	Symbol		C	Characteristic	Condition	Min.	Max.	Unit
1	t_{SCK}	CC	D	SCK Cycle Time(3)(4)(5)		24.4 ns	2.9 ms	—
2	t_{CSC}	CC	D	PCS to SCK Delay(6)		22(7)	—	ns
3	t_{ASC}	CC	D	After SCK Delay(8)		21(9)	—	ns
4	t_{SDC}	CC	D	SCK Duty Cycle		$(½t_{SC}) - 2$	$(½t_{SC}) + 2$	ns
5	t_A	CC	D	Slave Access Time ($\overline{SS}$ active to SOUT driven)		—	25	ns
6	t_{DIS}	CC	D	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)		—	25	ns
7	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time		4(10)	—	ns
8	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time		5(11)	—	ns

Table 47. DSPI timing[1][2] (continued)

#	Symbol		C	Characteristic	Condition	Min.	Max.	Unit
9	t_{SUI}	CC	Data Setup Time for Inputs					
			D	Master (MTFE = 0)	V_{DDEH}=4.75–5.25 V	20	—	ns
			D		V_{DDEH}=3–3.6 V	22	—	
			D	Slave		2	—	
			D	Master (MTFE = 1, CPHA = 0)[12]		8	—	
			D	Master (MTFE = 1, CPHA = 1)	V_{DDEH}=4.75–5.25 V	20	—	
			D		V_{DDEH}=3–3.6 V	22	—	
10	t_{HI}	CC	Data Hold Time for Inputs					
			D	Master (MTFE = 0)		–4	—	ns
			D	Slave		7	—	
			D	Master (MTFE = 1, CPHA = 0)[12]		21	—	
			D	Master (MTFE = 1, CPHA = 1)		–4	—	
11	t_{SUO}	CC	Data Valid (after SCK edge)					
			D	Master (MTFE = 0)	V_{DDEH}=4.75–5.25 V	—	5	ns
			D		V_{DDEH}=3–3.6 V	—	6.3	
			D	Slave	V_{DDEH}=4.75–5.25 V	—	25	
			D		V_{DDEH}=3–3.6 V	—	25.7	
			D	Master (MTFE = 1, CPHA = 0)		—	21	
			D	Master (MTFE = 1, CPHA = 1)	V_{DDEH}=4.75–5.25 V	—	5	
			D		V_{DDEH}=3–3.6 V	—	6.3	
12	t_{HO}	CC	Data Hold Time for Outputs					
			D	Master (MTFE = 0)	V_{DDEH}=4.75–5.25 V	–5	—	ns
			D		V_{DDEH}=3–3.6 V	–6.3	—	
			D	Slave		5.5	—	
			D	Master (MTFE = 1, CPHA = 0)		3	—	
			D	Master (MTFE = 1, CPHA = 1)	V_{DDEH}=4.75–5.25 V	–5	—	
			D		V_{DDEH}=3–3.6 V	–6.3	—	

1. All DSPI timing specifications use the fastest slew rate (SRC = 0b11) on pad type pad_msr. DSPI signals using pad type of pad_ssr have an additional delay based on the slew rate. DSPI timing is specified at V_{DDEH} = 3.0 to 3.6 V, T_A = T_L to T_H, and C_L = 50 pF with SRC = 0b11.
2. Data is verified at f_{SYS} = 102 MHz and 153 MHz (100 MHz and 150 MHz + 2% frequency modulation).
3. The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two SPC564A70 devices communicating over a DSPI link.
4. The actual minimum SCK cycle time is limited by pad performance.
5. For DSPI channels using LVDS output operation, up to 40 MHz SCK cycle time is supported. For non-LVDS output, maximum SCK frequency is 20 MHz. Appropriate clock division must be applied.
6. The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK].
7. Timing met when PCSSCK = 3 (01), and CSSCK = 2 (0000)

8. The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC].
9. Timing met when ASC = 2 (0000), and PASC = 3 (01)
10. Timing met when PCSSCK = 3
11. Timing met when ASC = 3
12. This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b10.

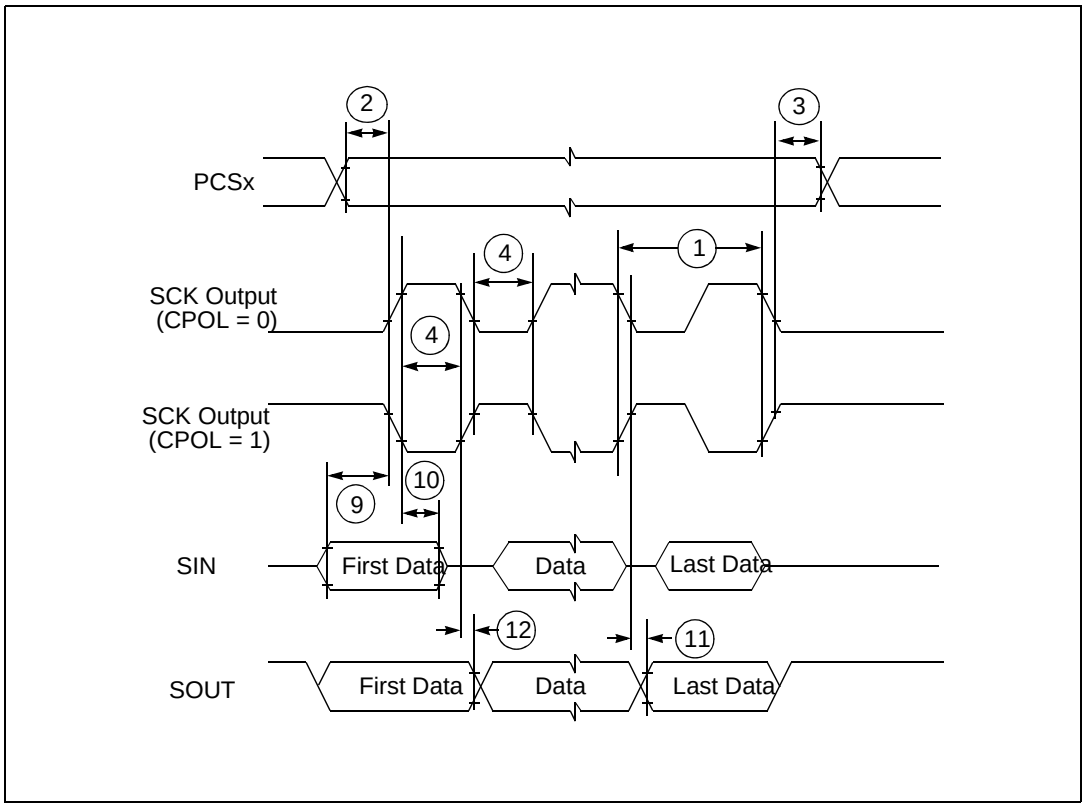


Figure 24. DSPI classic SPI timing (master, CPHA = 0)

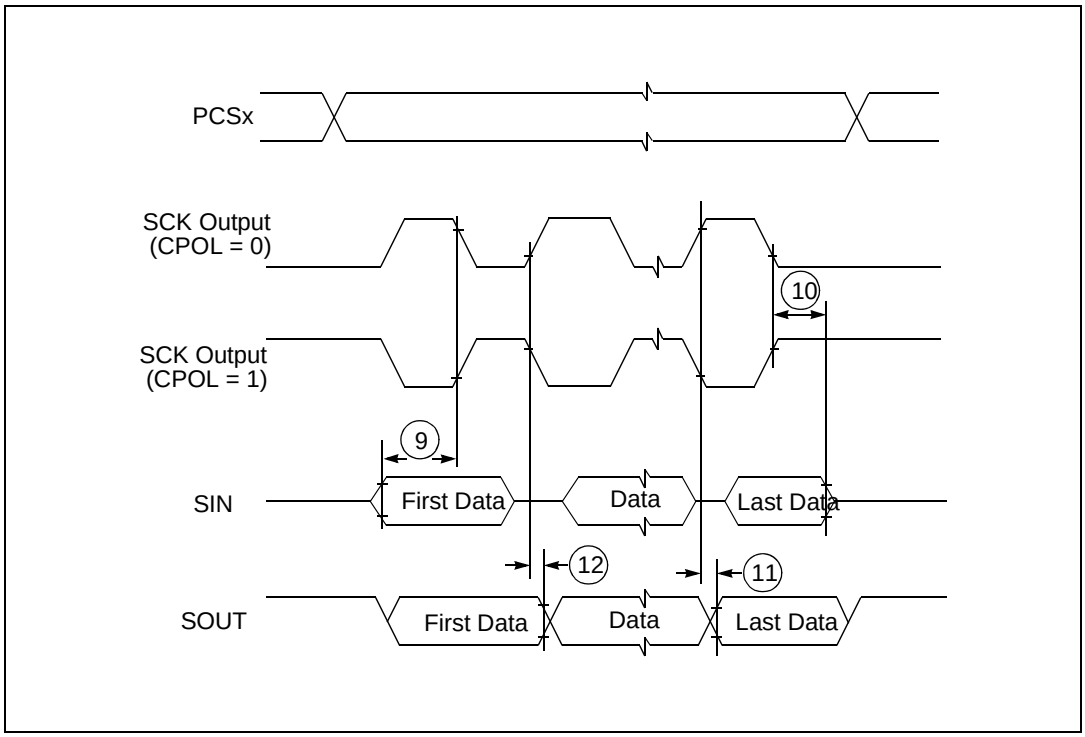


Figure 25. DSPI classic SPI timing (master, CPHA = 1)

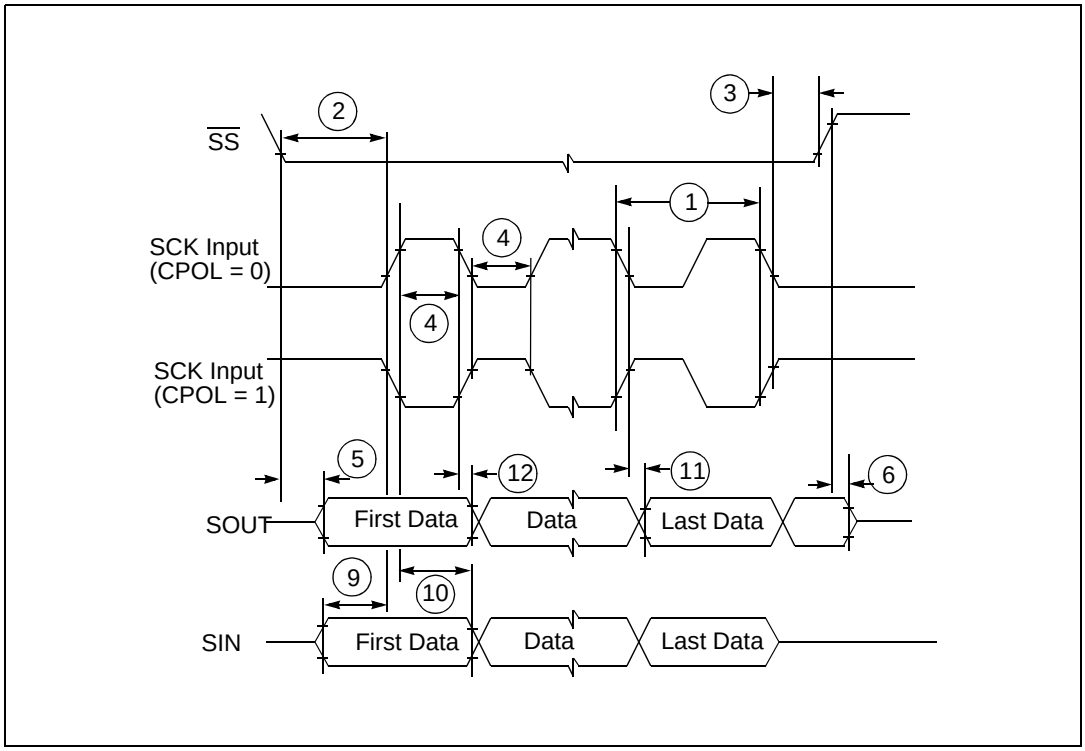


Figure 26. DSPI classic SPI timing (slave, CPHA = 0)

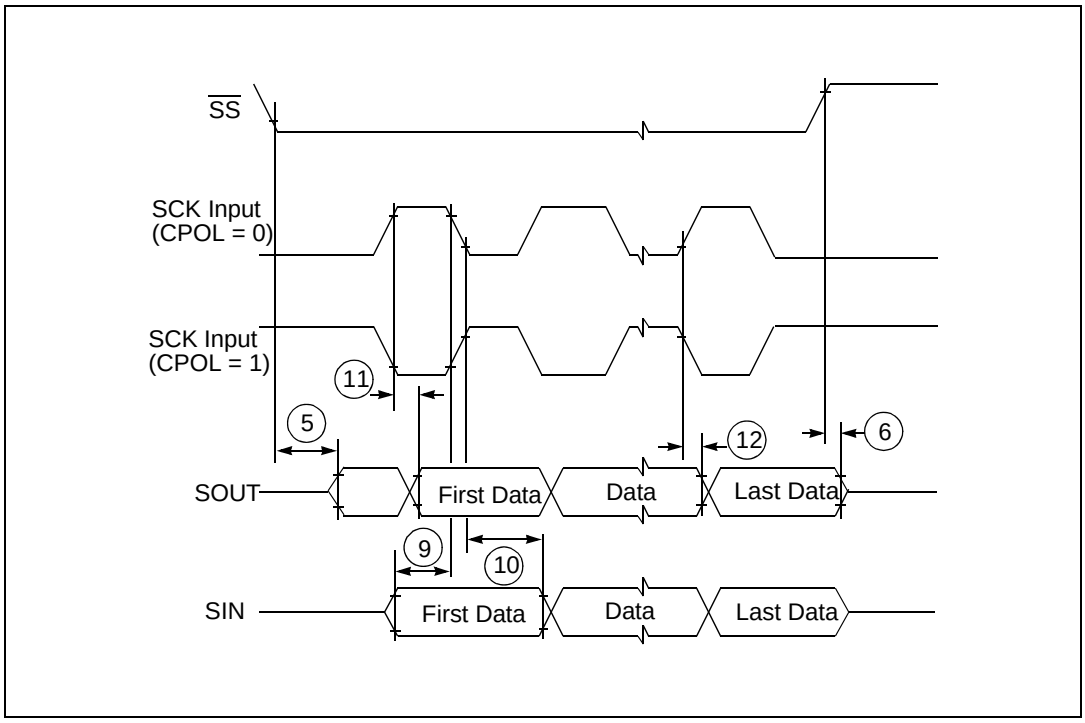


Figure 27. DSPI classic SPI timing (slave, CPHA = 1)

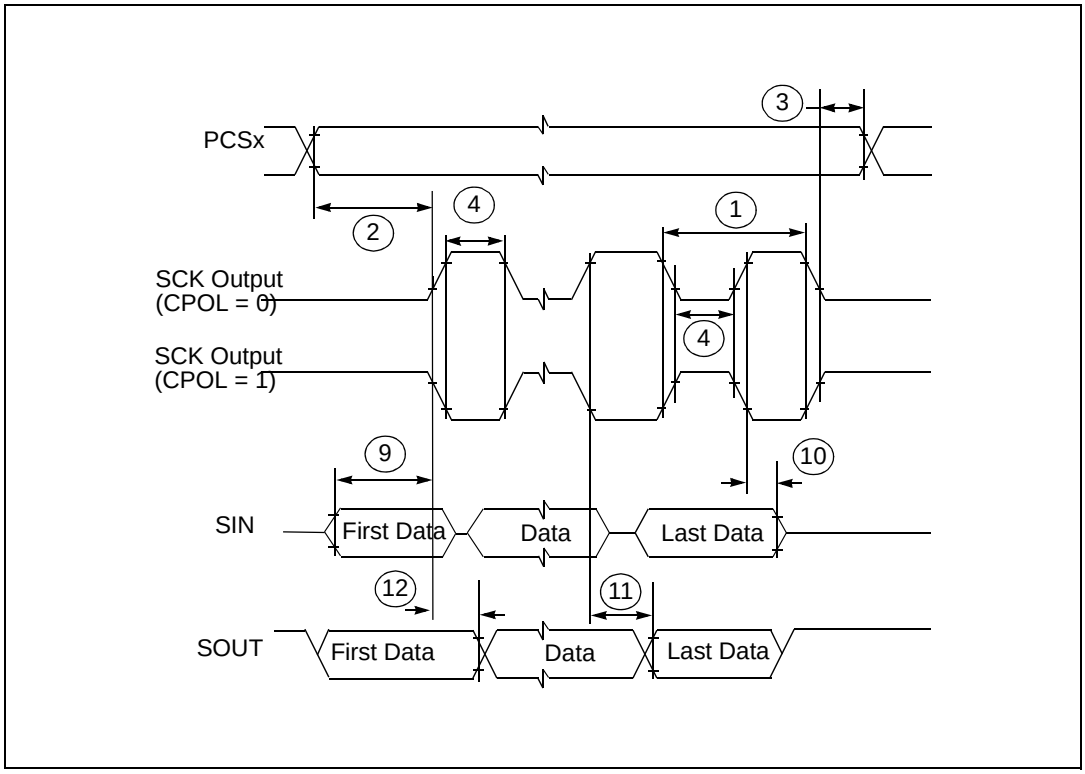


Figure 28. DSPI modified transfer format timing (master, CPHA = 0)

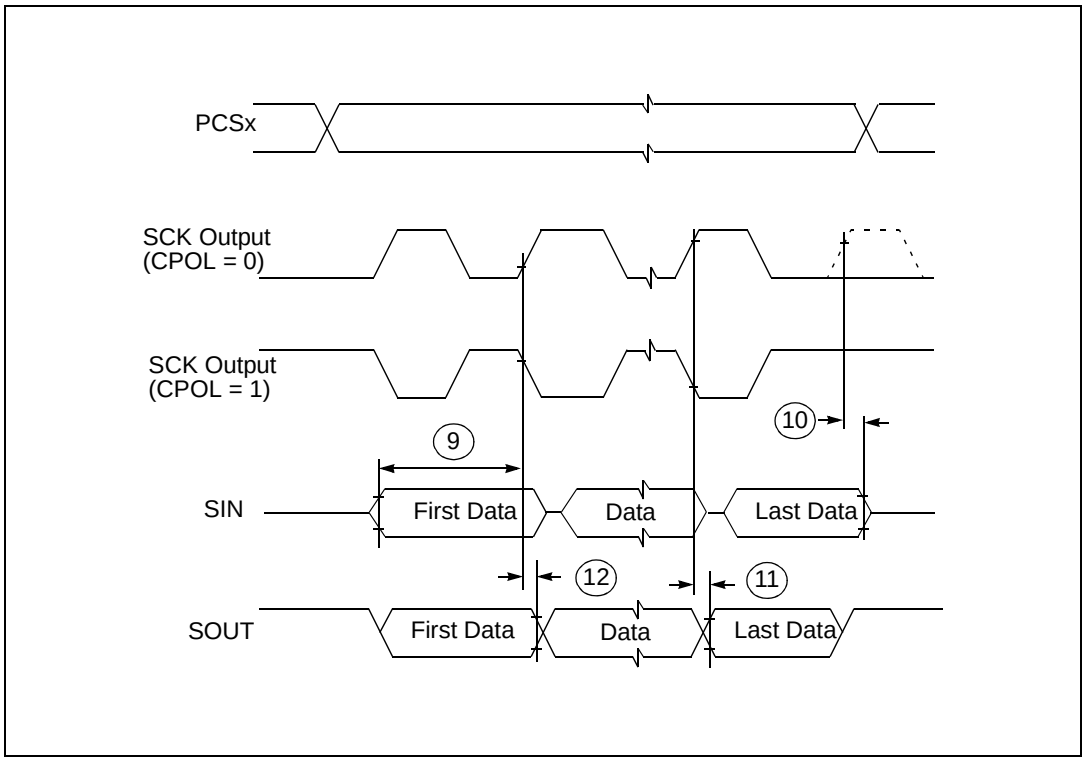


Figure 29. DSPI modified transfer format timing (master, CPHA = 1)

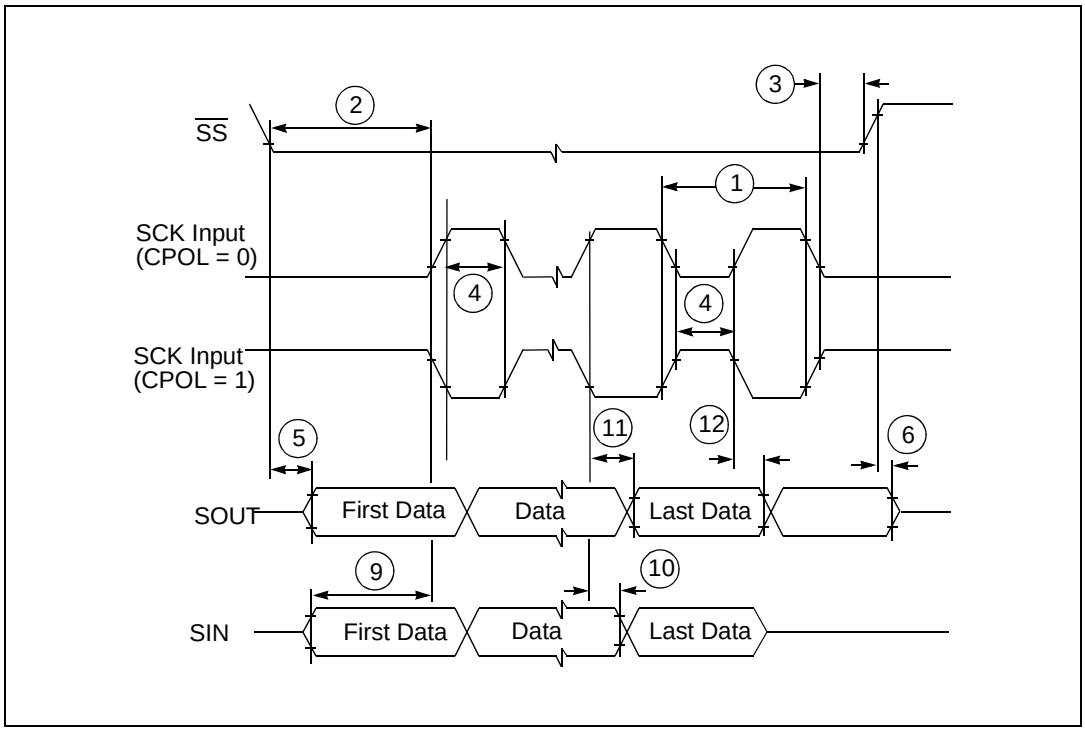


Figure 30. DSPI modified transfer format timing (slave, CPHA = 0)

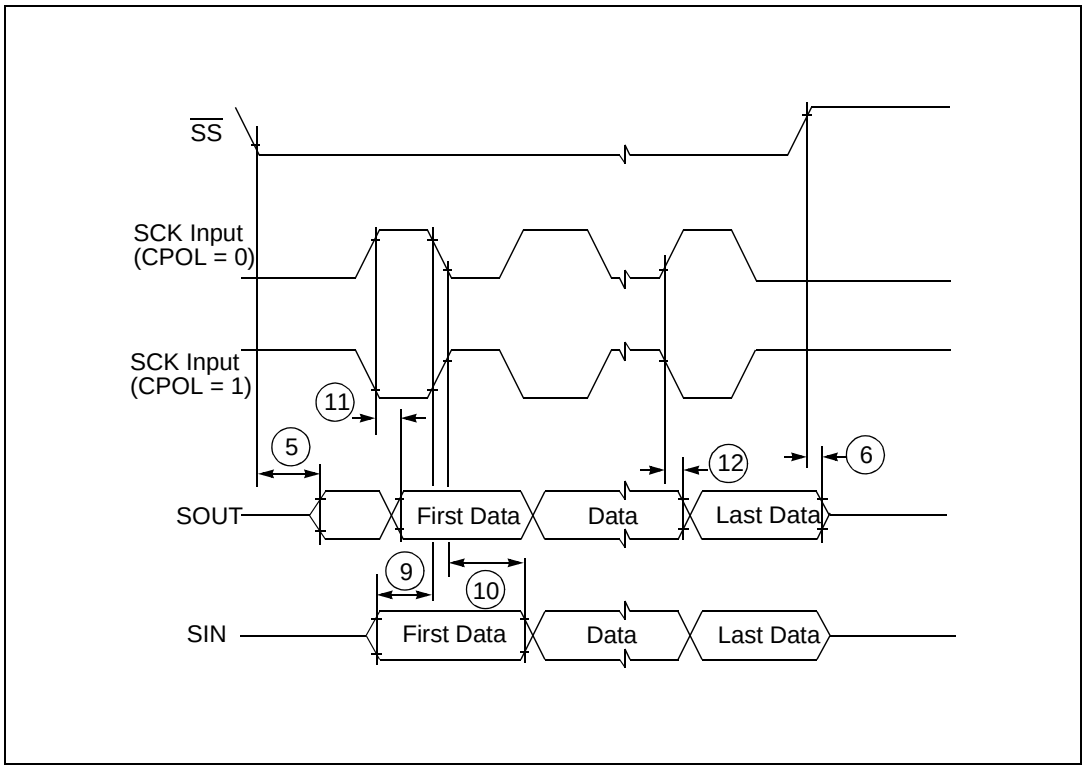


Figure 31. DSPI modified transfer format timing (slave, CPHA = 1)

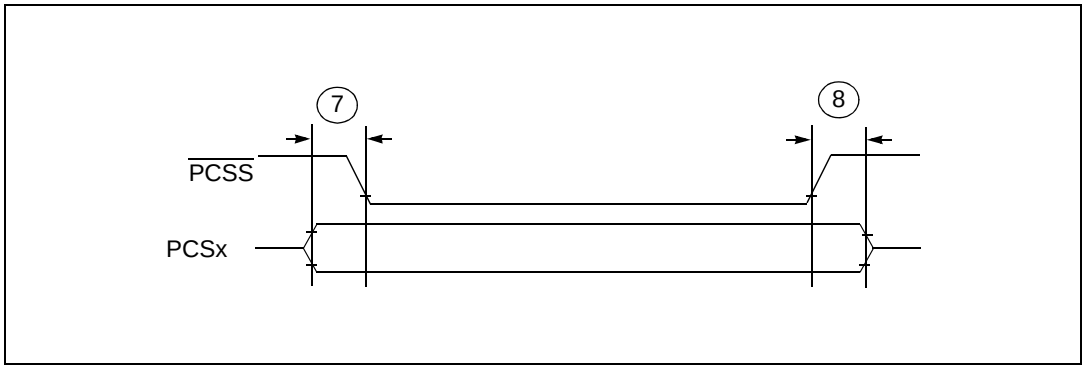


Figure 32. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

3.17.9 eQADC SSI timing

Table 48. eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V)(1)

CLOAD = 25 pF on all outputs. Pad drive strength set to maximum.								
#	Symbol		C	Rating	Value			Unit
					Min	Typ	Max	
1	f_{FCK}	CC	D	FCK Frequency (2)(3)	1/17		1/2	f_{SYS_CLK}
1	t_{FCK}	CC	D	FCK Period (t_{FCK} = 1/ f_{FCK})	2		17	t_{SYS_CLK}

Table 48. eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V)(1) (continued)

CLOAD = 25 pF on all outputs. Pad drive strength set to maximum.								
#	Symbol		C	Rating	Value			Unit
					Min	Typ	Max	
2	t_{FCKHT}	CC	D	Clock (FCK) High Time	t_{SYS_CLK} – 6.5		9 * t_{SYS_CLK} + 6.5	ns
3	t_{FCKLT}	CC	D	Clock (FCK) Low Time	t_{SYS_CLK} – 6.5		8 * t_{SYS_CLK} + 6.5	ns
4	t_{SDS_LL}	CC	D	SDS Lead/Lag Time	–7.5		7.5	ns
5	t_{SDO_LL}	CC	D	SDO Lead/Lag Time	–7.5		7.5	ns
6	t_{DVFE}	CC	D	Data Valid from FCK Falling Edge (t_{FCKLT} + t_{SDO_LL})	1			ns
7	t_{EQ_SU}	CC	D	eQADC Data Setup Time (Inputs)	22			ns
8	t_{EQ_HO}	CC	D	eQADC Data Hold Time (Inputs)	1			ns

1. SSI timing specified at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.75 V to 5.25 V, T_A = T_L to T_H, and C_L = 50 pF with SRC = 0b00.
2. Maximum operating frequency is highly dependent on track delays, master pad delays, and slave pad delays.
3. FCK duty is not 50% when it is generated through the division of the system clock by an odd number.

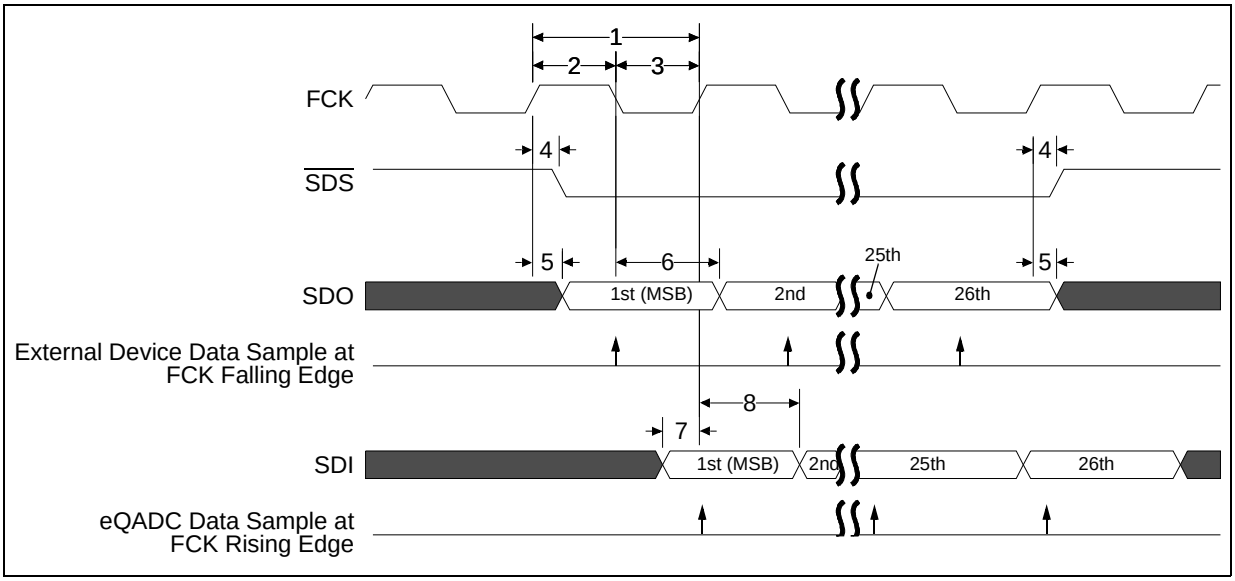


Figure 33. eQADC SSI timing

3.17.10 FlexCAN system clock source

Table 49. FlexCAN engine system clock divider threshold

#	Symbol	Characteristic	Value	Unit
1	f_{CAN_TH}	FlexCAN engine system clock threshold	100	MHz

Table 50. FlexCAN engine system clock divider

System frequency	Required SIU_SYSDIV[CAN_SRC] value
$\leq f_{CAN\_TH}$	0(1),(2)
$> f_{CAN\_TH}$	1(2)(3)

1. Divides system clock source for FlexCAN engine by 1
2. System clock is only selected for FlexCAN when CAN_CR[CLK_SRC] = 1
3. Divides system clock source for FlexCAN engine by 2

4 Packages

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.2 Package mechanical data

4.2.1 LQFP176

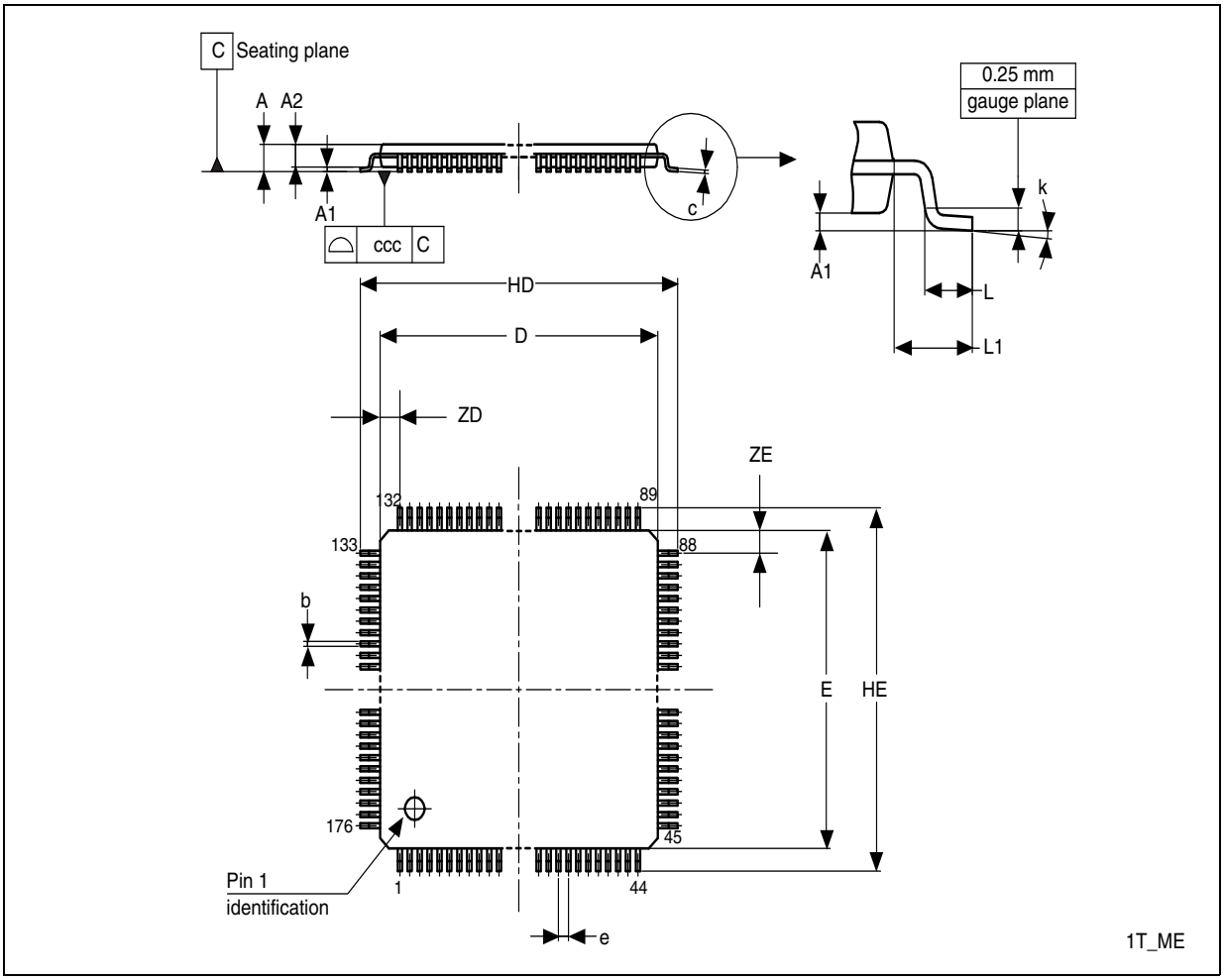


Figure 34. LQFP176 package mechanical drawing

Table 51. LQFP176 mechanical data[1]

Symbol	mm			inches[2]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.063
A1	0.050	—	0.150	0.002	—	—
A2	1.350	—	1.450	0.053	—	0.057
b	0.170	—	0.270	0.007	—	0.011
C	0.090	—	0.200	0.004	—	0.008
D	23.900	—	24.100	0.941	—	0.949
E	23.900	—	24.100	0.941	—	0.949
e	—	0.500	—	—	0.020	—
HD	25.900	—	26.100	1.020	—	1.028
HE	25.900	—	26.100	1.020	—	1.028
L[3]	0.450	—	0.750	0.018	—	0.030
L1	—	1.000	—	—	0.039	—
ZD	—	1.250	—	—	0.049	—
ZE	—	1.250	—	—	0.049	—
k	0 °	—	7 °	0 °	—	7 °
ccc	—	—	0.080	—	—	0.003

1. Controlling dimension: millimeter
2. Values in inches are converted from mm and rounded to 4 decimal digits.
3. L dimension is measured at gauge plane at 0.25 above the seating plane.

4.2.2 BGA208(c)

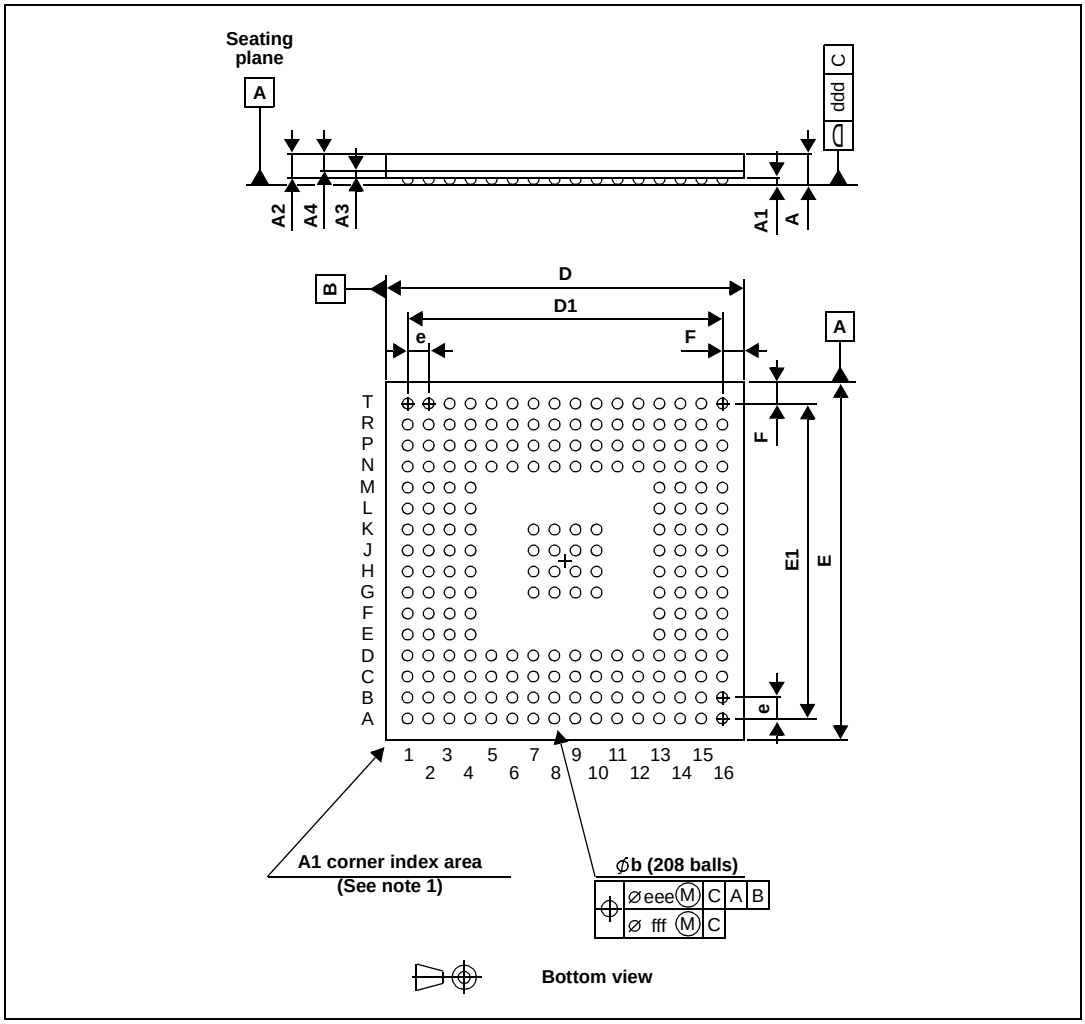


Figure 35. LBGA208 package mechanical drawing

1. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug.
A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

Table 52. LBGA208 mechanical data(1)

Symbol	mm			inches(2)		
	Min	Typ	Max	Min	Typ	Max
A(3)	—	—	1.70	—	—	1.55
A1	0.30	—	—	0.45	0.50	0.55

c. LBGA208 is available upon specific request. Please contact your ST sales office for details.

Table 52. LBGA208 mechanical data[1] (continued)

Symbol	mm			inches[2]		
	Min	Typ	Max	Min	Typ	Max
A2	—	1.085	—	1.03	1.085	1.14
A3	—	0.30	—	0.26	0.30	0.34
A4	—	—	0.80	0.77	0.785	0.80
b[4]	0.50	0.60	0.70	0.55	0.60	0.65
D	16.80	17.00	17.20	16.90	17.00	17.10
D1	—	15.00	—	—	15.00	—
E	16.80	17.00	17.20	16.90	17.00	17.10
E1	—	15.00	—	—	15.00	—
e	—	1.00	—	—	1.00	—
F	—	1.00	—	—	1.00	—
ddd	—	—	0.20	—	—	0.0079
eee[5]	—	—	0.25	—	—	0.0098
fff[6],[7]	—	—	0.10	—	—	0.0039

1. Controlling dimension: millimeter
2. Values in inches are converted from mm and rounded to 4 decimal digits.
3. LBGA stands for **L**ow profile **B**all **G**rid **A**rray.
   - Low profile: The total profile height (Dim A) is measured from the seating plane to the top of the component
   - The maximum total package height is calculated by the following methodology:
   A2 Typ + A1 Typ +√ ($A1^2$ + $A3^2$ + $A4^2$ tolerance values)
   - Low profile: 1.20 mm < A ≤ 1.70 mm
4. The typical ball diameter before mounting is 0.60 mm.
5. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
6. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.
7. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug. A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

4.2.3 PBGA324

Figure 36. PBGA324 package mechanical drawing

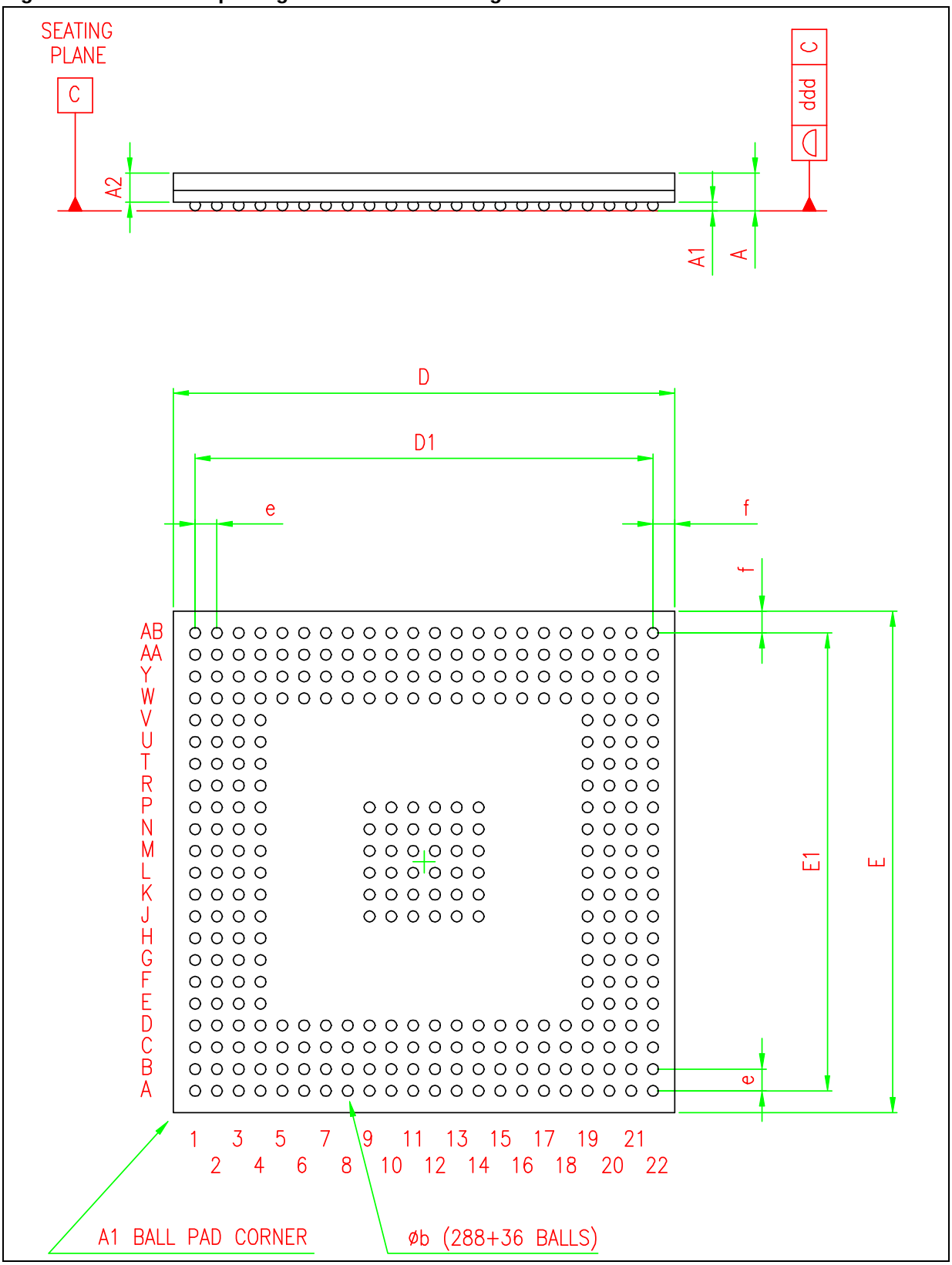


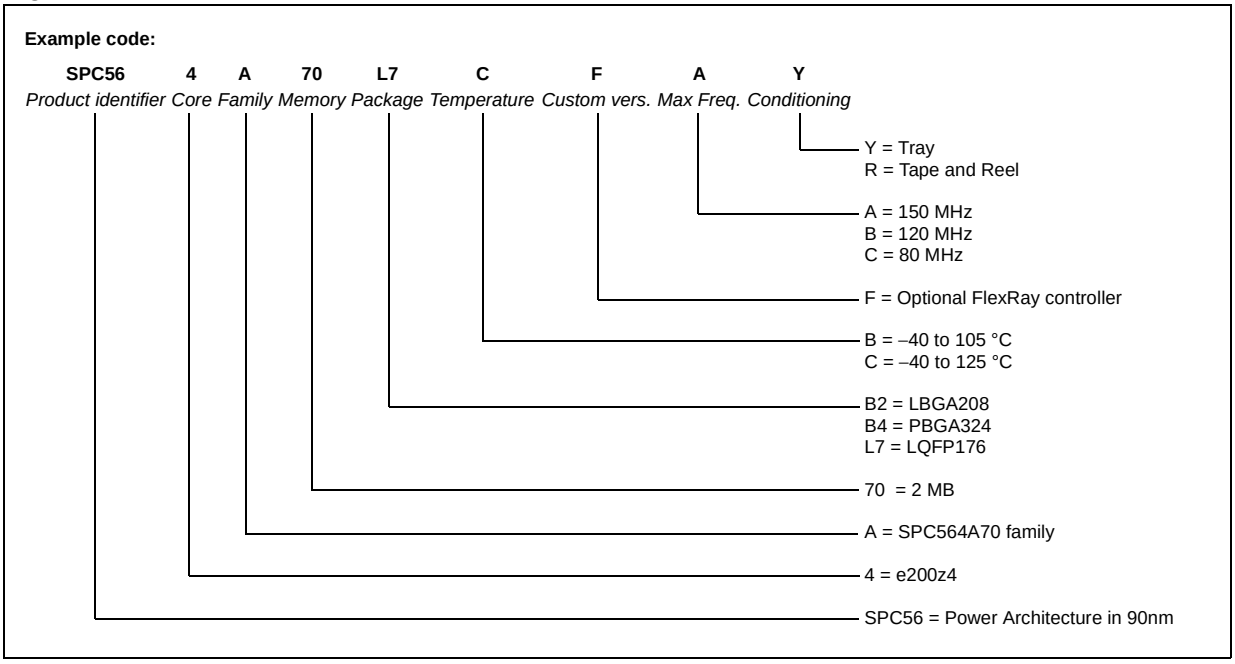
Table 53. PBGA324 package mechanical data

Symbol	Databook (mm)			Drawing (mm)		
	Min	Typ	Max	Min	Typ	Max
A(1) (2) (3)	—	1.720	—	1.620	1.720	1.820
A1	0.270	—	—	0.350	0.400	0.450
A2	—	1.320	—	—	1.320	—
b	0.550	0.6000	0.650	0.550	0.600	0.650
D	22.80	23.00	23.200	22.900	23.000	23.100
D1	—	21.00	—	—	21.000	—
E	22.800	23.000	23.200	22.900	23.000	23.100
E1	—	21.000	—	—	21.000	—
e	0.950	1.000	1.050	0.950	1.000	1.050
f	0.875	1.000	1.125	0.875	1.000	1.125
ddd	—	—	0.200	—	—	0.200

1. Max mounted height is 1.77 mm. Based on 0.35 mm ball pad diameter. Solder paste is 0.15 mm thickness and 0.35 mm diameter.
2. PBGA stands for Plastic Ball Grid Array.
3. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug. A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1corner. Exact shape of each corner is optional.

5 Ordering information

Figure 37. Product code structure



6 Revision history

Table 54 summarizes customer facing revisions to this document.

Table 54. Document revision history

Date	Revision	Changes
07-Oct-2010	1	Initial release.
11-Apr-2012	2	*Figure 1 (SPC564A70 series block diagram)*, added ECSM block and its definition in the elegend. *Table 3 (SPC564A70 series block summary)*, added the following blocks: REACN, SIU, ECSM, FMPLL, PIT and SWT. Updated *Table 9 (Absolute maximum ratings)* In *3, Electrical characteristics*, deleted the “Recommended operating conditions” subsection. *Table 15 (PMC operating conditions and external regulators supply voltage)*, removed minimum value of V_{DDREG} and its footnote. Updated *Table 16 (PMC electrical characteristics)* Updated *Section 3.6.1, Regulator example* Updated *Table 21 (DC electrical specifications)* *Figure 8 (Core voltage regulator controller external components preferred configuration)*, added “T1” label to indicate the transistor. *Table 21 (DC electrical specifications)*, changed maximum value of V_{IL_LS} to 0.9, was 1.1 *Table 22 (I/O pad average IDDE specifications)*, in the V_{DDE} column changed all 5.5 to 5.25 *Table 25 (DSPI LVDS pad specification)*: Renamed V_{OC}, was V_{OD} Updated minimum and maximum value of V_{OC} deleted all footnote *Table 27 (Temperature sensor electrical characteristics)*, updated minimum and maximum value of accuracy Updated *Section 3.12, eQADC electrical characteristics* Added *Section 3.13, Configuring SRAM wait states* Updated *Table 32 (APC, RWSC, WWSC settings vs. frequency of operation)* Updated *Table 33 (Flash program and erase specifications)* *Table 32 (APC, RWSC, WWSC settings vs. frequency of operation)*, changed all values in the WWSC column to 0b01. Updated *Table 33 (Flash program and erase specifications)* *Table 34 (Flash EEPROM module life)*: updated temperature value in the Retention description (was 150 °C, is 85 °C) added values for Retention *Table 35 (Pad AC specifications (VDDE = 4.75 V))*: changed maximum value of Medium to 12/12 changed maximum value of Slow to 20/20 Updated *Table 36 (Pad AC specifications (VDDE = 3.0 V))* *Table 38 (JTAG pin AC electrical characteristics)*: changed all parameter classification to D changed minumum value of t_{TMSS}, t_{TDIS} to 10 Updated *Table 39 (Nexus debug port timing)*

Table 54. Document revision history (continued)

Date	Revision	Changes
11-Apr-2012	2 (continued)	Added *Table 40 (Nexus debug port operating frequency)* *Table 40 (Nexus debug port operating frequency)*, added a footnote near the value of t_{AAI} *Table 45 (eMIOS timing)*: changed minumum value of t_{MOPW} to 1 removed the footnote of t_{MOPW} Merged "DSPI timing (V_{DDEH} = 3.0 to 3.6 V)" and "DSPI timing (V_{DDEH} = 4.5 to 5.5V)" tables into *Table 47 (DSPI timing)* and changed all parameter classification to D *Table 48 (eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V))* changed all parameter classification to D *Table 52 (LBGA208 mechanical data)* deleted Notes column and moved all footnote next to relative references *Table 53 (PBGA324 package mechanical data)* deleted Notes column and moved all footnote next to relative references [[ST_Specific]] *Table 12 (Thermal characteristics for 324-pin PBGA)*, updated values In *Section 3.6, Power management control (PMC) and power on reset (POR) electrical specifications*, deleted the "Voltage regulator controller (V_{RC}) electrical specifications" Updated *Section 4.2.1, LQFP176*
06-Jun-2012	3	Minor editorial changes and improvements throughout. In *Section 2.4, Signal summary*, *Table 4 (SPC564A70 signal properties)*, updated the following properties for the Nexus pins: – Added a footnote to the "Nexus" title for this pin group. – Added a footnote to the "Name" entry for $\overline{\text{EVTO}}$. – Updated the "Status During reset" entry for $\overline{\text{EVTO}}$. In *Section 3.2, Maximum ratings*, *Table 9 (Absolute maximum ratings)*, removed the "TBD - To be defined" footnote. In *Section 3.8, DC electrical specifications*, *Table 21 (DC electrical specifications)*, removed the "TBD - To be defined" footnote. In *Section 3.9, I/O pad current specifications*, *Table 22 (I/O pad average IDDE specifications)*: – Updated values and replaced TBDs with numerical data. – Removed the "TBD - To be defined" footnote. In *Section 3.9.1, I/O pad VRC33 current specifications*, *Table 23 (I/O pad VRC33 average IDDE specifications)*: – Updated values and replaced TBDs with numerical data. – Removed the "TBD - To be defined" footnote. In *Section 3.14, Platform flash controller electrical characteristics*, *Table 32 (APC, RWSC, WWSC settings vs. frequency of operation)*, removed the "TBD - To be defined" footnote. In *Table 54 (Document revision history)*, removed extraneous text from the Revision 2 entry.
18-Sep-2013	4	Updated Disclaimer.

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