

**FEATURES**

- Fully Integrated Signal Conditioning Transceiver
- 1.0–1.3 Gbps Operation
- Low Power CMOS Design (<300 mW)
- High Differential Output Voltage Swing (1600 mVp-p typical)
- 400 mVp-p Differential Input Sensitivity
- High Input Jitter Tolerance 0.606 UI
- Single 1.8 V Power Supply
- 2.5 V Tolerant Control Inputs
- Differential VML Transmit Outputs With No External Components Necessary

- No External Filter Components Required for PLLs
- Supports Loop-Back Modes
- Temperature Rating 0°C to 70°C
- Small Footprint 4 mm × 4 mm 24-Lead QFN Package

**APPLICATIONS**

- Resynchronization in Both Directions for 1.25 Gbps Links
- Repeater for 1.0625 Gbps Applications

**DESCRIPTION**

TLK1002A is a single-chip dual signal conditioning transceiver.

This chip supports data rates from 1.0 Gbps up to 1.3 Gbps. An on-chip clock generation phase-locked loop (PLL) generates the required half-rate clock from an externally applied reference clock. This reference clock equals approximately one tenth of the data rate. It may be off frequency from both received data streams by up to  $\pm 200$  ppm.

Both data paths are implemented identical. The implemented input buffers provide an input sensitivity of 400 mVp-p differential.

The data paths tolerate up to 0.606 UI total input jitter. Signal retiming is performed by means of phase-locked loop (PLL) circuits. The retimed output signals are fed to VML output buffers, which provide output amplitudes of typical 1600mVp-p differential across the external  $2 \times 50 \Omega$  load.

TLK1002A only requires a single 1.8 V supply voltage. Robust design avoids the necessity of special off-chip supply filtering.

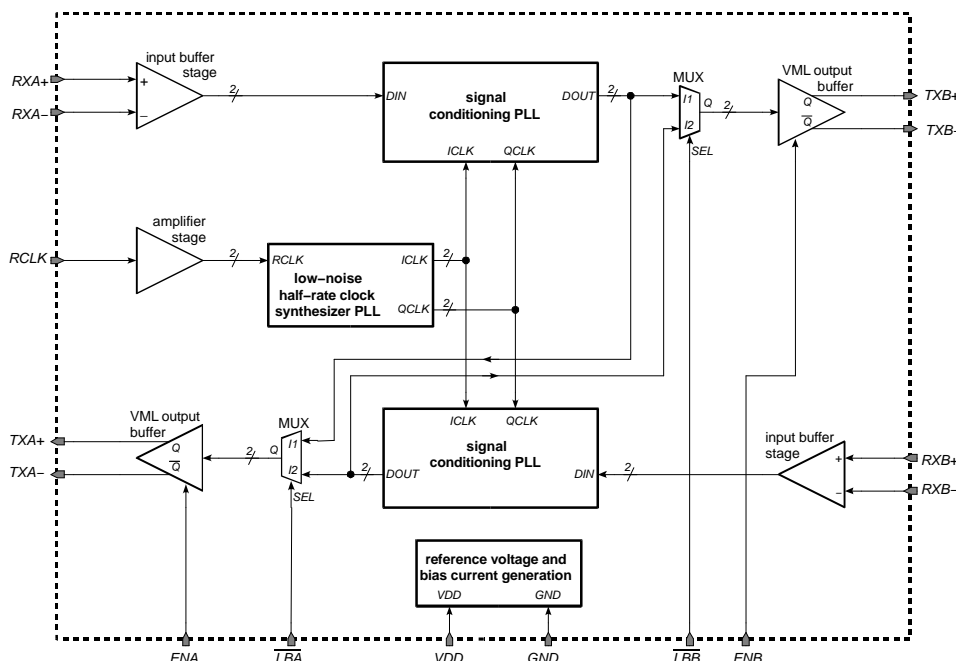
Advanced low power CMOS design leads to low power consumption.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## BLOCK DIAGRAM

A simplified block diagram of the TLK1002A circuit is shown in Figure 1. The main circuit parts are described in detail below.



**Figure 1. Simplified Block Diagram of the TLK1002A Transceiver**

## DATA PATHS

The serial input data streams are connected to the input ports  $RXA+/RXA-$  or  $RXB+/RXB-$  respectively. The input stages provide on-chip differential 100- $\Omega$  termination. The outputs of the input buffer stages are connected to the signal conditioning PLL circuits.

The PLL output signals are fed to multiplexer (MUX) stages, which are used to redirect the data signals if loop back mode is selected.

The multiplexer stages are connected to the output ports  $TXB+/TXB-$  or  $TXA+/TXA-$ , respectively, by means of VML output buffer stages. To enable the output buffer stages,  $ENA$  and  $ENB$ , which are internally pulled up, must be at high level ( $VDD$ ).

The loop back modes are enabled by means of the control-inputs  $\overline{LBA}$  and  $\overline{LBB}$ , which are implemented as active low inputs with integrated pull-up resistors. If  $\overline{LBA}$  is set to low level, the input data applied to the input port  $RXA+/RXA-$  is retimed and fed to both output ports  $TXB+/TXB-$  and  $TXA+/TXA-$ . If  $\overline{LBB}$  is pulled low, the retimed input data signal applied to  $RXB+/RXB-$  is available at  $TXA+/TXA-$  and  $TXB+/TXB-$ .

If a logic low signal is applied to both loop back control inputs the retimed signal connected to  $RXA+/RXA-$  appears at  $TXA+/TXA-$ , while the retimed signal applied to  $RXB+/RXB-$  is fed to  $TXB+/TXB-$ .

## DATA PATHS (continued)

### LOW-NOISE HALF-RATE CLOCK GENERATION PLL

In order to achieve the low power requirements, an on-chip half-rate clock synthesizer PLL is implemented. It generates the internally used inphase and quadrature clock signals with 5 times the reference clock frequency.

The required reference clock frequency equals approximately one tenth of the data rate. It may be off frequency from both transmit and receive data streams by up to  $\pm 200$  ppm.

A valid reference clock must be connected to the RCLK pin to ensure proper operation. In case of a clock absence of up to 4 cycles during clock switch over the CDR will independently re-acquire lock (i.e., without the need of any reset signal), however during re-locking erroneous bits will be transmitted for a limited period of time.

The reference clock may contain jitter, in the order of about 80 ps<sub>p-p</sub>. However, the jitter components below 10 MHz, which is the bandwidth of the clock generation PLL, must not exceed 40 ps<sub>p-p</sub>.

Increased reference clock jitter leads to increased output jitter as well as to reduced jitter tolerance.

### CONTROL INPUTS

TLK1002A provides a total of four control inputs, which activate the VML output buffer stages and enable the loop-back modes.

These control inputs may be driven from circuits using a different supply voltage. Thus, 2.5 V tolerance is mandatory at these pins. All control inputs provide on-chip pull-up resistors to *VDD*.

### REFERENCE VOLTAGE AND BIAS CURRENT GENERATION

The TLK1002A transceiver is supplied by a 1.8 V  $\pm 5\%$  supply voltage connected to *VDD*. The voltage is referred to ground (*GND*).

From this voltage all required reference voltages and bias currents are derived by means of the reference voltage and bias current generation block.

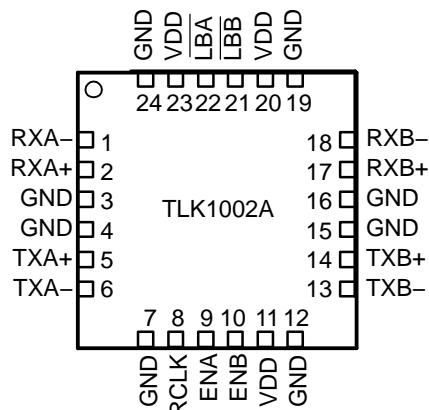
### PACKAGE

For the TLK1002A a small footprint 4 mm × 4 mm 24-lead QFN package is used, with a lead pitch of 0.5 mm. The pin out is shown below.

The thermal resistance of the package is about 47°C/W. At a total power consumption of 0.3 W assuming an ambient temperature of 70°C, the maximum junction temperature is below 85°C.

### PIN OUT

#### RGE PACKAGE (TOP VIEW)



### TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NO.	NAME		
1	RXA–	In	Inverted data input A. On board AC coupled. On-chip 100-Ω differential terminated to RXA+.
2	RXA+	In	Non-inverted data input A. On board AC coupled. On-chip 100-Ω differential terminated to RXA–.
3, 4, 7, 12, 15, 16, 19, 24, EP	GND	Supply	Circuit ground. The exposed die pad (EP) must be grounded.
5	TXA+	VML-out	Retimed non-inverted data output A. On board AC coupled.
6	TXA–	VML-out	Retimed inverted data output A. On board AC coupled.
8	RCLK	CMOS-in	Reference clock input. Self biased for AC coupling. This input is 2.5 V tolerant.
9	ENA	CMOS-in	Enable A, on-chip pulled up to VDD. When set to high level, the VML output buffer driving the TXA+/TXA– port is enabled. This input is 2.5 V tolerant.
10	ENB	CMOS-in	Enable B, on-chip pulled up to VDD. When set to high level, the VML output buffer driving the TXB+/TXB– port is enabled. This input is 2.5 V tolerant.
11, 20, 23	VDD	Supply	1.8 V ±5% supply voltage
13	TXB–	VML-out	Retimed inverted data output B. On board AC coupled.
14	TXB+	VML-out	Retimed non-inverted data output B. On board AC coupled.
17	RXB+	In	Non-inverted data input B. On board AC coupled. On-chip 100-Ω differential terminated to RXB–.
18	RXB–	In	Inverted data input B. On board AC coupled. On-chip 100-Ω differential terminated to RXB+.
21	$\overline{\text{LBB}}$	CMOS-in	Loop back B, on-chip pulled up to VDD. When pulled to low level, loop back mode B is enabled. The input data applied to the input port RXB+/RXB– is retimed and fed to both output ports TXA+/TXA– and TXB+/TXB–. This input is 2.5 V tolerant.
22	$\overline{\text{LBA}}$	CMOS-in	Loop back A, on-chip pulled up to VDD. When pulled to low level, loop back mode A is enabled. The input data applied to the input port RXA+/RXA– is retimed and fed to both output ports TXB+/TXB– and TXA+/TXA–. This input is 2.5 V tolerant.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		VALUE
V <sub>DD</sub>	Supply voltage <sup>(2)</sup>	–0.3 V to 2.5 V
V <sub>CMOS</sub>	Voltage range at CMOS input terminals (ENA, ENB, $\overline{\text{LBA}}$ , $\overline{\text{LBB}}$ , RCLK) <sup>(2)</sup>	–0.3 V to 3.0 V
	Electrical discharge	2k V (HBM)
T <sub>A</sub>	Characterized free-air temperature range (no airflow)	0°C to 70°C
T <sub>STG</sub>	Storage temperature range	–65°C to 85°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>DD</sub>	Supply voltage	1.7	1.8	1.9	V
T <sub>A</sub>	Ambient temperature (no airflow, no heatsink)	0		70	°C

# TLK1002A

## DUAL SIGNAL CONDITIONING TRANSCEIVER

SLLS661 – JUNE 2005

### DC ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DD}$ Supply voltage		1.7	1.8	1.9	V
$I_{VCC2}$ Current from 1.8 V supply	ENA = high, ENB = high, $V_{DD} = V_{DD,max}$ PRBS 1.25 Gbps data on both inputs			158	mA
$V_{IL,CMOS}$ Low level CMOS input voltage	$V_{DD} = 1.8$ V	–0.2		0.6	V
$V_{IH,CMOS}$ High level CMOS input voltage	$V_{DD} = 1.8$ V	$V_{DD} - 0.6$		2.7	V
$I_{L,CMOS}$ Low level CMOS input current	$V_{DD} = V_{DD,max}$ , $V_{IL} = 0.0$ V			–120	$\mu$ A
$I_{H,CMOS}$ High level CMOS input current	$V_{DD} = V_{DD,min}$ , $V_{IH} = 2.7$ V			165	$\mu$ A
$R_{PU}$ Integrated pull-up resistor to $V_{DD}$			20		k $\Omega$

### AC ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DATA PATHS</b>					
$Z_{D,IN}$ Differential input impedance			100		$\Omega$
$T_{J,IN}$ Total input jitter	BER $\leq 10^{-12}$ , 1.25 Gbps data			0.606	UI
$D_{J,IN}$ Deterministic input jitter	BER $\leq 10^{-12}$ , 1.25 Gbps data			0.373	UI <sub>pp</sub>
$V_{CM,IN}$ Common-mode input voltage			1200		mV
$V_{S,IN}$ Single-ended input voltage swing		200	800	1200	mV <sub>p-p</sub>
$V_{D,IN}$ Differential input voltage swing		400	1600	2400	mV <sub>p-p</sub>
$X1_{IN}$	BER $\leq 10^{-12}$ , 1.25 Gbps data, See <a href="#">Figure 2</a>			0.303	UI
$Y1_{IN}$		200			mV
$Y2_{IN}$				1200	mV
$t_{R,OUT}$ , $t_{F,OUT}$ Output signal rise/fall time	20% to 80%		150	260	ps
$T_{J,OUT}$ Total output jitter	1.25 Gbps input from 3.3G pattern generator at 0 ppm		0.20	0.28	UI
$D_{J,OUT}$ Deterministic output jitter	1.25 Gbps input from 3.3G pattern generator at 0 ppm			0.1	UI <sub>pp</sub>
$V_{CM,OUT}$ Common-mode output voltage		800	1000	1200	mV
$V_{S,OUT}$ Single-ended output voltage swing		440	800	1000	mV <sub>p-p</sub>
$V_{D,OUT}$ Differential output voltage		880	1600	2000	mV <sub>p-p</sub>
$X1_{OUT}$	1.25 Gbps input from 3.3G pattern generator at 0 ppm See <a href="#">Figure 3</a>			0.12	UI
$X2_{OUT}$				0.32	UI
$Y1_{OUT}$		440			mV
$Y2_{OUT}$				1000	mV
$t_D$ RX to TX latency				25	ns
$t_{INI}$ Lock acquisition from link down	See <sup>(1)</sup> and <sup>(2)</sup>		4		$\mu$ s
$t_{LCK}$ Lock recovery on link discontinuity	See <sup>(2)</sup>		1.6		$\mu$ s

- (1) Assuming maximum initial CDR phase offset and maximum frequency difference between reference clock and input data.  
(2) The output data may contain bit errors during lock-in time, dependent on the input-data sequence and the input-data jitter. However it is assured, that the output-data does not contain bits with widths deviating significantly from the nominal bit width.

## AC ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>REFERENCE CLOCK AC SPECIFICATIONS</b>					
$V_{IL,RCLK}$	Reference clock low level voltage	DC coupled		–0.3	0.3 V
$V_{IH,RCLK}$	Reference clock high level voltage	DC coupled		1.5	2.1 V
$V_{RCLK}$	Reference clock swing	AC coupled		1.2	2.4 $V_{p-p}$
$V_{IH,RCLK}$	Reference clock input threshold (self biasing)	AC coupled		0.9	V
	Clock duty cycle			40%	60%
$t_{R,RCLK}$ , $t_{F,RCLK}$	Rise / fall time	20% to 80%		300	1500 ps
$f_{0,RCLK}$	Reference clock frequency <sup>(3)</sup>			Baud/10	
$T_{JRCLK200}$	Reference clock total jitter <sup>(4)</sup>	Up to 10 MHz		40	$ps_{p-p}$
$T_{JRCLK}$			80		$ps_{p-p}$
$\Delta f_{RCLK}$	Frequency difference between reference clock and incoming data signal	Reference clock and incoming data are off the nominal data rate but in opposite direction		–200	200 ppm

(3) Reference clock is not locked to the data frequency and may deviate by  $\Delta f_{RCLK}$ .

(4) The reference clock may contain jitter, in the order of about 80  $ps_{p-p}$ . However, the jitter components below 10 MHz, which is the bandwidth of the clock generation PLL, must not exceed 40  $ps_{p-p}$ . Increased reference clock jitter leads to increased output jitter as well as to reduced jitter tolerance.

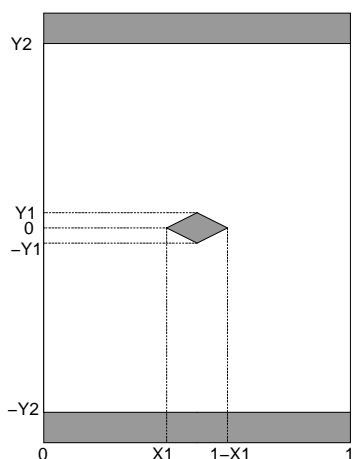


Figure 2. Input Eye Mask

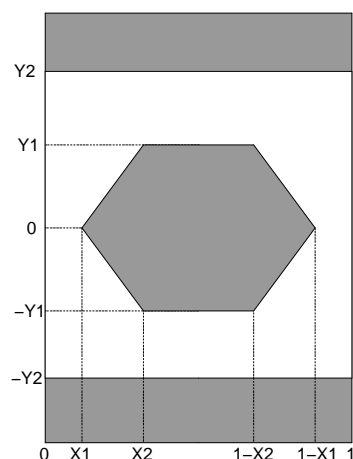


Figure 3. Output Eye Mask

## OPERATIONAL MODES

### NORMAL OPERATION MODE

In normal operation, the data signal at the  $RXA+/RXA-$  pins is applied to an input buffer stage, which drives a signal conditioning PLL. The retimed output signal is connected to the output pins  $TXB+/TXB-$  by means of a multiplexer stage and a VML output buffer.

On the other side, the input signal applied to the  $RXB+/RXB-$  pins is connected to a signal conditioning PLL by means of an input buffer stage. The retimed output signal of the PLL is connected to the output pins  $TXA+/TXA-$  using a multiplexer stage as well as a VML output driver.

## OPERATIONAL MODES (continued)

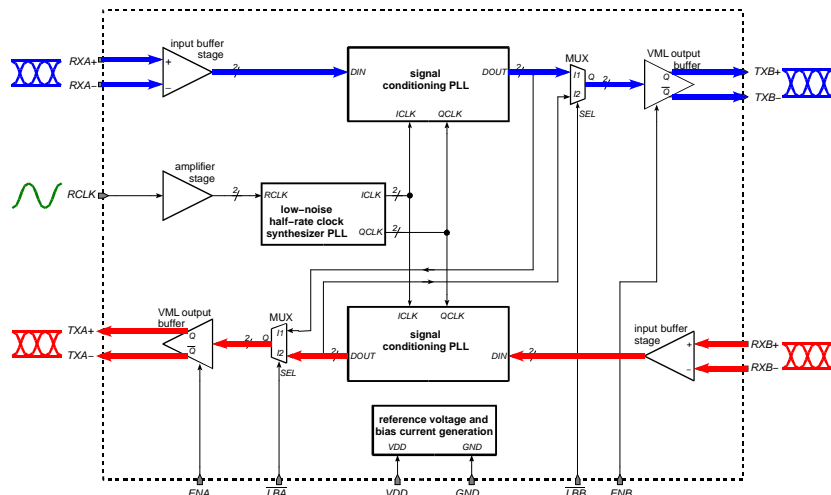


Figure 4. Data Path in Normal Operation Mode

### INTERNAL LOOP-BACK MODE A

In internal loop-back mode A operation, which is activated by pulling the  $\overline{LBA}$  pin to logic low level, the input data signal at the  $RXA+/RXA-$  pins is applied to the input buffer driving a signal conditioning PLL. The retimed output signal is connected to the output pins  $TXB+/TXB-$  by means of a multiplexer stage and a VML output buffer.

Furthermore, by means of a second multiplexer the same signal is fed to the second VML output buffer, which drives the  $TXA+/TXA-$  output.

The signal applied to the  $RXB+/RXB-$  input is not fed to any output in this mode.

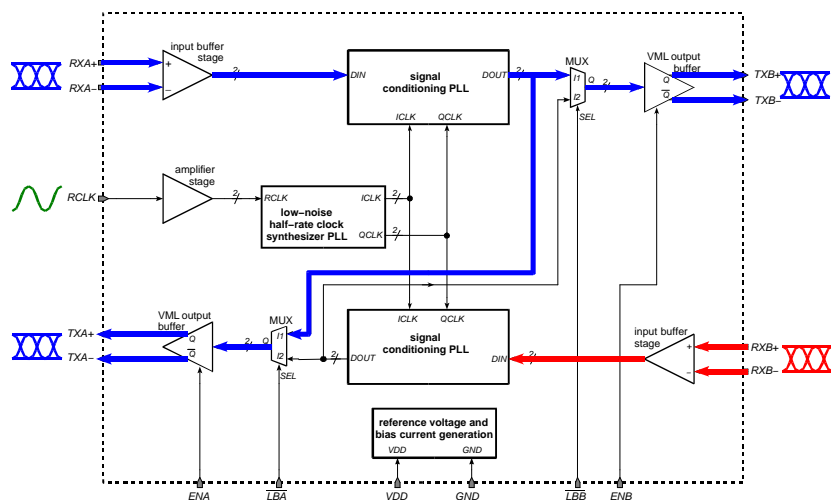


Figure 5. Data Path in Internal Loop-Back Mode A

### INTERNAL LOOP-BACK MODE B

In internal loop-back mode B operation, which is activated by pulling the  $\overline{LBB}$  pin low, the input data signal at the  $RXB+/RXB-$  pins is applied to an input buffer driving a signal conditioning PLL. The retimed output signal is connected to the output pins  $TXA+/TXA-$  by means of a multiplexer stage and a VML output buffer.

Additionally, by means of a second multiplexer, the same signal is fed to the second VML output buffer, which drives the  $TXB+/TXB-$  output.



## OPERATIONAL MODES (continued)

The signals applied to the  $RXA+/RXA-$  input is not fed to any output in this mode.

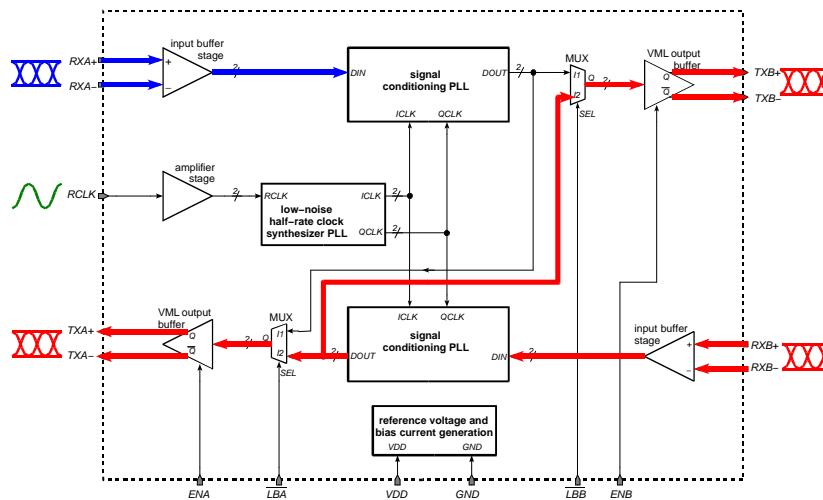


Figure 6. Data Path in Internal Loop-Back Mode B

## INTERNAL LOOP-BACK MODES A AND B

If both internal loop-back modes A and B are activated simultaneously, by pulling the  $\overline{LBA}$  and the  $\overline{LBB}$  pins low, the input data signal at  $RXA+/RXA-$  is applied to an input buffer driving a signal conditioning PLL. The retimed output signal is fed to the output  $TXA+/TXA-$  by means of a multiplexer stage and a VML output buffer.

The signals applied to the  $RXB+/RXB-$  input drives an input buffer connected to a signal conditioning PLL. The retimed output signal is connected to the output pins  $TXB+/TXB-$  by means of a multiplexer stage and a VML output buffer.

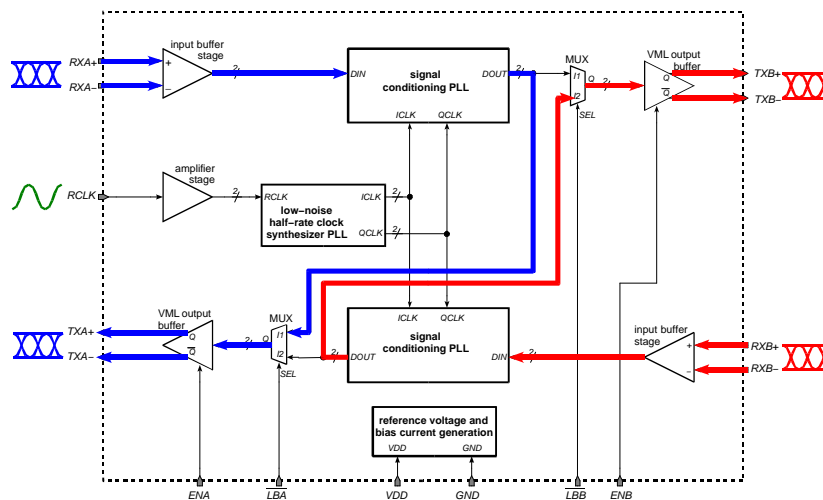


Figure 7. Data Path in Internal Loop-Back Modes A and B

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLK1002ARGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	TLK 1002A	<a href="#">Samples</a>
TLK1002ARGERG4	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	TLK 1002A	<a href="#">Samples</a>
TLK1002ARGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	TLK 1002A	<a href="#">Samples</a>
TLK1002ARGETG4	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	TLK 1002A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLK1002ARGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
TLK1002ARGET	VQFN	RGE	24	250	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS

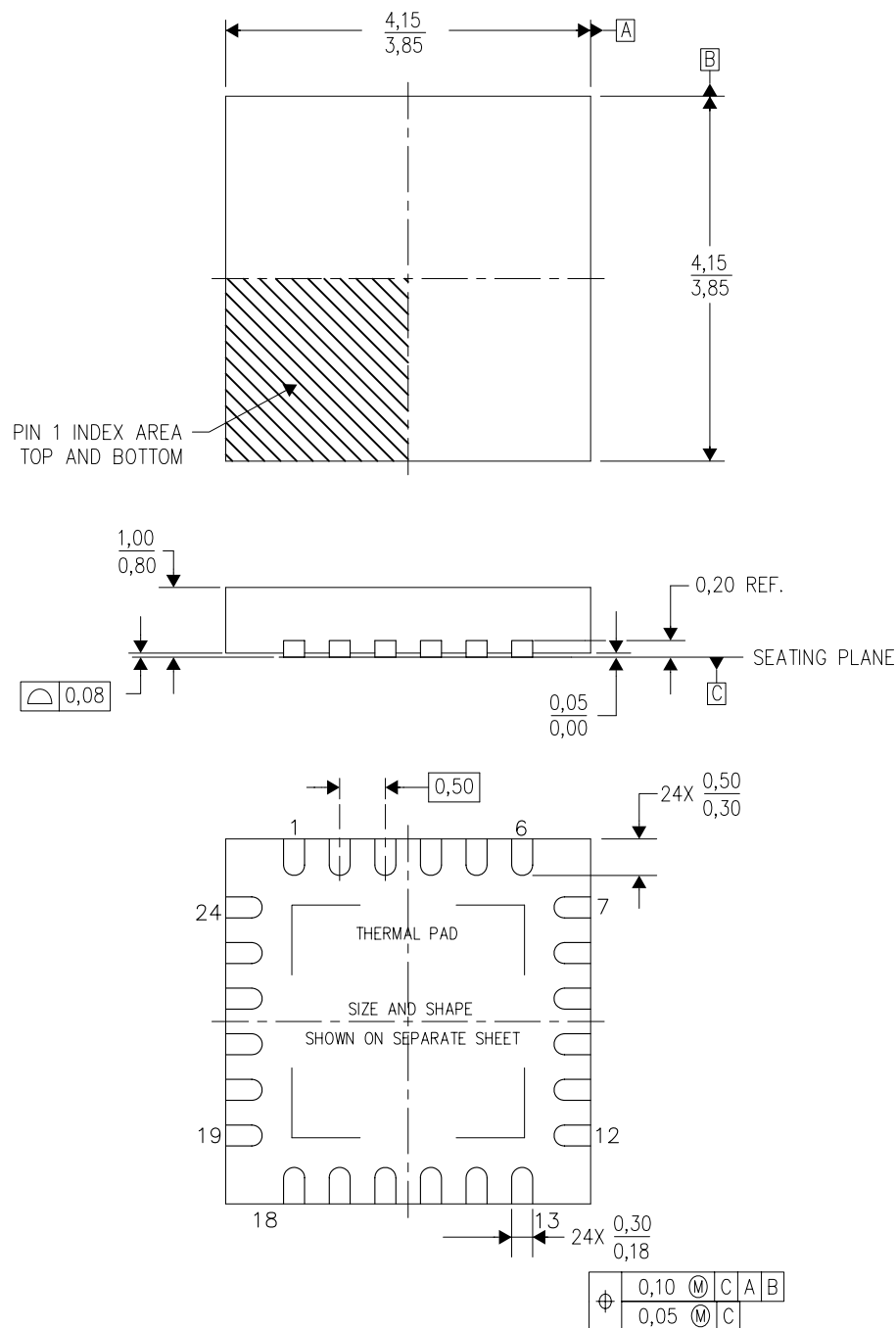


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLK1002ARGER	VQFN	RGE	24	3000	338.1	338.1	20.6
TLK1002ARGET	VQFN	RGE	24	250	338.1	338.1	20.6

RGE (S-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



4204104/G 07/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-Leads (QFN) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Falls within JEDEC MO-220.

## THERMAL PAD MECHANICAL DATA

RGE (S-PVQFN-N24)

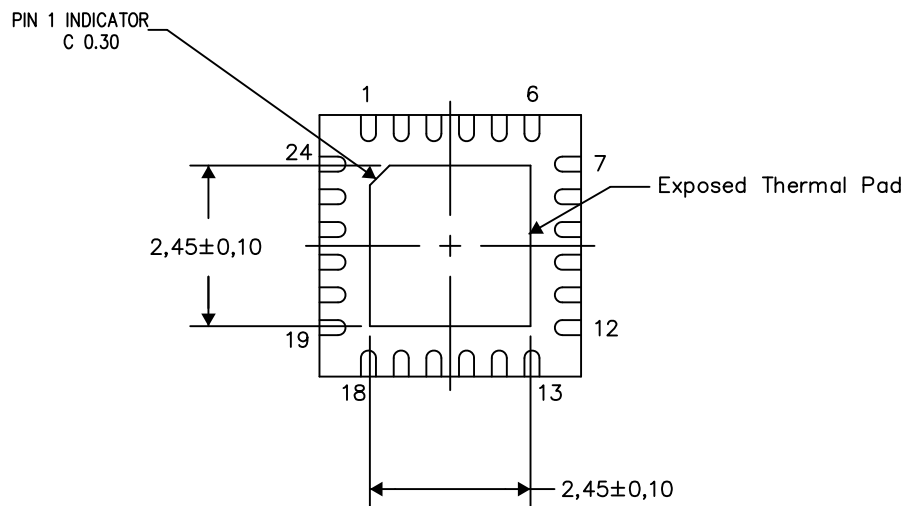
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

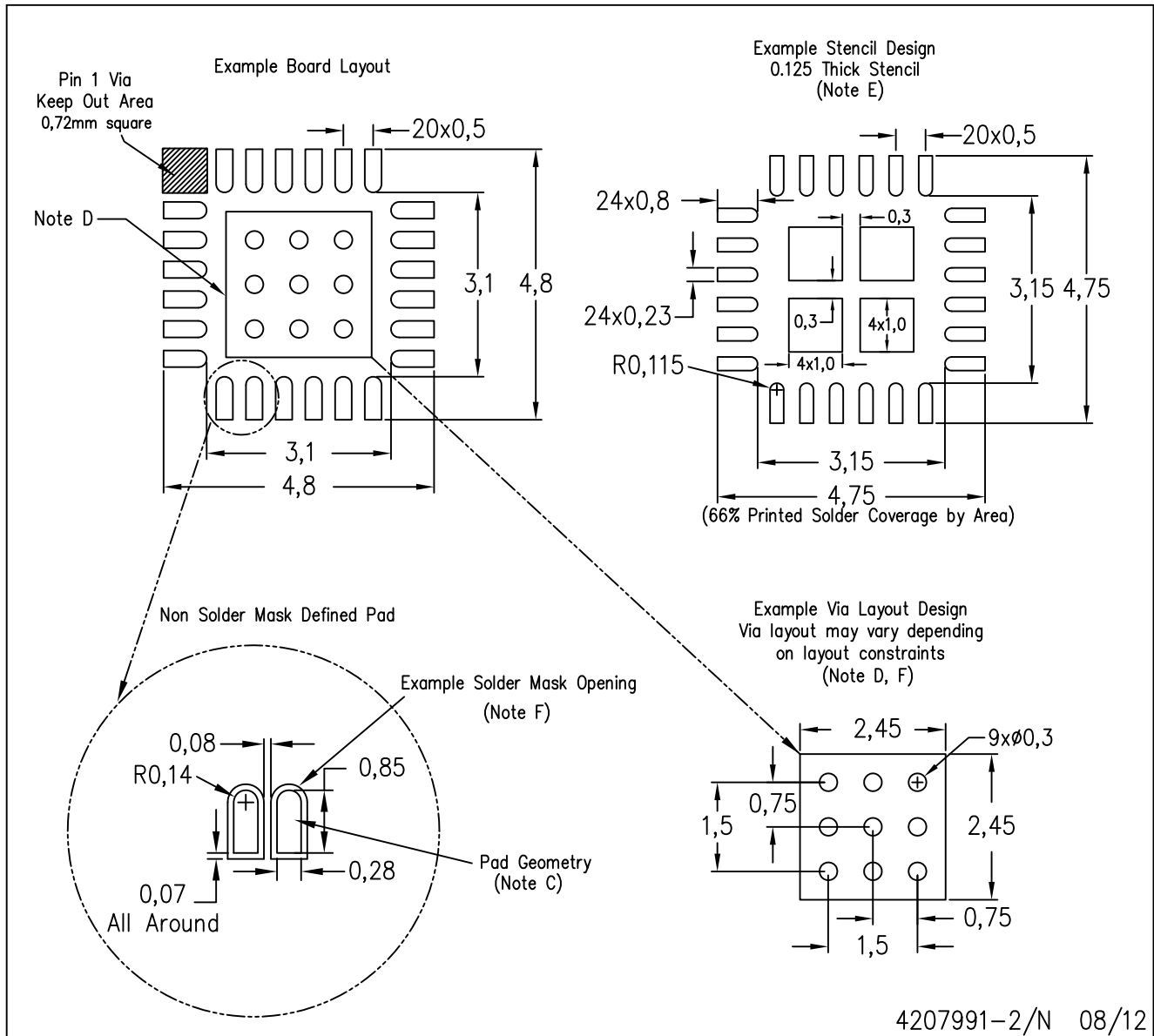
Exposed Thermal Pad Dimensions

4206344-3/AB 09/12

NOTES: A. All linear dimensions are in millimeters

RGE (S-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)



**Стандарт  
Электрон  
Связь**

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

**Наши контакты:**

**Телефон:** +7 812 627 14 35

**Электронная почта:** [sales@st-electron.ru](mailto:sales@st-electron.ru)

**Адрес:** 198099, Санкт-Петербург,  
Промышленная ул, дом № 19, литера Н,  
помещение 100-Н Офис 331