

STM32L151x6/8/B STM32L152x6/8/B

Ultra-low-power 32-bit MCU ARM[®]-based Cortex[®]-M3, 128KB Flash, 16KB SRAM, 4KB EEPROM, LCD, USB, ADC, DAC

Datasheet - production data

Features

- Ultra-low-power platform
 - 1.65 V to 3.6 V power supply
 - -40°C to 85°C/105°C temperature range
 - 0.3 μA Standby mode (3 wakeup pins)
 - 0.9 µA Standby mode + RTC
 - 0.57 μA Stop mode (16 wakeup lines)
 - 1.2 μA Stop mode + RTC
 - 9 μA Low-power run mode
 - 214 µA/MHz Run mode
 - 10 nA ultra-low I/O leakage
 - < 8 µs wakeup time</p>
- Core: ARM[®] Cortex[®]-M3 32-bit CPU
 - From 32 kHz up to 32 MHz max
 - 1.25 DMIPS/MHz (Dhrystone 2.1)
 - Memory protection unit
- Reset and supply management
 - Ultra-safe, low-power BOR (brownout reset) with 5 selectable thresholds
 - Ultra-low-power POR/PDR
 - Programmable voltage detector (PVD)
- Clock sources
 - 1 to 24 MHz crystal oscillator
 - 32 kHz oscillator for RTC with calibration
 - High Speed Internal 16 MHz factorytrimmed RC (+/- 1%)
 - Internal low-power 37 kHz RC
 - Internal multispeed low-power 65 kHz to 4.2 MHz
 - PLL for CPU clock and USB (48 MHz)
- · Pre-programmed bootloader
 - USART supported
- Development support
 - Serial wire debug supported
 - JTAG and trace supported
- Up to 83 fast I/Os (73 I/Os 5V tolerant), all mappable on 16 external interrupt vectors
- Memories
 - Up to 128 Kbytes Flash memory with ECC
 - Up to 16 Kbytes RAM







- Up to 4 Kbytes of true EEPROM with ECC
- 80-byte backup register
- LCD Driver (except STM32L151x/6/8/B devices) for up to 8x40 segments
 - Support contrast adjustment
 - Support blinking mode
 - Step-up converter on board
- Rich analog peripherals (down to 1.8 V)
 - 12-bit ADC 1 Msps up to 24 channels
 - 12-bit DAC 2 channels with output buffers
 - 2x ultra-low-power-comparators (window mode and wake up capability)
- DMA controller 7x channels
- 8x peripheral communication interfaces
 - 1x USB 2.0 (internal 48 MHz PLL)
 - 3x USARTs (ISO 7816, IrDA)
 - 2x SPIs 16 Mbit/s
 - 2x I2Cs (SMBus/PMBus)
- 10x timers: 6x 16-bit with up to 4 IC/OC/PWM channels, 2x 16-bit basic timers, 2x watchdog timers (independent and window)
- Up to 20 capacitive sensing channels supporting touchkey, linear and rotary touch sensors
- CRC calculation unit, 96-bit unique ID

Table 1. Device summary

Reference	Part number		
STM32L151x6/8/B	STM32L151CB, STM32L151C8, STM32L151C6, STM32L151RB, STM32L151R8, STM32L151R6, STM32L151VB, STM32L151V8		
STM32L152x6/8/B	STM32L152CB, STM32L152C8, STM32L152C6, STM32L152RB, STM32L152R8, STM32L152R6, STM32L152VB, STM32L152V8		

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L151x6/8/B and STM32L152x6/8/B ultra-low-power ARM[®] Cortex[®]-M3 based microcontrollers product line.

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B family includes devices in 3 different package types: from 48 to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B microcontroller family suitable for a wide range of applications:

- Medical and handheld equipment
- Application control and user interface
- · PC peripherals, gaming, GPS and sport equipment
- Alarm systems, Wired and wireless sensors, Video intercom
- Utility metering

This STM32L151x6/8/B and STM32L152x6/8/B datasheet should be read in conjunction with the STM32L1xxxx reference manual (RM0038).

The document "Getting started with STM32L1xxxx hardware development" AN3216 gives a hardware implementation overview. Both documents are available from the STMicroelectronics website www.st.com.

For information on the ARM[®] Cortex[®]-M3 core please refer to the Cortex[®]-M3 Technical Reference Manual, available from the www.arm.com website.

Figure 1 shows the general block diagram of the device family.

Caution: This datasheet does not apply to STM32L15xx6/8/B-A covered by a separate datasheet.



2 Description

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices incorporate the connectivity power of the universal serial bus (USB) with the high-performance ARM[®] Cortex[®]-M3 32-bit RISC core operating at 32 MHz frequency (33.3 DMIPS), a memory protection unit (MPU), high-speed embedded memories (Flash memory up to 128 Kbytes and RAM up to 16 Kbytes) and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

All the devices offer a 12-bit ADC, 2 DACs and 2 ultra-low-power comparators, six general-purpose 16-bit timers and two basic timers, which can be used as time bases.

Moreover, the STM32L151x6/8/B and STM32L152x6/8/B devices contain standard and advanced communication interfaces: up to two I²Cs and SPIs, three USARTs and a USB. The STM32L151x6/8/B and STM32L152x6/8/B devices offer up to 20 capacitive sensing channels to simply add touch sensing functionality to any application.

They also include a real-time clock and a set of backup registers that remain powered in Standby mode.

Finally, the integrated LCD controller (except STM32L151x6/8/B devices) has a built-in LCD voltage generator that allows to drive up to 8 multiplexed LCDs with contrast independent of the supply voltage.

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. It is available in the -40 to +85 °C temperature range, extended to 105°C in low power dissipation state. A comprehensive set of power-saving modes allows the design of low-power applications.







2.1 Device overview

Table 2. Ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B device features and peripheral counts

Peripheral		ST	STM32L15xCx		STM32L15xRx			STM32L15xVx		
Flash (Kbytes)		32	64	128	32	64	128	64	128	
Data EEPROM (Kb	ytes)					4				
RAM (Kbytes)		10	10	16	10	10	16	10	16	
Timers	General- purpose		6							
	Basic					2				
	SPI					2				
Communication	I ² C					2				
interfaces	USART		3							
	USB		1							
GPIOs			37			51			83	
12-bit synchronized ADC Number of channels		1	1 1 1 1 1 1 1 4 channels 20 channels 24 c			24 ch	1 annels			
12-bit DAC Number of channe		2 2								
LCD (STM32L152xx Only) COM x SEG		4x18			4x32 8x28			4x44 8x40		
Comparator		2								
Capacitive sensing	g channels		13 20							
Max. CPU frequency		32 MHz								
Operating voltage	1	1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V without BOR option								
Operating tempera		Ambient temperatures: -40 to +85 °C Junction temperature: -40 to + 105 °C								
Packages		LQFP), BGA100				

2.2 Ultra-low-power device continuum

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices are fully pin-to-pin and software compatible. Besides the full compatibility within the family, the devices are part of STMicroelectronics microcontrollers ultra-low-power strategy which also includes STM8L101xx and STM8L15xx devices. The STM8L and STM32L families allow a continuum of performance, peripherals, system architecture and features.

They are all based on STMicroelectronics ultra-low leakage process.

Note:

The ultra-low-power STM32L and general-purpose STM32Fxxxx families are pin-to-pin compatible. The STM8L15xxx devices are pin-to-pin compatible with the STM8L101xx devices. Please refer to the STM32F and STM8L documentation for more information on these devices.

2.2.1 Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM® Cortex®-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-low-power performance to range from 5 up to 33.3 DMIPs.

2.2.2 Shared peripherals

STM8L15xxx and STM32L1xxxx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC, DAC and comparators
- Digital peripherals: RTC and some communication interfaces

2.2.3 Common system strategy

To offer flexibility and optimize performance, the STM8L15xx and STM32L1xxxx families use a common architecture:

- Same power supply range from 1.65 V to 3.6 V, (1.65 V at power down only for STM8L15xx devices)
- Architecture optimized to reach ultra-low consumption both in low power modes and Run mode
- Fast startup strategy from low power modes
- Flexible system clock
- Ultrasafe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector.

2.2.4 Features

ST ultra-low-power continuum also lies in feature compatibility:

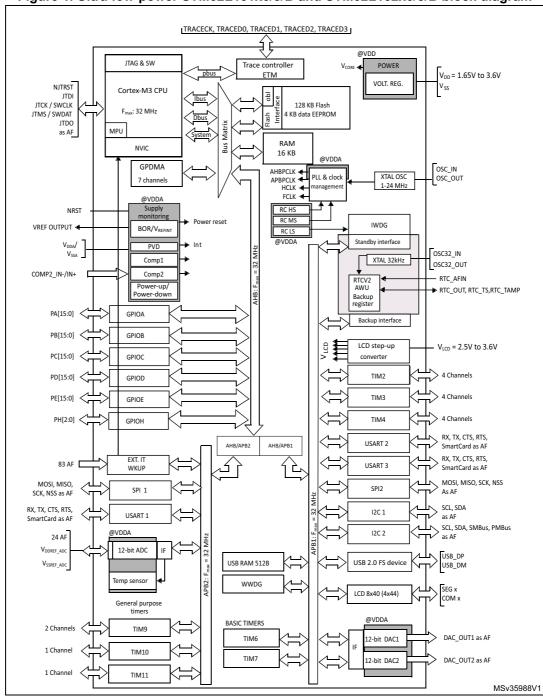
- More than 10 packages with pin count from 20 to 144 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 384 Kbytes

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3 Functional overview

Figure 1 shows the block diagram.

Figure 1. Ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B block diagram



1. AF = alternate function on I/O port pin.



3.1 Low power modes

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices support dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply:

- In Range 1 (V_{DD} range limited to 1.71-3.6 V), the CPU runs at up to 32 MHz (refer to *Table 17* for consumption).
- In Range 2 (full V_{DD} range), the CPU runs at up to 16 MHz (refer to Table 17 for consumption)
- In Range 3 (full V_{DD} range), the CPU runs at up to 4 MHz (generated only with the multispeed internal RC oscillator clock source). Refer to *Table 17* for consumption.

Seven low power modes are provided to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

• Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Sleep mode power consumption: refer to *Table 19*.

• Low power run mode

This mode is achieved with the multispeed internal (MSI) RC oscillator set to the minimum clock (65 kHz), execution from SRAM or Flash memory, and internal regulator in low power mode to minimize the regulator's operating current. In the Low power run mode, the clock frequency and the number of enabled peripherals are both limited.

Low power run mode consumption: refer to *Table 20: Current consumption in Low power run mode*.

• Low power sleep mode

This mode is achieved by entering the Sleep mode with the internal voltage regulator in Low power mode to minimize the regulator's operating current. In the Low power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

When wakeup is triggered by an event or an interrupt, the system reverts to the run mode with the regulator on.

Low power sleep mode consumption: refer to *Table 21: Current consumption in Low power sleep mode*.

• Stop mode with RTC

Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSI RC and HSE crystal oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low power mode.

The device can be woken up from Stop mode by any of the EXTI line, in 8 μ s. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on), it can be the RTC alarm(s), the USB wakeup, the RTC tamper events, the RTC timestamp event or the RTC wakeup.

• Stop mode without RTC

Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and



HSE crystal oscillators are disabled. The voltage regulator is in the low power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.

Stop mode consumption: refer to *Table 22: Typical and maximum current consumptions in Stop mode*.

Standby mode with RTC

Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC CSR).

The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

Standby mode without RTC

Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI, RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

The device exits Standby mode in $60~\mu s$ when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Standby mode consumption: refer to Table 23.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering the Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

	Functionalities depending on the operating power supply range					
Operating power supply range	DAC and ADC USB Operation		Dynamic voltage scaling range	I/O operation		
V _{DD} = 1.65 to 1.71 V	Not functional	Not functional	Range 2 or Range 3	Degraded speed performance		
$V_{DD} = 1.71 \text{ to } 1.8 \text{ V}^{(1)}$	Not functional	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance		
V_{DD} = 1.8 to 2.0 $V^{(1)}$	Conversion time up to 500 Ksps	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance		



Table 3. Functionalities depending on the operating power supply range (continued)

	Functionalities depending on the operating power supply range					
Operating power supply range	DAC and ADC operation USB		Dynamic voltage scaling range	I/O operation		
V _{DD} = 2.0 to 2.4 V	Conversion time up to 500 Ksps	Functional ⁽²⁾	Range 1, Range 2 or Range 3	Full speed operation		
V _{DD} = 2.4 to 3.6 V	Conversion time up to 1 Msps	Functional ⁽²⁾	Range 1, Range 2 or Range 3	Full speed operation		

The CPU frequency changes from initial to final must respect "F_{CPU} initial < 4*F_{CPU} final" to limit V_{CORE} drop due to current consumption peak when frequency increases. It must also respect 5 µs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5 µs, then switch from 16 MHz to 32 MHz.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
2.1 MHz to 4.2 MHz (1ws) 32 kHz to 2.1 MHz (0ws)	Range 3

^{2.} Should be USB compliant from I/O voltage standpoint, the minimum V_{DD} is 3.0 V.

Table 5. Working mode-dependent functionalities (from Run/active down to standby)

			Low-	Low-		Stop	Standby	
lps	Run/Active	Sleep	power Run			Wakeup capability		Wakeup capability
CPU	Υ	-	Υ	-	-	-	-	-
Flash	Y	Υ	Y	Y	-	-	-	-
RAM	Υ	Υ	Y	Y	Υ	-	-	-
Backup Registers	Y	Υ	Y	Y	Υ	-	Υ	-
EEPROM	Υ	-	Y	Y	Υ	-	-	-
Brown-out rest (BOR)	Υ	Y	Y	Y	Υ	Y	Υ	-
DMA	Y	Υ	Y	Y	-	-	-	-
Programmable Voltage Detector (PVD)	Y	Υ	Y	Y	Υ	Y	Υ	-
Power On Reset (POR)	Υ	Υ	Y	Y	Υ	Υ	Υ	-
Power Down Rest (PDR)	Υ	Y	Y	Y	Υ	-	Υ	-
High Speed Internal (HSI)	Υ	Y	-	-	-	-	-	-
High Speed External (HSE)	Υ	Y	-	-	-	-	-	-
Low Speed Internal (LSI)	Υ	Y	Y	Y	Υ	-	Υ	-
Low Speed External (LSE)	Υ	Y	Y	Y	Υ	-	Υ	-
Multi-Speed Internal (MSI)	Y	Υ	Y	Y	-	-	-	-
Inter-Connect Controller	Υ	Υ	Y	Y	-	-	-	-
RTC	Y	Υ	Y	Y	Υ	Y	Υ	-
RTC Tamper	Υ	Υ	Y	Y	Υ	Y	Υ	Y
Auto Wakeup (AWU)	Υ	Υ	Y	Y	Υ	Y	Υ	Y
LCD	Υ	Υ	Y	Y	Υ	-	-	-
USB	Υ	Υ	-	-	-	Y	-	-
USART	Υ	Υ	Y	Y	Y (1)		-	-
SPI	Υ	Υ	Y	Y	-	-	-	-
I2C	Υ	Υ	Y	Y	-	(1)	-	-
ADC	Y	Υ	-	-	-	-	-	-



			Low-	Low-	Stop		Standby	
lps	Ips Run/Active Sleep power power Run Sleep		•		Wakeup capability		Wakeup capability	
DAC	Υ	Υ	Y	Y	Υ	-	-	-
Temperature sensor	Y	Y	Y	Υ	Υ	Y -		-
Comparators	Y	Y	Y	Y	Υ	Y	-	-
16-bit and 32-bit Timers	Y	Y	Y	Y	-			-
IWDG	Y	Υ	Y	Υ	Υ	YY		Y
WWDG	Y	Y	Y	Y	-	-	-	-
Touch sensing	Y	-	-	-	-	-	-	-
Systick Timer	Y	Y	Y	Y			-	-
GPIOs	Y	Υ	Y	Υ	Υ	YY		3 Pins
Wakeup time to Run mode	0 µs	0.36 µs	3 µs	32 µs	< 8 µs		50 µs	
		Downto 50 μΑ/MHz (from Flash)	Down to 9 µA	Down to 4.4 µA	0.5 μA (No RTC) V _{DD} =1.8V		0.3 μA (No RTC) V _{DD} =1.8V	
Consumption V _{DD} =1.8V to 3.6V (Typ)	Down to 214 µA/MHz (from Flash)				1.4 µA (with RTC) V _{DD} =1.8V		1 μA (with RTC) V _{DD} =1.8V	
					0.5 μA (No RTC) V _{DD} =3.0V		0.3 μA (No RTC) V _{DD} =3.0V	
						δ μΑ (with) V _{DD} =3.0V	1.3 µA (with RTC) V _{DD} =3.0V	

Table 5. Working mode-dependent functionalities (from Run/active down to standby) (continued)

3.2 ARM® Cortex®-M3 core with MPU

The ARM® Cortex®-M3 processor is the industry leading processor for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The memory protection unit (MPU) improves system reliability by defining the memory attributes (such as read/write access permissions) for different memory regions. It provides up to eight different regions and an optional predefined background region.

Owing to its embedded ARM core, the STM32L151x6/8/B and STM32L152x6/8/B devices are compatible with all ARM tools and software.



The startup on communication line wakes the CPU which was made possible by an EXTI, this induces a delay before entering run mode.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices embed a nested vectored interrupt controller able to handle up to 45 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.3 Reset and supply management

3.3.1 Power supply schemes

- V_{DD} = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator.
 Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC is used).
 V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

The device exists in two versions:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the V_{DD} min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.



Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for any external reset circuit.

Note:

The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32K osc, RCC CSR).

3.3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from Flash memory
- Boot from System Memory
- Boot from embedded RAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1 or USART2. See STM32™ microcontroller system memory boot mode AN2606 for details.



3.4 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness. It features:

- Clock prescaler: to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching**: clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management**: to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- Master clock source: three different clock sources can be used to drive the master clock:
 - 1-24 MHz high-speed external crystal (HSE), that can supply a PLL
 - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
 - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz) with a consumption proportional to speed, down to 750 nA typical. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.
- Auxiliary clock source: two ultra-low-power clock sources that can be used to drive the LCD controller and the real-time clock:
 - 32.768 kHz low-speed external crystal (LSE)
 - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog.
 The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- RTC and LCD clock sources: the LSI, LSE or HSE sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **USB clock source:** the embedded PLL has a dedicated 48 MHz clock output to supply the USB interface.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 2.1 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- Clock security system (CSS): this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.
- Clock-out capability (MCO: microcontroller clock output): it outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.



MSI RC MSI ADCCLK to ADC Peripheral clock enable 16 MHz HSI RC HSI USBCI K PLLVCO/2 to USB interface PLLSRC PLLMUL SW PLLDIV x3,x4,x6,x8 HSI SYSCLK 32 MHz max /2,/3,/4 x12,x16,x24 OSC_OUT [PLLCLK x32,x48 1-24 MHz HSE HSE OSC OSC_IN CSS HCLK to AHB bus, core, memory and DMA 32 MHz max Clock Enable → to Cortex System timer /8 ▶ FCLK Cortex free running clock AHB APB1 PCLK1 32 MHz max Prescale Prescaler to APB1 /1, 2..512 /1, 2, 4, 8, 16 Peripheral Clock peripherals Enable If (APB1 prescaler =1) x1 to TIM2,3,4,6 and 7 else x2 Peripheral Clock APB2 32 MHz max PCLK2 Prescaler peripherals to APB2 /1, 2, 4, 8, 16 Peripheral Clock Enable to TIM9, 10, and 11 If (APB2 prescaler =1) x else x TIMxCLK TIMx0 Peripheral Clock Enable Timer 9, 10, 11 ETR OSC32_IN to RTC LSE OSC RTCCLK 32.768 kHz OSC32_OUT to LCD RTCSEL[1:0] to Independent Watchdog (IWDG) LSI RC **IWDGCLK** Legend: HSE = High-speed external clock signal SYSCLK HSI = High-speed internal clock signalHSI /1,2,4, LSI = Low-speed internal clock signal MCO 8,16 LSE = Low-speed external clock signal PLLCLK LSI LSE MSI = Multispeed internal clock signal MCOSEL

Figure 2. Clock tree



3.5 Low power real-time clock and backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are made automatically. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes.

- The programmable wakeup time ranges from 120 µs to 36 hours
- Stop mode consumption with LSI and Auto-wakeup: 1.2 μA (at 1.8 V) and 1.4 μA (at 3.0 V)
- Stop mode consumption with LSE, calendar and Auto-wakeup: 1.3 μ A (at 1.8V), 1.6 μ A (at 3.0 V)

The RTC can be calibrated with an external 512 Hz output, and a digital compensation circuit helps reduce drift due to crystal deviation.

There are twenty 32-bit backup registers provided to store 80 bytes of user application data. They are cleared in case of tamper detection.

3.6 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated AFIO registers. All GPIOs are high current capable. The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to the AHB with a toggling speed of up to 16 MHz.

External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 83 GPIOs can be connected to the 16 external interrupt lines. The 7 other lines are connected to RTC, PVD, USB or Comparator events.



3.7 Memories

The STM32L151x6/8/B and STM32L152x6/8/B devices have the following features:

- Up to 16 Kbytes of embedded RAM accessed (read/write) at CPU clock speed with 0
 wait states. With the enhanced bus matrix, operating the RAM does not lead to any
 performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
 - 32, 64 or 128 Kbytes of embedded Flash program memory
 - 4 Kbytes of data EEPROM
 - Options bytes

The options bytes are used to write-protect the memory (with 4 Kbytes granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- Level 2: chip readout protection, debug features (Cortex[®]-M3 JTAG and serial wire) and boot in RAM selection disabled (JTAG fuse)

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.8 DMA (direct memory access)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C , USART, general-purpose timers and ADC.

3.9 LCD (liquid crystal display)

The LCD drives up to 8 common terminals and 44 segment terminals to drive up to 320 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD}. This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode



3.10 ADC (analog-to-digital converter)

A 12-bit analog-to-digital converters is embedded into STM32L151x6/8/B and STM32L152x6/8/B devices with up to 24 external channels, performing conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start trigger and injection trigger, to allow the application to synchronize A/D conversions and timers. An injection mode allows high priority conversions to be done by interrupting a scan mode which runs in as a background task.

The ADC includes a specific low power mode. The converter is able to operate at maximum speed even if the CPU is operating at a very low frequency and has an auto-shutdown function. The ADC's runtime and analog front-end current consumption are thus minimized whatever the MCU operating mode.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode, see *Table 58: Temperature sensor calibration values*.

3.10.2 Internal voltage reference (V_{RFFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value (when no external voltage, VREF+, is available for ADC). The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode see *Table 16: Embedded internal reference voltage*.

3.11 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.



This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channels' independent or simultaneous conversions
- DMA capability for each channel (including the underrun interrupt)
- external triggers for conversion
- input reference voltage V_{RFF+}

Eight DAC trigger inputs are used in the STM32L151x6/8/B and STM32L152x6/8/B devices. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.12 Ultra-low-power comparators and reference voltage

The STM32L151x6/8/B and STM32L152x6/8/B devices embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- one comparator with fixed threshold
- one comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
 - DAC output
 - External I/O
 - Internal reference voltage (V_{REFINT}) or V_{REFINT} submultiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low power / low current output buffer (driving current capability of 1 µA typical).

3.13 Routing interface

This interface controls the internal routing of I/Os to TIM2, TIM3, TIM4 and to the comparator and reference voltage output.

3.14 Touch sensing

The STM32L151x6/8/B and STM32L152x6/8/B devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 20 capacitive sensing channels distributed over 10 analog I/O groups. Only software capacitive sensing acquisition mode is supported.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven



implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. The capacitive sensing acquisition only requires few external components to operate.

Reliable touch sensing functionality can be quickly and easily implemented using the free STM32L1xx STMTouch touch sensing firmware library.

3.15 Timers and watchdogs

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices include six general-purpose timers, two basic timers and two watchdog timers.

Table 6 compares the features of the general-purpose and basic timers.

Table 6. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs	
TIM2, TIM3, TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No	
TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	
TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	



3.15.1 General-purpose timers (TIM2, TIM3, TIM4, TIM9, TIM10 and TIM11)

There are six synchronizable general-purpose timers embedded in the STM32L151x6/8/B and STM32L152x6/8/B devices (see Table 6 for differences).

TIM2, TIM3, TIM4

These timers are based on a 16-bit auto-reload up/down-counter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare. PWM or onepulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2, TIM3, TIM4 general-purpose timers can work together or with the TIM10, TIM11 and TIM9 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM10, TIM11 and TIM9

These timers are based on a 16-bit auto-reload up-counter and a 16-bit prescaler. They include a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4 full-featured generalpurpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

3.15.2 **Basic timers (TIM6 and TIM7)**

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit time bases.

3.15.3 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit down-counter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches 0.

3.15.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit down-counter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.



3.15.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit down-counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.16 Communication interfaces

3.16.1 I2C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7- and 10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

3.16.2 Universal synchronous/asynchronous receiver transmitter (USART)

All USART interfaces are able to communicate at speeds of up to 4 Mbit/s. They provide hardware management of the CTS and RTS signals and are ISO 7816 compliant. They support IrDA SIR ENDEC and have LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

3.16.3 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

3.16.4 Universal serial bus (USB)

The STM32L151x6/8/B and STM32L152x6/8/B devices embed a USB device peripheral compatible with the USB full speed 12 Mbit/s. The USB interface implements a full speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and supports suspend/resume. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).



3.17 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.18 Development support

Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG JTMS and JTCK pins are shared with SWDAT and SWCLK, respectively, and a specific sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

The JTAG port can be permanently disabled with a JTAG fuse.

Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L151x6/8/B and STM32L152x6/8/B device through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

4 Pin descriptions

Figure 3. STM32L15xVx UFBGA100 ballout

			1 190		7111102	LISXV	X 0. D	OAI	o bui	iout			
	1	2	3	4	5	6	7	8	9	10	11	12	
											_		
Α	(PE3)	(PE1)	(PB8)	Booto	(PD7)	(PD5)	(PB4)	(PB3)	(PA15)	(PA14)	(PA13)	(PA12)	
В	(PE4)	(PE2)	(PB9)	(PB7)	(PB6)	(PD6)	(PD4)	(PD3)	(PD1)	PC12)	(PC10)	(PA11)	
С	PC13, WKUP2	(PE5)	(PEO)	VDD_B	(PB5)			(PD2)	(PDO)	(PC11)	(PH2)	(PA10)	
D	PC14) OSC32_II	MUKP3	ńss_b							(PA9)	(PA8)	(PC9)	
Е	PC15) OSC32_	VLCD)	ŃSS_A							(PC8)	(PC7)	(PC6)	
F	SC_IN	(VSS_)5					 				WSS_P	ivss_h	
G	PH1 QSC_O					_	 				(VDD)12	(VDD_)1	
н	(PCO)	(NRST)	VDD_4							PD15)	PD14)	(PD13)	
J	VSSA)	(PC1)	(PC2)							PD12)	PD11)	(PD10)	
К	VREA	(PC3)	(PA2)	(PA5)	(PC4)			(PD9)	(PD8)	(PB15)	PB14)	(PB13)	
L	(VRE#+	(PAO) WKUP1	(PA3)	(PA6)	(PC5)	(PB2)	(PE8)	(PE10)	(PE12)	(PB10)	(PB11)	(PB12)	
М	NDDA	(PA1)	(PA4)	(PA7)	(PB0)	(PB1)	(PE7)	(PE9)	(PE11)	(PE13	(PE1)	(PE19	
													ai17096f

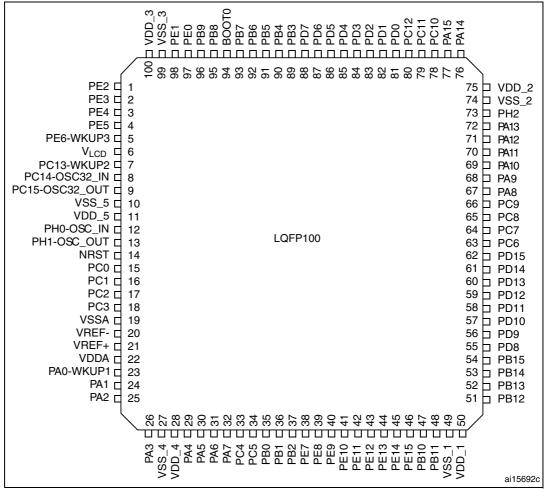


Figure 4. STM32L15xVx LQFP100 pinout



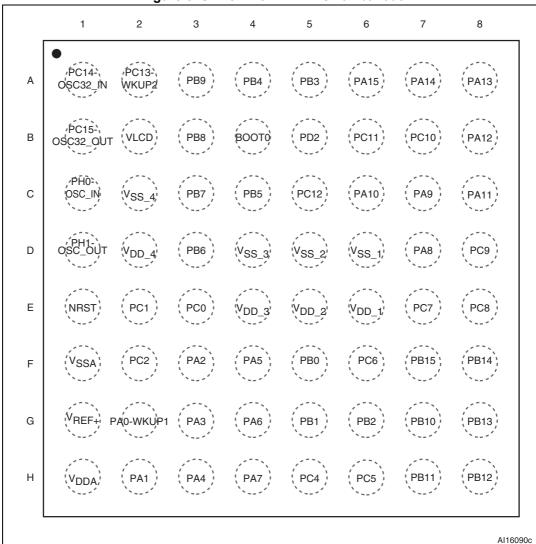


Figure 5. STM32L15xRx TFBGA64 ballout

PB8
BOOTI
PB7
PB6
PB8
PB8
PD2
PC11
PC11
PC11
PC11 VDD_ VSS_ PB9 $64 \ 63 \ 62 \ 61 \ 60 \ 59 \ 58 \ 57 \ 56 \ 55 \ 54 \ 53 \ 52 \ 51 \ 50 \ 49$ 48 🗖 VDD_2 V_{LCD} □ 47 🗖 VSS 2 PC13-WKUP2 2 PC14-OSC32_IN 3 46 🗖 PA13 PC15-OSC32_OUT 4 45 PA12 44 🗖 PA11 PH0-OSC_IN 5 43 PA10 PH1-OSC_OUT 🗖 6 42 PA9 NRST 🗖 7 41 PA8 PC0 🔲 8 LQFP64 40 PC9 PC1 🔲 9 PC2 🗖 10 39 PC8 PC3 🗖 11 38 PC7 VSSA 🗖 12 37 PC6 VDDA 🔲 13 36 PB15 35 PB14 PA0-WKUP1 14 PA1 🗖 15 34 🏻 PB13 33 🏻 PB12 PA2 🔲 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 VDD_4
PA4 |
PA5 |
PA6 |
PA7 |
PC5 |
PB0 |
PB1 | PB10 ai15693d

Figure 6. STM32L15xRx LQFP64 pinout

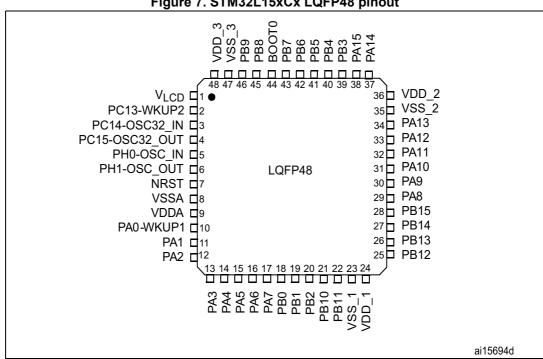


Figure 7. STM32L15xCx LQFP48 pinout

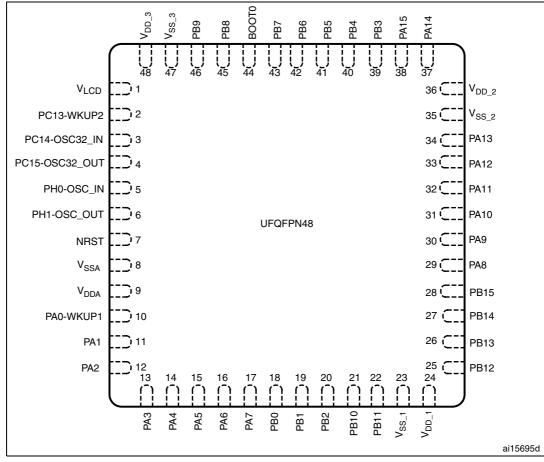


Figure 8. STM32L15xCx UFQFPN48 pinout



Table 7. Legend/abbreviations used in the pinout table

Na	me	Abbreviation Definition					
Pin r	name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name					
		S	Supply pin				
Pin	type	I	Input only pin				
		I/O	Input / output pin				
		FT	5 V tolerant I/O				
I/O etr	ucture	TC Standard 3.3 V I/O					
1/0 811	ucture	B Dedicated BOOT0 pin					
		RST Bidirectional reset pin with embedded weak pull-up resist					
No	tes	Unless otherwis and after reset	e specified by a note, all I/Os are set as floating inputs during				
	Alternate functions	Functions selected through GPIOx_AFR registers					
Pin functions	Additional functions	Functions directly selected/enabled through peripheral registers					

Table 8. STM32L151x6/8/B and STM32L152x6/8/B pin definitions

		Pins							Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48	Pin name	Pin type ⁽¹⁾	I/O structure	Main function ⁽²⁾ (after reset)	Alternate functions	Additional functions
1	-	-	B2	-	PE2	I/O	FT	PE2	TRACECLK/LCD_SEG38/ TIM3_ETR	-
2	-	-	A1	-	PE3	I/O	FT	PE3	TRACED0/LCD_SEG39/ TIM3_CH1	-
3	-	1	B1	-	PE4	I/O	FT	PE4	TRACED1/TIM3_CH2	-
4	-	-	C2	-	PE5	I/O	FT	PE5	TRACED2/TIM9_CH1	-
5	-	1	D2	-	PE6-WKUP3	I/O	FT	PE6	TRACED3/TIM9_CH2	WKUP3
6	1	B2	E2	1	V _{LCD} ⁽³⁾	S		V_{LCD}	-	-
7	2	A2	C1	2	PC13- WKUP2	I/O	FT	PC13	-	RTC_TAMP1/ RTC_TS/ RTC_OUT/ WKUP2
8	3	A1	D1	3	PC14- OSC32_IN ⁽⁴⁾	I/O	TC	PC14	-	OSC32_IN
9	4	B1	E1	4	PC15- OSC32_OUT	I/O	тс	PC15	-	OSC32_OUT
10	-	-	F2	-	V _{SS_5}	S	-	V _{SS_5}	-	-
11	-	-	G2	-	V _{DD_5}	S	-	V _{DD_5}	-	-
12	5	C1	F1	5	PH0- OSC_IN ⁽⁵⁾	I/O	тс	PH0	-	OSC_IN
13	6	D1	G1	6	PH1- OSC_OUT	I/O	TC	PH1	-	OSC_OUT
14	7	E1	H2	7	NRST	I/O	RST	NRST	-	-
15	8	E3	H1	-	PC0	I/O	FT	PC0	LCD_SEG18	ADC_IN10/ /COMP1_INP
16	9	E2	J2	-	PC1	I/O	FT	PC1	LCD_SEG19	ADC_IN11/ COMP1_INP
17	10	F2	J3	-	PC2	I/O	FT	PC2	LCD_SEG20	ADC_IN12/ COMP1_INP
18	11	_(6)	K2	-	PC3	I/O	тс	PC3	LCD_SEG21	ADC_IN13/ COMP1_INP



Table 8. STM32L151x6/8/B and STM32L152x6/8/B pin definitions (continued)

		Pins	5						Pins functions	,
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48	Pin name	Pin type ⁽¹⁾	I/O structure	Main function ⁽²⁾ (after reset)	Alternate functions	Additional functions
19	12	F1	J1	8	V_{SSA}	S	-	V_{SSA}	-	-
20	-	ı	K1	-	V _{REF-}	S	ı	V _{REF-}	-	-
21	1	G1 (6)	L1	-	V _{REF+}	S	ı	V _{REF+}	-	-
22	13	H1	M1	9	V_{DDA}	S	-	V_{DDA}	-	-
23	14	G2	L2	10	PA0-WKUP1	I/O	FT	PA0	USART2_CTS/ TIM2_CH1_ETR	WKUP1/ ADC_IN0/ COMP1_INP
24	15	H2	M2	11	PA1	I/O	FT	PA1	USART2_RTS/ TIM2_CH2/LCD_SEG0	ADC_IN1/ COMP1_INP
25	16	F3	K3	12	PA2	I/O	FT	PA2	USART2_TX/TIM2_CH3/ TIM9_CH1/LCD_SEG1	ADC_IN2/ COMP1_INP
26	17	G3	L3	13	PA3	I/O	TC	PA3	USART2_RX/TIM2_CH4/ TIM9_CH2/LCD_SEG2	ADC_IN3/ COMP1_INP
27	18	C2	E3	-	V _{SS_4}	S	-	V _{SS_4}	-	-
28	19	D2	Н3	-	V_{DD_4}	S	ı	V _{DD_4}	-	-
29	20	НЗ	МЗ	14	PA4	I/O	TC	PA4	SPI1_NSS/USART2_CK	ADC_IN4/ DAC_OUT1/ COMP1_INP
30	21	F4	K4	15	PA5	I/O	TC	PA5	SPI1_SCK/ TIM2_CH1_ETR	ADC_IN5/ DAC_OUT2/ COMP1_INP
31	22	G4	L4	16	PA6	I/O	FT	PA6	SPI1_MISO/TIM3_CH1/ LCD_SEG3/TIM10_CH1	ADC_IN6 /COMP1_INP
32	23	H4	M4	17	PA7	I/O	FT	PA7	SPI1_MOSI//TIM3_CH2/ LCD_SEG4/TIM11_CH1	ADC_IN7/ COMP1_INP
33	24	H5	K5	-	PC4	I/O	FT	PC4	LCD_SEG22	ADC_IN14/ COMP1_INP
34	25	Н6	L5	-	PC5	I/O	FT	PC5	LCD_SEG23	ADC_IN15/ COMP1_INP

Table 8. STM32L151x6/8/B and STM32L152x6/8/B pin definitions (continued)

		Pins	s						Pins functions	,
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48	Pin name	Pin type ⁽¹⁾	I/O structure	Main function ⁽²⁾ (after reset)	Alternate functions	Additional functions
35	26	F5	M5	18	PB0	I/O	тс	PB0	TIM3_CH3/LCD_SEG5	ADC_IN8/ COMP1_INP/ VREF_OUT
36	27	G5	M6	19	PB1	I/O	FT	PB1	TIM3_CH4/LCD_SEG6	ADC_IN9/ COMP1_INP/ VREF_OUT
37	28	G6	L6	20	PB2	I/O	FT	PB2/BOOT1	BOOT1	-
38	-	ı	M7	ı	PE7	I/O	TC	PE7	-	ADC_IN22/ COMP1_INP
39	-	-	L7	-	PE8	I/O	TC	PE8	-	ADC_IN23/ COMP1_INP
40	-	1	M8	1	PE9	I/O	тс	PE9	TIM2_CH1_ETR	ADC_IN24/ COMP1_INP
41	-	ı	L8	ı	PE10	I/O	TC	PE10	TIM2_CH2	ADC_IN25/ COMP1_INP
42	-	-	M9	-	PE11	I/O	FT	PE11	TIM2_CH3	-
43	-	-	L9	-	PE12	I/O	FT	PE12	TIM2_CH4/SPI1_NSS	-
44	-	-	M10	-	PE13	I/O	FT	PE13	SPI1_SCK	-
45	-	-	M11	-	PE14	I/O	FT	PE14	SPI1_MISO	-
46	-	-	M12	-	PE15	I/O	FT	PE15	SPI1_MOSI	-
47	29	G7	L10	21	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX/ TIM2_CH3/LCD_SEG10	-
48	30	H7	L11	22	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX/ TIM2_CH4/LCD_SEG11	-
49	31	D6	F12	23	V _{SS_1}	S	-	V _{SS_1}	-	-
50	32	E6	G12	24	V _{DD_1}	S	-	V _{DD_1}	-	-
51	33	Н8	L12	25	PB12	I/O	FT	PB12	SPI2_NSS/I2C2_SMBA/ USART3_CK/ LCD_SEG12/TIM10_CH1	ADC_IN18/ COMP1_INP
52	34	G8	K12	26	PB13	I/O	FT	PB13	SPI2_SCK/USART3_CTS/ LCD_SEG13/ TIM9_CH1	ADC_IN19/ COMP1_INP



Table 8. STM32L151x6/8/B and STM32L152x6/8/B pin definitions (continued)

		Pin	S						Pins functions	-
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48	Pin name	Pin type ⁽¹⁾	I/O structure	Main function ⁽²⁾ (after reset)	Alternate functions	Additional functions
53	35	F8	K11	27	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_RTS/ LCD_SEG14//TIM9_CH2	ADC_IN20/ COMP1_INP
54	36	F7	K10	28	PB15	I/O	FT	PB15	SPI2_MOSI/LCD_SEG15/ TIM11_CH1	ADC_IN21/ COMP1_INP/ RTC_REFIN
55	-	-	K9	-	PD8	I/O	FT	PD8	USART3_TX/ LCD_SEG28	-
56	-	-	K8	-	PD9	I/O	FT	PD9	USART3_RX/ LCD_SEG29	-
57	1	-	J12	1	PD10	I/O	FT	PD10	USART3_CK/ LCD_SEG30	-
58	-	-	J11	-	PD11	I/O	FT	PD11	USART3_CTS/ LCD_SEG31	-
59	-	1	J10	1	PD12	I/O	FT	PD12	TIM4_CH1/ USART3_RTS/ LCD_SEG32	-
60	-	-	H12	-	PD13	I/O	FT	PD13	TIM4_CH2/LCD_SEG33	-
61	-	-	H11	-	PD14	I/O	FT	PD14	TIM4_CH3/LCD_SEG34	-
62	-	-	H10	-	PD15	I/O	FT	PD15	TIM4_CH4/LCD_SEG35	-
63	37	F6	E12	-	PC6	I/O	FT	PC6	TIM3_CH1/LCD_SEG24	-
64	38	E7	E11	-	PC7	I/O	FT	PC7	TIM3_CH2/LCD_SEG25	-
65	39	E8	E10	-	PC8	I/O	FT	PC8	TIM3_CH3/LCD_SEG26	-
66	40	D8	D12	-	PC9	I/O	FT	PC9	TIM3_CH4/LCD_SEG27	-
67	41	D7	D11	29	PA8	I/O	FT	PA8	USART1_CK/MCO/ LCD_COM0	-
68	42	C7	D10	30	PA9	I/O	FT	PA9	USART1_TX/LCD_COM1	-
69	43	C6	C12	31	PA10	I/O	FT	PA10	USART1_RX/LCD_COM2	-
70	44	C8	B12	32	PA11	I/O	FT	PA11	USART1_CTS/ SPI1_MISO	USB_DM

Table 8. STM32L151x6/8/B and STM32L152x6/8/B pin definitions (continued)

		Pin	s						Pins functions	,
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48	Pin name	Pin type ⁽¹⁾	I/O structure	Main function ⁽²⁾ (after reset)	Alternate functions	Additional functions
71	45	В8	A12	33	PA12	I/O	FT	PA12	USART1_RTS/ SPI1_MOSI	USB_DP
72	46	A8	A11	34	PA13	I/O	FT	JTMS- SWDIO	JTMS-SWDIO	-
73	-	-	C11	-	PH2	I/O	FT	PH2	-	-
74	47	D5	F11	35	V _{SS_2}	S		V _{SS_2}	-	-
75	48	E5	G11	36	V_{DD_2}	S	-	V _{DD_2}	-	-
76	49	A7	A10	37	PA14	I/O	FT	JTCK -SWCLK	JTCK-SWCLK	-
77	50	A6	A9	38	PA15	I/O	FT	JTDI	TIM2_CH1_ETR/PA15/ SPI1_NSS/ LCD_SEG17	-
78	51	В7	B11	1	PC10	I/O	FT	PC10	USART3_TX/LCD_SEG28 /LCD_SEG40/LCD_COM4	-
79	52	В6	C10	1	PC11	I/O	FT	PC11	USART3_RX/LCD_SEG29 /LCD_SEG41/LCD_COM5	-
80	53	C5	B10	-	PC12	I/O	FT	PC12	USART3_CK/LCD_SEG30 /LCD_SEG42/LCD_COM6	-
81	1	-	C9	-	PD0	I/O	FT	PD0	SPI2_NSS/TIM9_CH1	-
82	-	-	В9	-	PD1	I/O	FT	PD1	SPI2_SCK	-
83	54	B5	C8	1	PD2	I/O	FT	PD2	TIM3_ETR/LCD_SEG31/ LCD_SEG43/LCD_COM7	-
84	-	-	В8	-	PD3	I/O	FT	PD3	USART2_CTS/ SPI2_MISO	-
85	-	-	В7	-	PD4	I/O	FT	PD4	USART2_RTS/ SPI2_MOSI	-
86	-	-	A6	-	PD5	I/O	FT	PD5	USART2_TX	-
87	-	-	В6	-	PD6	I/O	FT	PD6	USART2_RX	-
88	-	-	A5	-	PD7	I/O	FT	PD7	USART2_CK/TIM9_CH2	
89	55	A5	A8	39	PB3	I/O	FT	JTDO	TIM2_CH2/PB3/ SPI1_SCK/LCD_SEG7/ JTDO	COMP2_INM



Table 8. STM32L151x6/8/B and STM32L152x6/8/B pin definitions (continued)

		Pins	5						Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48	Pin name	Pin type ⁽¹⁾	I/O structure	Main function ⁽²⁾ (after reset)	Alternate functions	Additional functions
90	56	A4	A7	40	PB4	I/O	FT	NJTRST	TIM3_CH1/PB4/ SPI1_MISO/LCD_SEG8/ NJTRST	COMP2_INP
91	57	C4	C5	41	PB5	I/O	FT	PB5	I2C1_SMBA/TIM3_CH2/ SPI1_MOSI/LCD_SEG9	COMP2_INP
92	58	D3	B5	42	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1/ USART1_TX	
93	59	C3	B4	43	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2/ USART1_RX	PVD_IN
94	60	B4	A4	44	воото	I	В	воото	-	-
95	61	ВЗ	А3	45	PB8	I/O	FT	PB8	TIM4_CH3/I2C1_SCL/ LCD_SEG16/TIM10_CH1	-
96	62	A3	В3	46	PB9	I/O	FT	PB9	TIM4_CH4/I2C1_SDA/ LCD_COM3/TIM11_CH1	-
97	1	1	C3	-	PE0	I/O	FT	PE0	TIM4_ETR/LCD_SEG36/ TIM10_CH1	-
98	-	-	A2	-	PE1	I/O	FT	PE1	LCD_SEG37/TIM11_CH1	-
99	63	D4	D3	47	V _{SS_3}	S	-	V _{SS_3}	-	-
100	64	E4	C4	48	V_{DD_3}	S	ı	V _{DD_3}	-	-

^{1.} I = input, O = output, S = supply.

6. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The V_{REF+} functionality is provided instead.

Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively. Refer to *Table 2 on page 11*.

^{3.} Applicable to STM32L152xx devices only. In STM32L151xx devices, this pin should be connected to V_{DD} .

^{4.} The PC14 and PC15 I/Os are only configured as OSC32_IN/OSC32_OUT when the LSE oscillator is on (by setting the LSEON bit in the RCC_CSR register). The LSE oscillator pins OSC32_IN/OSC32_OUT can be used as general-purpose PC14/PC15 I/Os, respectively, when the LSE oscillator is off (after reset, the LSE oscillator is off). The LSE has priority over the GPIO function. For more details, refer to Using the OSC32_IN/OSC32_OUT pins as GPIO PC14/PC15 port pins section in the STM32L1xxxx reference manual (RM0038).

The PH0 and PH1 I/Os are only configured as OSC_IN/OSC_OUT when the HSE oscillator is on (by setting the HSEON bit in the RCC_CR register). The HSE oscillator pins OSC_IN/OSC_OUT can be used as general-purpose PH0/PH1 I/Os, respectively, when the HSE oscillator is off (after reset, the HSE oscillator is off). The HSE has priority over the GPIO function



Table 9. Alternate function input/output

								nction number							
D. A	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
Port name						A	Iternate f	unction							·
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
воото	воото	-	-	-	-	-	-	-	-	-	-	-	-	-	-
NRST	NRST	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PA0-WKUP1	-	TIM2_CH1_ETR	-	-	-	-	-	USART2_CTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PA1	-	TIM2_CH2	-	-	-	-	-	USART2_RTS	-	-	[SEG0]	-	-	TIMx_IC2	EVENTOUT
PA2	-	TIM2_CH3	-	TIM9_CH1	-	-	-	USART2_TX	-	-	[SEG1]	-	-	TIMx_IC3	EVENTOUT
PA3	-	TIM2_CH4	-	TIM9_CH2	-	-	-	USART2_RX	-	-	[SEG2]	-	-	TIMx_IC4	EVENTOUT
PA4	-	-	-	-	-	SPI1_NSS	-	USART2_CK	-	-	-	-	-	TIMx_IC1	EVENTOUT
PA5	-	TIM2_CH1_ETR	-	-	-	SPI1_SCK	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PA6	-	-	TIM3_CH1	TIM10_CH1	-	SPI1_MISO	-	-	-	-	[SEG3]	-	-	TIMx_IC3	EVENTOUT
PA7	-	-	TIM3_CH2	TIM11_CH1	-	SPI1_MOSI	-	-	-	-	[SEG4]	-	-	TIMx_IC4	EVENTOUT
PA8	мсо	-	-	-	-	-	-	USART1_CK	-	-	[COM0]	-	-	TIMx_IC1	EVENTOUT
PA9	-	-	-	-	-	-	-	USART1_TX	-	-	[COM1]	-	-	TIMx_IC2	EVENTOUT
PA10	-	-	-	-	-	-	-	USART1_RX	-	-	[COM2]	-	-	TIMx_IC3	EVENTOUT
PA11	-	-	-	-	-	SPI1_MISO	-	USART1_CTS	-	-	-	-	-	TIMx_IC4	EVENTOUT
PA12	-	-	-	-	-	SPI1_MOSI	-	USART1_RTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PA13	JTMS- SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PA14	JTCK- SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PA15	JTDI	TIM2_CH1_ETR	-	-	-	SPI1_NSS	-	-	-	-	SEG17	-	-	TIMx_IC4	EVENTOUT
PB0	-	-	TIM3_CH3	-	-	-	-	-	-	-	[SEG5]	-	-	-	EVENTOUT
PB1	-	-	TIM3_CH4	-	-	-	-	-		-	[SEG6]	-	-	-	EVENTOUT
PB2	BOOT1	-	-	-	-	-	-	-		-	-	-	-	-	EVENTOUT
PB3	JTDO	TIM2_CH2	-	-	-	SPI1_SCK	-	-		-	[SEG7]	-	-	-	EVENTOUT
PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO	-	-	-	-	[SEG8]	-	-	-	EVENTOUT

Pin descriptions

Table 9. Alternate function input/output (continued)

						Digital al	ternate fu	nction number							
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
Port name		•	1	•		А	lternate f	unction	•			•			
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
PB5	-	-	TIM3_CH2	-	I2C1_ SMBA	SPI1_MOSI	-	-	-	-	[SEG9]	-	-	-	EVENTOUT
PB6	-	-	TIM4_CH1	-	I2C1_SCL	-	-	USART1_TX	-	-	-	-	-	-	EVENTOUT
PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	USART1_RX	-	-	-	-	-	-	EVENTOUT
PB8	-	-	TIM4_CH3	TIM10_CH1*	I2C1_SCL	-	-	-	-	-	SEG16	-	-	-	EVENTOUT
PB9	-	-	TIM4_CH4	TIM11_CH1*	I2C1_SDA	-	-	-	-	-	[COM3]	-	-	-	EVENTOUT
PB10	-	TIM2_CH3	-	-	I2C2_SCL	-	-	USART3_TX	-	-	SEG10	-	-	-	EVENTOUT
PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	-	-	SEG11	-	-	-	EVENTOUT
PB12	=	-	-	TIM10_CH1	I2C2_ SMBA	SPI2_NSS	-	USART3_CK	-	-	SEG12	-	-	-	EVENTOUT
PB13	-	-	-	TIM9_CH1	-	SPI2_SCK	-	USART3_CTS	-	-	SEG13	-	-	-	EVENTOUT
PB14	-	-	-	TIM9_CH2	-	SPI2_MISO	-	USART3_RTS	-	-	SEG14	-	-	-	EVENTOUT
PB15	-	-	-	TIM11_CH1	-	SPI2_MOSI	-	-	-	-	SEG15	-	-	-	EVENTOUT
PC0	-	-	-	-	-	-	-	-	-	-	SEG18	-	-	TIMx_IC1	EVENTOUT
PC1	-	-	-	-	-	-	-	-	-	-	SEG19	-	-	TIMx_IC2	EVENTOUT
PC2	-	-	-	-	-	-	-	-	-	-	SEG20	-	-	TIMx_IC3	EVENTOUT
PC3	-	-	-	-	-	-	-	-	-	-	SEG21	-	-	TIMx_IC4	EVENTOUT
PC4	-	-	-	-	-	-	-	-	-	-	SEG22	-	-	TIMx_IC1	EVENTOUT
PC5	-	-	-	-	-	-	-	-	-	-	SEG23	-	-	TIMx_IC2	EVENTOUT
PC6	-	-	TIM3_CH1	-	-	-	-	-	-	-	SEG24	-	-	TIMx_IC3	EVENTOUT
PC7	-	-	TIM3_CH2	-	-	-	-	-	-	-	SEG25	-	-	TIMx_IC4	EVENTOUT
PC8	-	-	TIM3_CH3	-	-	-	-	-	-	-	SEG26	-	-	TIMx_IC1	EVENTOUT
PC9	-	-	TIM3_CH4	-	-	-	-	-	-	-	SEG27	-	-	TIMx_IC2	EVENTOUT
PC10	-	-	-	-	-	-	-	USART3_TX	-	-	COM4 / SEG28 / SEG40	-	-	TIMx_IC3	EVENTOUT





Table 9. Alternate function input/output (continued)

						Digital al	ternate fu	nction number							
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
Port name			1	l		A	lternate f	unction		I					
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
PC11		-	-	-	-	-	-	USART3_RX	-	-	COM5 / SEG29 / SEG41	-		TIMx_IC4	EVENTOUT
PC12	-	-	-	-	-	-	-	USART3_CK	-	-	COM6 / SEG30 / SEG42	-	-	TIMx_IC1	EVENTOUT
PC13- WKUP2	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PC14- OSC32_IN	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PC15- OSC32_OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PD0	-	-	-	TIM9_CH1	-	SPI2_NSS	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PD1	-	-	-	-	-	SPI2_SCK	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PD2	-	-	TIM3_ETR	-	-	-	-	-	-	-	COM7 / SEG31 / SEG43	-	-	TIMx_IC3	EVENTOUT
PD3	-	-	-	-	-	SPI2_MISO	-	USART2_CTS	-	-	-	-	-	TIMx_IC4	EVENTOUT
PD4	-	-	-	-	-	SPI2_MOSI	-	USART2_RTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PD5	-	-	-	-	-	-		USART2_TX	-	-		-	-	TIMx_IC2	EVENTOUT
PD6	-	-	-	-	-	-	-	USART2_RX	-	-	-	-	-	TIMx_IC3	EVENTOUT
PD7	-	-	-	TIM9_CH2	-	-	-	USART2_CK	-	-	-	-	-	TIMx_IC4	EVENTOUT
PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	-	-	TIMx_IC1	EVENTOUT
PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	-	-	TIMx_IC2	EVENTOUT
PD10	-	-	-	-	-	-	-	USART3_CK	-	-	-	-	-	TIMx_IC3	EVENTOUT
PD11	-	-	-	-	-	-	-	USART3_CTS	-	-	-	-	-	TIMx_IC4	EVENTOUT
PD12	-	-	TIM4_CH1	-	-	-	-	USART3_RTS	-	-	-	-	-	TIMx_IC1	EVENTOUT

Pin descriptions

Table 9. Alternate function input/output (continued)

						Digital al	ternate fu	nction number							
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
Port name			L			A	lternate fu	unction		I	I		I		
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
PD13	-	-	TIM4_CH2	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PD15	-	-	TIM4_CH4	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PE0	-	-	TIM4_ETR	TIM10_CH1	-	-	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PE1	-	-		TIM11_CH1	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PE2	TRACEC K	-	TIM3_ETR	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PE3	TRACED 0	-	TIM3_CH1	-	-	-	-	-	-	-	-	_	-	TIMx_IC4	EVENTOUT
PE4	TRACED 1	-	TIM3_CH2	-	-	-	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PE5	TRACED 2	-	-	TIM9_CH1*	-	-	1	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PE6	TRACED 3	-	-	TIM9_CH2*	-	-	1	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PE7	-	-	-	-	1	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PE8	-	-	-	-	1	-	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PE9	-	TIM2_CH1_ETR	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PE10	-	TIM2_CH2	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PE11	-	TIM2_CH3	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PE12	-	TIM2_CH4	-	-	1	SPI1_NSS	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PE13	-	-	-	-	1	SPI1_SCK	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PE14	-	-	-	-	-	SPI1_MISO	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PE15	-	-	-	-	-	SPI1_MOSI	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PH0- OSC_IN	-	-	-	-	1	-	-	-	-	-	-	-	-	-	-





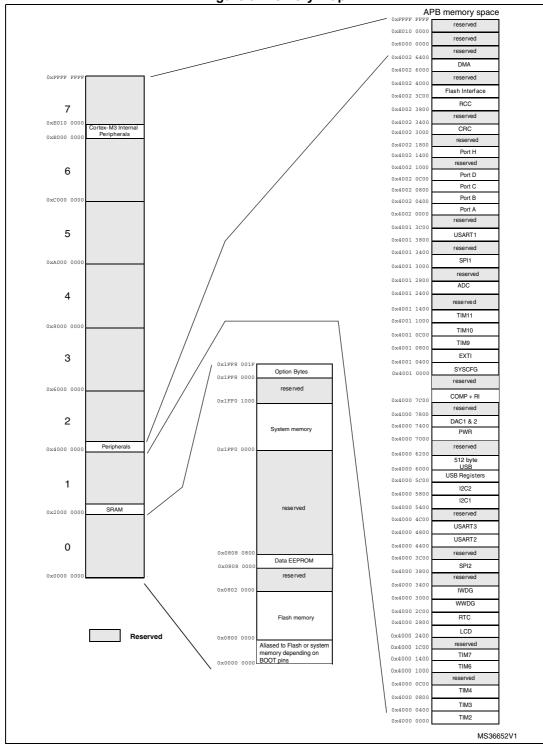
Table 9. Alternate function input/output (continued)

						Digital al	ternate fu	nction number							
Boot waren	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
Port name						А	Iternate f	unction							
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
PH1- OSC_OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PH2	-	=	-	=	=	-	-	=	-	-	-	-	-	-	-

5 Memory mapping

The memory map is shown in Figure 9.

Figure 9. Memory map





6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25$ °C and $T_A = T_A$ max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\sigma$).

Please refer to device ErrataSheet for possible latest changes of electrical characteristics.

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.6 V (for the 1.65 V \leq V_{DD} \leq 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean $\pm 2\sigma$).

6.1.3 Typical curves

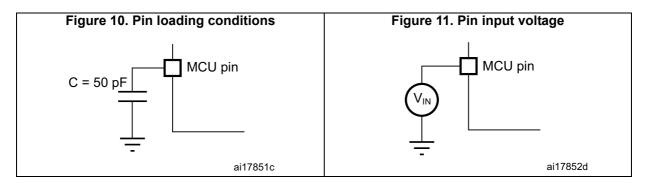
Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 10.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.



6.1.6 Power supply scheme

Standby-power circuitry (OSC32K,RTC, Wake-up logic RTC backup registers) Ю GP I/Os Logic Kernel logic (CPU, Digital & Memories) Regulator N × 100 nF + 1 × 10 µF V_{SS1/2/.../N} 100 nF Analog: + 1 µF ADC/ RCs, 100 nF V_{REF} DAC PLL, MS32461V1

Figure 12. Power supply scheme

6.1.7 Optional LCD power supply scheme

Option 2

Option 2

V_{SS1/2/...N}

V_{SEL}

Step-up

Converter

V_{CD}

V_{SS1/2/...N}

MS32462V1

Figure 13. Optional LCD power supply scheme

- 1. Option 1: LCD power supply is provided by a dedicated VLCD supply source, VSEL switch is open.
- Option 2: LCD power supply is provided by the internal step-up converter, VSEL switch is closed, an external capacitance is needed for correct behavior of this converter.

6.1.8 Current consumption measurement

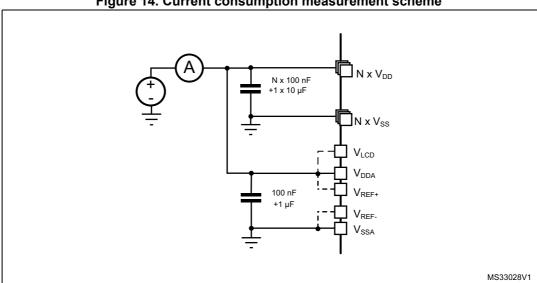


Figure 14. Current consumption measurement scheme

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 10: Voltage characteristics*, *Table 11: Current characteristics*, and *Table 12: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Symbol	Ratings	Min	Max	Unit
V _{DD} -V _{SS}	External main supply voltage (including V _{DDA} and V _{DD}) ⁽¹⁾	-0.3	4.0	
V _{IN} ⁽²⁾	Input voltage on five-volt tolerant pin	V _{SS} -0.3	V _{DD} +4.0	V
VIN.	Input voltage on any other pin	V _{SS} -0.3	4.0	
∆V _{DDx}	Variations between different V _{DD} power pins	-	50	mV
V _{SSX} -V _{SS}	Variations between all different ground pins ⁽³⁾	-	50	IIIV
V _{REF+} –V _{DDA}	Allowed voltage difference for V _{REF+} > V _{DDA}	-	0.4	V
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	see Section 6	.3.11	-

Table 10. Voltage characteristics

- 2. V_{IN} maximum must always be respected. Refer to *Table 11* for maximum allowed injected current values.
- 3. Include VREF- pin.

Unit Symbol Ratings Max. Total current into V_{DD}/V_{DDA} power lines (source)⁽¹⁾ 80 $I_{VDD\Sigma}$ Total current out of V_{SS} ground lines (sink)⁽¹⁾ 80 $I_{VSS\Sigma}$ 25 Output current sunk by any I/O and control pin I_{10} Output current sourced by any I/O and control pin - 25 Injected current on five-volt tolerant I/O(3) -5/+0I_{INJ(PIN)} (2) Injected current on any other pin (4) ± 5 mΑ Total injected current (sum of all I/O and control pins)⁽⁵⁾ ΣI_{INJ(PIN)} ± 25

Table 11. Current characteristics

- All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
- 2. Negative injection disturbs the analog performance of the device. See note in Section 6.3.17.
- Positive current injection is not possible on these I/Os. A negative injection is induced by V_{IN}<V_{SS}. I_{INJ(PIN)} must never be exceeded. Refer to *Table 10* for maximum allowed input voltage values.
- 4. A positive injection is induced by V_{IN} > V_{DD} while a negative injection is induced by V_{IN} < V_{SS}. I_{INJ(PIN)} must never be exceeded. Refer to *Table 10: Voltage characteristics* for the maximum allowed input voltage
- When several inputs are submitted to a current injection, the maximum ΣI_{INJ(PIN)} is the absolute sum of the
 positive and negative injected currents (instantaneous values).



All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

Table 12. Thermal characteristics

Symbol	Ratings	Value	Unit
T _{STG}	Storage temperature range	-65 to +150	°C
T _J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 13. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit	
f _{HCLK}	Internal AHB clock frequency	-	0	32		
f _{PCLK1}	Internal APB1 clock frequency	-	0	32	MHz	
f _{PCLK2}	Internal APB2 clock frequency	-	0	32		
		BOR detector disabled	1.65	3.6		
V_{DD}	Standard operating voltage	BOR detector enabled, at power on	1.8	3.6	V	
		BOR detector disabled, after power on	1.65	3.6		
V _{DDA} ⁽¹⁾	Analog operating voltage (ADC and DAC not used)	Must be the same voltage as	1.65	3.6	V	
VDDA`	Analog operating voltage (ADC or DAC used)	$V_{DD}^{(2)}$	1.8	3.6	V	
	Input voltage on FT pins ⁽³⁾	2.0 V ≤V _{DD} ≤ 3.6 V	-0.3	5.5		
V_{IN}	Input voltage on BOOT0 pin Input voltage on any other pin	$1.65 \text{ V} \le \text{V}_{DD} \le 2.0 \text{ V}$	-0.3 0 -0.3	5.25 5.5 V _{DD} +0.3	V	
P_D	Power dissipation at T _A = 85 °C ⁽⁴⁾	BGA100 package	-	339	mW	
TA	Temperature range	Maximum power dissipation	pation –40 85		°C	
IA	remperature range	Low power dissipation ⁽⁵⁾	-40	105		
TJ	Junction temperature range	-40 °C ≤T _A ≤105°C	-40	105	°C	

^{1.} When the ADC is used, refer to *Table 54: ADC characteristics*.



^{2.} It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.

^{3.} To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up/pull-down resistors must be disabled.

If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see *Table 12: Thermal characteristics on page 53*).

In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_J max (see *Table 12: Thermal characteristics on page 53*).

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in the following table.

Table 14. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
	V rice time rate	BOR detector enabled	0	-	∞	
t _{VDD} ⁽¹⁾	V _{DD} rise time rate	BOR detector disabled	0	-	1000	υοΛ/
'VDD'	// fall time rate	BOR detector enabled	20	-	∞	µs/V
	V _{DD} fall time rate	BOR detector disabled	0	-	1000	
T (1)	Reset temporization	V _{DD} rising, BOR enabled	-	2	3.3	ma
T _{RSTTEMPO} ⁽¹⁾	Reset temporization	V _{DD} rising, BOR disabled ⁽²⁾	0.4	0.7	1.6	ms
V	Power on/power down reset	Falling edge	1	1.5	1.65	V
V _{POR/PDR}	threshold	Rising edge	1.3	1.5	1.65	V
	Brown-out reset threshold 0	Falling edge	1.67	1.7	1.74	
V _{BOR0}	Brown-out reset threshold o	Rising edge	1.69	1.76	1.8	
	Brown-out reset threshold 1	Falling edge	1.87	1.93	1.97	
V _{BOR1}	Brown-out reset threshold 1	Rising edge	1.96	2.03	2.07	
W	Brown-out reset threshold 2	Falling edge	2.22	2.30	2.35	V
V _{BOR2}	brown-out reset threshold 2	Rising edge	2.31	2.41	2.44	V
	Brown-out reset threshold 3	Falling edge	2.45	2.55	2.60	
V _{BOR3}	Drown-out reset threshold 3	Rising edge	2.54	2.66	2.7	
	Drown out root throshold 4	Falling edge	2.68	2.8	2.85	
V _{BOR4}	Brown-out reset threshold 4	Rising edge	2.78	2.9	2.95	

Table 14. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V	Programmable voltage detector	Falling edge	1.8	1.85	1.88	
V_{PVD0}	threshold 0	Rising edge	1.88	1.94	1.99	
V	PVD threshold 1	Falling edge	1.98	2.04	2.09	
V_{PVD1}	PVD tilleshold 1	Rising edge	2.08	2.14	2.18	
V	PVD threshold 2	Falling edge	2.20	2.24	2.28	
V_{PVD2}	PVD tilleshold 2	Rising edge	2.28	2.34	2.38	
V	PVD threshold 3	Falling edge	2.39	2.44	2.48	V
V_{PVD3}		Rising edge	2.47	2.54	2.58	v
M	PVD threshold 4	Falling edge	2.57	2.64	2.69	
V_{PVD4}		Rising edge	2.68	2.74	2.79	
V	DVD throughold 5	Falling edge	2.77	2.83	2.88	
V_{PVD5}	PVD threshold 5	Rising edge	2.87	2.94	2.99	
M	DVD throughold C	Falling edge	2.97	3.05	3.09	
V_{PVD6}	PVD threshold 6	Rising edge	3.08	3.15	3.20	
		BOR0 threshold	-	40	-	
V_{hyst}	Hysteresis voltage	All BOR and PVD thresholds excepting BOR0	-	100	-	mV

^{1.} Guaranteed by characterization results.

^{2.} Valid for device version without BOR at power up. Please see option "T" in Ordering information scheme for more details.

6.3.3 Embedded internal reference voltage

The parameters given in the following table are based on characterization results, unless otherwise specified.

Table 15. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address		
IVDELINI ('AI	Raw data acquired at temperature of 30 °C, V _{DDA} = 3 V	0x1FF8 0078-0x1FF8 0079		

Table 16. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{REFINT out} ⁽¹⁾	Internal reference voltage	-40 °C < T _J < +105 °C	1.202	1.224	1.242	V
I _{REFINT}	Internal reference current consumption	-	-	1.4	2.3	μΑ
T _{VREFINT}	Internal reference startup time	-	-	2	3	ms
V _{VREF_MEAS}	V _{DDA} and V _{REF+} voltage during V _{REFINT} factory measure	-	2.99	3	3.01	V
A _{VREF_MEAS}	Accuracy of factory-measured V _{REF} value ⁽²⁾	Including uncertainties due to ADC and V _{DDA} /V _{REF+} values	-	-	±5	mV
T _{Coeff} ⁽³⁾	Temperature coefficient	-40 °C < T _J < +105 °C	-	25	100	ppm/°C
A _{Coeff} ⁽³⁾	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
V _{DDCoeff} ⁽³⁾	Voltage coefficient	3.0 V < V _{DDA} < 3.6 V	-	-	2000	ppm/V
T _{S_vrefint} (3)(4)	ADC sampling time when reading the internal reference voltage	-	5	10	-	μs
T _{ADC_BUF} ⁽³⁾	Startup time of reference voltage buffer for ADC	-	-	-	10	μs
I _{BUF_ADC} (3)	Consumption of reference voltage buffer for ADC	-	-	13.5	25	μА
I _{VREF_OUT} (3)	VREF_OUT output current ⁽⁵⁾	-	-	-	1	μA
C _{VREF_OUT} (3)	VREF_OUT output load	-	-	-	50	pF
I _{LPBUF} ⁽³⁾	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V _{REFINT_DIV1} (3)	1/4 reference voltage	-	24	25	26	
V _{REFINT_DIV2} (3)	1/2 reference voltage	-	49	50	51	% V _{REFINT}
V _{REFINT_DIV3} (3)	3/4 reference voltage	-	74	75	76	

^{1.} Tested in production.

^{2.} The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.

^{3.} Guaranteed by characterization results.

^{4.} Shortest sampling time can be determined in the application by multiple iterations.

^{5.} To guarantee less than 1% VREF_OUT deviation.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 14: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

The current consumption values are derived from the tests performed under ambient temperature Ta=25°C and VDD supply voltage conditions summarized in *Table 13: General operating conditions*, unless otherwise specified. The MCU is placed under the following conditions:

The MCU is placed under the following conditions:

- V_{DD} = 3.6 V
- All I/O pins are configured in analog input mode.
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time, 64-bit access and prefetch is adjusted depending on fhclk frequency and voltage range to provide the best CPU performance.
- When the peripherals are enabled f_{APB1} = f_{APB2} = f_{AHB}
- When PLL is ON, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used).
- The HSE user clock applied to OSC_IN input follows the characteristics specified in Table 26: High-speed external user clock characteristics.



Table 17. Current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	eter Conditi	litions	f	Тур	Max ⁽¹⁾			Unit
Symbol	raiametei	Cond	iiioiis	f _{HCLK}	тур	55 °C	85 °C	105 °C	
			Range 3,	1 MHz	270	400	400	400	
			V _{CORE} =1.2 V	2 MHz	470	600	600	600	μA
		f _{HSE} = f _{HCLK}	VOS[1:0] = 11	4 MHz	890	1025	1025	1025	
		up to 16 MHz,	Range 2.	4 MHz	1	1.3	1.3	1.3	
Supply	included f _{HSE} = f _{HCLK} /2	V _{CORE} =1.5 V	8 MHz	2	2.5	2.5	2.5		
	above 16 MHz	VOS[1:0] = 10	16 MHz	3.9	5	5	5		
	Supply		Range 1, V _{CORE} =1.8 V VOS[1:0] = 01	8 MHz	2.16	3	3	3	
I _{DD (Run}	current in Run mode,			16 MHz	4.8	5.5	5.5	5.5	
from	code			32 MHz	9.6	11	11	11	
Flash)	executed from Flash	HSI clock source (16 MHz)	Range 2, V _{CORE} =1.5 V VOS[1:0] = 10	16 MHz	4	5	5	5	mA
			Range 1, V _{CORE} =1.8 V VOS[1:0] = 01	32 MHz	9.4	11	11	11	
		MSI clock, 65 kHz	Range 3,	65 kHz	0.05	0.085	0.09	0.1	
		MSI clock, 524 kHz	V _{CORE} =1.2 V	524 kHz	0.15	0.185	0.19	0.2	
		MSI clock, 4.2 MHz	VOS[1:0] = 11	4.2 MHz	0.9	1	1	1	

^{1.} Guaranteed by characterization results, unless otherwise specified.



^{2.} Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 18. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions		f _{HCLK}	Тур		Unit		
Syllibol	Farailletei	Cond	Conditions		тур	55 °C	85 °C	105 °C	
			Range 3,	1 MHz	200	300	300	300	
			V _{CORE} =1.2 V	2 MHz	380	500	500	500	μΑ
		f _{HSE} = f _{HCLK}	VOS[1:0] = 11	4 MHz	720	860	860	860 ⁽³⁾	
		up to 16 MHz,	Range 2.	4 MHz	0.9	1	1	1	
		included f _{HSE} = f _{HCLK} /2	V _{CORE} =1.5 V	8 MHz	1.65	2	2	2	
	Supply current in Run mode, code executed	above 16 MHz (PLL ON) ⁽²⁾	VOS[1:0] = 10	16 MHz	3.2	3.7	3.7	3.7	
 i			Range 1, V _{CORE} =1.8 V VOS[1:0] = 01	8 MHz	2	2.5	2.5	2.5	
				16 MHz	4	4.5	4.5	4.5	
from	from RAM,			32 MHz	7.7	8.5	8.5	8.5	mA
RAM)	Flash switched off	HSI clock source (16 MHz)	Range 2, V _{CORE} =1.5 V VOS[1:0] = 10	16 MHz	3.3	3.8	3.8	3.8	
			Range 1, V _{CORE} =1.8 V VOS[1:0] = 01	32 MHz	7.8	9.2	9.2	9.2	
		MSI clock, 65 kHz	COIL	65 kHz	40	60	60	80	
		MSI clock, 524 kHz		524 kHz	110	140	140	160	μΑ
		MSI clock, 4.2 MHz	VOS[1:0] = 11	4.2 MHz	700	800	800	820	

^{1.} Guaranteed by characterization results, unless otherwise specified.

^{2.} Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

^{3.} Tested in production.

Table 19. Current consumption in Sleep mode

Comple of	Downston	Cond	litions	_	True		Max ⁽¹)	l lmi4
Symbol	Parameter	Cond	litions	f _{HCLK}	Тур	55 °C	85 °C	105 °C	Unit
			Range 3, V _{CORE} =1.2 V VOS[1:0] = 11	1 MHz	80	140	140	140	
				2 MHz	150	210	210	210	
				4 MHz	280	330	330	330 ⁽³⁾	
		f _{HSE} = f _{HCLK} up to 16 MHz included,	Range 2,	4 MHz	280	400	400	400	
		$f_{HSE} = f_{HCLK}/2$	V _{CORE} =1.5 V	8 MHz	450	550	550	550	
	Supply	above 16 MHz (PLL ON) ⁽²⁾	VOS[1:0] = 10	16 MHz	900	1050	1050	1050	
	current in Sleep	,	Range 1,	8 MHz	550	650	650	650	
	mode, code		V _{CORE} =1.8 V	16 MHz	1050	1200	1200	1200	
execute from R Flash	executed		VOS[1:0] = 01	32 MHz	2300	2500	2500	2500	μA
	switched	HSI clock source (16 MHz)	Range 2, V _{CORE} =1.5 V VOS[1:0] = 10	16 MHz	1000	1100	1100	1100	
			Range 1, V _{CORE} =1.8 V VOS[1:0] = 01	32 MHz	2300	2500	2500	2500	
		MSI clock, 65 kHz	Range 3, V _{CORE} =1.2 V VOS[1:0] = 11	65 kHz	30	50	50	60	
I _{DD} (Sleep)		MSI clock, 524 kHz		524 kHz	50	70	70	80	
(Sieep)		MSI clock, 4.2 MHz		4.2 MHz	200	240	240	250	
			Range 3, V _{CORE} =1.2 V VOS[1:0] = 11	1 MHz	80	140	140	140	
				2 MHz	150	210	210	210	
				4 MHz	290	350	350	350	
		f _{HSE} = f _{HCLK} up to 16 MHz included,	Range 2,	4 MHz	300	400	400	400	
	Supply	$f_{HSE} = f_{HCLK}/2$	V _{CORE} =1.5 V	8 MHz	500	600	600	600	
	current in	above 16 MHz (PLL ON) ⁽²⁾	VOS[1:0] = 10	16 MHz	1000	1100	1100	1100	
	Sleep mode,	,	Range 1,	8 MHz	550	650	650	650	μA
	code		V _{CORE} =1.8 V	16 MHz	1050	1200	1200	1200	μ/ (
	executed from Flash		VOS[1:0] = 01	32 MHz	2300	2500	2500	2500	
		F	Range 2, V _{CORE} =1.5 V VOS[1:0] = 10	16 MHz	1000	1100	1100	1100	
		(16 MHz)	Range 1, V _{CORE} =1.8 V VOS[1:0] = 01	32 MHz	2300	2500	2500	2500	



Table 19. Current consumption in Sleep mode (continued)

Complete	Parameter	Conditions		f _{HCLK}	Typ	Max ⁽¹⁾			Unit
Symbol					Тур	55 °C	85 °C	105 °C	Oilit
	Supply current in Sleep	MSI clock, 65 kHz	Range 3, V _{CORE} =1.2V VOSI1:01 = 11	65 kHz	40	70	70	80	
		MSI clock, 524 kHz		524 kHz	60	90	90	100	
(Sleep)	mode, code executed from Flash	MSI clock, 4.2 MHz		4.2 MHz	210	250	250	260	μА

- 1. Guaranteed by characterization results, unless otherwise specified.
- 2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register)
- 3. Tested in production



Table 20. Current consumption in Low power run mode

Symbol	Parameter		Conditions		Тур	Max (1)	Unit
				T _A = -40 °C to 25 °C	9	12	
			MSI clock, 65 kHz f _{HCLK} = 32 kHz	T _A = 85 °C	17.5	24	
		All peripherals	HOLK 02 KIIZ	T _A = 105 °C	31	46	
		OFF, code		T _A = -40 °C to 25 °C	14	17	
		executed from RAM,	MSI clock, 65 kHz f _{HCLK} = 65 kHz	T _A = 85 °C	22	29	
		Flash switched	HCLK OO MIZ	T _A = 105 °C	35	51	
		OFF, V _{DD}		$T_A = -40 ^{\circ}\text{C} \text{ to } 25 ^{\circ}\text{C}$	37	42	
Supply current in		from 1.65 V to 3.6 V	MSI clock, 131 kHz	T _A = 55 °C	37	42	
	Supply		f _{HCLK} = 131 kHz	T _A = 85 °C	37	42	μΑ
				T _A = 105 °C	48	65	
Run)	Low power run mode	All	MSI clock, 65 kHz f _{HCLK} = 32 kHz	$T_A = -40 ^{\circ}\text{C} \text{ to } 25 ^{\circ}\text{C}$	24	32	
	ruii iiiou e			T _A = 85 °C	33	42	
				T _A = 105 °C	48	64	
		peripherals		T _A = -40 °C to 25 °C	31	40	
		OFF, code executed	MSI clock, 65 kHz f _{HCLK} = 65 kHz	T _A = 85 °C	40	48	
		from Flash, V _{DD} from	HOLK SO WIL	T _A = 105 °C	54	70	
		1.65 V to		T _A = -40 °C to 25 °C	48	58	
		3.6 V	MSI clock, 131 kHz	T _A = 55 °C	54	63	
			f _{HCLK} = 131 kHz	T _A = 85 °C	56	65	
				T _A = 105 °C	70	90	
I _{DD} Max (LP Run) ⁽²⁾	Max allowed current in Low power run mode	V _{DD} from 1.65 V to 3.6 V	-	-	-	200	

^{1.} Guaranteed by characterization results, unless otherwise specified.

^{2.} This limitation is related to the consumption of the CPU core and the peripherals that are powered by the regulator. Consumption of the I/Os is not included in this limitation.

Table 21. Current consumption in Low power sleep mode

Symbol	Parameter		Conditions		Тур	Max (1)	Unit
			MSI clock, 65 kHz f _{HCLK} = 32 kHz Flash OFF	T _A = -40 °C to 25 °C	4.4	-	
			MSI clock, 65 kHz	$T_A = -40 ^{\circ}\text{C} \text{ to } 25 ^{\circ}\text{C}$	17.5	25	
			f _{HCLK} = 32 kHz	T _A = 85 °C	22	27	
		All	Flash ON	T _A = 105 °C	31	39	
		peripherals OFF, V _{DD}	MSI clock, 65 kHz	$T_A = -40 ^{\circ}\text{C} \text{ to } 25 ^{\circ}\text{C}$	18	26	
		from 1.65 V	f _{HCLK} = 65 kHz,	T _A = 85 °C	23	28	
		to 3.6 V	Flash ON	T _A = 105 °C	31	40	
				T _A = -40 °C to 25 °C	22	30	
	Supply current in Low power sleep			T _A = 55 °C	24	32	
I _{DD} (LP			f _{HCLK} = 131 kHz, Flash ON	T _A = 85 °C	26	34	
Sleep)				T _A = 105 °C	34	45	
	mode		MSI clock, 65 kHz f _{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	17.5	25	μA
				T _A = 85 °C	22	27	- µ' \
				T _A = 105 °C	31	39	
		TIM9 and USART1		T _A = -40 °C to 25 °C	18	26	
		enabled,	MSI clock, 65 kHz f _{HCLK} = 65 kHz	T _A = 85 °C	23	28	
		Flash ON, V _{DD} from	HCLK - 05 KHZ	T _A = 105 °C	31	40	
		1.65 V to 3.6 V		$T_A = -40 ^{\circ}\text{C} \text{ to } 25 ^{\circ}\text{C}$	22	30	
		3.0 V	MSI clock, 131 kHz	T _A = 55 °C	24	32	
			f _{HCLK} = 131 kHz	T _A = 85 °C	26	34	
				T _A = 105 °C	34	45	
I _{DD} Max (LP Sleep)	Max allowed current in Low power Sleep mode	V _{DD} from 1.65 V to 3.6 V	-	-	-	200	

^{1.} Guaranteed by characterization results, unless otherwise specified.



Table 22. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Co	onditions		Typ (1)	Max (1)(2)	Unit
				$T_A = -40$ °C to 25°C $V_{DD} = 1.8 \text{ V}$	1.2	2.75	
			LCD	$T_A = -40^{\circ}C \text{ to } 25^{\circ}C$	1.4	4	
			OFF	T _A = 55°C	2.6	6	
				T _A = 85°C	4.8	10	
		RTC clocked by LSI,		T _A = 105°C	10.2	23	
		regulator in LP mode,		$T_A = -40^{\circ}C \text{ to } 25^{\circ}C$	3.3	6	
		HSI and HSE OFF (no independent	LCD ON (static	T _A = 55°C	4.5	8	
		watchdog)	duty) ⁽³⁾	T _A = 85°C	6.6	12	
				T _A = 105°C	13.6	27	
	Supply current in Stop mode with RTC enabled			$T_A = -40$ °C to 25°C	7.7	10	
			LCD ON (1/8 duty) ⁽⁴⁾	T _A = 55°C	8.6	12	-
				T _A = 85°C	10.7	16	
				T _A = 105°C	19.8	40	
			LCD OFF	$T_A = -40$ °C to 25°C	1.6	4	
I _{DD} (Stop				T _A = 55°C	2.7	6	μA
with RTC)				T _A = 85°C	4.8	10	
				T _A = 105°C	10.3	23	
		RTC clocked by LSE	LCDON	$T_A = -40$ °C to 25°C	3.6	6	
		external clock (32.768 kHz), regulator in LP		T _A = 55°C	4.6	8	
		mode, HSI and HSE	(static duty) ⁽³⁾	T _A = 85°C	6.7	12	
		OFF (no independent watchdog)	,	T _A = 105°C	10.9	23	
				$T_A = -40^{\circ}C$ to 25°C	7.6	10	
			LCD ON (1/8	T _A = 55°C	8.6	12	
			duty) ⁽⁴⁾	T _A = 85°C	10.7	16	
				T _A = 105°C	19.8	40	
				T _A = -40°C to 25°C V _{DD} = 1.8 V	1.45	-	
		RTC clocked by LSE (no independent watchdog) ⁽⁵⁾	LCD OFF	T _A = -40°C to 25°C V _{DD} = 3.0 V	1.9	-	
				T _A = -40°C to 25°C V _{DD} = 3.6 V	2.2	-	

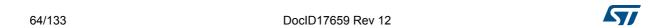


Table 22. Typical and maximum current consumptions in Stop mode (continued)

Symbol	Parameter	Conditions	Typ (1)	Max (1)(2)	Unit	
I _{DD} (Stop)	Supply current	Regulator in LP mode, HSI and HSE OFF, independent watchdog and LSI enabled	$T_A = -40^{\circ}\text{C to } 25^{\circ}\text{C}$	1.1	2.2	
	in Stop mode		$T_A = -40$ °C to 25°C	0.5	0.9	μA
		Regulator in LP mode, LSI, HSI and HSE OFF (no independent watchdog)	T _A = 55°C	1.9	5	, m., r.
			T _A = 85°C	3.7	8	
			T _A = 105°C	8.9	20 ⁽⁶⁾	
	RMS (root	MSI = 4.2 MHz		2	-	
	mean square) supply current	MSI = 1.05 MHz	.,	1.45	-	
I _{DD} (WU from Stop)	during wakeup time when exiting from Stop mode	MSI = 65 kHz ⁽⁷⁾	$V_{DD} = 3.0 \text{ V}$ $T_{A} = -40^{\circ}\text{C to } 25^{\circ}\text{C}$	1.45	-	mA

- 1. The typical values are given for V_{DD} = 3.0 V and max values are given for V_{DD} = 3.6 V, unless otherwise specified.
- 2. Guaranteed by characterization results, unless otherwise specified
- 3. LCD enabled with external VLCD, static duty, division ratio = 256, all pixels active, no LCD connected
- LCD enabled with external VLCD, 1/8 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
- Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8pF loading capacitors.
- 6. Tested in production
- 7. When MSI = 64 kHz, the RMS current is measured over the first 15 µs following the wakeup event. For the remaining time of the wakeup period, the current is similar to the Run mode current.



Table 23. Typical and r	naximum current consu	ımptions in Standby	mode

Symbol	Parameter	Conditions		Тур ⁽¹⁾	Max (1)(2)	Unit	
			T _A = -40 °C to 25 °C V _{DD} = 1.8 V	0.9	-		
		RTC clocked by LSI (no	$T_A = -40 ^{\circ}\text{C} \text{ to } 25 ^{\circ}\text{C}$	1.1	1.8		
		independent watchdog)	T _A = 55 °C	1.42	2.5		
			T _A = 85 °C	1.87	3		
I _{DD}	Supply current in Standby		T _A = 105 °C	2.78	5		
(Standby with RTC)	mode with RTC enabled		T _A = -40 °C to 25 °C V _{DD} = 1.8 V	1	-		
		RTC clocked by LSE (no independent watchdog) ⁽³⁾			1.33	2.9	
					1.59	3.4	
		T _A = 85 °C		2.01	4.3	μA	
			T _A = 105 °C	3.27	6.3		
		Independent watchdog and LSI enabled	T _A = -40 °C to 25 °C	1.1	1.6		
I _{DD}	Supply current in Standby		T _A = -40 °C to 25 °C		0.55		
(Standby)	mode with RTC disabled	Independent watchdog	T _A = 55 °C	0.5	8.0		
		and LSI OFF	T _A = 85 °C	1	1.7		
			T _A = 105 °C	2.5	4 ⁽⁴⁾		
I _{DD (WU} from Standby)	RMS supply current during wakeup time when exiting from Standby mode	-	V _{DD} = 3.0 V T _A = -40 °C to 25 °C	1	-		

^{1.} The typical values are given for V_{DD} = 3.0 V and max values are given for V_{DD} = 3.6 V, unless otherwise specified.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
 - with all peripherals clocked off
 - with only one peripheral clocked on

^{2.} Guaranteed by characterization results, unless otherwise specified.

Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8pF loading capacitors.

^{4.} Tested in production.

Table 24. Peripheral current consumption⁽¹⁾

Peripheral		Туріса				
		Range 1, V _{CORE} =1.8 V VOS[1:0] = 01	Range 2, V _{CORE} =1.5 V VOS[1:0] = 10	Range 3, V _{CORE} =1.2 V VOS[1:0] = 11	Low power sleep and run	Unit
	TIM2	13	10.5	8	10.5	
	TIM3	14	12	9	12	
	TIM4	12.5	10.5	8	11	
	TIM6	5.5	4.5	3.5	4.5	
	TIM7	5.5	5	3.5	4.5	
	LCD	5.5	5	3.5	5	
	WWDG	4	3.5	2.5	3.5	
ADD4	SPI2	5.5	5	4	5	μΑ/MHz
APB1	USART2	9	8	5.5	8.5	(f _{HCLK})
	USART3	10.5	9	6	8	
	I2C1	8.5	7	5.5	7.5	
	I2C2	8.5	7	5.5	6.5	
	USB	12.5	10	6.5	10	
	PWR	4.5	4	3	3.5	
	DAC	9	7.5	6	7	
	COMP	4.5	4	3.5	4.5	
	SYSCFG & RI	3	2.5	2	2.5	
	TIM9	9	7.5	6	7	
	TIM10	6.5	5.5	4.5	5.5	
APB2	TIM11	7	6	4.5	5.5	μΑ/MHz (f _{HCLK})
	ADC ⁽²⁾	11.5	9.5	8	9	('HCLK)
	SPI1	5	4.5	3	4	
	USART1	9	7.5	6	7.5	



Table 24. Peripheral current consumption⁽¹⁾ (continued)

	Typical consumption, V _{DD} = 3.0 V, T _A = 25 °C						
Peripheral		Range 1, V _{CORE} =1.8 V VOS[1:0] = 01	Range 2, V _{CORE} =1.5 V VOS[1:0] = 10	Range 3, V _{CORE} =1.2 V VOS[1:0] = 11	Low power sleep and run	Unit	
	GPIOA	5	4.5	3.5	4		
	GPIOB	5	4.5	3.5	4.5		
	GPIOC	5	4.5	3.5	4.5		
	GPIOD	5	4.5	3.5	4.5		
AHB	GPIOE	5	4.5	3.5	4.5	µA/MHz	
	GPIOH	4	4	3	3.5	(f _{HCLK})	
	CRC	1	0.5	0.5	0.5		
	FLASH	13	11.5	9	18.5		
	DMA1	12	10	8	10.5		
All enabled		166	138	106	130		
I _{DD (RTC)}							
I _{DD (LCD)}							
I _{DD (ADC)} ⁽³⁾							
I _{DD (DAC)} ⁽⁴⁾							
I _{DD (COMP1)}			μΑ				
1	Slow mode		2				
I _{DD} (COMP2)	Fast mode	5					
I _{DD (PVD / BOR)} (5)							
I _{DD (IWDG)}			0.25				

Data based on differential I_{DD} measurement between all peripherals OFF an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (Range 1), f_{HCLK} = 16 MHz (Range 2), f_{HCLK} = 4 MHz (Range 3), f_{HCLK} = 64kHz (Low power run/sleep), f_{APB1} = f_{HCLK}, f_{APB2} = f_{HCLK}, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling.

^{2.} HSI oscillator is OFF for this measure.

^{3.} Data based on a differential IDD measurement between ADC in reset configuration and continuous ADC conversion (HSI consumption not included).

Data based on a differential IDD measurement between DAC in reset configuration and continuous DAC conversion of VDD/2. DAC is in buffered mode, output is left floating.

^{5.} Including supply current of internal reference voltage.

6.3.5 Wakeup time from Low power mode

The wakeup times given in the following table are measured with the MSI RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is the MSI oscillator in the range configured before entering Stop mode
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13*.

Table 25. Low-power mode wakeup timings

Symbol	Parameter	Conditions		Max ⁽¹⁾	Unit
t _{WUSLEEP}	Wakeup from Sleep mode	f _{HCLK} = 32 MHz	0.36	-	
	Wakeup from Low power sleep mode	f _{HCLK} = 262 kHz Flash enabled	32	-	
twusleep_lp	f _{HCLK} = 262 kHz	f _{HCLK} = 262 kHz Flash switched OFF	34	-	
	Wakeup from Stop mode, regulator in Run mode	f _{HCLK} = f _{MSI} = 4.2 MHz	8.2	-	
		f _{HCLK} = f _{MSI} = 4.2 MHz Voltage Range 1 and 2	8.2	9.3	
	Wakeup from Stop mode, regulator in low power mode	f _{HCLK} = f _{MSI} = 4.2 MHz Voltage Range 3	7.8	11.2	μs
t _{WUSTOP}		f _{HCLK} = f _{MSI} = 2.1 MHz	10	12	
		$f_{HCLK} = f_{MSI} = 1.05 \text{ MHz}$	15.5	20	
		$f_{HCLK} = f_{MSI} = 524 \text{ kHz}$	29	35	
		$f_{HCLK} = f_{MSI} = 262 \text{ kHz}$	53	63	
		f _{HCLK} = f _{MSI} = 131 kHz	105	118	
		f _{HCLK} = MSI = 65 kHz	210	237	
t	Wakeup from Standby mode FWU bit = 1	f _{HCLK} = MSI = 2.1 MHz	50	103	
twustdby	Wakeup from Standby mode FWU bit = 0	f _{HCLK} = MSI = 2.1 MHz	2.5	3.2	ms

^{1.} Guaranteed by characterization results, unless otherwise specified



6.3.6 **External clock source characteristics**

High-speed external user clock generated from an external source

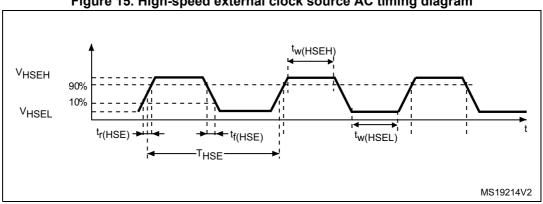
In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in Section 6.3.13. However, the recommended clock input waveform is shown in Figure 15: High-speed external clock source AC timing diagram.

Table 26. High-speed external user clock characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f	User external clock source	CSS is on or PLL is used	1	8	32	MHz
f _{HSE_ext}	frequency	CSS is off, PLL not used	0	0		IVITIZ
V _{HSEH}	OSC_IN input pin high level voltage		0.7V _{DD}	-	V_{DD}	V
V _{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	0.3V _{DD}	V
t _{w(HSEH)} t _{w(HSEL)}	OSC_IN high or low time	-	12	i	ı	ns
t _{r(HSE)}	OSC_IN rise or fall time		-	-	20	115
C _{in(HSE)}	OSC_IN input capacitance	-	-	2.6	-	pF
DuCy _(HSE)	Duty cycle	-	45		55	%
IL	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	μA

^{1.} Guaranteed by design.

Figure 15. High-speed external clock source AC timing diagram





10

_

55

±1

pF

%

μΑ

0.6

45

Low-speed external user clock generated from an external source

The characteristics given in the following table result from tests performed using a lowspeed external clock source, and under ambient temperature and supply voltage conditions summarized in Table 13.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{LSE_ext}	User external clock source frequency		1	32.768	1000	kHz
V _{LSEH}	OSC32_IN input pin high level voltage		0.7V _{DD}	-	V _{DD}	V
V _{LSEL}	OSC32_IN input pin low level voltage	-	V _{SS}	-	0.3V _{DD}	V
$\begin{array}{c} t_{\text{w(LSEH)}} \\ t_{\text{w(LSEL)}} \end{array}$	OSC32_IN high or low time		465	-	ı	ns
t _{r(LSE)}	OSC32 IN rise or fall time		_	_	10	115

Table 27. Low-speed external user clock characteristics⁽¹⁾

Duty cycle

t_{f(LSE)}

 $C_{\text{IN(LSE)}}$

 $DuCy_{(LSE)}$

ΙL

OSC32 IN rise or fall time

OSC32_IN input capacitance

OSC32_IN Input leakage current

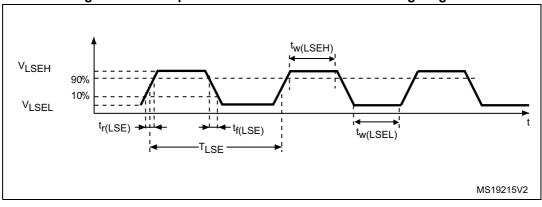


Figure 16. Low-speed external clock source AC timing diagram

 $V_{SS} \leq V_{IN} \leq V_{DD}$

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 28. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).



Guaranteed by design.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{OSC_IN}	Oscillator frequency	-	1		24	MHz
R _F	Feedback resistor	-		200	-	kΩ
С	Recommended load capacitance versus equivalent serial resistance of the crystal (R _S) ⁽³⁾	R _S = 30 Ω	-	20	-	pF
I _{HSE}	HSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	3	mA
	HSE oscillator power	C = 20 pF f _{OSC} = 16 MHz	-	-	2.5 (startup) 0.7 (stabilized)	mA
IDD(HSE)	consumption	C = 10 pF $f_{OSC} = 16 MHz$	-	-	2.5 (startup) 0.46 (stabilized)	IIIA
9 _m	Oscillator transconductance	Startup	3.5	-	-	mA /V
t _{SU(HSE)}	Startup time	V _{DD} is stabilized	-	1	-	ms

Table 28. HSE oscillator characteristics⁽¹⁾⁽²⁾

- 1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
- 2. Guaranteed by characterization results.
- 3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
- 4. t_{SU(HSE)} is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 17*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} . Refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website *www.st.com*.

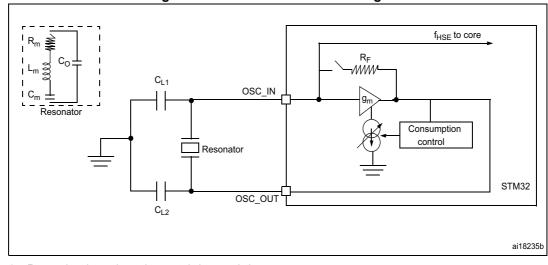


Figure 17. HSE oscillator circuit diagram

1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 29*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{LSE}	Low speed external oscillator frequency	-	-	32.768	-	kHz
R_{F}	Feedback resistor	-	-	1.2	-	$M\Omega$
C ⁽²⁾	Recommended load capacitance versus equivalent serial resistance of the crystal (R _S) ⁽³⁾	R _S = 30 kΩ	-	8	1	pF
I _{LSE}	LSE driving current	$V_{DD} = 3.3 \text{ V}, V_{IN} = V_{SS}$	-	-	1.1	μA
		V _{DD} = 1.8 V	-	450	-	
I _{DD (LSE)}	LSE oscillator current consumption	V _{DD} = 3.0 V	-	600	-	nA
		V _{DD} = 3.6V - 750	750	-		
9 _m	Oscillator transconductance	-	3	-	-	μA/V
t _{SU(LSE)} ⁽⁴⁾	Startup time	V _{DD} is stabilized	-	1	-	s

Table 29. LSE oscillator characteristics $(f_{LSE} = 32.768 \text{ kHz})^{(1)}$

The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details.



Guaranteed by characterization results.

^{2.} Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".

 t_{SU(LSE)} is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note:

For CL1 and CL2, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Figure 18). CL1 and CL2, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2. Load capacitance CL has the following formula: $CL = CL1 \times CL2 / (CL1 + CL2) + Cstray$ where Cstray is the pin capacitance and board or trace PCB-related capacitance. Typically.

it is between 2 pF and 7 pF.

Caution:

To avoid exceeding the maximum value of CL1 and CL2 (15 pF) it is strongly recommended to use a resonator with a load capacitance CL \leq 7 pF. Never use a resonator with a load capacitance of 12.5 pF.

Example: if a resonator is chosen with a load capacitance of CL = 6 pF and Cstray = 2 pF, then CL1 = CL2 = 8 pF.

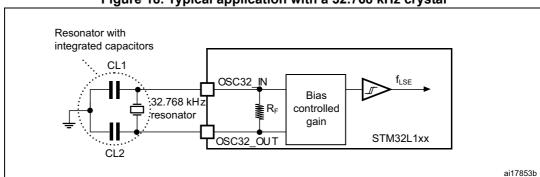


Figure 18. Typical application with a 32.768 kHz crystal

6.3.7 Internal clock source characteristics

The parameters given in the following table are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13*.

High-speed internal (HSI) RC oscillator

Table 30. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{HSI}	Frequency	V _{DD} = 3.0 V	-	16	-	MHz
TRIM ⁽¹⁾⁽²⁾	HSI user-trimmed	Trimming code is not a multiple of 16	-	±0.4	0.7	%
TRIM` '` '	resolution	Trimming code is a multiple of 16	-	-	±1.5	%
		V _{DDA} = 3.0 V, T _A = 25 °C	-1 ⁽³⁾	-	1 ⁽³⁾	%
		$V_{DDA} = 3.0 \text{ V}, T_{A} = 0 \text{ to } 55 ^{\circ}\text{C}$	-1.5	-	1.5	%
	Accuracy of the	$V_{DDA} = 3.0 \text{ V}, T_{A} = -10 \text{ to } 70 ^{\circ}\text{C}$	-2	-	2	%
ACC _{HSI} ⁽²⁾	factory-calibrated	V _{DDA} = 3.0 V, T _A = -10 to 85 °C	-2.5	-	2	%
	HSI oscillator	$V_{DDA} = 3.0 \text{ V}, T_A = -10 \text{ to } 105 ^{\circ}\text{C}$	-4	-	2	%
		V _{DDA} = 1.65 V to 3.6 V T _A = -40 to 105 °C	-4	-	3	%
t _{SU(HSI)} ⁽²⁾	HSI oscillator startup time	-	-	3.7	6	μs
I _{DD(HSI)} ⁽²⁾	HSI oscillator power consumption	-	-	100	140	μΑ

^{1.} The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).

Low-speed internal (LSI) RC oscillator

Table 31. LSI oscillator characteristics

Symbol	Symbol Parameter		Тур	Max	Unit
f _{LSI} ⁽¹⁾ LSI frequency		26	38	56	kHz
$D_{LSI}^{(2)}$ LSI oscillator frequency drift $0^{\circ}\text{C} \leq T_{A} \leq 85^{\circ}\text{C}$		-10	-	4	%
t _{su(LSI)} (3) LSI oscillator startup time		-	-	200	μs
I _{DD(LSI)} ⁽³⁾ LSI oscillator power consumption		-	400	510	nA

^{1.} Tested in production.



^{2.} Guaranteed by characterization results.

^{3.} Tested in production.

^{2.} This is a deviation for an individual part, once the initial frequency has been measured.

^{3.} Guaranteed by design.

Multi-speed internal (MSI) RC oscillator

Table 32. MSI oscillator characteristics

Symbol	Parameter	Condition	Тур	Max	Unit
		MSI range 0	65.5	-	
		MSI range 1	131	-	kHz
		MSI range 2	262	- - - -	KΠZ
f _{MSI}	Frequency after factory calibration, done at V_{DD} = 3.3 V and T_A = 25 °C	MSI range 3	524	-	
	LIDD old value (A Zo C	MSI range 4	1.05	-	
		MSI range 5	2.1	-	MHz
		MSI range 6	4.2	-	
ACC _{MSI}	Frequency error after factory calibration	-	±0.5	-	%
D _{TEMP(MSI)} ⁽¹⁾	MSI oscillator frequency drift 0 °C ≤T _A ≤85 °C	-	±3	-	%
D _{VOLT(MSI)} ⁽¹⁾	MSI oscillator frequency drift 1.65 V ≤V _{DD} ≤3.6 V, T _A = 25 °C	-	-	2.5	%/V
		MSI range 0	0.75	-	
		MSI range 1	1	-	
		MSI range 2	1.5	-	
I _{DD(MSI)} ⁽²⁾	MSI oscillator power consumption	MSI range 3 2.5	-	μA	
		MSI range 4	4.5	-	
		MSI range 5	8	-	
		MSI range 6	15	-	
		MSI range 0	30	-	
		MSI range 1	20	-	
		MSI range 2	15	-	
		MSI range 3	10	-	
t	MSI oscillator startup time	MSI range 4	6	-	116
tsu(MSI)	Mor oscillator startup time	MSI range 5	5		μs
		MSI range 6, Voltage range 1 and 2	3.5	-	
		MSI range 6, Voltage range 3	5	-	



Symbol	Parameter	Condition	Тур	Max	Unit
		MSI range 0	-	40	
		MSI range 1	-	20	
		MSI range 2	-	10	
		MSI range 3	-	4	
+ (2)	t _{STAB(MSI)} (2) MSI oscillator stabilization time	MSI range 4	-	2.5	μs
STAB(MSI)`		MSI range 5	-	2	
		MSI range 6, Voltage range 1 and 2	-	2	
		MSI range 3, Voltage Range 3	-	3	
formanon	MSI oscillator frequency overshoot	Any range to range 5	-	4	MHz
f _{OVER(MSI)}	INOT OSCINATOR ITEQUETICS OVERSHOOT	Any range to range 6	-	6	IVII IZ

Table 32. MSI oscillator characteristics (continued)

6.3.8 **PLL** characteristics

The parameters given in *Table 33* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13*.

Table 33. PLL characteristics

Symbol	Parameter		Value		Unit
Symbol	rarameter	Min	Тур	Max ⁽¹⁾	Oilit
f	PLL input clock ⁽²⁾	2	-	24	MHz
f _{PLL_IN}	PLL input clock duty cycle	45	-	55	%
f _{PLL_OUT}	PLL output clock	2	-	32	MHz
t _{LOCK}	Worst case PLL lock time PLL input = 2 MHz PLL VCO = 96 MHz	-	100	130	μs
Jitter	Cycle-to-cycle jitter	-	-	± 600	ps
I _{DDA} (PLL)	Current consumption on V _{DDA}	-	220	450	
I _{DD} (PLL)	Current consumption on V _{DD}	-	120	150	μΑ

^{1.} Guaranteed by characterization results.



^{1.} This is a deviation for an individual part, once the initial frequency has been measured.

^{2.} Guaranteed by characterization results.

Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by $f_{\text{PLL_OUT}}$.

6.3.9 Memory characteristics

The characteristics are given at T_A = -40 to 105 $^{\circ}$ C unless otherwise specified.

RAM memory

Table 34. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
VRM	Data retention mode ⁽¹⁾	STOP mode (or RESET)	1.65	-	-	V

Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

Flash memory and data EEPROM

Table 35. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Тур	Max ⁽¹⁾	Unit
V _{DD}	Operating voltage Read / Write / Erase	-	1.65	-	3.6	V
	Programming / erasing time for	Erasing	ı	3.28	3.94	
t _{prog}	byte / word / double word / half- page	Programming	-	3.28	3.94	ms
	Average current during whole program/erase operation	T - 25 °C V - 3 6 V	-	300	-	μA
l _{DD}	Maximum current (peak) during program/erase operation	$T_A = 25 ^{\circ}\text{C}, V_{DD} = 3.6 ^{\circ}\text{V}$	-	1.5	2.5	mA

^{1.} Guaranteed by design.

Table 36. Flash memory, data EEPROM endurance and data retention

Symbol	Dozometov	Conditions	Value			Unit	
Symbol	Parameter	Conditions	Min ⁽¹⁾	Тур	Max	Oilit	
NCYC ⁽²⁾	Cycling (erase / write) Program memory	$T_A = -40^{\circ}C$ to	10	-	-	- kcycles	
	Cycling (erase / write) EEPROM data memory	105 °C	300	-	-		
	Data retention (program memory) after 10 kcycles at T _A = 85 °C	TRET = +85 °C	30	-	-		
t _{RET} ⁽²⁾	Data retention (EEPROM data memory) after 300 kcycles at T_A = 85 °C	TRET = 100 C	30	-	-	voare	
TRET'-'	Data retention (program memory) after 10 kcycles at T _A = 105 °C	TRET = +105 °C	10	-	-	years	
	Data retention (EEPROM data memory) after 300 kcycles at T _A = 105 °C	11121 - 1103 0	10	-	-		

^{1.} Guaranteed by characterization results.

^{2.} Characterization is done according to JEDEC JESD22-A117.

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 37*. They are based on the EMS levels and classes defined in application note AN1709.

Level/ **Symbol Parameter Conditions** Class $V_{DD} = 3.3 \text{ V, LQFP100, T}_{A} = +25 \text{ °C,}$ Voltage limits to be applied on any I/O pin to V_{FESD} $f_{HCLK} = 32 \text{ MHz}$ 2B induce a functional disturbance conforms to IEC 61000-4-2 $V_{DD} = 3.3 \text{ V, LQFP100, } T_A = +25$ Fast transient voltage burst limits to be V_{EFTB} applied through 100 pF on V_{DD} and V_{SS} 4A f_{HCLK} = 32 MHz pins to induce a functional disturbance conforms to IEC 61000-4-4

Table 37. EMS characteristics

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.



To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

				Max vs	s. frequency		
Symbol	Parameter	Conditions	Monitored frequency band	4 MHz voltage Range 3	16 MHz voltage Range 2	32 MHz voltage Range 1 -5 -7	Unit
		V _{DD} = 3.3 V,	0.1 to 30 MHz	3	-6	-5	
c	Peak level	T _A = 25 °C,	30 to 130 MHz	18	4	-7	dΒμV
S _{EMI}	reak level	LQFP100 package compliant with IEC	130 MHz to 1GHz	15	5	-7	
	61967-2	61967-2	SAE EMI Level	2.5	2	1	-

Table 38. EMI characteristics

6.3.11 Electrical sensitivity characteristics

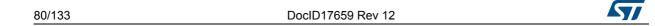
Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Symbol	Ratings	Conditions	Packages	Class	Maximum value ⁽¹⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	All	2	2000	V
V _{ESD(CDM)}	Electrostatic discharge voltage (charge device model)	T _A = +25 °C, conforming to JESD22-C101	All	III	500	V

Table 39, ESD absolute maximum ratings



^{1.} Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 40. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T _A = +105 °C conforming to JESD78A	II level A

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error, out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation, LCD levels, etc.).

The test results are given in Table 41.

Table 41. I/O current injection susceptibility

		Functional s		
Symbol	Description	Negative injection	Positive injection	Unit
	Injected current on all 5 V tolerant (FT) pins	-5	+0	mA
INJ	Injected current on any other pin	-5	+5	IIIA

Note:

It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 42* are derived from tests performed under conditions summarized in *Table 13*. All I/Os are CMOS and TTL compliant.

Table 42. I/O static characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit		
V _{IL}	Input low level voltage	-	-	-	-	0.3V _{DD} ⁽¹⁾			
V	Input high level voltage	Stand	lard I/O	0.7.\/	-	-			
V _{IH}	imput mgm lever voltage	FT	I/O	0.7 V _{DD}	-	-	V		
V.	I/O Schmitt trigger voltage	Stand	lard I/O	-	10% V _{DD} ⁽³⁾	-			
V _{hys}	hysteresis ⁽²⁾	FT	T/O	-	5% V _{DD} ⁽⁴⁾	-			
			/ _{IN} ≤V _{DD} vith LCD	-	-	±50			
	Input leakage current ⁽⁵⁾	V _{SS} ≤V _{IN} ≤V _{DD} I/Os with analog switches		-	-	±50			
I _{lkg}		I/Os wit	/ _{IN} ≤V _{DD} th analog s and LCD	-	-	±50	nA		
			/ _{IN} ≤V _{DD} vith USB	-	-	TBD			
		FT I/O V _{DD} ≤V _{IN} ≤5V		-	-	TBD			
			V _{SS} ≤V _{IN} ≤V _{DD} Standard I/Os		-	-	±50		
R _{PU}	Weak pull-up equivalent resistor ⁽⁶⁾⁽¹⁾	$V_{IN} = V_{SS}$		30	45	60	kΩ		
R _{PD}	Weak pull-down equivalent resistor ⁽⁶⁾	$V_{IN} = V_{DD}$		$V_{IN} = V_{DD}$		30	45	60	kΩ
C _{IO}	I/O pin capacitance	-	-	-	5	-	pF		

^{1.} Tested in production

^{2.} Hysteresis voltage between Schmitt trigger switching levels. Based on characterization.

^{3.} With a minimum of 200 mV. Based on characterization results.

^{4.} With a minimum of 100 mV. Based on characterization results.

^{5.} The max. value may be exceeded if negative current is injected on adjacent pins.

Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with the non-standard V_{OL}/V_{OH} specifications given in *Table 43*.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum Run consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating $I_{VDD\Sigma}$ (see *Table 11*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating $I_{VSS\Sigma}$ (see *Table 11*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13*. All I/Os are CMOS and TTL compliant.

Table 43. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V _{OL} ⁽¹⁾⁽²⁾	Output low level voltage for an I/O pin	I _{IO} = 8 mA	-	0.4	
V _{OH} ⁽³⁾⁽²⁾	Output high level voltage for an I/O pin	2.7 V < V _{DD} < 3.6 V	2.4	-	
V _{OL} (1)(4)	Output low level voltage for an I/O pin	I _{IO} = 4 mA	-	0.45	V
V _{OH} (3)(4)	Output high level voltage for an I/O pin	1.65 V < V _{DD} < 2.7 V	V _{DD} -0.45	-	V
V _{OL} ⁽¹⁾⁽⁴⁾	Output low level voltage for an I/O pin	I _{IO} = 20 mA	-	1.3	
V _{OH} ⁽³⁾⁽⁴⁾	Output high level voltage for an I/O pin	2.7 V < V _{DD} < 3.6 V	V _{DD} -1.3	-	

The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 11* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

^{2.} Tested in production.

The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 11* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.

^{4.} Guaranteed by characterization results.

Input/output AC characteristics

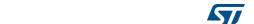
The definition and values of input/output AC characteristics are given in *Figure 19* and *Table 44*, respectively.

Unless otherwise specified, the parameters given in *Table 44* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13*.

Table 44. I/O AC characteristics⁽¹⁾

OSPEEDRx [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Max ⁽²⁾	Unit	
	f	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	400	kHz	
00	f _{max(IO)out}	waximum nequency.	$C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	400	NI IZ	
00	t _{f(IO)out}	Output rise and fall time	$C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	625	ns	
	t _{r(IO)out}	Output rise and fail time	$C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	625	115	
	f	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	2	MUZ	
01	† _{max(IO)out}	waximum nequency.	$C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	1	MHz	
01	t _{f(IO)out}	Output rise and fall time	$C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	125	ne	
	t _{r(IO)out}		$C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	250	ns	
	Е	I Maximum frequency(3) F	$C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	10	MHz	
10	F _{max(IO)out}		$C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	2	IVII IZ	
10	t _{f(IO)out}	Output rise and fall time	C _L = 50 pF, V _{DD} = 2.7 V to 3.6 V	-	25	20	
	t _{r(IO)out}	Output rise and fail time	$C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	125	ns	
	_	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	50	MHz	
11	F _{max(IO)out}	waximum nequency.	$C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	8	IVII IZ	
''	t _{f(IO)out}	Output rise and fall time	$C_L = 30 \text{ pF}, V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	5		
	I Output lise and fall tille i		$C_L = 50 \text{ pF}, V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	30		
-	t _{EXTIPW}	Pulse width of external signals detected by the EXTI controller	-	8	-	ns	

The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32L151x6/8/B and STM32L152x6/8/B reference manual for a description of GPIO Port configuration register.



^{2.} Guaranteed by design.

^{3.} The maximum frequency is defined in *Figure 19*.

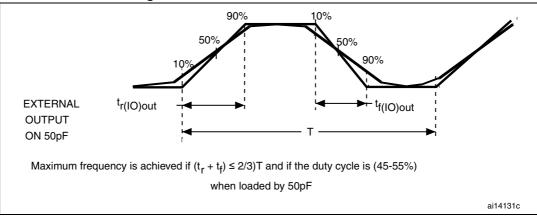


Figure 19. I/O AC characteristics definition

6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, RPU (see *Table 45*).

Unless otherwise specified, the parameters given in *Table 45* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 13*.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{IL(NRST)} ⁽¹⁾	NRST input low level voltage	-	-	-	8.0	
V _{IH(NRST)} ⁽¹⁾	NRST input high level voltage	-	1.4	-		
V _{OL(NRST)} ⁽¹⁾	NRST output low level voltage	$I_{OL} = 2 \text{ mA}$ 2.7 V < V_{DD} < 3.6 V	i	-	0.4	V
		I _{OL} = 1.5 mA 1.65 V < V _{DD} < 2.7 V	-	-	0.4	
V _{hys(NRST)} ⁽¹⁾	NRST Schmitt trigger voltage hysteresis	-	-	10%V _{DD} ⁽²⁾		mV
R _{PU}	Weak pull-up equivalent resistor ⁽³⁾	$V_{IN} = V_{SS}$	30	45	60	kΩ
V _{F(NRST)} ⁽¹⁾	NRST input filtered pulse	-	-	-	50	ns
V _{NF(NRST)} ⁽¹⁾	NRST input not filtered pulse	-	350	-		ns

Table 45. NRST pin characteristics

^{1.} Guaranteed by design.

^{2. 200} mV minimum value

^{3.} The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is around 10%.

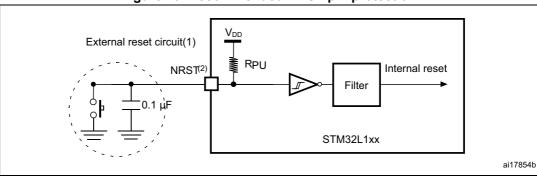


Figure 20. Recommended NRST pin protection

- 1. The reset network protects the device against parasitic resets.
- 2. The user must ensure that the level on the NRST pin can go below the V_{IL(NRST)} max level specified in *Table 45*. Otherwise the reset will not be taken into account by the device.

6.3.15 TIM timer characteristics

The parameters given in *Table 46* are guaranteed by design.

Refer to Section 6.3.13: I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Symbol	Parameter	Conditions	Min	Max	Unit
+	Timer resolution time	-	1	-	t _{TIMxCLK}
t _{res(TIM)}	Timer resolution time	f _{TIMxCLK} = 32 MHz	31.25	-	ns
f	Timer external clock	-	0	f _{TIMxCLK} /2	MHz
f _{EXT}	frequency on CH1 to CH4	f _{TIMxCLK} = 32 MHz	0	16	MHz
Res _{TIM}	Timer resolution	-	-	16	bit
	16-bit counter clock	-	1	65536	t _{TIMxCLK}
^t COUNTER	period when internal clock is selected (timer's prescaler disabled)	f _{TIMxCLK} = 32 MHz	0.0312	2048	μs
t	Maximum possible count	-	-	65536 × 65536	t _{TIMxCLK}
tmax_count	I Waximum possible count	f _{TIMxCLK} = 32 MHz	-	134.2	S

Table 46. TIMx⁽¹⁾ characteristics

^{1.} TIMx is used as a general term to refer to the TIM2, TIM3 and TIM4 timers.

6.3.16 Communication interfaces

I²C interface characteristics

The STM32L151x6/8/B and STM32L152x6/8/B product line I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: SDA and SCL are not "true" open-drain I/O pins. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in *Table 47*. Refer also to *Section 6.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 47. I²C characteristics

Comple el	Downwoodow	Standard mode I ² C ⁽¹⁾		Fast mode	l l m i 4	
Symbol	Parameter	Min	Max	Min	Max	Unit
t _{w(SCLL)}	SCL clock low time	4.7	-	1.3	-	ше
t _{w(SCLH)}	SCL clock high time	4.0	-	0.6	-	μs
t _{su(SDA)}	SDA setup time	250	-	100	-	
t _{h(SDA)}	SDA data hold time	0	-	0	900 ⁽³⁾	
t _{r(SDA)}	SDA and SCL rise time	-	1000	20 + 0.1C _b	300	ns
t _{f(SDA)}	SDA and SCL fall time	-	300	-	300	
t _{h(STA)}	Start condition hold time	4.0	-	0.6	-	
t _{su(STA)}	Repeated Start condition setup time	4.7	-	0.6	-	μs
t _{su(STO)}	Stop condition setup time	4.0	-	0.6	-	μs
t _{w(STO:STA)}	Stop to Start condition time (bus free)	4.7	-	1.3	-	μs
C _b	Capacitive load for each bus line	-	400	-	400	pF

^{1.} Guaranteed by design.

f_{PCLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to
achieve fast mode I²C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I²C fast
mode clock.

^{3.} The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL sinnal

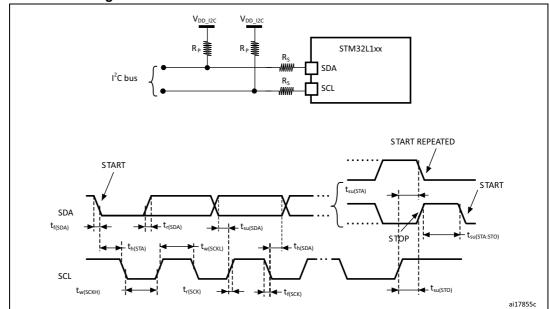


Figure 21. I²C bus AC waveforms and measurement circuit

- 1. R_S = series protection resistors
- 2. R_P = pull-up resistors
- 3. V_{DD_I2C} = I2C bus supply
- Measurement points are done at CMOS levels: 0.3V_{DD} and 0.7V_{DD}.

Table 48. SCL frequency (f_{PCLK1} = 32 MHz, $V_{DD} = V_{DD_I2C} = 3.3 V$)⁽¹⁾⁽²⁾

f //LU-\	I2C_CCR value
f _{SCL} (kHz)	$R_P = 4.7 \text{ k}\Omega$
400	0x801B
300	0x8024
200	0x8035
100	0x00A0
50	0x0140
20	0x0320

- 1. R_P = External pull-up resistance, f_{SCL} = I^2C speed.
- 2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed is ±2%. These variations depend on the accuracy of the external components used to design the application.

SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 13*.

Refer to Section 6.3.12: I/O current injection characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 49. SPI characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max ⁽²⁾	Unit
_		Master mode	-	16	
f _{SCK} 1/t _{c(SCK)}	SPI clock frequency	Slave mode	-	16	MHz
" *C(3CK)		Slave transmitter	-	12 ⁽³⁾	
$\begin{matrix} t_{r(SCK)}^{(2)} \\ t_{f(SCK)}^{(2)} \end{matrix}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	6	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
t _{su(NSS)}	NSS setup time	Slave mode	4t _{HCLK}	-	
t _{h(NSS)}	NSS hold time	Slave mode	2t _{HCLK}	-	
t _{w(SCKH)} ⁽²⁾ t _{w(SCKL)} ⁽²⁾	SCK high and low time	Master mode	t _{SCK} /2-	t _{SCK} /2+	
t _{su(MI)} ⁽²⁾	Data input setup time	Master mode	5	-	
t _{su(SI)} ⁽²⁾	Data input setup time	Slave mode	6	-	
t _{h(MI)} ⁽²⁾	Data input hold time	Master mode	5	-	ns
t _{h(SI)} ⁽²⁾	Data input hold time	Slave mode	5	-	
t _{a(SO)} ⁽⁴⁾	Data output access time	Slave mode	0	3t _{HCLK}	
t _{v(SO)} (2)	Data output valid time	Slave mode	-	33	
t _{v(MO)} ⁽²⁾	Data output valid time	Master mode	-	6.5	
t _{h(SO)} ⁽²⁾	Data output hold time	Slave mode	17	-	
t _{h(MO)} ⁽²⁾	Data output hold time	Master mode	0.5	-	

^{1.} The characteristics above are given for voltage Range 1.



^{2.} Guaranteed by characterization results.

The maximum SPI clock frequency in slave transmitter mode is given for an SPI slave input clock duty cycle (DuCy(SCK)) ranging between 40 to 60%.

^{4.} Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.

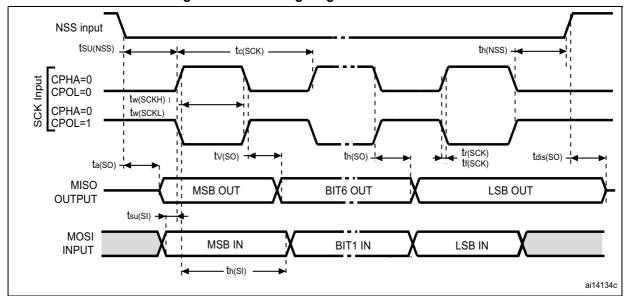
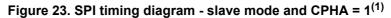
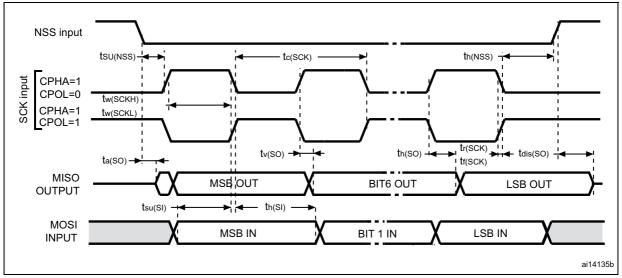


Figure 22. SPI timing diagram - slave mode and CPHA = 0





1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

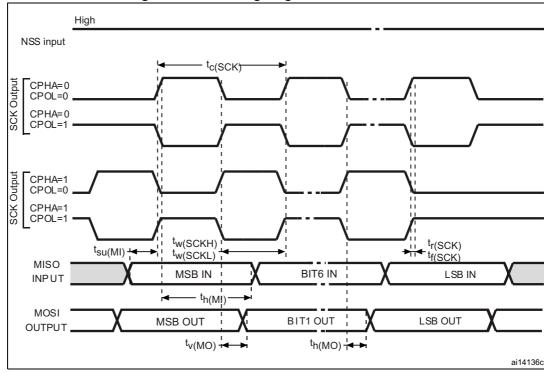


Figure 24. SPI timing diagram - master mode⁽¹⁾

1. Measurement points are done at CMOS levels: $0.3V_{\rm DD}$ and $0.7V_{\rm DD.}$

USB characteristics

The USB interface is USB-IF certified (full speed).

Table 50. USB startup time

Symbol	Parameter	Max	Unit
t _{STARTUP} ⁽¹⁾	USB transceiver startup time	1	μs

1. Guaranteed by design.

Table 01: 00B B0 electroal ellaracteriotics							
Symbol	Parameter	Conditions	Min. ⁽¹⁾	Max. ⁽¹⁾	Unit		
Input leve	els						
V _{DD}	USB operating voltage ⁽²⁾	-	3.0	3.6	V		
V _{DI} ⁽³⁾	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-			
V _{CM} ⁽³⁾	Differential common mode range	Includes V _{DI} range	0.8	2.5	V		
V _{SE} ⁽³⁾	Single ended receiver threshold	-	1.3	2.0			
Output levels							
V _{OL} ⁽⁴⁾	Static output level low	R_L of 1.5 k Ω to 3.6 $V^{(5)}$	-	0.3	V		
V _{OH} ⁽⁴⁾	Static output level high	R_L of 15 k Ω to $V_{SS}^{(5)}$	2.8	3.6	V		

Table 51, USB DC electrical characteristics

- 1. All the voltages are measured from the local ground potential.
- 2. To be compliant with the USB 2.0 full speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 k Ω resistor to a 3.0-to-3.6 V voltage range.
- 3. Guaranteed by characterization results.
- 4. Tested in production.
- 5. R_L is the load connected on the USB drivers.

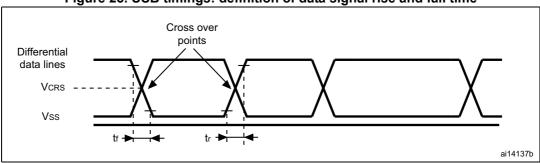


Figure 25. USB timings: definition of data signal rise and fall time

Table 52. USB: full speed electrical characteristics

	Driver characteristics ⁽¹⁾							
Symbol	Parameter	Conditions	Min	Max	Unit			
t _r	Rise time ⁽²⁾	C _L = 50 pF	4	20	ns			
t _f	Fall Time ⁽²⁾	C _L = 50 pF	4	20	ns			
t _{rfm}	Rise/ fall time matching	t _r /t _f	90	110	%			
V _{CRS}	Output signal crossover voltage		1.3	2.0	V			

- 1. Guaranteed by design.
- Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

6.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 54* are guaranteed by design.

Table 53. ADC clock frequency

Symbol	Parameter		Conditions		Min	Max	Unit
				$V_{REF+} = V_{DDA}$		16	
	Voltage	2.4 V ≤V _{DDA} ≤3.6 V	$V_{REF+} < V_{DDA}$ $V_{REF+} > 2.4 V$		8		
f _{ADC}	f _{ADC} ADC clock frequency	Range 1 &		V _{REF+} < V _{DDA} V _{REF+} ≤2.4 V	0.480	4	MHz
			I 1.8 V ≤Vnn∧ ≤2.4 V +	$V_{REF+} = V_{DDA}$		8	
				$V_{REF+} < V_{DDA}$		4	
			Voltage Range 3			4	

Table 54. ADC characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
V_{DDA}	Power supply	-	1.8	-	3.6	V	
V _{REF+}	Positive reference voltage	2.4 V ≤V _{DDA} ≤3.6 V V _{REF+} must be below or equal to V _{DDA}	1.8 ⁽¹⁾	-	V_{DDA}	٧	
V _{REF-}	Negative reference voltage	-	-	V_{SSA}	-	V	
I _{VDDA}	Current on the V _{DDA} input pin	-	-	1000	1450	μA	
1 (2)	Current on the V _{REF} input	Peak	-	400	700	μA	
I _{VREF} ⁽²⁾	pin	Average	-	400	450	μA	
V _{AIN}	Conversion voltage range ⁽³⁾	-	0 ⁽⁴⁾	-	V _{REF+}	V	
	12-bit sampling rate	Direct channels	0.03	-	1	Mono	
	12-bit sampling rate	Multiplexed channels	0.03	-	0.76	Msps	
	10 hit compling rate	Direct channels	0.03	-	1.07	Mono	
f	10-bit sampling rate	Multiplexed channels	0.03	-	0.8	Msps	
f _S	0 hit compling rate	Direct channels	0.03	-	1.23	Mono	
	8-bit sampling rate	Multiplexed channels	0.03	-	0.89	Msps	
	6-bit sampling rate	Direct channels	0.03	-	1.45	Msps	
	o-bit sampling rate	Multiplexed channels	0.03	-	1	ινιομο	

Table 34. ADC characteristics (continued)							
Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
		Direct channels 2.4 V ≤V _{DDA} ≤3.6 V	0.25	-	-		
	Sampling time ⁽⁵⁾	Multiplexed channels 2.4 V ≤V _{DDA} ≤3.6 V	0.56	-	-	μs	
t _S		Direct channels 1.8 V ≤V _{DDA} ≤2.4 V	0.56	-	-	μδ	
		Multiplexed channels 1.8 V ≤V _{DDA} ≤2.4 V	1	-	-		
		-	4	-	384	1/f _{ADC}	
		f _{ADC} = 16 MHz	1	-	24.75	μs	
t _{CONV}	Total conversion time (including sampling time)	-	4 to 384 (sampling phase) +12 (successiv approximation)		ccessive	1/f _{ADC}	
0	Internal sample and hold	Direct channels	-	10	-		
C _{ADC}	capacitor	Multiplexed channels	-	16	-	pF	
f	External trigger frequency	12-bit conversions	-	-	Tconv+1	1/f _{ADC}	
f _{TRIG}	Regular sequencer	6/8/10-bit conversions	-	-	Tconv	1/f _{ADC}	
f	External trigger frequency	12-bit conversions	-	-	Tconv+2	1/f _{ADC}	
f _{TRIG}	Injected sequencer	6/8/10-bit conversions	-	-	Tconv+1	1/f _{ADC}	
R _{AIN}	Signal source impedance ⁽⁵⁾	-	-	-	50	κΩ	
4	Injection trigger conversion	f _{ADC} = 16 MHz	219	-	281	ns	
t _{lat}	latency	-	3.5	-	4.5	1/f _{ADC}	
+	Regular trigger conversion	f _{ADC} = 16 MHz	156	-	219	ns	
t _{latr}	latency	-	2.5	-	3.5	1/f _{ADC}	
t _{STAB}	Power-up time	-	-	-	3.5	μs	

Table 54. ADC characteristics (continued)

- 2. The current consumption through $V_{\mbox{\scriptsize REF}}$ is composed of two parameters:
 - one constant (max 300 μA)
 - one variable (max 400 $\mu\text{A})\text{, only during sampling time + 2 first conversion pulses.$

So, peak consumption is 300+400 = 700 μA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 μA at 1Msps

- 3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to Section 4: Pin descriptions for further details.
- 4. V_{SSA} must be tied to ground.
- 5. See Table 56: Maximum source impedance RAIN max for $R_{\mbox{\scriptsize AIN}}$ limitation.

T

The V_{REF+} input can be grounded iif neither the ADC nor the DAC are used (this allows to shut down an external voltage reference).

Table 55. ADC accuracy⁽¹⁾⁽²⁾

Symbol	Parameter	Test conditions	Min ⁽³⁾	Тур	Max ⁽³⁾	Unit
ET	Total unadjusted error		-	2	4	
EO	Offset error	2.4 V ≤ V _{DDA} ≤ 3.6 V	-	1	2	
EG	Gain error	$2.4 \text{ V} \le \text{V}_{\text{REF+}} \le 3.6 \text{ V}$ $f_{\text{ADC}} = 8 \text{ MHz}, R_{\text{AIN}} = 50 \Omega$	-	1.5	3.5	LSB
ED	Differential linearity error	$T_A = -40 \text{ to } 105 ^{\circ}\text{C}$	-	1	2	
EL	Integral linearity error		-	1.7	3	
ENOB	Effective number of bits	2.4 V ≤ V _{DDA} ≤ 3.6 V	9.2	10	-	bits
SINAD	Signal-to-noise and distortion ratio	$V_{DDA} = V_{REF+}$ $f_{ADC} = 16$ MHz, $R_{AIN} = 50$ Ω	57.5	62	-	
SNR	Signal-to-noise ratio	T _A = -40 to 105 ° C 1 kHz ≤ F _{input} ≤ 100 kHz	57.5	62	-	dB
THD	Total harmonic distortion		-74	-75	-	
ET	Total unadjusted error		-	4	6.5	
EO	Offset error	$2.4 \text{ V} \leq \text{V}_{\text{DDA}} \leq 3.6 \text{ V}$	-	2	4	
EG	Gain error	1.8 V ≤ V _{REF+} ≤ 2.4 V f_{ADC} = 4 MHz, R_{AIN} = 50 Ω	-	4	6	LSB
ED	Differential linearity error	$T_A = -40 \text{ to } 105 ^{\circ}\text{C}$	-	1	2	
EL	Integral linearity error		-	1.5	3	
ET	Total unadjusted error		-	2	3	
EO	Offset error	$1.8 \text{ V} \le \text{V}_{\text{DDA}} \le 2.4 \text{ V}$	-	1	1.5	
EG	Gain error	1.8 V ≤ V_{REF+} ≤ 2.4 V f_{ADC} = 4 MHz, R_{AIN} = 50 Ω T_{A} = -40 to 105 ° C	-	1.5	2	LSB
ED	Differential linearity error		-	1	2	
EL	Integral linearity error		-	1	1.5	

^{1.} ADC DC accuracy values are measured after internal calibration.

ADC accuracy vs. negative injection current: Injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.
 Any positive injection current within the limits specified for I_{INJ(PIN)} and ΣI_{INJ(PIN)} in Section 6.3.12 does not affect the ADC accuracy.

^{3.} Guaranteed by characterization results.

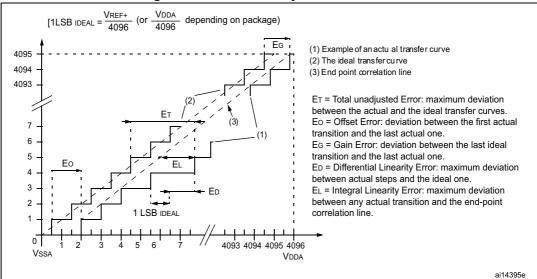
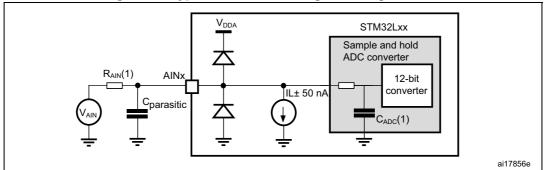


Figure 26. ADC accuracy characteristics

Figure 27. Typical connection diagram using the ADC



- Refer to Table 56: Maximum source impedance RAIN max for the value of R_{AIN} and Table 54: ADC characteristics for the value of CADC
- C_{parasitic} represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high C_{parasitic} value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.



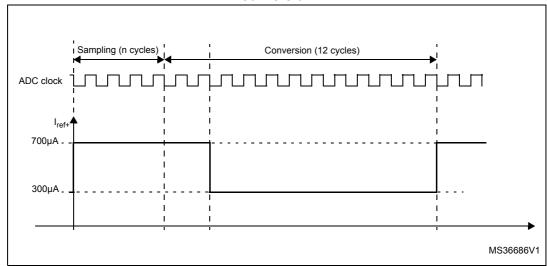


Figure 28. Maximum dynamic current consumption on V_{REF+} supply pin during ADC conversion

Table 56. Maximum source impedance R_{AIN} max⁽¹⁾

	t			AIII	
Ts (µs)	Multiplexe	d channels	Direct o	Ts (cycles) f _{ADC} = 16 MHz ⁽²⁾	
	2.4 V < V _{DDA} < 3.6 V 1.8 V < V _{DDA} <		2.4 V < V _{DDA} < 3.3 V	1.8 V < V _{DDA} < 2.4 V	ADC
0.25	Not allowed	Not allowed	0.7	Not allowed	4
0.5625	0.8	Not allowed	2.0	1.0	9
1	2.0	0.8	4.0	3.0	16
1.5	3.0	1.8	6.0	4.5	24
3	6.8	4.0	15.0	10.0	48
6	15.0	10.0	30.0	20.0	96
12	32.0	25.0	50.0	40.0	192
24	50.0	50.0	50.0	50.0	384

^{1.} Guaranteed by design.

General PCB design guidelines

Power supply decoupling should be performed as shown in The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

^{2.} Number of samples calculated for f_{ADC} = 16 MHz. For f_{ADC} = 8 and 4 MHz the number of sampling cycles can be reduced with respect to the minimum sampling time Ts (us).

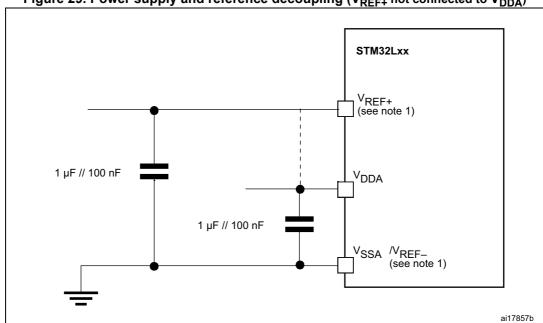
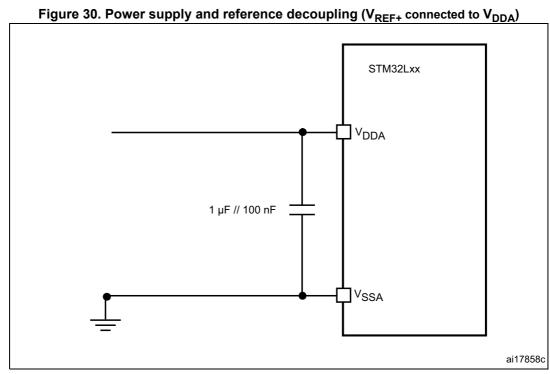


Figure 29. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})

1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

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6.3.18 DAC electrical specifications

Data guaranteed by design, unless otherwise specified.

Table 57. DAC characteristics

Symbol	Parameter	C	onditions	Min	Тур	Max	Unit		
V_{DDA}	Analog supply voltage		-	1.8	-	3.6	V		
V _{REF+}	Reference supply voltage	V _{REF+} must always be below V _{DDA}		1.8	-	3.6	٧		
V _{REF-}	Lower reference voltage	-		-			V _{SSA}		V
. (1)	Current consumption on	No load, mic	idle code (0x800)	-	130	220	μA		
I _{DDVREF+} (1)	V_{REF+} supply V_{REF+} = 3.3 V	No load, wo	rst code (0x000)	1	220	350	μA		
. (1)	Current consumption on	No load, mic	No load, middle code (0x800)		210	320	μA		
I _{DDA} ⁽¹⁾	V _{DDA} supply V _{DDA} = 3.3 V	No load, worst code (0xF1C)		-	320	520	μA		
R_L	Resistive load	DAC output	Connected to V _{SSA}	5	-	-	kΩ		
IVL	ixesistive load	buffer ON	Connected to V _{DDA}	25	-	-	K22		
C_L	Capacitive load	DAC output	buffer ON	-	-	50	pF		
R _O	Output impedance	DAC output	buffer OFF	12	16	20	kΩ		
	Voltage on DAC_OUT	DAC output	buffer ON	0.2	-	V _{DDA} – 0.2	٧		
V _{DAC_OUT}	output	DAC output	buffer OFF	0.5	-	V _{REF+} – 1LSB	mV		
DNL ⁽¹⁾	Differential non	$C_L \le 50 \text{ pF, f}$ DAC output	=	-	1.5	3			
DIVL	linearity ⁽²⁾	No R_{LOAD} , $C_{L} \le 50$ pF DAC output buffer OFF		-	1.5	3			
INL ⁽¹⁾	Integral non linearity ⁽³⁾	$C_L \le 50$ pF, $R_L \ge 5$ k Ω DAC output buffer ON		ı	2	4			
IIVL	integral non-inteanty	No R _{LOAD} , C DAC output		-	2	4	LSB		
Offset ⁽¹⁾	Offset error at code	$C_L \le 50$ pF, $R_L \ge 5$ k Ω DAC output buffer ON		-	±10	±25			
	0x800 ⁽⁴⁾	No R _{LOAD} , C _L ≤ 50 pF DAC output buffer OFF		-	±5	±8			
Offset1 ⁽¹⁾	Offset error at code 0x001 ⁽⁵⁾	No R _{LOAD} , O DAC output		-	±1.5	±5			



Table 57. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
dOffset/dT ⁽¹⁾	Offset error temperature	V _{DDA} = 3.3V, T _A = 0 to 50 °C DAC output buffer OFF	-20	-10	0	μV/°C
dOliseva ()	coefficient (code 0x800)	V _{DDA} = 3.3V, T _A = 0 to 50 °C DAC output buffer ON	0	20	50	μν/ Ο
Gain ⁽¹⁾	Gain error ⁽⁶⁾	$C_L \le 50$ pF, $R_L \ge 5$ k Ω DAC output buffer ON	-	+0.1 / -0.2%	+0.2 / - 0.5%	%
Gain	Gain error	No R_{LOAD} , $C_{L} \le 50 pF$ DAC output buffer OFF	-	+0 / -0.2%	+0 / -0.4%	70
dGain/dT ⁽¹⁾	Gain error temperature	V _{DDA} = 3.3V, T _A = 0 to 50 °C DAC output buffer OFF	-10	-2	0	μV/°C
uGaiii/u i · /	coefficient	V _{DDA} = 3.3V, T _A = 0 to 50 °C DAC output buffer ON	-40	-8	0	μν/ С
TUE ⁽¹⁾	Total unadjusted error	$C_L \le 50$ pF, $R_L \ge 5$ k Ω DAC output buffer ON	-	12	30	LSB
	Total unaujusteu erroi	No R_{LOAD} , $C_L \le 50 pF$ DAC output buffer OFF	-	8	12	LOB
tsettling	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes till DAC_OUT reaches final value ±1LSB	$C_L \le 50$ pF, $R_L \ge 5$ k Ω	-	7	12	μs
Update rate	Max frequency for a correct DAC_OUT change (95% of final value) with 1 LSB variation in the input code	$C_L \le 50 \text{ pF, } R_L \ge 5 \text{ k}\Omega$	-	-	1	Msps
t _{WAKEUP}	Wakeup time from off state (setting the ENx bit in the DAC Control register) ⁽⁷⁾	$C_L \le 50 \text{ pF}, R_L \ge 5 \text{ k}\Omega$	-	9	15	μs
PSRR+	V _{DDA} supply rejection ratio (static DC measurement)	$C_L \le 50 \text{ pF, } R_L \ge 5 \text{ k}\Omega$	-	-60	-35	dB

- 1. Guaranteed by characterization results.
- 2. Difference between two consecutive codes 1 LSB.
- 3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
- 4. Difference between the value measured at Code (0x800) and the ideal value = V/2.
- 5. Difference between the value measured at Code (0x001) and the ideal value.
- Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{DDA} – 0.2) V when buffer is ON.
- 7. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

Buffered/Non-buffered DAC

Buffer(1)

12-bit digital to analog converter

C L

ai17157V3

Figure 31. 12-bit buffered /non-buffered DAC

 The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.19 Temperature sensor characteristics

Table 58. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V _{DDA} = 3 V	0x1FF8 007A-0x1FF8 007B
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C V _{DDA} = 3 V	0x1FF8 007E-0x1FF8 007F

Table 59. Temperature sensor characteristics

Symbol	Parameter	Min	Тур	Max	Unit
T _L ⁽¹⁾	V _{SENSE} linearity with temperature	-	±1	<u>+2</u>	°C
Avg_Slope ⁽¹⁾	Average slope	1.48	1.61	1.75	mV/°C
V ₁₁₀	Voltage at 110°C ±5°C ⁽²⁾	612	626.8	641.5	mV
I _{DDA(TEMP)} ⁽³⁾	Current consumption	-	3.4	6	μΑ
t _{START} (3)	Startup time	-	-	10	
T _{S_temp} ⁽⁴⁾⁽³⁾	ADC sampling time when reading the temperature	10	-	-	μs

- 1. Guaranteed by characterization results.
- 2. Measured at V_{DD} = 3 V ±10 mV. V110 ADC conversion result is stored in the TS_CAL2 byte.
- 3. Guaranteed by design.
- ${\bf 4.} \quad {\bf Shortest\ sampling\ time\ can\ be\ determined\ in\ the\ application\ by\ multiple\ iterations.}$



6.3.20 Comparator

Table 60. Comparator 1 characteristics

Symbol	Parameter	Conditions	Min ⁽¹⁾	Тур	Max ⁽¹⁾	Unit
V_{DDA}	Analog supply voltage	-	1.65		3.6	V
R _{400K}	R _{400K} value	-	-	400	-	kΩ
R _{10K}	R _{10K} value	-	-	10	-	K22
V _{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t _{START}	Comparator startup time	-	-	7	10	ue
td	Propagation delay ⁽²⁾	-	-	3	10	μs
Voffset	Comparator offset	-	-	±3	±10	mV
d _{Voffset} /dt	Comparator offset variation in worst voltage stress conditions	$V_{DDA} = 3.6 \text{ V}$ $V_{IN+} = 0 \text{ V}$ $V_{IN-} = V_{REFINT}$ $T_A = 25 ^{\circ} \text{ C}$	0	1.5	10	mV/1000 h
I _{COMP1}	Current consumption ⁽³⁾	-	-	160	260	nA

^{1.} Guaranteed by characterization results.

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^{2.} The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.

^{3.} Comparator consumption only. Internal reference voltage not included.

Table 61. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Тур	Max ⁽¹⁾	Unit
V_{DDA}	Analog supply voltage	-	1.	-	3.6	V
V _{IN}	Comparator 2 input voltage range	-	0	-	V_{DDA}	V
+ .	Comparator startup time	Fast mode	-	15	20	
t _{START} Compara	Comparator startup time	Slow mode	-	20	25	
+	Propagation delay ⁽²⁾ in slow mode	1. V ≤V _{DDA} ≤2.7 V	-	1.8	3.5	
t _{d slow} Propagation delay ⁽²⁾ in s	Propagation delay. 7 in slow mode	2.7 V ≤V _{DDA} ≤3.6 V	-	2.5	6	μs
+	t _{d fast} Propagation delay ⁽²⁾ in fast mode	1. V ≤V _{DDA} ≤2.7 V	-	0.8	2	
t _{d fast}	Propagation delay. All last mode	2.7 V ≤V _{DDA} ≤3.6 V	-	1.2	4	
V _{offset}	Comparator offset error	-	-	±4	±20	mV
dThreshold/ dt	Threshold voltage temperature coefficient	$\begin{split} V_{DDA} &= 3.3V \\ T_{A} &= 0 \text{ to } 50 ^{\circ}\text{C} \\ V_{-} &= V_{REFINT}, \\ 3/4 \ V_{REFINT}, \\ 1/2 \ V_{REFINT}, \\ 1/4 \ V_{REFINT} \end{split}$	-	15	100	ppm /°C
1	Current consumption(3)	Fast mode	-	3.5	5	
I _{COMP2}	Current consumption ⁽³⁾	Slow mode	-	0.5	2	μA

^{1.} Guaranteed by characterization results.

^{2.} The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.

Comparator consumption only. Internal reference voltage (necessary for comparator operation) is not included.

LCD controller (STM32L152xx only) 6.3.21

The STM32L152xx embeds a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the V_{LCD} pin to decouple this converter.

Table 62. LCD controller characteristics

Symbol	Parameter	Min	Тур	Max	Unit	
V_{LCD}	LCD external voltage	-	-	3.6		
V _{LCD0}	LCD internal reference voltage 0	-	2.6	-		
V _{LCD1}	LCD internal reference voltage 1	-	2.73	-		
V _{LCD2}	LCD internal reference voltage 2	-	2.86	-		
V _{LCD3}	LCD internal reference voltage 3	-	2.98	-	V	
V _{LCD4}	LCD internal reference voltage 4	-	3.12	-		
V _{LCD5}	LCD internal reference voltage 5	-	3.26	-		
V _{LCD6}	LCD internal reference voltage 6	-	3.4	-		
V _{LCD7}	LCD internal reference voltage 7	-	3.55	-		
C _{ext}	V _{LCD} external capacitance	0.1	-	2	μF	
. (1)	Supply current at V _{DD} = 2.2 V	-	3.3	-		
I _{LCD} ⁽¹⁾	Supply current at V _{DD} = 3.0 V	-	3.1	-	μA	
R _{Htot} ⁽²⁾	Low drive resistive network overall value	5.28	6.6	7.92	МΩ	
R _L ⁽²⁾	High drive resistive network total value	192	240	288	kΩ	
V ₄₄	Segment/Common highest level voltage	-	-	V_{LCD}	V	
V ₃₄	Segment/Common 3/4 level voltage	-	3/4 V _{LCD}	-		
V ₂₃	Segment/Common 2/3 level voltage	-	2/3 V _{LCD}	-		
V ₁₂	Segment/Common 1/2 level voltage	-	1/2 V _{LCD}	-	.,	
V ₁₃	Segment/Common 1/3 level voltage	-	1/3 V _{LCD}	-	V	
V ₁₄	Segment/Common 1/4 level voltage	-	1/4 V _{LCD}	-	<u> </u>	
V ₀	Segment/Common lowest level voltage	0	-	-	<u> </u>	
ΔVxx ⁽³⁾	Segment/Common level voltage error T _A = -40 to 85 ° C	-	-	±50	mV	

^{1.} LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio= 64, all pixels active, no LCD



^{2.} Guaranteed by design.

^{3.} Guaranteed by characterization results.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

7.1 LQFP100 14 x 14 mm, 100-pin low-profile quad flat package information

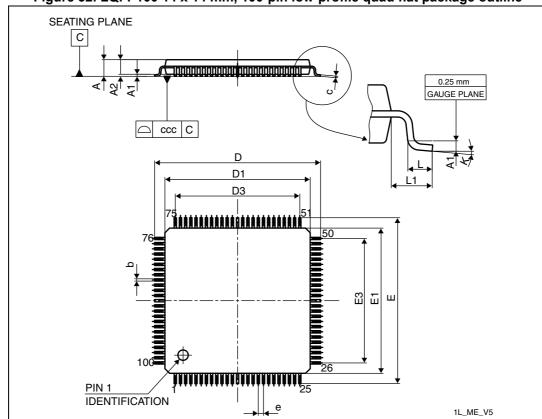


Figure 32. LQFP100 14 x 14 mm, 100-pin low-profile quad flat package outline

1. Drawing is not to scale.

Table 63. LQPF100 14 x 14 mm, 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Тур	Max	Min	Тур	Max
Α	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
С	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
е	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

^{1.} Values in inches are converted from mm and rounded to 4 decimal digits.

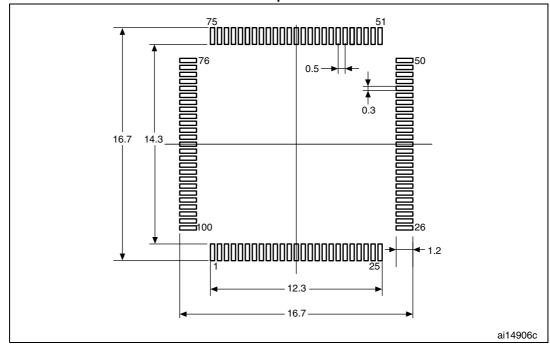


Figure 33. LQPF100 14 x 14 mm, 100-pin low-profile quad flat package recommended footprint

1. Dimensions are in millimeters.

LQFP100 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

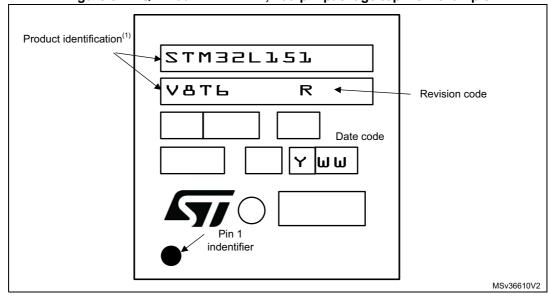


Figure 34. LQFP100 14 x 14 mm, 100-pin package top view example

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.



7.2 LQFP64 10 x 10 mm, 64-pin low-profile quad flat package information

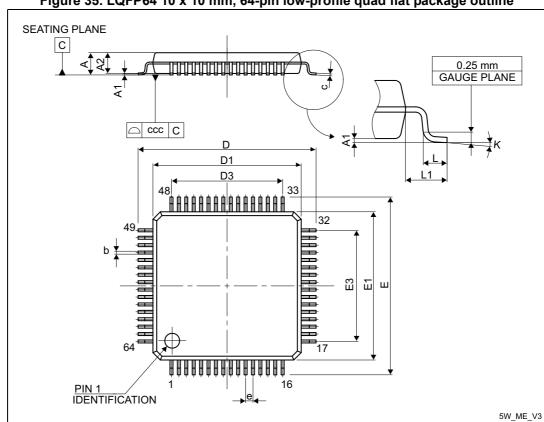


Figure 35. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package outline

1. Drawing is not to scale.

Table 64. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical data

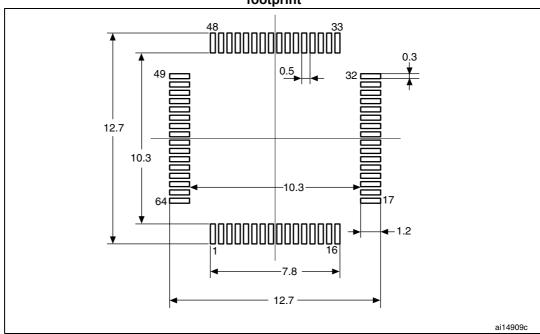
data									
Symbol	millimeters			inches ⁽¹⁾					
	Min	Тур	Max	Тур	Min	Max			
Α	-	-	1.600	-	-	0.0630			
A1	0.050	-	0.150	0.0020	-	0.0059			
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571			
b	0.170	0.220	0.270	0.0067	0.0087	0.0106			
С	0.090	-	0.200	0.0035	-	0.0079			
D	-	12.000	-	-	0.4724	-			
D1	-	10.000	-	-	0.3937	-			
D3	-	7.500	-	-	0.2953	-			
Е	-	12.000	-	-	0.4724	-			
E1	-	10.000	-	-	0.3937	-			

Table 64. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical data (continued)

Cumbal	millimeters			inches ⁽¹⁾		
Symbol	Min	Тур	Max	Тур	Min	Max
E3	-	7.500	-	-	0.2953	-
е	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

^{1.} Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 36. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package recommended footprint

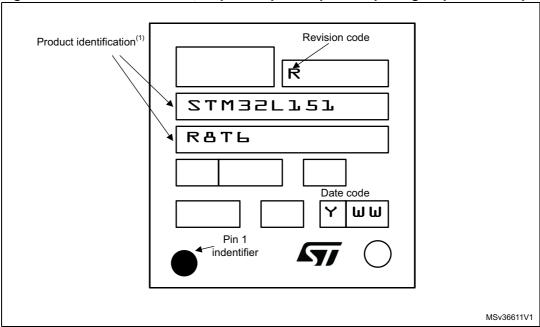


1. Dimensions are in millimeters.

LQFP64 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 37. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package top view example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

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7.3 LQFP48 7 x 7 mm, 48-pin low-profile quad flat package information

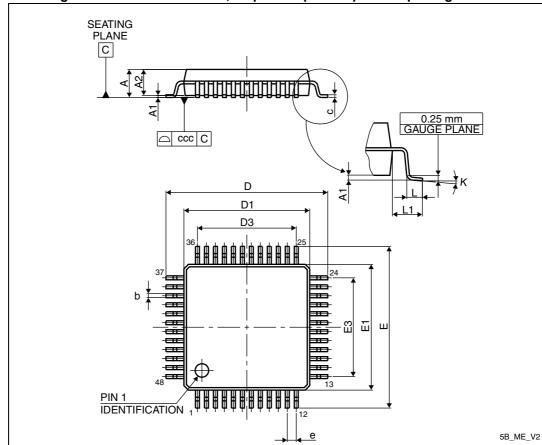


Figure 38. LQFP48 7 x 7 mm, 48-pin low-profile quad flat package outline

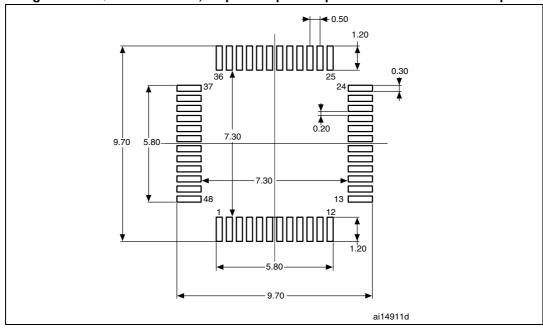
1. Drawing is not to scale.

Table 65. LQFP48 7 x 7 mm, 48-pin low-profile quad flat package mechanical data

Symbol		millimeters			inches ⁽¹⁾		
Symbol	Min	Тур	Max	Min	Тур	Max	
Α	-	-	1.600	-	-	0.0630	
A1	0.050	-	0.150	0.0020	-	0.0059	
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571	
b	0.170	0.220	0.270	0.0067	0.0087	0.0106	
С	0.090	-	0.200	0.0035	-	0.0079	
D	8.800	9.000	9.200	0.3465	0.3543	0.3622	
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835	
D3	-	5.500	-	-	0.2165	-	
Е	8.800	9.000	9.200	0.3465	0.3543	0.3622	
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835	
E3	-	5.500	-	-	0.2165	-	
е	-	0.500	-	-	0.0197	-	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295	
L1	-	1.000	-	-	0.0394	-	
k	0°	3.5°	7°	0°	3.5°	7°	
CCC	-	-	0.080	-	-	0.0031	

^{1.} Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 39. LQFP48 7 x 7 mm, 48-pin low-profile quad flat recommended footprint



1. Dimensions are in millimeters.

LQFP48 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Product identification (1)

Pin 1 identification

Product identification

Revision code

MS36612V1

Figure 40. LQFP48 7 x 7 mm, 48-pin low-profile quad flat package top view example



^{1.} Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.4 UFQFPN48 7 x 7 mm, 0.5 mm pitch, package information

Pin 1 identifier laser marking area D Seating \triangle ddd b Detail Y D Exposed pad D2 area C 0.500x45° R 0.125 typ Detail Z E2 A0B9 ME V3

Figure 41. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package outline

- 1. Drawing is not to scale.
- 2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
- 3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

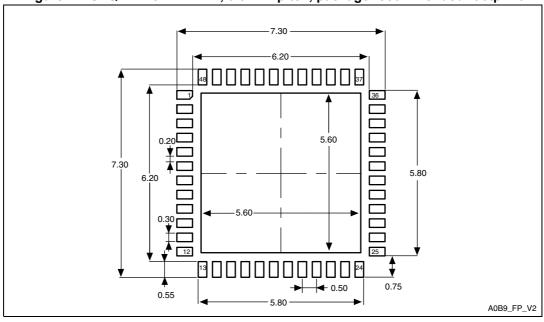
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Table 66. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
Symbol	Min	Тур	Max	Min	Тур	Max
Α	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
Т	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
е	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

^{1.} Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 42. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package recommended footprint



1. Dimensions are in millimeters.

UFQFPN48 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

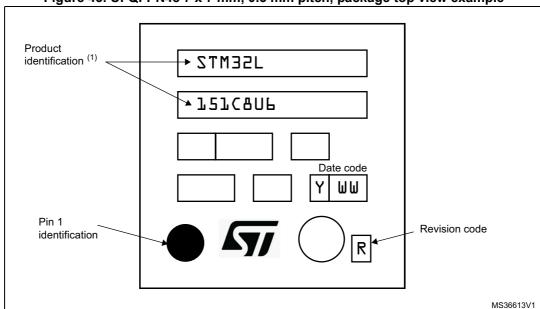


Figure 43. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package top view example

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.



7.5 UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package information

Figure 44. UFBGA100, 7 x 7 mm, 0.5 mm pitch, package outline Z Seating plane \triangle ddd Z A4 A3 A2 A1 A X E1 -A1 ball A1 ball identifier index area \$\ddot\document\docum 00000000000 00000 00000 000 000 000 000 00 00 D1 D 0 0 00 000 000 000 000 00000 00000 00000000000 Υ 000000000000 М 12 Øb (100 balls) **BOTTOM VIEW TOP VIEW** A0C2_ME_V4

1. Drawing is not to scale.

Table 67. UFBGA100 7 x 7 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
Symbol	Min	Тур	Max	Min Typ		Max
Α	-	-	0.6	-	-	0.0236
A1	0.05	0.08	0.11	0.002	0.0031	0.0043
A2	0.4	0.45	0.5	0.0157	0.0177	0.0197
A3	0.08	0.13	0.18	0.0031	0.0051	0.0071
A4	0.27	0.32	0.37	0.0106	0.0126	0.0146
b	0.2	0.25	0.3	0.0079	0.0098	0.0118
D	6.95	7	7.05	0.2736	0.2756	0.2776
D1	5.45	5.5	5.55	0.2146	0.2165	0.2185
Е	6.95	7	7.05	0.2736	0.2756	0.2776
E1	5.45	5.5	5.55	0.2146	0.2165	0.2185
е	-	0.5	-	-	0.0197	-
F	0.7	0.75	0.8	0.0276	0.0295	0.0315
ddd	-	-	0.1	-	-	0.0039



Table 67. UFBGA100 7 x 7 mm, 0.5 mm pitch, package mechanical data (continued)

Symbol		millimeters inches ⁽¹⁾				
Symbol	Min	Тур	Max	Min	Тур	Max
eee	-	-	0.15	-	-	0.0059
fff	-	-	0.05	-	-	0.002

^{1.} Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 45. UFBGA100 7 x 7 mm, 0.5 mm pitch, package recommended footprint

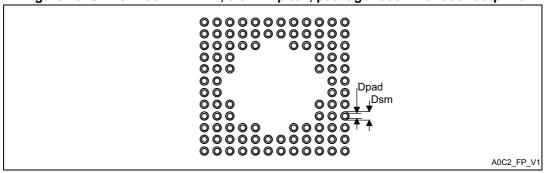


Table 68. UFBGA100 7 x 7 mm, 0.5 mm pitch, recommended PCB design rules

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

UFBGA100 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

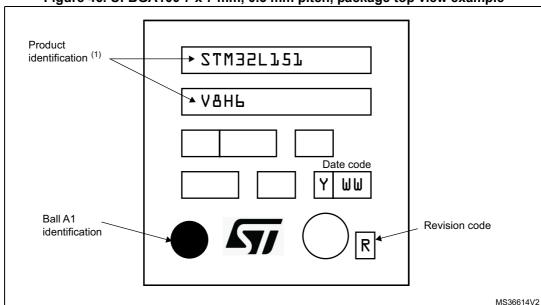


Figure 46. UFBGA100 7 x 7 mm, 0.5 mm pitch, package top view example

^{1.} Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball 7.6 grid array package information

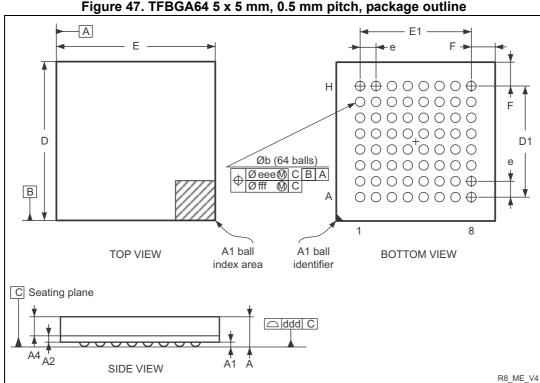


Figure 47. TFBGA64 5 x 5 mm, 0.5 mm pitch, package outline

1. Drawing is not to scale.

Table 69. TFBGA64 5 x 5 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
Symbol	Min	Тур	Max	Min	Тур	Max
Α	-	-	1.200	-	-	0.0472
A1	0.150	-	-	0.0059	-	-
A2	-	0.200	-	-	0.0079	-
A4	-	-	0.600	-	-	0.0236
b	0.250	0.300	0.350	0.0098	0.0118	0.0138
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	-	3.500	-	-	0.1378	-
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	-	3.500	-	-	0.1378	-
е	-	0.500	-	-	0.0197	-
F	-	0.750	-	-	0.0295	-
ddd	-	-	0.080	-	-	0.0031

Table 69. TFBGA64 5 x 5 mm, 0.5 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
Symbol	Min	Тур	Max	Min	Тур	Max
eee	-	-	0.15	-	-	0.0059
fff	-	-	0.05	-	-	0.002

^{1.} Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 48. TFBGA64, 5 x 5 mm, 0.5 mm pitch, recommended footprint

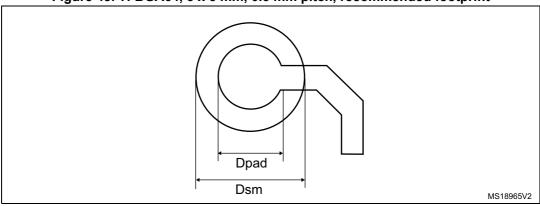


Table 70. TFBGA64 5 x 5 mm, 0.5 mm pitch, recommended PCB design rules

Dimension	Recommended values
Pitch	0.5
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

TFBGA64 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

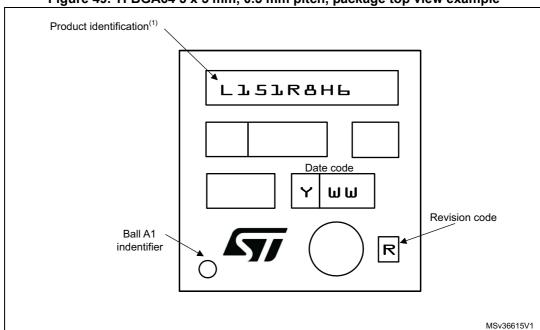


Figure 49. TFBGA64 5 x 5 mm, 0.5 mm pitch, package top view example

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7.7 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

 $T_J \max = T_A \max + (P_D \max \times \Theta_{JA})$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in ° C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$ max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

P_{I/O} max represents the maximum power dissipation on output pins where:

$$\mathsf{P}_\mathsf{I/O} \; \mathsf{max} = \Sigma \; (\mathsf{V}_\mathsf{OL} \times \mathsf{I}_\mathsf{OL}) + \Sigma ((\mathsf{V}_\mathsf{DD} - \mathsf{V}_\mathsf{OH}) \times \mathsf{I}_\mathsf{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Symbol	Parameter	Value	Unit
	Thermal resistance junction-ambient BGA100 - 7 x 7 mm	59	
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	46	
0	Thermal resistance junction-ambient TFBGA64 - 5 x 5 mm	65	°C/W
$\Theta_{\sf JA}$	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	45	- C/VV
	Thermal resistance junction-ambient LQFP48 - 7 x 7 mm / 0.5 mm pitch	55	
	Thermal resistance junction-ambient UFQFPN48 - 7 x 7 mm / 0.5 mm pitch	16	

Table 71. Thermal characteristics

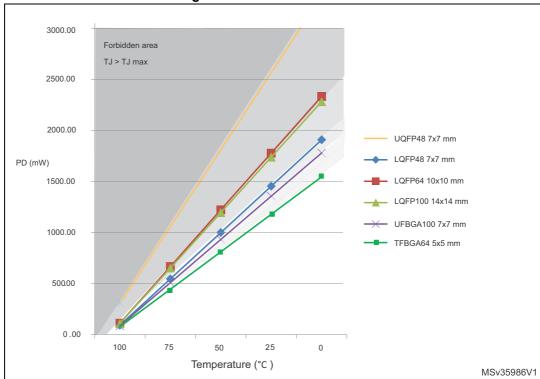


Figure 50. Thermal resistance

7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

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8 Ordering information

Table 72. Ordering information scheme STM32 L 151 C 8 Example: **Device family** STM32 = ARM-based 32-bit microcontroller **Product type** L = Low power Device subfamily 151: Devices without LCD 152: Devices with LCD Pin count C = 48 pinsR = 64 pinsV = 100 pins Flash memory size 6 = 32 Kbytes of Flash memory 8 = 64 Kbytes of Flash memory B = 128 Kbytes of Flash memory **Package** H = BGA T = LQFPU = UFQFPN Temperature range 6 = Industrial temperature range, -40 to 85 °C No character = V_{DD} range: 1.8 to 3.6 V and BOR enabled T = V_{DD} range: 1.65 to 3.6 V and BOR disabled Packing

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.



TR = tape and reel

No character = tray or tube

9 Revision history

Table 73. Document revision history

2	Initial release. Removed 5 V tolerance (FT) from PA3, PB0 and PC3 in <i>Table 8:</i> STM32L15xx6/8/B pin definitions
2	
2	Updated Table 14: Embedded reset and power control block characteristics Updated Table 16: Embedded internal reference voltage Added Table 53: ADC clock frequency Updated Table 54: ADC characteristics
3	Modified consumptions on page 1 and in Section 3.1: Low power modes LED_SEG8 removed on PB6. Updated Section 6: Electrical characteristics VFQFPN48 replaced by UFQFPN48
4	Section 3.3.2: Power supply supervisor: updated note. Table 8: STM32L15xx6/8/B pin definitions: modified main function (after reset) and alternate function for OSC_IN and OSC_OUT pins; modified footnote 5; added footnote to OSC32_IN and OSC32_OUT pins; C1 and D1 removed on PD0 and PD1 pins (TFBGA64 column). Section 3.11: DAC (digital-to-analog converter): updated bullet list. Table 10: Voltage characteristics on page 52: updated footnote 3 regarding I _{INJ(PIN)} . Table 11: Current characteristics on page 52: updated footnote 4 regarding positive and negative injection. Table 14: Embedded reset and power control block characteristics on page 54: updated typ and max values for T _{RSTTEMPO} (V _{DD} rising, BOR enabled). Table 17: Current consumption in Run mode, code with data processing running from Flash on page 58: removed values for HSI clock source (16 MHz), Range 3. Table 18: Current consumption in Run mode, code with data processing running from RAM on page 59: removed values for HSI clock source (16 MHz), Range 3. Table 19: Current consumption in Sleep mode on page 60 removed values for HSI clock source (16 MHz), Range 3 for both RAM and Flash; changed units. Table 20: Current consumption in Low power run mode on page 62: updated parameter and max value of I _{DD} Max (LP Run). Table 21: Current consumption in Low power sleep mode on page 63: updated symbol, parameter, and max value of I _{DD} Max (LP Sleep). Table 22: Typical and maximum current consumptions in Stop mode on page 64 updated values for I _{DD} (Stop with RTC) - RTC clocked by LSE external clock (32.768 kHz), regulator in LP mode, HSI and HSE OFF (no independent watchdog).

Table 73. Document revision history (continued)

		Changes Updated Table 23: Typical and maximum current consumptions in
25-Feb-2011	4 (continued)	Standby mode on page 66 (I _{DD} (WU from Standby) instead of (I _{DD} (WU from Stop). Table 25: Low-power mode wakeup timings on page 69: updated condition for Wakeup from Stop mode, regulator in Run mode; updated max values for Wakeup from Stop mode, regulator in low power mode; updated max values for twostpm. Table 24: Peripheral current consumption on page 67: updated values for column Low power sleep and run; updated Flash values; renamed ADC1 to ADC; updated I _{DD} (LCD) value; updated units; added values for I _{DD} (RTC) and I _{DD} (IWDG); updated footnote 1 and 3; added foot note 2 concerning ADC. Table 26: High-speed external user clock characteristics on page 70: added min value for two time; added max value for trender of the column of the c
		Added Table 56: R_{AIN} max for f_{ADC} = 16 MHz on page 98 Figure 29: Power supply and reference decoupling (VREF+ not connected to VDDA): replaced all 10 nF capacitors with 100 nF capacitors. Figure 30: Power supply and reference decoupling (VREF+ connected to VDDA): replaced 10 nF capacitor with 100 nF capacitor.



Table 73. Document revision history (continued)

Date	Revision	Changes
17-June-2011	5	Modified 1st page (low power features) Added STM32L15xC6 and STM32L15xR6 devices (32 Kbytes of Flash memory). Modified Section 3.6: GPIOs (general-purpose inputs/outputs) on page 22 Modified Section 6.3: Operating conditions on page 53 Modified Table 55: ADC accuracy on page 95, Table 57: DAC characteristics on page 99 and Table 60: Comparator 1 characteristics on page 102
25-Jan-2012	6	Features: updated internal multispeed low power RC. Table 2: Ultralow power STM32L15xx6/8/B device features and peripheral counts: LCD 4x44 and 8x40 available for both 64- and 128-Kbyte devices; two comparators available for all devices. Table 3: Functionalities depending on the operating power supply range: added footnote 1. Figure 8: STM32L15xCx UFQFPN48 pinout: replaced VFQPN48 by UFQFPN48 as name of package. Table 8: STM32L15xx6/8/B pin definitions: replaced PH0/PH1 by PC14/PC15. Table 9: Alternate function input/output: removed EVENT OUT from PH2 port, AFIO15 column. Table 19: Current consumption in Sleep mode: updated MSI conditions and f _{HCLK} . Table 20: Current consumption in Low power run mode: updated some temperature conditions; added footnote 2. Table 21: Current consumption in Low power sleep mode: updated some temperature conditions and one of the MSI clock conditions. Table 22: Typical and maximum current consumptions in Stop mode: updated I _{DD} (WU from Stop) parameter. Table 23: Typical and maximum current consumptions in Standby mode: updated I _{DD} (WU from Standby) parameter. Table 25: Low-power mode wakeup timings: updated f _{HCLK} value for t _{WUSLEEP_LP} ; updated typical value of parameter "Wakeup from Stop mode, regulator in Run mode". Table 24: Peripheral current consumption: replaced GPIOF by GPIOH. Table 35: Flash memory and data EEPROM characteristics: updated all information for I _{DD} . Figure 19: I/O AC characteristics: amended footnote 2. Table 47: I2C characteristics: amended footnote 2. Table 54: ADC characteristics: updated f _S max value for direct channels, 6-bit sampling rate. Table 55: ADC accuracy: Updated the first, third and fourth f _{ADC} test condition. Table 59: Temperature sensor characteristics: updated typ, min, and max values of the T _{S_temp} parameter.



Table 73. Document revision history (continued)

Doto		. Document revision history (continued)
Date	Revision	Changes
26-Oct-2012	7	Updated Section 3.10: ADC (analog-to-digital converter) Updated Table 3: Functionalities depending on the operating power supply range, added Table 4: CPU frequency range depending on dynamic voltage scaling and Table 5: Working mode-dependent functionalities (from Run/active down to standby). Updated Table 27: Low-speed external user clock characteristicsAdded footnote 2. in Table 14: Embedded reset and power control block characteristics Updated Table 22: Typical and maximum current consumptions in Stop mode and Table 23: Typical and maximum current consumptions in Standby mode Updated footnote 4. in Table 22: Typical and maximum current consumptions in Stop mode Updated footnote 4. in Table 22: Typical and maximum current consumptions in Stop mode Updated Table 44: I/O AC characteristics Updated Table 47: I2C characteristics Updated Table 49: SPI characteristics Updated Table 49: SPI characteristics Updated "non-robust" Table 54: ADC characteristics Removed the note "position of 4.7 µf capacitor" in Section 6.1.6: Power supply scheme Updated Table 66: UFQFPN48 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch quad flat no-lead package mechanical data Updated Table 65: LQFP48 7 x 7 mm, 48-pin low-profile quad flat package mechanical data Added the resistance of TFBGA in Table 71: Thermal characteristics Added Figure 50: Thermal resistance
07-Feb-2013	8	Removed AHB1/AHB2 in Figure 1: Ultralow power STM32L15xx6/8/B block diagram Added IWDG and WWDG rows in Table 5: Working mode-dependent functionalities (from Run/active down to standby). Updated I _{DD} (Supply current during wakeup time from Standby mode) in Table 23: Typical and maximum current consumptions in Standby mode The comment "HSE = 16 MHz(2) (PLL ON for fHCLK above 16 MHz)" replaced by "fHSE = fHCLK up to 16 MHz included, fHSE = fHCLK/2 above 16 MHz (PLL ON)(2)" in Table 19: Current consumption in Sleep mode Updated Stop mode current to 1.2 µA in Ultra-low-power platform Updated entire Section 7: Package information Removed alternate function "I2C2_SMBA" for GPIO pin "PH2" in Table 8: STM32L15xx6/8/B pin definitions Updated Table 27: Low-speed external user clock characteristics and definition of symbol "R _{AIN} " in Table 54: ADC characteristics Removed first sentence in I2C interface characteristics



Table 73. Document revision history (continued)

Date	Revision	Changes
Date 12-Nov-2013	Revision	Changed voltage Range 1 minimum to 1.71 V and updated dynamic voltage scaling range in Table 3: Functionalities depending on the operating power supply range Updated LCD and ADC features in Table 2: Ultralow power STM32L15xx6/8/B device features and peripheral counts. Updated Table 3: Functionalities depending on the operating power supply range. Updated Table 5: Working mode-dependent functionalities (from Run/active down to standby). Updated Figure 3: STM32L15xVx UFBGA100 ballout Added Table 7: Legend/abbreviations used in the pinout table. Updated Figure 10: Pin loading conditions and Figure 11: Pin input voltage. Updated Figure 10: Pin loading conditions and Figure 11: Pin input voltage. Updated Figure 10: Pin loading conditions and Figure 11: Pin input voltage. Updated Figure 10: Power supply scheme. Replaced "2" by "0" in Section 6.1.1 and Section 6.1.2. Updated Table 10: Voltage characteristics. Updated Table 16: Embedded internal reference voltage. Added Section 6.1.7: Optional LCD power supply scheme. Updated Table 16: Embedded internal reference voltage. Added this Note in Section : High-speed external clock generated from a crystal/ceramic resonator Updated Section : Functional susceptibility to I/O current injection. This Section 6.3.5: Wakeup time from Low power mode was previously a paragraph in Section 6.3.4: Supply current characteristics. Updated fi _{HSE} conditions in Table 17: Current consumption in Run mode, code with data processing running from Flash and Table 18: Current consumption in Run mode, code with data processing running from Flash and Table 18: Current consumption in Run mode, code with data processing running from Flash and Table 18: Current consumption in Run mode, code with data processing running from Flash and Table 18: Current consumption in Run mode, code with data processing running from Flash and Table 18: Current consumption in Run mode, code with data processing running from Flash and Table 29: LSE oscillator characteristics (fLSE = 32.768 kHz). Updated Table 28: HSE os



Table 73. Document revision history (continued)

Date	Revision	Changes
12-Nov-2013	9 (continued)	Updated Table 54: ADC characteristics and Figure 27: Typical connection diagram using the ADC. Table 58: Temperature sensor calibration values was previously in Section 3.10.1: Temperature sensor. Updated Table 59: Temperature sensor characteristics. In Table 61: Comparator 2 characteristics, parameter dThreshold/dt, replaced any occurrence of "VREF+" by "V _{REFINT} "Updated Table 63: LQPF100 14 x 14 mm, 100-pin low-profile quad flat package mechanical data, Table 64: LQFP64 10 x 10 mm 64-pin low-profile quad flat package mechanical data, Table 65: LQFP48 7 x 7 mm, 48-pin low-profile quad flat package mechanical data and Table 66: UFQFPN48 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch quad flat no-lead package mechanical data. Updated Figure 33: LQFP100 recommended footprint. Updated Figure 46: TFBGA64 - 5.0x5.0x1.2 mm, 0.5 mm pitch, thin fine-pitch ball grid array package outline title. Remove minimum and typical values of A dimension in Table 67: UFBGA100 7 x 7 x 0.6 mm 0.5 mm pitch, ultra thin fine-pitch ball grid array package mechanical data Deleted second footnote in Figure 42: UFQFPN48 recommended footprint. Updated Section 8: Ordering information title and added first sentence. Changed BOR disabled option identifier in Table 72: Ordering information scheme.
22-Jul-2014	10	Updated Figure 14, Figure 15. Updated Table 5. Updated Figure 6.3.4. Updated note 5 inside Table 54. Updated Ro value inside Table 54.



Table 73. Document revision history (continued)

Date	Revision	Changes
Date	Kevision	<u> </u>
30-Jan-2015	11	Updated DMIPS features in cover page and Section 2: Description. Updated Table 8: STM32L151x6/8/B and STM32L152x6/8/B pin definitions and Table 9: Alternate function input/output putting additional functions. Updated package top view marking in Section 7.1: Package mechanical data. Updated Figure 9: Memory map. Updated Table 56: Maximum source impedance RAIN max adding note 2. Updated Table 72: Ordering information scheme.
28-Apr-2016	12	Updated Section 7: Package information structure: Paragraph titles and paragraph heading level. Updated Section 7: Package information for all package device markings, adding text for device orientation versus pin 1/ ball A1 identifier. Updated Figure 34: LQFP100 14 x 14 mm, 100-pin package top view example removing gate mark. Updated Table 64: LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical data. Updated Section 7.5: UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package information adding Table 68: UFBGA100 7 x 7 mm, 0.5 mm pitch, recommended PCB design rules and Figure 45: UFBGA100 7 x 7 mm, 0.5 mm pitch, package recommended footprint. Updated Section 7.6: TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package information adding Table 70: TFBGA64 5 x 5 mm, 0.5 mm pitch, recommended PCB design rules and changing Figure 48: TFBGA64, 5 x 5 mm, 0.5 mm pitch, recommended footprint. Updated Table 16: Embedded internal reference voltage temperature coefficient at 100ppm/°C. Updated Table 61: Comparator 2 characteristics new maximum threshold voltage temperature coefficient at 100ppm/°C. Updated Table 61: Comparator 2 characteristics new maximum threshold voltage temperature coefficient at 100ppm/°C. Updated Table 61: Voltage characteristics adding note about V _{REF} -pin. Updated Table 5: Working mode-dependent functionalities (from Run/active down to standby) LSI and LSE functionalities putting "Y" in Standby mode. Removed note 1 below Figure 2: Clock tree. Updated Table 57: DAC characteristics resistive load.



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