Panasonic

AN32151A

http://www.semicon.panasonic.co.jp/en/

7 x 17 Dots Matrix LED Driver LSI

FEATURES

- 7 x 17 LED Matrix Driver
  (Total LED that can be driven = 119)
- Internal memory RAM (1-side)
- LDO (1-ch)
- I^2C interface + SPI interface
- 49 pin Wafer Level Chip Size Package (WLCSP)

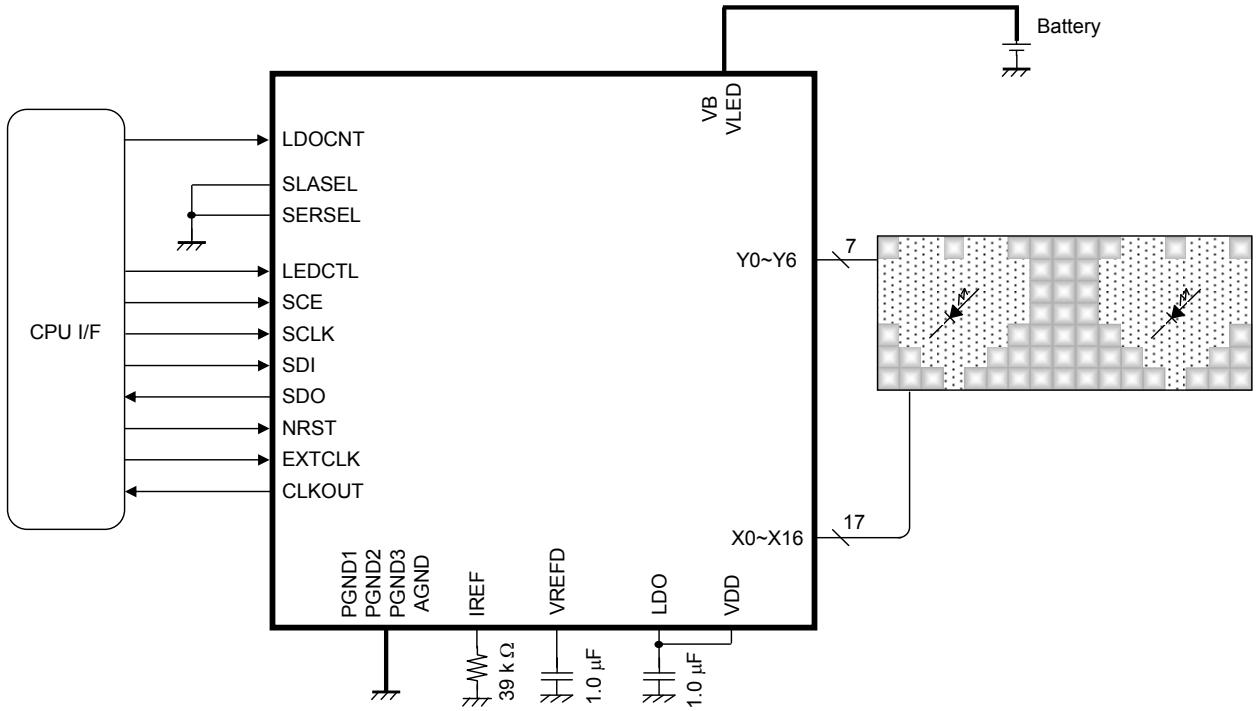
DESCRIPTION

AN32151A is a 7 x 17 LED Matrix Driver equipped with RAM.

APPLICATIONS

- Mobile Phone
- Smart Phone
- PCs
- Game Consoles
- Home Appliances etc.

TYPICAL APPLICATION



Note)
The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

Established : 2009-07-23
Revised : 2013-04-01

CONTENTS

Established : 2009-07-23
Revised : 2013-04-01

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply voltage	VDD_{MAX}	4.3	V	*1
	VB_{MAX}	6.0	V	*1
	$VLED_{MAX}$	6.5	V	*1
Operating ambience temperature	T_{opr}	–30 to + 85	°C	*2
Operating junction temperature	T_j	– 30 to + 125	°C	*2
Storage temperature	T_{stg}	– 55 to + 125	°C	*2
Input Voltage Range	SCE, SLASEL, SCLK, SDI	– 0.3 to 4.3	V	—
	SERSEL, EXTCLK, NRST, LDOCNT, LEDCTL	– 0.3 to 6.0	V	—
Output Voltage Range	SDO, CLKOUT	– 0.3 to 4.3	V	—
	LDO	– 0.3 to 6.0	V	—
	X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16 Y0, Y1, Y2, Y3, Y4, Y5, Y6	– 0.3 to 6.5	V	—
ESD	HBM	1.5 to 2.0	kV	—

Note) This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range.
When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.
*1: VDD_{MAX} = VDD, VB_{MAX} = VB, $VLED_{MAX}$ = VLED.
The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
*2: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

POWER DISSIPATION RATING

PACKAGE	θ_{JA}	P_D (Ta=25 °C)	P_D (Ta=85 °C)
49 pin Wafer Level Chip Size Package (WLCSP)	171.05 °C /W	0.585 W	0.234 W

Note) For the actual usage, please refer to the P_D-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

CAUTION

Although this LSI has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

Established : 2009-07-23
Revised : 2013-04-01

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage range	VDD	1.7	2.6	3.5	V	*1
	VB	3.1	3.6	4.6	V	*1
	VLED	3.1	4.9	5.6	V	*1
Input Voltage Range	SCE, SLASEL, SCLK, SDI	– 0.3	—	VDD + 0.3	V	*2
	SERSEL, EXTCLK, NRST, LDOCNT, LEDCTL	– 0.3	—	VB + 0.3	V	*2
Output Voltage Range	SDO, CLKOUT	– 0.3	—	VDD + 0.3	V	*2
	LDO	– 0.3	—	VB + 0.3	V	*2
	X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16 Y0, Y1, Y2, Y3, Y4, Y5, Y6	– 0.3	—	VLED + 0.3	V	*2

Note) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
Do not apply external currents and voltages to any pin not specifically mentioned.
Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for AGND, PGND1, PGND2 and PGND3.
VDD is voltage for VDD. VB is voltage for VB. VLED is voltage for VLED.
*2: (VDD + 0.3) V must not exceed 4.3 V. (VB + 0.3) V must not exceed 6 V.
(VLED + 0.3) V must not exceed 6.5 V.

Established : 2009-07-23
Revised : 2013-04-01

ELECTRICAL CHARACTERISTICS

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current consumption							
Current consumption (1) Off mode	ICC1	VB = 3.6 V LDOCNT = Low	—	0	1	µA	—
Current consumption (2) Normal mode	ICC2	VB = 3.6 V LDOCNT = High ILOAD = 0 µA	—	14	20	µA	—
Reference voltage source							
Output voltage	VREF	VB = 3.6 V I_{VREF} = 0 µA	1.17	1.20	1.23	V	—
EXTCLK, NRST, LDOCNT, SERSEL, LEDCTL							
High-level input voltage range	VIH1	High-level recognition voltage	1.4	—	VB + 0.3	V	—
Low-level input voltage range	VIL1	Low-level recognition voltage	–0.3	—	0.4	V	—
High-level input current	IIH1	Vin = 1.85 V	—	0	1	µA	—
Low-level input current	IIL1	Vin = 0 V	—	0	1	µA	—
SCLK, SDI							
High-level input voltage range	VIH2	High-level recognition voltage	VDD × 0.7	—	VDD_{max} + 0.5	V	—
Low-level input voltage range	VIL2	Low-level recognition voltage	– 0.5	—	VDD × 0.3	V	—
High-level input current	IIH2	Vin = 1.85 V	—	0	1	µA	—
Low-level input current	IIL2	Vin = 0 V	—	0	1	µA	—
Low-level output voltage (1)	VOL1	I_{SDI} = 3 mA, VDD > 2 V VOL1 = V_{SDI}	0	—	0.4	V	—
Low-level output voltage (2)	VOL2	I_{SDI} = 3 mA, VDD < 2 V VOL2 = V_{SDI}	0	—	VDD × 0.2	V	—
Clock frequency	FSCL	Input frequency at SCLK	0	—	400	kHz	—

Established : 2009-07-23
Revised : 2013-04-01

ELECTRICAL CHARACTERISTICS (continued)

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SCE, SLASEL							
High-level input voltage range	VIH3	High-level recognition voltage	VDD × 0.7	—	VDD_{max} + 0.5	V	—
Low-level input voltage range	VIL3	Low-level recognition voltage	– 0.5	—	VDD × 0.3	V	—
High-level input current	IIH3	Vin = 1.85 V	—	0	1	µA	—
Low-level input current	IIL3	Vin = 0 V	—	0	1	µA	—
SDO, CLKOUT							
High-level output voltage	VOH4	Iin = – 2 mA	VDD × 0.8	—	—	V	—
Low-level output voltage	VOL4	Iin = 2 mA	—	—	VDD × 0.2	V	—
Constant voltage source (LDO)							
Output voltage (1)	VL1	I_{LDO} = – 10 µA	1.79	1.85	1.91	V	—
Output voltage (2)	VL2	VB = 3.1 V I_{LDO} = – 30 mA	1.79	1.85	1.91	V	—
Short-circuit protection current	IPT1	LDOCNT = "H" REG18 = [1] V_{LDO} = 0 V	50	100	200	mA	—
Ripple rejection ratio (1)	PSL11	VB = 3.6 V + 0.2 V[p-p] f = 1 kHz I_{LDO} = – 15 mA PSL11 = 20log(acV_{LDO} / 0.2)	—	– 45	– 40	dB	—
Ripple rejection ratio (2)	PSL12	VB = 3.6 V + 0.2 V[p-p] f = 10 kHz I_{LDO} = – 15 mA PSL12 = 20log(acV_{LDO} / 0.2)	—	– 35	– 25	dB	—
Oscillator							
Oscillation frequency	FOSC	OSCEN = [1]	0.96	1.2	1.44	MHz	—
SDO, CLKOUT							
High-level output voltage	VOH4	Iin = – 2 mA	VDD × 0.8	—	—	V	—
Low-level output voltage	VOL4	Iin = 2 mA	—	—	VDD × 0.2	V	—

Established : 2009-07-23
Revised : 2013-04-01

ELECTRICAL CHARACTERISTICS (continued)

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Constant current source (for matrix LED)							
Output current (1)	IMX1	At 1.400 mA setup V_{X0} to V_{X16} = 1 V IMX1 = I_{X0} to I_{X16}	1.288	1.400	1.512	mA	*1, 2
Output current (2)	IMX2	At 2.800 mA setup V_{X0} to V_{X16} = 1 V IMX2 = I_{X0} to I_{X16}	2.576	2.800	3.024	mA	*1, 2
Output current (3)	IMX4	At 5.600 mA setup V_{X0} to V_{X16} = 1 V IMX4 = I_{X0} to I_{X16}	5.152	5.600	6.048	mA	*1, 2
Output current (4)	IMX8	At 11.20 mA setup V_{X0} to V_{X16} = 1 V IMX8 = I_{X0} to I_{X16}	10.30	11.20	12.10	mA	*1, 2
Output current (5)	IMX16	At 21.00 mA setup V_{X0} to V_{X16} = 1 V IMX16 = I_{X0} to I_{X16}	19.32	21.00	22.68	mA	*1, 2
Leak current at Off mode	IMXOFF	At Off setup V_{X0} to V_{X16} = 4.75 V IMXOFF = I_{X0} to I_{X16}	—	—	1	μA	—
Error between channels	IMXCH	Difference current between the average of all channels and each channel	– 5	—	5	%	*2
SCAN switch							
Resistance at switch On	RSCAN	V_{VLED}= 4.62 V I_{Y0} to I_{Y6} = – 5 mA RSCAN = V_{Y0} to V_{Y6} / 5 mA	—	1	2	Ω	—

Note) *1 : Values when recommended parts (ERJ2RHD393X) are used for IREF pin. The other current settings are combination of above items.

*2 : All of the setting values of matrix block are with absolute accuracy of ± 8 %, the error between channels of ± 5 %.

Established : 2009-07-23
Revised : 2013-04-01

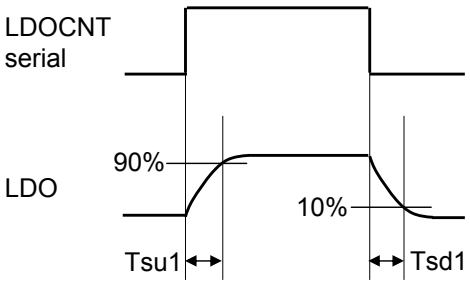
ELECTRICAL CHARACTERISTICS (continued)

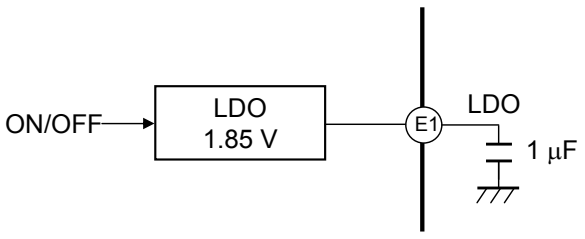
VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Constant current source (for matrix LED)							
Saturation voltage	Vsat	Voltage value when the setting current value changes to 5 % or more of by V_{X0} to V_{X16}	—	0.2	0.4	V	—
TSD (Thermal shutdown protection circuit)							
Detection temperature	Tdet	Temperature which LDO, Constant current circuit, and Matrix SW turn off.	—	160	—	°C	*3 *4
Recovery temperature	Tsd11	Recovering temperature	—	110	—	°C	*4 *5
Constant voltage regulator (LDO) Output capacitor : 1 µF, Output capacitor's ESR : less than 0.1 Ω							
Rise time	Tsu1	Time until output voltage reaches 0 V to 0%. (No load)	—	0.25	—	ms	*4
Fall time	Tsd1	Time until output voltage reaches 10 %.	—	5	—	ms	*4
Maximum load current	IOMAX1	—	—	15	—	mA	*4
Load transient response (1)	Vtr11	Iout = –50 µA → –15 mA (1 µs)	—	70	—	mV	*4
Load transient response (2)	Vtr12	Iout = –15 mA → –50 µA (1 µs)	—	70	—	mV	*4

Note) *3 : LDO, Constant current circuit, and Matrix SW turn off when TSD operates.
*4 : Typical Design Value
*5 : LDO only recovers after TSD becomes ON state. Logic block becomes reset state.





Established : 2009-07-23
Revised : 2013-04-01

ELECTRICAL CHARACTERISTICS (continued)

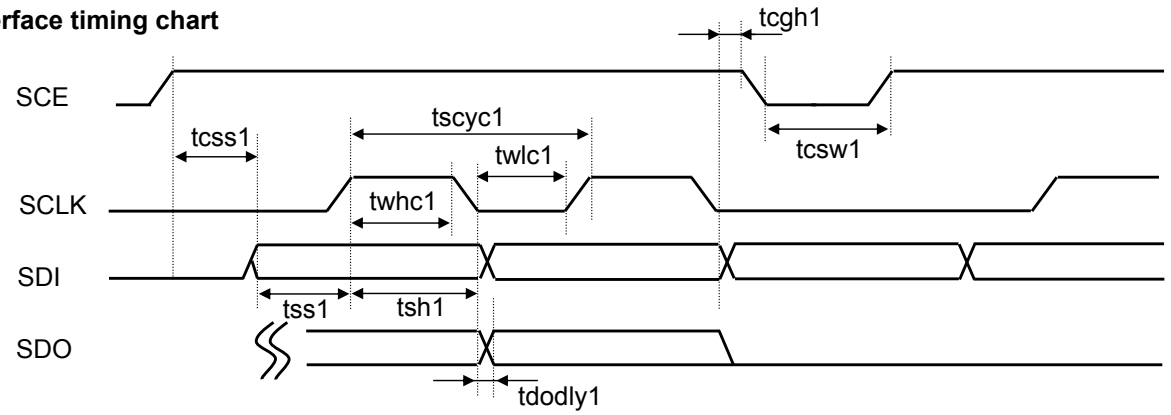
VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Microcomputer interface characteristics (VDD = 1.85 V ± 3%) Reception timing							
SCLK cycle period	tscyc1	—	—	152	—	ns	*4
SCLK cycle period High period	twhc1	—	—	70	—	Ns	*4
SCLK cycle period Low period	Twlc1	—	—	70	—	Ns	*4
Serial data setup time	Tss1	—	—	62	—	ns	*4
Serial data hold time	tsh1	—	—	62	—	ns	*4
Transceiving interval	tcsw1	—	—	62	—	ns	*4
Chip enable setup time	tcss1	—	—	5	—	ns	*4
Chip enable hold time	tcgh1	—	—	5	—	ns	*4
Microcomputer interface characteristics (VDD = 1.85 V ± 3%) Transmission timing							
SCLK cycle period	tscyc1	—	—	152	—	ns	*4
SCLK cycle period High period	twhc1	—	—	70	—	ns	*4
SCLK cycle period Low period	twlc1	—	—	70	—	ns	*4
Serial data setup time	tss1	—	—	62	—	ns	*4
Serial data hold time	tsh1	—	—	62	—	ns	*4
Transceiving interval	tcsw1	—	—	62	—	ns	*4
Chip enable setup time	tcss1	—	—	5	—	ns	*4
Chip enable hold time	tcgh1	—	—	5	—	ns	*4
DC delay time	tdodly1	Read mode only	—	30	—	ns	*4

Note) *4 : Typical Design Value

Interface timing chart



Established : 2009-07-23
Revised : 2013-04-01

ELECTRICAL CHARACTERISTICS (continued)

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
I²C bus (Internal I/O stage characteristics)							
Hysteresis of Schmitt trigger input 1	Vhys1	Hysteresis of SCLK, SDI VDD > 2 V	0.05 × VDD	—	—	V	*6 *7
Hysteresis of Schmitt trigger input 2	Vhys2	Hysteresis of SCLK, SDI VDD < 2 V	0.1 × VDD	—	—	V	*6 *7
Output fall time from V_{IHmin} to V_{ILmax}	Tof	Bus capacitance : 10 pF to 400pF $I_P \leq 6$ mA (V_{OLmax} = 0.6 V) I_P : Max. sink current	20 + 0.1C_b	—	250	ns	*6 *7
Pulse width of spikes which must be suppressed by the input filter	Tsp	—	0	—	50	ns	*6 *7
Capacitance for each I/O pin	Ci	—	—	—	10	pF	*6 *7

Note) *6 : The timing of Fast-mode and Normal mode devices in I²C-bus is specified in Page.12. All values referred to V_{IHMIN} and V_{ILMAX} level.

*7 : These are values checked by design but not production tested.

Established : 2009-07-23
Revised : 2013-04-01

ELECTRICAL CHARACTERISTICS (continued)

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
I²C bus (Bus line specifications)							
Hold time (repeated) START condition	$t_{HD:STA}$	The first clock pulse is generated after this period	0.6	—	—	µs	*6 *7
Low period of the SCL clock	t_{LOW}	—	1.3	—	—	µs	*6 *7
High period of the SCL clock	t_{HIGH}	—	0.6	—	—	µs	*6 *7
Set-up time for a repeat START condition	$t_{SU:STA}$	—	0.6	—	—	µs	*6 *7
Data hold time	$t_{HD:DAT}$	—	0	—	0.9	µs	*6 *7
Data set-up time	$t_{SU:DAT}$	—	100	—	—	ns	*6 *7
Rise time of both SDA and SCL signals	tr	—	20 + 0.1C_b	—	300	ns	*6 *7
Fall time of both SDA and SCL signals	t_f	—	20 + 0.1C_b	—	300	ns	*6 *7
Set-up time of STOP condition	$t_{SU:STO}$	—	0.6	—	—	µs	*6 *7
Bus free time between STOP and START condition	t_{BUF}	—	1.3	—	—	µs	*6 *7
Capacitive load for each bus line	C_b	—	—	—	400	pF	*6 *7
Noise margin at the Low-level for each connected device (with hysteresis)	V_{aL}	—	0.1 × VDD	—	—	V	*6 *7
Noise margin at the High-level for each connected device (with hysteresis)	V_{aH}	—	0.2 × VDD	—	—	V	*6 *7

Note) *6 : The timing of Fast-mode and Normal mode devices in I²C-bus is specified in Page.12. All values referred to V_{IHMIN} and V_{ILMAX} level.

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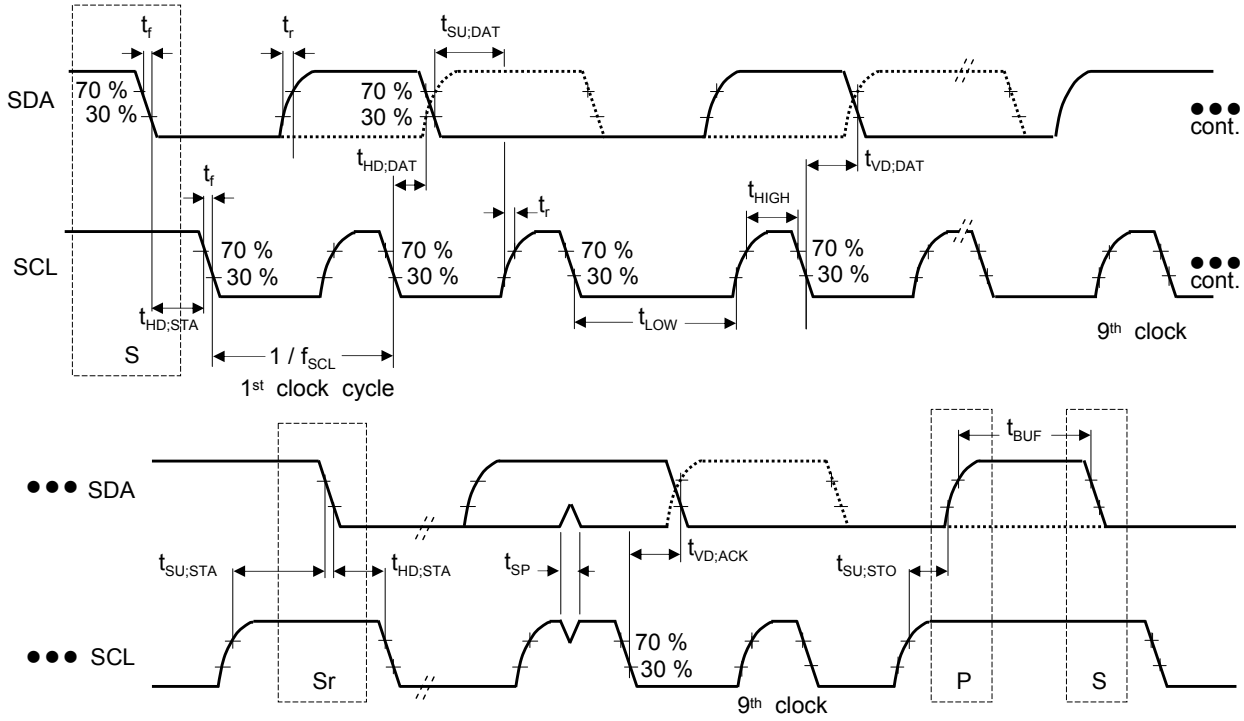
Established : 2009-07-23
Revised : 2013-04-01

ELECTRICAL CHARACTERISTICS (continued)

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.



V_{ILMAX} = 0.3 V_{DD}

V_{IHMIN} = 0.7 V_{DD}

S : START condition

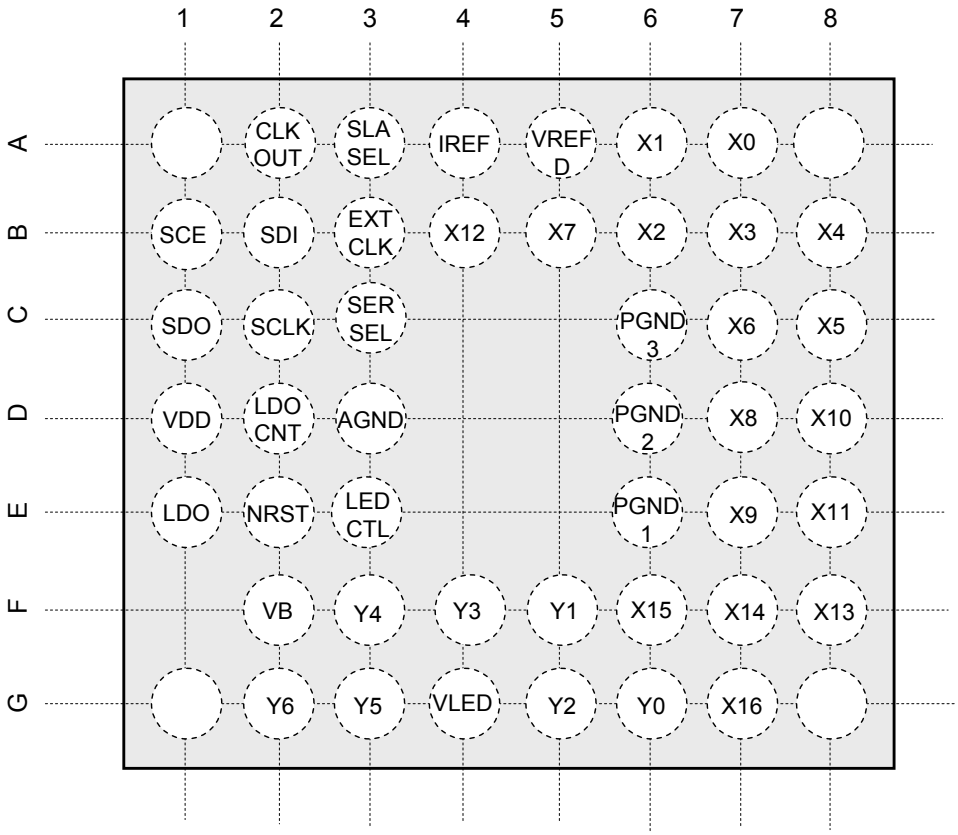
Sr : Repeat START condition

P : STOP condition

Established : 2 0 0 0-0 7-2 3
Revised : 2 0 0 1-0 4 0 1

PIN CONFIGURATION

Top View



Note) Four-cornered pins have been connected to GND.

Established : 2009-07-23
Revised : 2013-04-01

PIN FUNCTIONS

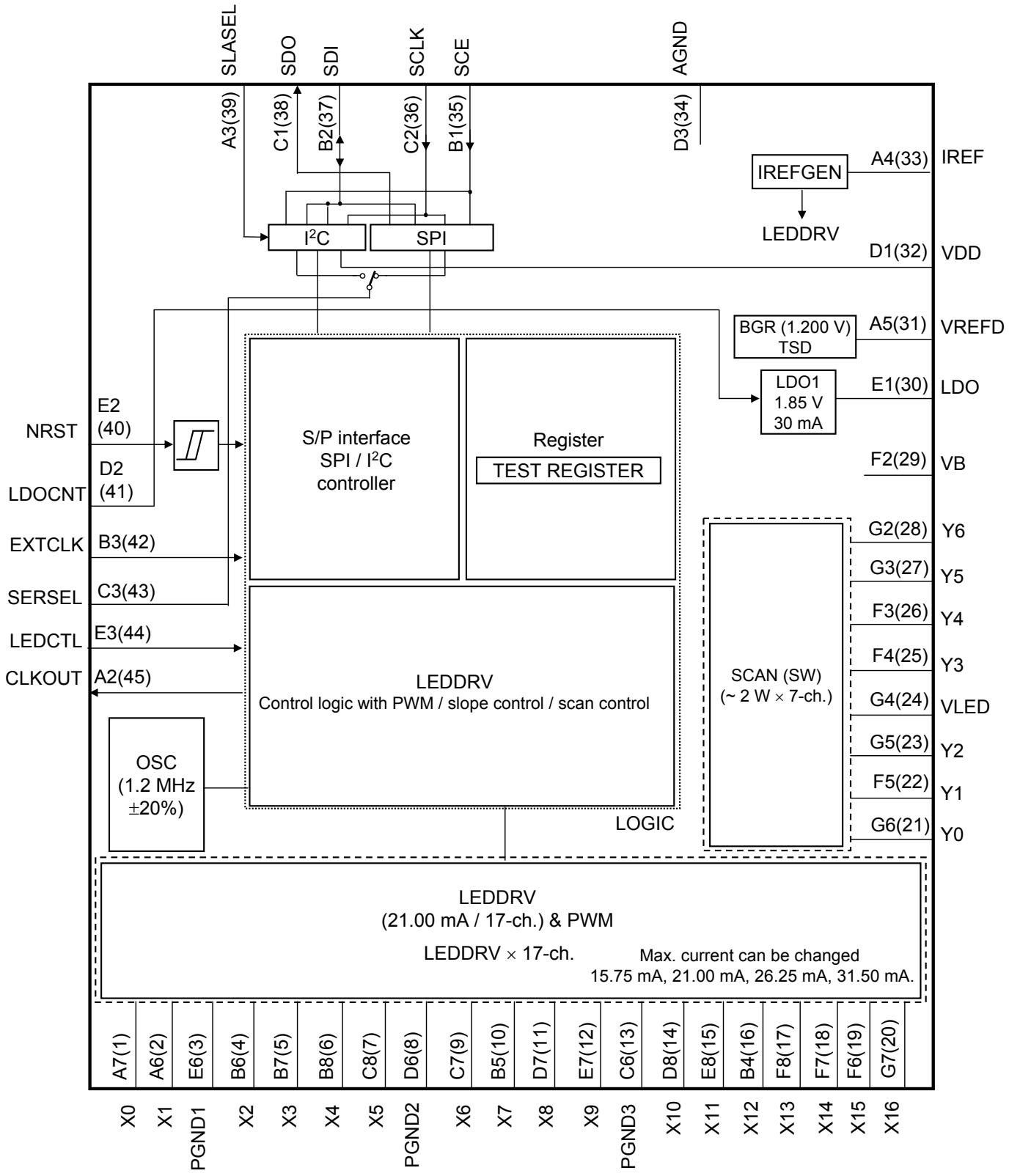
Pin No.	Pin name	Type	Description
A7(1)	X0	Output	PWM control output pin with constant current circuit This pin is connected with A column of matrix LED.
A6(2)	X1	Output	PWM control output pin with constant current circuit This pin is connected with B column of matrix LED.
E6(3) D6(8) C6(13)	PGND1 PGND2 PGND3	Ground	Ground pin for matrix LED
B6(4)	X2	Output	PWM control output pin with constant current circuit This pin is connected with C column of matrix LED.
B7(5)	X3	Output	PWM control output pin with constant current circuit This pin is connected with D column of matrix LED.
B8(6)	X4	Output	PWM control output pin with constant current circuit This pin is connected with E column of matrix LED.
C8(7)	X5	Output	PWM control output pin with constant current circuit This pin is connected with F column of matrix LED.
C7(9)	X6	Output	PWM control output pin with constant current circuit This pin is connected with G column of matrix LED.
B5(10)	X7	Output	PWM control output pin with constant current circuit This pin is connected with H column of matrix LED.
D7(11)	X8	Output	PWM control output pin with constant current circuit This pin is connected with I column of matrix LED.
E7(12)	X9	Output	PWM control output pin with constant current circuit This pin is connected with J column of matrix LED.
D8(14)	X10	Output	PWM control output pin with constant current circuit This pin is connected with K column of matrix LED.
E8(15)	X11	Output	PWM control output pin with constant current circuit This pin is connected with L column of matrix LED.
B4(16)	X12	Output	PWM control output pin with constant current circuit This pin is connected with M column of matrix LED.
F8(17)	X13	Output	PWM control output pin with constant current circuit This pin is connected with N column of matrix LED.
F7(18)	X14	Output	PWM control output pin with constant current circuit This pin is connected with O column of matrix LED.
F6(19)	X15	Output	PWM control output pin with constant current circuit This pin is connected with P column of matrix LED.
G7(20)	X16	Output	PWM control output pin with constant current circuit This pin is connected with Q column of matrix LED.
G6(21)	Y0	Output	PWM control output pin with constant current circuit This pin is connected with the 1st row of matrix LED.
F5(22)	Y1	Output	PWM control output pin with constant current circuit This pin is connected with the 2nd row of matrix LED.

PIN FUNCTIONS (continued)

Pin No.	Pin name	Type	Description
G5(23)	Y2	Output	PWM control output pin with constant current circuit This pin is connected with the 3rd row of matrix LED.
G4(24)	VLED	Power supply	Power supply's connection pin for matrix LED This pin should be connected with the output of battery or step-up converter.
F4(25)	Y3	Output	PWM control output pin with constant current circuit This pin is connected with the 4th row of matrix LED.
F3(26)	Y4	Output	PWM control output pin with constant current circuit This pin is connected with the 5th row of matrix LED.
G3(27)	Y5	Output	PWM control output pin with constant current circuit This pin is connected with the 6th row of matrix LED.
G2(28)	Y6	Output	PWM control output pin with constant current circuit This pin is connected with the 7th row of matrix LED.
F2(29)	VB	Power supply	Power supply's connection pin for BGR circuit and LDO circuit
E1(30)	LDO	Output	Power supply's connection pin for serial interface input block and internal logic.
A5(31)	VREFD	Output	BGR circuit output pin
D1(32)	VDD	Power supply	Power supply pin for output interface
A4(33)	IREF	Output	Resistor connection pin for constant current setup
D3(34)	AGND	Ground	Ground pin for analogue circuitry
B1(35)	SCE	Input	SPI interface chip-enable pin (High active) (Slave address selection control pin 1 at I^2C mode)
C2(36)	SCLK	Input	Common clock input pin in both SPI interface and I^2C interface
B2(37)	SDI	Input / Output	Data input pin for SPI interface Data input/output pin for I^2C interface
C1(38)	SDO	Output	Data output pin for SPI interface
A3(39)	SLASEL	Input	Slave address selection control pin 2 at I^2C mode
E2(40)	NRST	Input	Reset input pin (Low active)
D2(41)	LDOCNT	Input	LDO ON/OFF control pin
B3(42)	EXTCLK	Input	External clock input pin
C3(43)	SERSEL	Input	SPI, I^2C selection pin
E3(44)	LEDCTL	Input	LED lit external synchronous input pin
A2(45)	CLKOUT	Output	Internal clock output pin

Established : 2009-07-23
Revised : 2013-04-01

FUNCTIONAL BLOCK DIAGRAM



Note) This block diagram is for explaining functions.
Part of the block diagram may be omitted, or it may be simplified.

Established : 2009-07-23
Revised : 2013-04-01

OPERATION

1. Power supply sequence control

Power supply turn on/off sequence

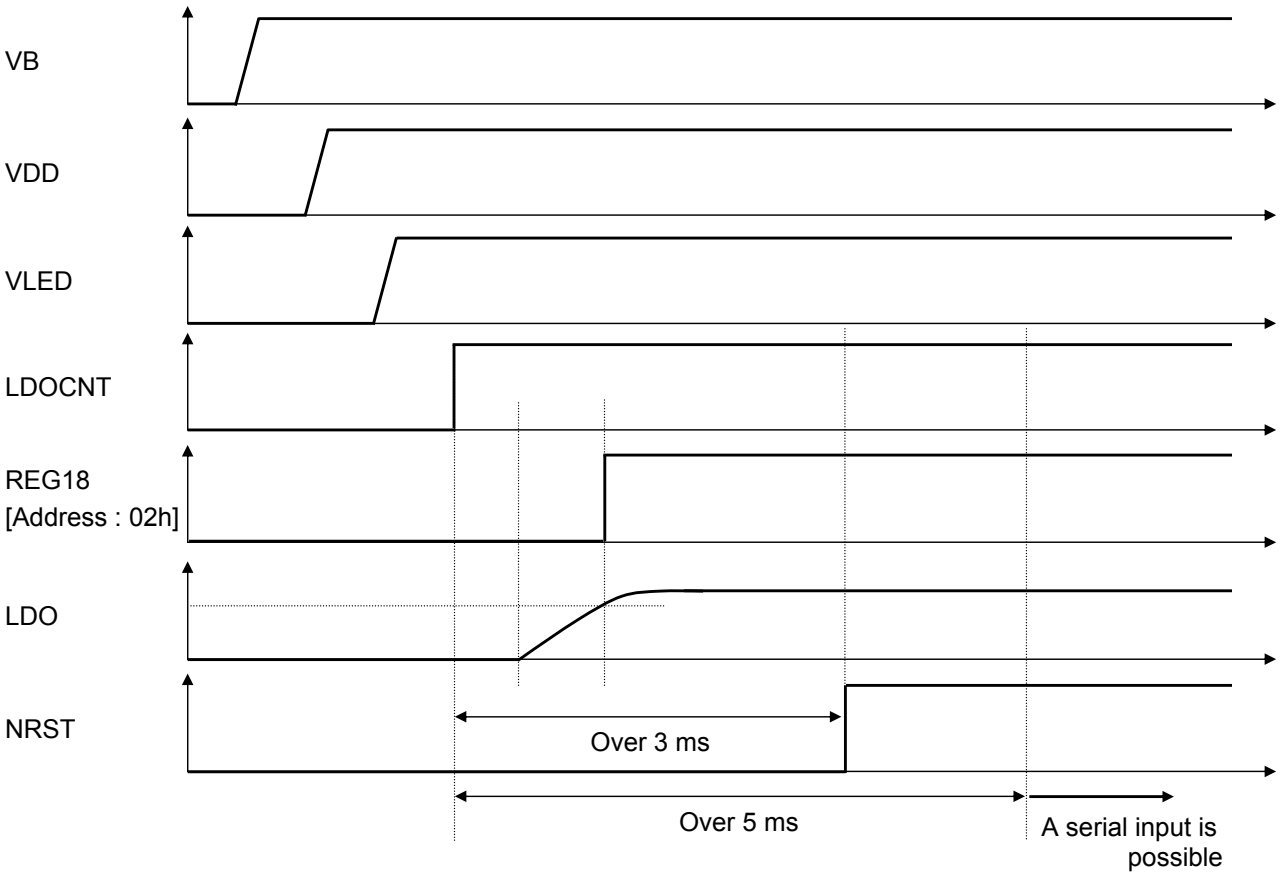
Mode	LDOCNT	REG18	Remarks
OFF	Low	0	LDOCNT should be set to High for the recovery from OFF mode.
OFF ↓ Normal mode	Low → High	0/1	Serial signal is not received at LDOCNT = Low and REG18 = [0].
	High	0/1	
Normal mode ↓ OFF	High → Low	0	LDO turns on at LDOCNT = High regardless of REG18. Serial signal is not received at NRST = Low. Serial signal can be received 5 ms or more after LDOCNT = High. NRST should have one or more Low period of internal clock. Inputting signal except rectangular wave into NRST pin is prohibited. When NRST = Low, the settings of all registers become default values. (Since the default value of REG18 bit becomes [1] at NRST= Low, LDO shifts to OFF mode at LDOCNT = Low.) All register setting become default setting when LDO turns off. The setting order to change to off mode is as follows. REG18 = [0] → LDOCNT = Low → NRST = Low

Established : 2009-07-23
Revised : 2013-04-01

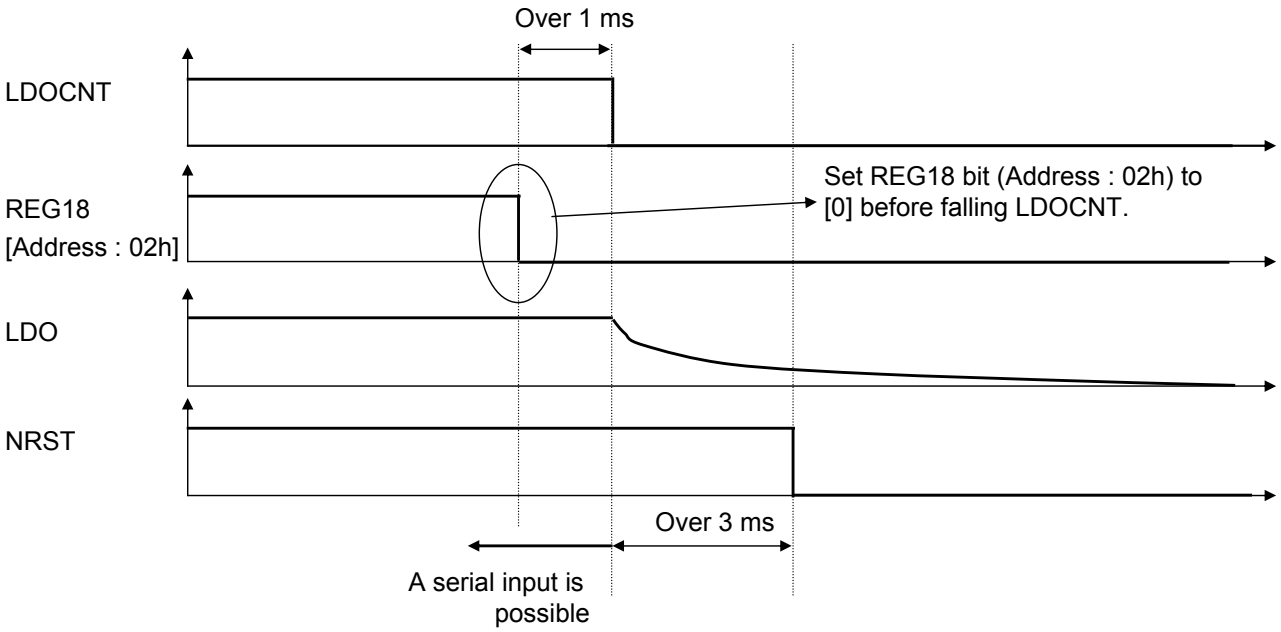
OPERATION (continued)

1. Power supply sequence control (continued)

Shift to Normal mode from OFF mode



Shift to OFF mode from Normal mode



Established : 2009-07-23
Revised : 2013-04-01

OPERATION (continued)

2. Register map (1)

Sub Address	R/W	Data name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	R/W	RST	—	—	—	—	—	—	RAMRST	SRST
01h	R/W	POWERCNT	—	—	—	—	—	—	—	OSCEN
02h	R/W	LDOCNT	—	—	—	—	—	—	—	REG18
03h	R	LSITEST	For test (Access inhibit)							
04h	R/W	OPTION	LEDACT	DISMTX	—	—	—	—	CLKOUT	EXTCLK
05h	R/W	MTXON	—	—	—	—	IMAX[1:0]		—	MTXON
06h	R/W	XCONST1	X16	X15	X14	X13	X12	X11	X10	X9
07h	R/W	XCONST2	X8	X7	X6	X5	X4	X3	X2	X1
08h	R/W	XCONST3	—	—	—	—	—	—	—	X0

Established : 2009-07-23
Revised : 2013-04-01

OPERATION (continued)

2. Register map (2)

Sub Address	R/W	Data name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
09h	R/W	A1	BLA1[3:0]				FRA1[1:0]		DLA1[1:0]	
0Ah	R/W	A2	BLA2[3:0]				FRA2[1:0]		DLA2[1:0]	
0Bh	R/W	A3	BLA3[3:0]				FRA3[1:0]		DLA3[1:0]	
0Ch	R/W	A4	BLA4[3:0]				FRA4[1:0]		DLA4[1:0]	
0Dh	R/W	A5	BLA5[3:0]				FRA5[1:0]		DLA5[1:0]	
0Eh	R/W	A6	BLA6[3:0]				FRA6[1:0]		DLA6[1:0]	
0Fh	R/W	A7	BLA7[3:0]				FRA7[1:0]		DLA7[1:0]	
10h	R/W	B1	BLB1[3:0]				FRB1[1:0]		DLB1[1:0]	
11h	R/W	B2	BLB2[3:0]				FRB2[1:0]		DLB2[1:0]	
12h	R/W	B3	BLB3[3:0]				FRB3[1:0]		DLB3[1:0]	
13h	R/W	B4	BLB4[3:0]				FRB4[1:0]		DLB4[1:0]	
14h	R/W	B5	BLB5[3:0]				FRB5[1:0]		DLB5[1:0]	
15h	R/W	B6	BLB6[3:0]				FRB6[1:0]		DLB6[1:0]	
16h	R/W	B7	BLB7[3:0]				FRB7[1:0]		DLB7[1:0]	
17h	R/W	C1	BLC1[3:0]				FRC1[1:0]		DLC1[1:0]	
18h	R/W	C2	BLC2[3:0]				FRC2[1:0]		DLC2[1:0]	
19h	R/W	C3	BLC3[3:0]				FRC3[1:0]		DLC3[1:0]	
1Ah	R/W	C4	BLC4[3:0]				FRC4[1:0]		DLC4[1:0]	
1Bh	R/W	C5	BLC5[3:0]				FRC5[1:0]		DLC5[1:0]	
1Ch	R/W	C6	BLC6[3:0]				FRC6[1:0]		DLC6[1:0]	
1Dh	R/W	C7	BLC7[3:0]				FRC7[1:0]		DLC7[1:0]	
1Eh	R/W	D1	BLD1[3:0]				FRD1[1:0]		DLD1[1:0]	
1Fh	R/W	D2	BLD2[3:0]				FRD2[1:0]		DLD2[1:0]	
20h	R/W	D3	BLD3[3:0]				FRD3[1:0]		DLD3[1:0]	
21h	R/W	D4	BLD4[3:0]				FRD4[1:0]		DLD4[1:0]	
22h	R/W	D5	BLD5[3:0]				FRD5[1:0]		DLD5[1:0]	
23h	R/W	D6	BLD6[3:0]				FRD6[1:0]		DLD6[1:0]	
24h	R/W	D7	BLD7[3:0]				FRD7[1:0]		DLD7[1:0]	
25h	R/W	E1	BLE1[3:0]				FRE1[1:0]		DLE1[1:0]	
26h	R/W	E2	BLE2[3:0]				FRE2[1:0]		DLE2[1:0]	
27h	R/W	E3	BLE3[3:0]				FRE3[1:0]		DLE3[1:0]	
28h	R/W	E4	BLE4[3:0]				FRE4[1:0]		DLE4[1:0]	
29h	R/W	E5	BLE5[3:0]				FRE5[1:0]		DLE5[1:0]	
2Ah	R/W	E6	BLE6[3:0]				FRE6[1:0]		DLE6[1:0]	
2Bh	R/W	E7	BLE7[3:0]				FRE7[1:0]		DLE7[1:0]	

Established : 2009-07-23
Revised : 2013-04-01

OPERATION (continued)

2. Register map (2) (continued)

Sub Address	R/W	Data name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
2Ch	R/W	F1	BLF1[3:0]				FRF1[1:0]		DLF1[1:0]	
2Dh	R/W	F2	BLF2[3:0]				FRF2[1:0]		DLF2[1:0]	
2Eh	R/W	F3	BLF3[3:0]				FRF3[1:0]		DLF3[1:0]	
2Fh	R/W	F4	BLF4[3:0]				FRF4[1:0]		DLF4[1:0]	
30h	R/W	F5	BLF5[3:0]				FRF5[1:0]		DLF5[1:0]	
31h	R/W	F6	BLF6[3:0]				FRF6[1:0]		DLF6[1:0]	
32h	R/W	F7	BLF7[3:0]				FRF7[1:0]		DLF7[1:0]	
33h	R/W	G1	BLG1[3:0]				FRG1[1:0]		DLG1[1:0]	
34h	R/W	G2	BLG2[3:0]				FRG2[1:0]		DLG2[1:0]	
35h	R/W	G3	BLG3[3:0]				FRG3[1:0]		DLG3[1:0]	
36h	R/W	G4	BLG4[3:0]				FRG4[1:0]		DLG4[1:0]	
37h	R/W	G5	BLG5[3:0]				FRG5[1:0]		DLG5[1:0]	
38h	R/W	G6	BLG6[3:0]				FRG6[1:0]		DLG6[1:0]	
39h	R/W	G7	BLG7[3:0]				FRG7[1:0]		DLG7[1:0]	
3Ah	R/W	H1	BLH1[3:0]				FRH1[1:0]		DLH1[1:0]	
3Bh	R/W	H2	BLH2[3:0]				FRH2[1:0]		DLH2[1:0]	
3Ch	R/W	H3	BLH3[3:0]				FRH3[1:0]		DLH3[1:0]	
3Dh	R/W	H4	BLH4[3:0]				FRH4[1:0]		DLH4[1:0]	
3Eh	R/W	H5	BLH5[3:0]				FRH5[1:0]		DLH5[1:0]	
3Fh	R/W	H6	BLH6[3:0]				FRH6[1:0]		DLH6[1:0]	
40h	R/W	H7	BLH7[3:0]				FRH7[1:0]		DLH7[1:0]	
41h	R/W	I1	BLI1[3:0]				FRI1[1:0]		DLI1[1:0]	
42h	R/W	I2	BLI2[3:0]				FRI2[1:0]		DLI2[1:0]	
43h	R/W	I3	BLI3[3:0]				FRI3[1:0]		DLI3[1:0]	
44h	R/W	I4	BLI4[3:0]				FRI4[1:0]		DLI4[1:0]	
45h	R/W	I5	BLI5[3:0]				FRI5[1:0]		DLI5[1:0]	
46h	R/W	I6	BLI6[3:0]				FRI6[1:0]		DLI6[1:0]	
47h	R/W	I7	BLI7[3:0]				FRI7[1:0]		DLI7[1:0]	
48h	R/W	J1	BLJ1[3:0]				FRJ1[1:0]		DLJ1[1:0]	
49h	R/W	J2	BLJ2[3:0]				FRJ2[1:0]		DLJ2[1:0]	
4Ah	R/W	J3	BLJ3[3:0]				FRJ3[1:0]		DLJ3[1:0]	
4Bh	R/W	J4	BLJ4[3:0]				FRJ4[1:0]		DLJ4[1:0]	
4Ch	R/W	J5	BLJ5[3:0]				FRJ5[1:0]		DLJ5[1:0]	
4Dh	R/W	J6	BLJ6[3:0]				FRJ6[1:0]		DLJ6[1:0]	
4Eh	R/W	J7	BLJ7[3:0]				FRJ7[1:0]		DLJ7[1:0]	

Established : 2009-07-23
Revised : 2013-04-01

OPERATION (continued)

2. Register map (2) (continued)

Sub Address	R/W	Data name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
4Fh	R/W	K1	BLK1[3:0]				FRK1[1:0]		DLK1[1:0]	
50h	R/W	K2	BLK2[3:0]				FRK2[1:0]		DLK2[1:0]	
51h	R/W	K3	BLK3[3:0]				FRK3[1:0]		DLK3[1:0]	
52h	R/W	K4	BLK4[3:0]				FRK4[1:0]		DLK4[1:0]	
53h	R/W	K5	BLK5[3:0]				FRK5[1:0]		DLK5[1:0]	
54h	R/W	K6	BLK6[3:0]				FRK6[1:0]		DLK6[1:0]	
55h	R/W	K7	BLK7[3:0]				FRK7[1:0]		DLK7[1:0]	
56h	R/W	L1	BLL1[3:0]				FRL1[1:0]		DLL1[1:0]	
57h	R/W	L2	BLL2[3:0]				FRL2[1:0]		DLL2[1:0]	
58h	R/W	L3	BLL3[3:0]				FRL3[1:0]		DLL3[1:0]	
59h	R/W	L4	BLL4[3:0]				FRL4[1:0]		DLL4[1:0]	
5Ah	R/W	L5	BLL5[3:0]				FRL5[1:0]		DLL5[1:0]	
5Bh	R/W	L6	BLL6[3:0]				FRL6[1:0]		DLL6[1:0]	
5Ch	R/W	L7	BLL7[3:0]				FRL7[1:0]		DLL7[1:0]	
5Dh	R/W	M1	BLM1[3:0]				FRM1[1:0]		DLM1[1:0]	
5Eh	R/W	M2	BLM2[3:0]				FRM2[1:0]		DLM2[1:0]	
5Fh	R/W	M3	BLM3[3:0]				FRM3[1:0]		DLM3[1:0]	
60h	R/W	M4	BLM4[3:0]				FRM4[1:0]		DLM4[1:0]	
61h	R/W	M5	BLM5[3:0]				FRM5[1:0]		DLM5[1:0]	
62h	R/W	M6	BLM6[3:0]				FRM6[1:0]		DLM6[1:0]	
63h	R/W	M7	BLM7[3:0]				FRM7[1:0]		DLM7[1:0]	
64h	R/W	N1	BLN1[3:0]				FRN1[1:0]		DLN1[1:0]	
65h	R/W	N2	BLN2[3:0]				FRN2[1:0]		DLN2[1:0]	
66h	R/W	N3	BLN3[3:0]				FRN3[1:0]		DLN3[1:0]	
67h	R/W	N4	BLN4[3:0]				FRN4[1:0]		DLN4[1:0]	
68h	R/W	N5	BLN5[3:0]				FRN5[1:0]		DLN5[1:0]	
69h	R/W	N6	BLN6[3:0]				FRN6[1:0]		DLN6[1:0]	
6Ah	R/W	N7	BLN7[3:0]				FRN7[1:0]		DLN7[1:0]	
6Bh	R/W	O1	BLO1[3:0]				FRO1[1:0]		DLO1[1:0]	
6Ch	R/W	O2	BLO2[3:0]				FRO2[1:0]		DLO2[1:0]	
6Dh	R/W	O3	BLO3[3:0]				FRO3[1:0]		DLO3[1:0]	
6Eh	R/W	O4	BLO4[3:0]				FRO4[1:0]		DLO4[1:0]	
6Fh	R/W	O5	BLO5[3:0]				FRO5[1:0]		DLO5[1:0]	
70h	R/W	O6	BLO6[3:0]				FRO6[1:0]		DLO6[1:0]	
71h	R/W	O7	BLO7[3:0]				FRO7[1:0]		DLO7[1:0]	

Established : 2009-07-23
Revised : 2013-04-01

OPERATION (continued)

2. Register map (2) (continued)

Sub Address	R/W	Data name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
72h	R/W	P1	BLP1[3:0]				FRP1[1:0]		DLP1[1:0]	
73h	R/W	P2	BLP2[3:0]				FRP2[1:0]		DLP2[1:0]	
74h	R/W	P3	BLP3[3:0]				FRP3[1:0]		DLP3[1:0]	
75h	R/W	P4	BLP4[3:0]				FRP4[1:0]		DLP4[1:0]	
76h	R/W	P5	BLP5[3:0]				FRP5[1:0]		DLP5[1:0]	
77h	R/W	P6	BLP6[3:0]				FRP6[1:0]		DLP6[1:0]	
78h	R/W	P7	BLP7[3:0]				FRP7[1:0]		DLP7[1:0]	
79h	R/W	Q1	BLQ1[3:0]				FRQ1[1:0]		DLQ1[1:0]	
7Ah	R/W	Q2	BLQ2[3:0]				FRQ2[1:0]		DLQ2[1:0]	
7Bh	R/W	Q3	BLQ3[3:0]				FRQ3[1:0]		DLQ3[1:0]	
7Ch	R/W	Q4	BLQ4[3:0]				FRQ4[1:0]		DLQ4[1:0]	
7Dh	R/W	Q5	BLQ5[3:0]				FRQ5[1:0]		DLQ5[1:0]	
7Eh	R/W	Q6	BLQ6[3:0]				FRQ6[1:0]		DLQ6[1:0]	
7Fh	R/W	Q7	BLQ7[3:0]				FRQ7[1:0]		DLQ7[1:0]	

Established : 2009-07-23
Revised : 2013-04-01

OPERATION (continued)

3. Register map (1) Detail descriptions

Address 00h to 08h

Sub address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
00h RST	Data name	—	—	—	—	—	—	RAMRST	SRST
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : SRST Soft reset control bit
[0] : Reset release state (default)
[1] : Reset control

*After Reset operation, this register returns from “1” to “0” automatically.

D1 : RAMRST RAM reset control bit for address 09h to 7Fh
[0] : RAM reset release state (default)
[1] : RAM reset control

*After Reset operation, this register returns from “1” to “0” automatically.

Sub address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
01h POWERCNT	Data name	—	—	—	—	—	—	—	OSCEN
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : OSCEN ON/OFF bit for internal oscillator
[0] : Internal oscillator is off. (default)
[1] : Internal oscillator is on

- The variation width of internal oscillator is 0.96 MHz to 1.44 MHz.
- The variation width of internal clock is 694.4 ns to 1042 ns.

OPERATION (continued)

3. Register map (1) Detail descriptions (continued)

Address 00h to 08h(continued)

Sub address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
02h LDOCNT	Data name	—	—	—	—	—	—	—	REG18
	Default	0	0	0	0	0	0	0	1
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : REG18 ON/OFF control for LDO (at LDOCNT = Low)

[0] : LDO OFF

[1] : LDO ON (default)

- LDO turns on regardless of the state of REG18 at LDOCNT = High.
- Set LDOCNT to Low after setting REG18 to "0" to shift to OFF mode.

Sub address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
03h LSITEST	Data name	—	—	—	—	—	—	—	—
	Default	0	0	0	0	0	0	0	1
	mode	R	R	R	R	R	R	R	R

D7-0 : Register for LSI Test

- Access is prohibited

Established : 2009-07-23
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OPERATION (continued)

3. Register map (1) Detail descriptions (continued)

Address 00h to 08h(continued)

Sub address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
04h OPTION	Data name	LEDACT	DISMTX	—	—	—	—	CLKOUT	EXTCLK
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

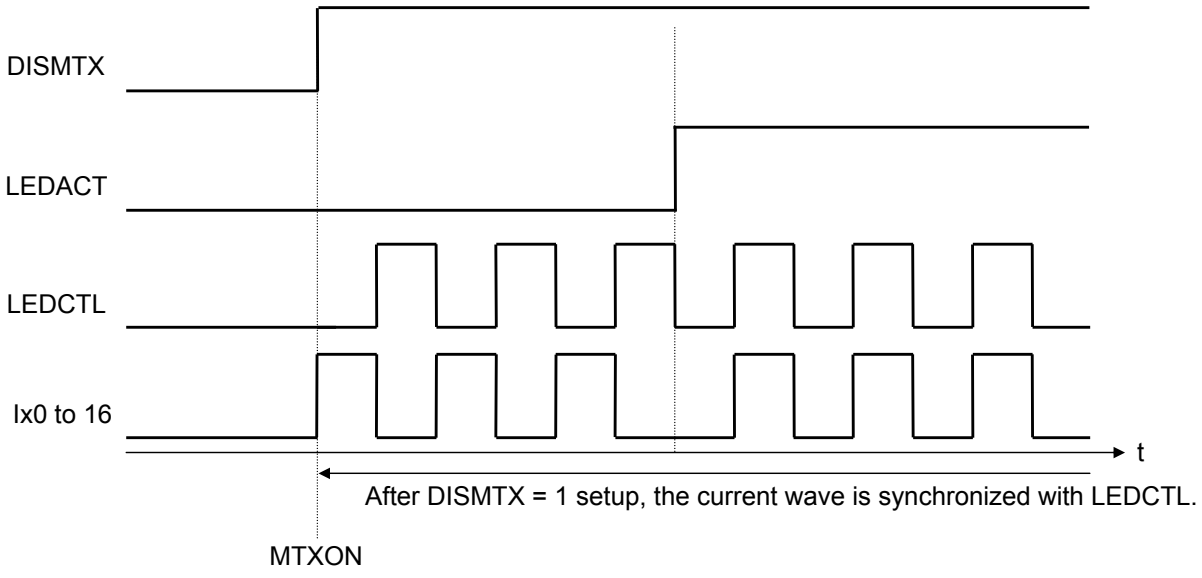
- LED is turned on/off by setting the voltage which is applied to LEDCTL pin to High/Low.
- LED is turned on/off in synchronization with input/output level by inputting the voltage signal which changes with time to this pin
- For example, when music signal is input as input signal, LED is blinked synchronizing with music signal. In this case, the input pin voltage amplitude of 1.5 V[p-p] or more is used.
- Add pull-up/pull-down resistors to the system control side or outside because the input is open-gate, and fix the logic.
- Set up whether the external pin controls the matrix of LED.
  (Default setting is setup which is not controlled.)

D7 : LEDACT LED lights-out setup by LEDCTL pin
[0] : Lighting at LEDCTL = Low (default)
[1] : Lighting at LEDCTL = High

D6 : DISMTX Lights-out ON/OFF setup of Matrix 7 × 17LED by LEDCTL pin
[0] : Lights-out control OFF by LEDCTL pin (default)
[1] : Lights-out control ON by LEDCTL pin

D1 : CLKOUT Internal clock output switch setup of this LSI
[0] : Internal clock is not output from CLKOUT pin. CLKOUT = Low (default)
[1] : Internal clock is output from CLKOUT pin.

D0 : EXTCLK Internal / External switch setup for operation synchronous clock of this LSI
[0] : Internal clock operation (default)
[1] : External clock (EXTCLK pin) operation



Established : 2009-07-23
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OPERATION (continued)

3. Register map (1) Detail descriptions (continued)

Address 00h to 08h(continued)

Sub address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
05h MTXON	Data name	—	—	—	—	IMAX[0:1]		—	MTXON
	Default	0	0	0	0	0	1	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : MTXON ON/OFF setup of matrix LED
[0] : OFF (default)
[1] : ON

- During MTXON = [1], subsequent RAM and the control contents to a register are sequentially processed and lit up.
- When EXTCLK (address 04h) is set to [0], set MTXON to [1] in 5 ms after OSCEN (address 01h) is set to [1].
- When EXTCLK (address 04h) is set to [1], set MTXON to [1] in 5 ms after the clock is input into EXTCLK pin.
- Set MTXON to [1], and then set up other addresses to display the matrix part.

D3-2 : IMAX[1:0] Maximum value selection bit for current setup
[00] : 15.75 mA
[01] : 21.00 mA (default)
[10] : 26.25 mA
[11] : 31.50 mA

- The constant current is output according to the maximum constant current of this setting. The current of each step is set to 1/15 of maximum value.

Established : 2009-07-23
Revised : 2013-04-01

OPERATION (continued)

3. Register map (1) Detail descriptions (continued)

Address 00h to 08h(continued)

Sub address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
06h XCONST1	Data name	X16	X15	X14	X13	X12	X11	X10	X9
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7 : X16 Constant current mode setup selection bit of X16
0 : Matrix operation (default)
1 : Constant current operation

D6 : X15 Constant current mode setup selection bit of X15
0 : Matrix operation (default)
1 : Constant current operation

D5 : X14 Constant current mode setup selection bit of X14
0 : Matrix operation (default)
1 : Constant current operation

D4 : X13 Constant current mode setup selection bit of X13
0 : Matrix operation (default)
1 : Constant current operation

D3 : X12 Constant current mode setup selection bit of X12
0 : Matrix operation (default)
1 : Constant current operation

D2 : X11 Constant current mode setup selection bit of X11
0 : Matrix operation (default)
1 : Constant current operation

D1 : X10 Constant current mode setup selection bit of X10
0 : Matrix operation (default)
1 : Constant current operation

D0 : X9 Constant current mode setup selection bit of X9
0 : Matrix operation (default)
1 : Constant current operation

- When these bits are set to "1", Xx pin becomes the constant current mode. And the brightness for each Xx pin is controlled by the setting of LED which is connected between Xx pin and Y0 pin.

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OPERATION (continued)

3. Register map (1) Detail descriptions (continued)

Address 00h to 08h(continued)

Sub address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
07h XCONST2	Data name	X8	X7	X6	X5	X4	X3	X2	X1
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7 : X8 Constant current mode setup selection bit of X8
0 : Matrix operation (default)
1 : Constant current operation
D6 : X7 Constant current mode setup selection bit of X7
0 : Matrix operation (default)
1 : Constant current operation
D5 : X6 Constant current mode setup selection bit of X6
0 : Matrix operation (default)
1 : Constant current operation
D4 : X5 Constant current mode setup selection bit of X5
0 : Matrix operation (default)
1 : Constant current operation
D3 : X4 Constant current mode setup selection bit of X4
0 : Matrix operation (default)
1 : Constant current operation
D2 : X3 Constant current mode setup selection bit of X3
0 : Matrix operation (default)
1 : Constant current operation
D1 : X2 Constant current mode setup selection bit of X2
0 : Matrix operation (default)
1 : Constant current operation
D0 : X1 Constant current mode setup selection bit of X1
0 : Matrix operation (default)
1 : Constant current operation

- When these bits are set to "1", Xx pin becomes the constant current mode. And the brightness for each Xx pin is controlled by the setting of LED which is connected between Xx pin and Y0 pin.

Sub address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
08h XCONST3	Data name	—	—	—	—	—	—	—	X0
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : X0 Constant current mode setup selection bit of X0
0 : Matrix operation (default)
1 : Constant current operation

- When these bits are set to "1", Xx pin becomes the constant current mode. And the brightness for each Xx pin is controlled by the setting of LED which is connected between Xx pin and Y0 pin.

OPERATION (continued)

3. Register map (2) Detail descriptions

Address 09h to 7Fh

Sub address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
09h A1	Data name	BLA1[3:0]				FRA1[1:0]		DLA1[1:0]	
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-4 : BLA1[3:0] Luminance setup of LED No. A1
In case of Address 13h IMAX = [01](default)

[0000] : 0.00 mA (default)	[1000] : 11.20 mA
[0001] : 1.40 mA	[1001] : 12.60 mA
[0010] : 2.80 mA	[1010] : 14.00 mA
[0011] : 4.20 mA	[1011] : 15.40 mA
[0100] : 5.60 mA	[1100] : 16.80 mA
[0101] : 7.00 mA	[1101] : 18.20 mA
[0110] : 8.40 mA	[1110] : 19.60 mA
[0111] : 9.80 mA	[1111] : 21.00 mA

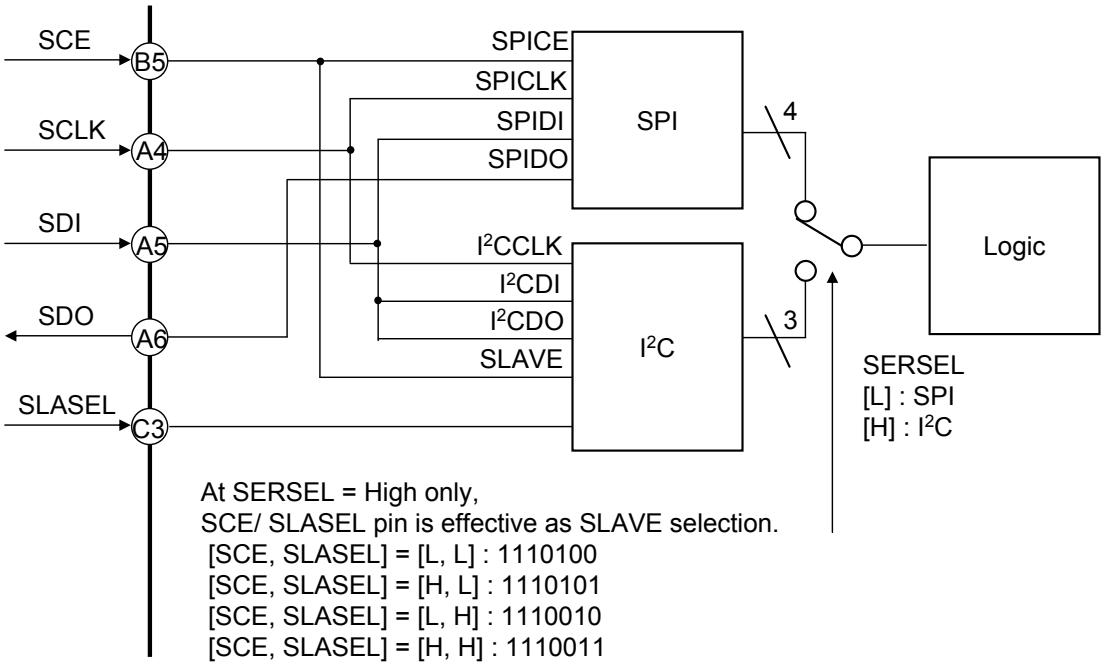
D3-2 : FRA1[1:0] Firefly operation and cycle setup of LED No. A1
[00] : Always lighting mode (default)
[01] : Firefly lighting cycle 1 s
[10] : Firefly lighting cycle 2 s
[11] : Firefly lighting cycle 3 s

D1-0 : DLA1[1:0] Firefly operation delay setup of LED No. A1
[00] : No delay (default)
[01] : Delay 25%
[10] : Delay 50%
[11] : Delay 75%

- The luminance setup value of [D7-4] can be changed by IMAX[1:0] of Address 13h.
  (Exp.) at IMAX[1:0] = [00]
  [0000] : 0.00 mA (default)
  [0001] : 1.05 mA
  [0010] : 2.10 mA
  |
  [1111] : 15.75 mA * 1.05 mA/STEP
- The above operation is performed with the same control for addresses to 7Fh corresponding to each LED number.
- The waiting time for 2 or more internal clocks (2 μs or more) is required after the data from address 09h to 7Fh is written in. Please input other serial commands after that.
- Address 09h to 7Fh are set as above.

OPERATION (continued)

4. Interface configuration



At SERSEL = High only,
SCE/ SLASEL pin is effective as SLAVE selection.
[SCE, SLASEL] = [L, L] : 1110100
[SCE, SLASEL] = [H, L] : 1110101
[SCE, SLASEL] = [L, H] : 1110010
[SCE, SLASEL] = [H, H] : 1110011

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OPERATION (continued)

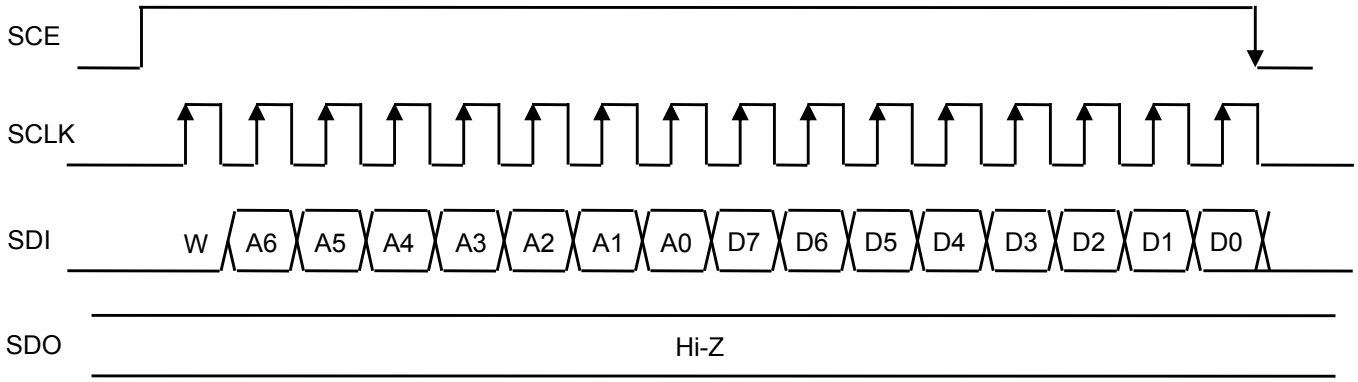
5. SPI interface

The interface with microcomputer consists of 16-bit serial register (8-bit of command, 8-bit of address), address decoder, and transmission register (8-bit).
Serial interface consists of 4 pins of serial clock pin (SCLK), serial data input pin (SDI), serial data output pin (SDO), and chip enable input pin (SCE).

(1) Reception operation

In the case of MSB first, Write is recognized by SDI = Low at the 1st clock of SCLK.
Data is taken into internal shift register at the rising edge of SCLK.
(The frequency of SCLK can be used up to 13 MHz.)
In High period of SCE, reception of data becomes enable. (active High)
In the case of MSB first, data is transmitted in order of control register address (8-bit) and control command (8-bit).

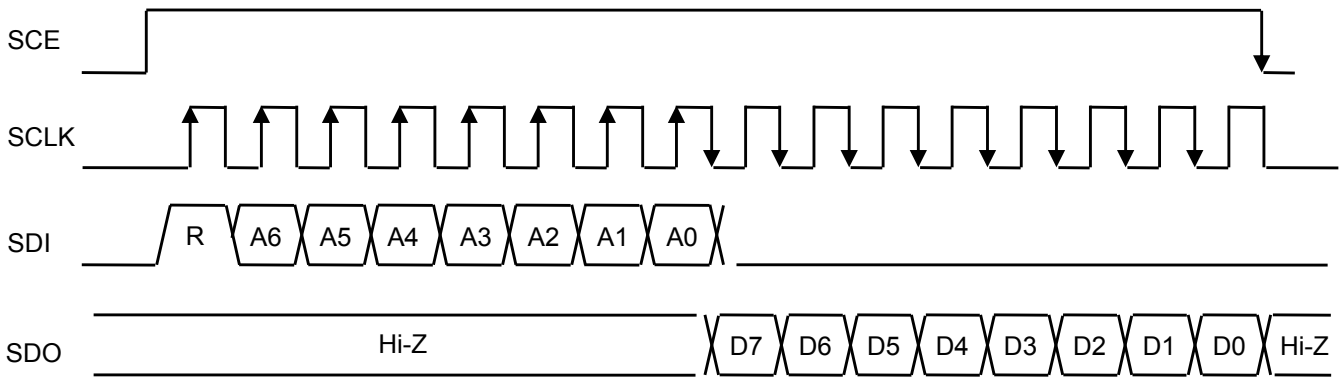
Reception timing



(2) Transmission operation

In the case of MSB first, Read is recognized by SDI = High at the 1st clock of SCLK.
Data is taken into internal shift register at the rising edge of SCLK.
(The frequency of SCLK can be used up to 13 MHz.)
In High period of SCE, reception of data becomes enable. (active High)
In the case of MSB first, data is transmitted in order of control register address (8-bit) and control command (8-bit).
It is not possible to read RAM.

Transmission timing



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OPERATION (continued)

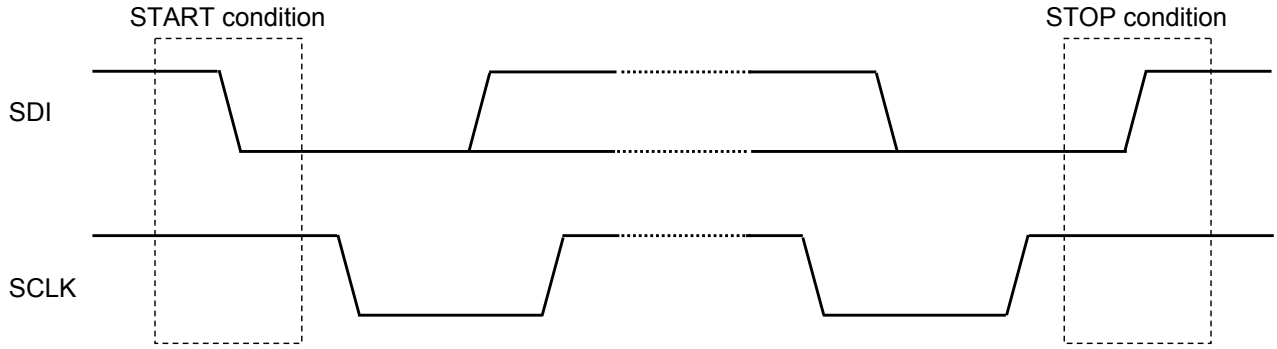
6. I²C interface

6.1 Basic Rules

- This LSI, I²C-bus, is designed to correspond to the Standard-mode (100 kbps) and Fast-mode(400 kbps) devices in the version 2.1 of NXP's specification. However, it does not correspond to the H_S-mode (to 3.4 Mbps).
- This LSI will be operated as a slave device in the I²C-bus system.
- The program operation check of this LSI has not been conducted on the multi-master bus system and the mix-speed bus system, yet. The connected confirmation of this LSI to the CBUS receiver also has not been checked. Please confirm with our company if it will be used in these mode systems.
- Purchase of Panasonic I²C Components conveys a license under the NXP I²C patent right to use these components in an I²C systems, provided that the system conforms to the I²C standard specifications as defined by NXP.

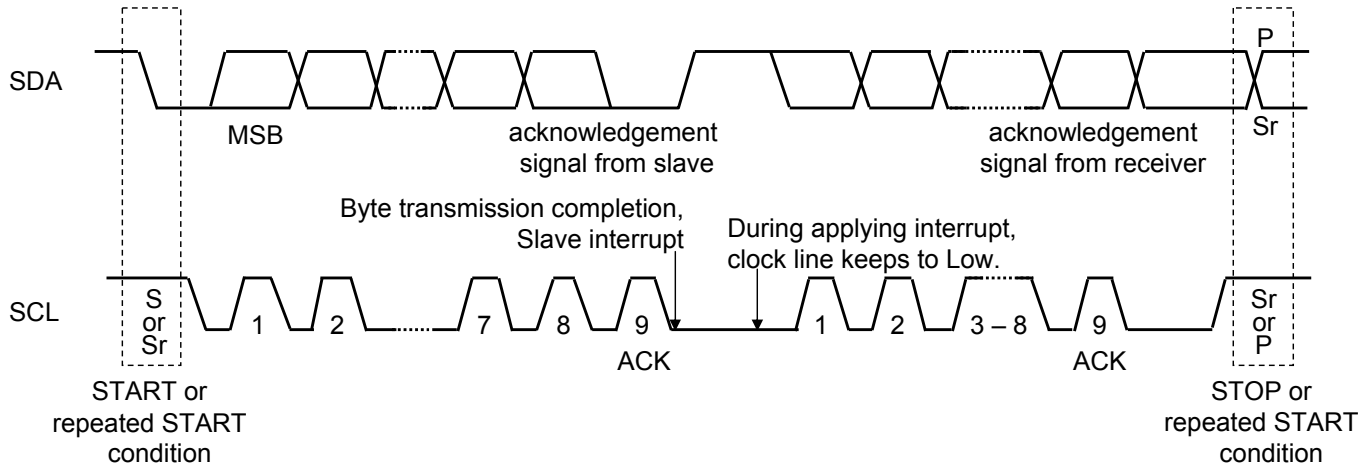
6.2 START and STOP conditions

A High to Low transition on the SDA line while SCL is High is one such unique case. This situation indicates START condition. A Low to High transition on the SDA line while SCL is High defines STOP condition.
START and STOP conditions are always generated by the master. After START condition occur, the bus will be busy.
The bus is considered to be free again a certain time after the STOP condition.



6.3 Transferring Data

Every byte put on the SDI line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.



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OPERATION (continued)

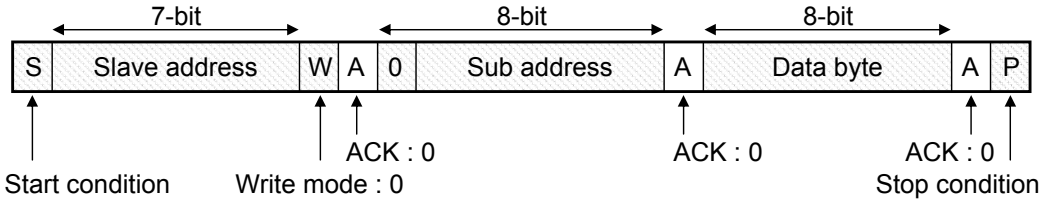
6. I²C interface (continued)

6.4 Data format

When I²C format is used in this LSI, use it while SERSEL pin is fixed to High-level.
It is possible to select Slave address by switching SCE pin and SLASEL pin to Low-level and High-level.

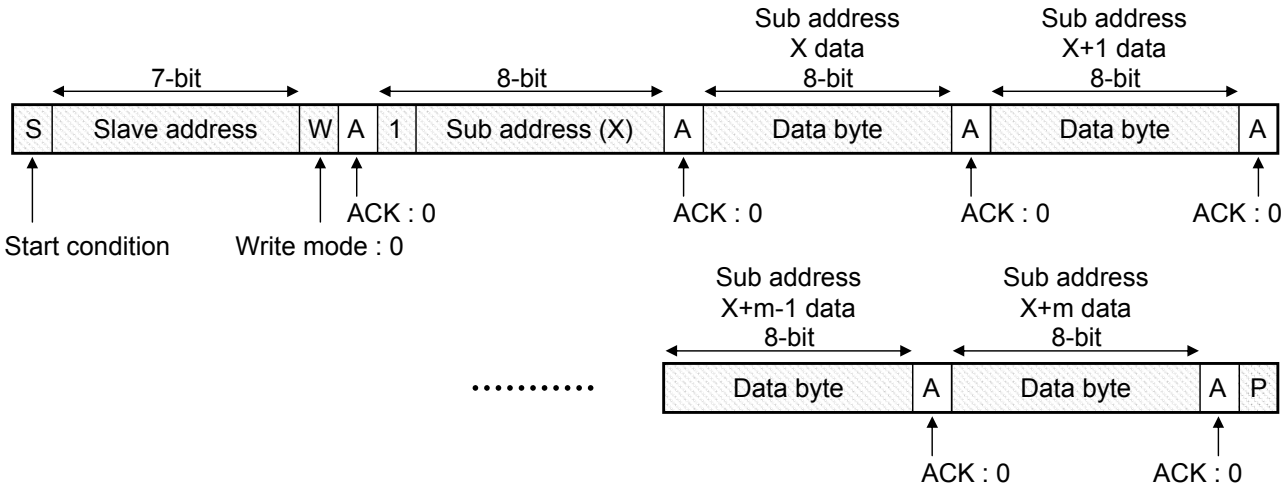
Write mode

When MSB of Sub address 8 bit is "0", Sub address is not incremented automatically.
The next data byte is written in the same Sub address by transmitting data byte continuously.



Write mode (Auto increment mode)

When MSB of Sub address 8 bit is "1", the mode becomes Auto increment mode.
Data byte can be written in Sub address by transmitting data byte continuously.
Sub address is incremented automatically.



: Data transmission from Master

: Data transmission from Slave

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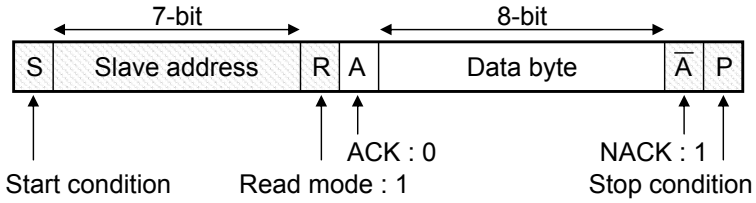
OPERATION (continued)

6. I²C interface (continued)

6.4 Data format (continued)

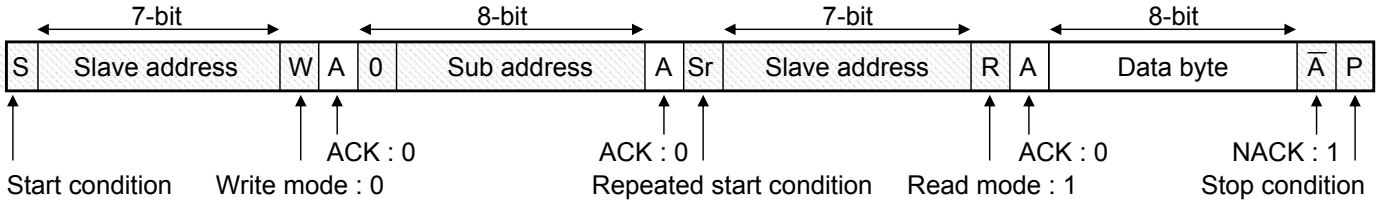
Read mode (in case Sub address is not specified)

When Sub address 8 bit is not specified and data is read, this LSI allows to read the value of adjacent Sub address specified in the last Write mode.
The next data byte reads the same Sub address by transmitting data byte continuously.



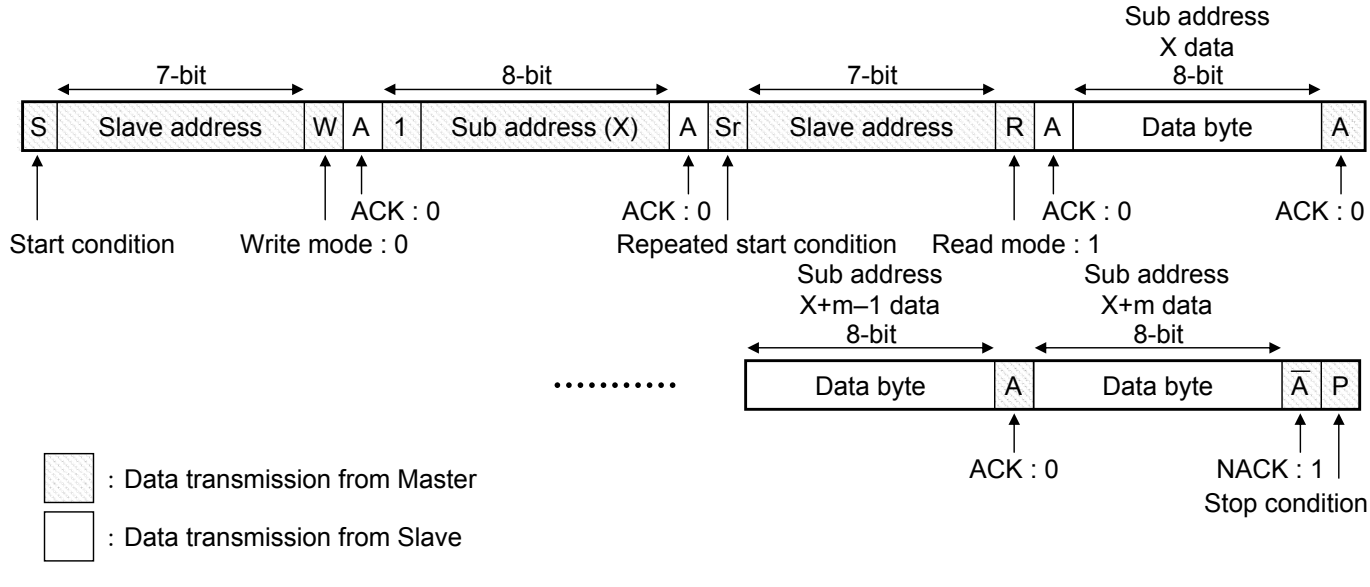
Read mode (in case Sub address is specified)

When MSB of Sub address 8 bit is "0", Sub address is not incremented automatically.
The next data byte reads the same Sub address by transmitting data byte continuously.



Read mode (Auto increment mode)

When MSB of Sub address 8 bit is "1", the mode becomes Auto increment mode.
It is possible to read data byte in continuous Sub address by transmitting data byte continuously.
Sub address is incremented automatically.



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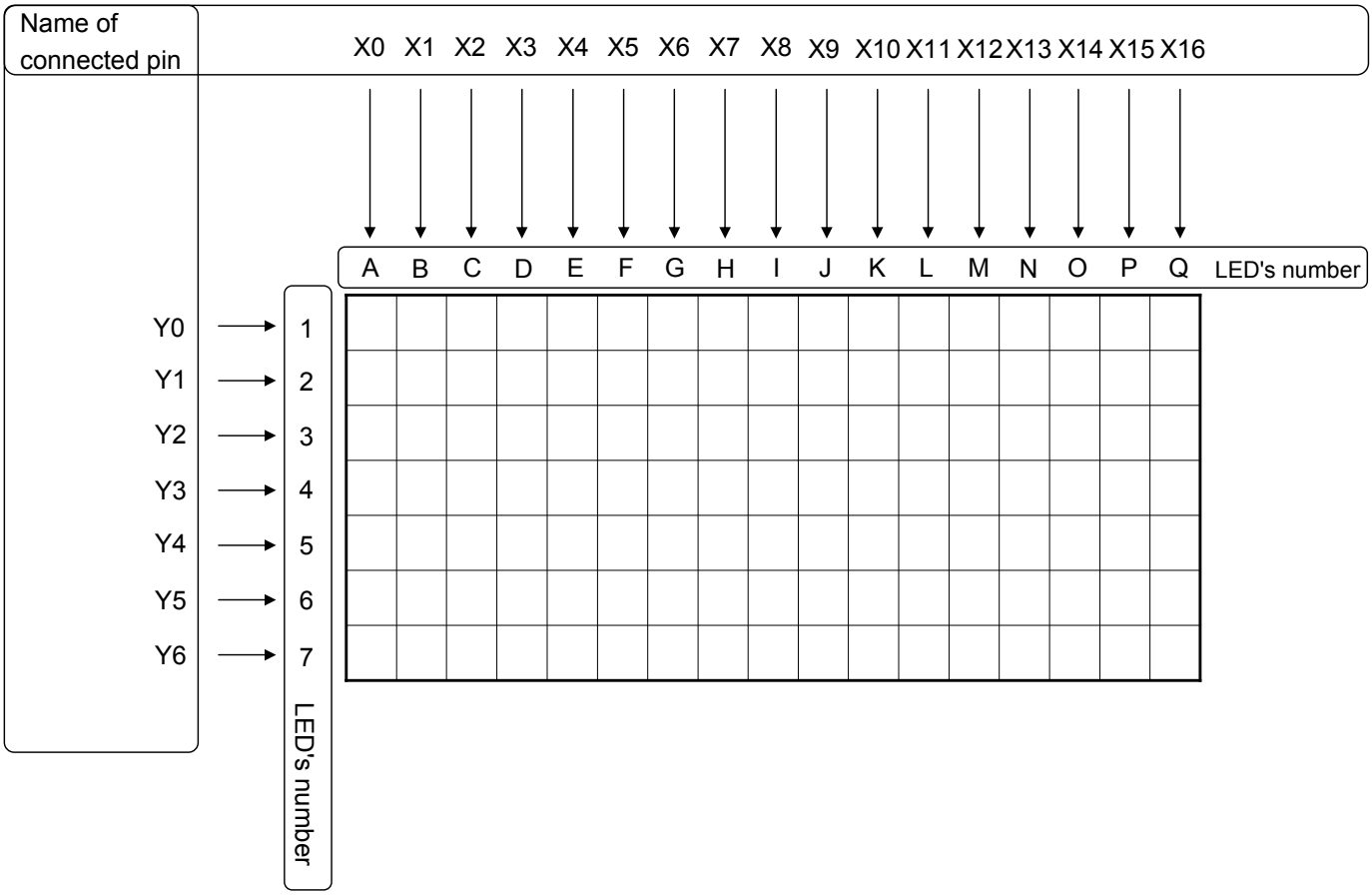
OPERATION (continued)

7. Functions and sequences of each block

7.1 LED matrix driver

LED matrix driver block (LED 0 to 16, Y0 to 6) can control each driver independently.

LED matrix driver block can perform current value setting and firefly setting to 119 LEDs respectively.
LED matrix driver can display characters and patterns by driving 7 × 17 LED independently.
In this product standards, the number of LED driven by each pin is shown by the following figure.
Internal logic circuit is operated by the external clock which is input into the internal clock and EXTCLK pin (Pad No.42).
Maximum frequency of EXTCLK pin is 1.44 MHz.



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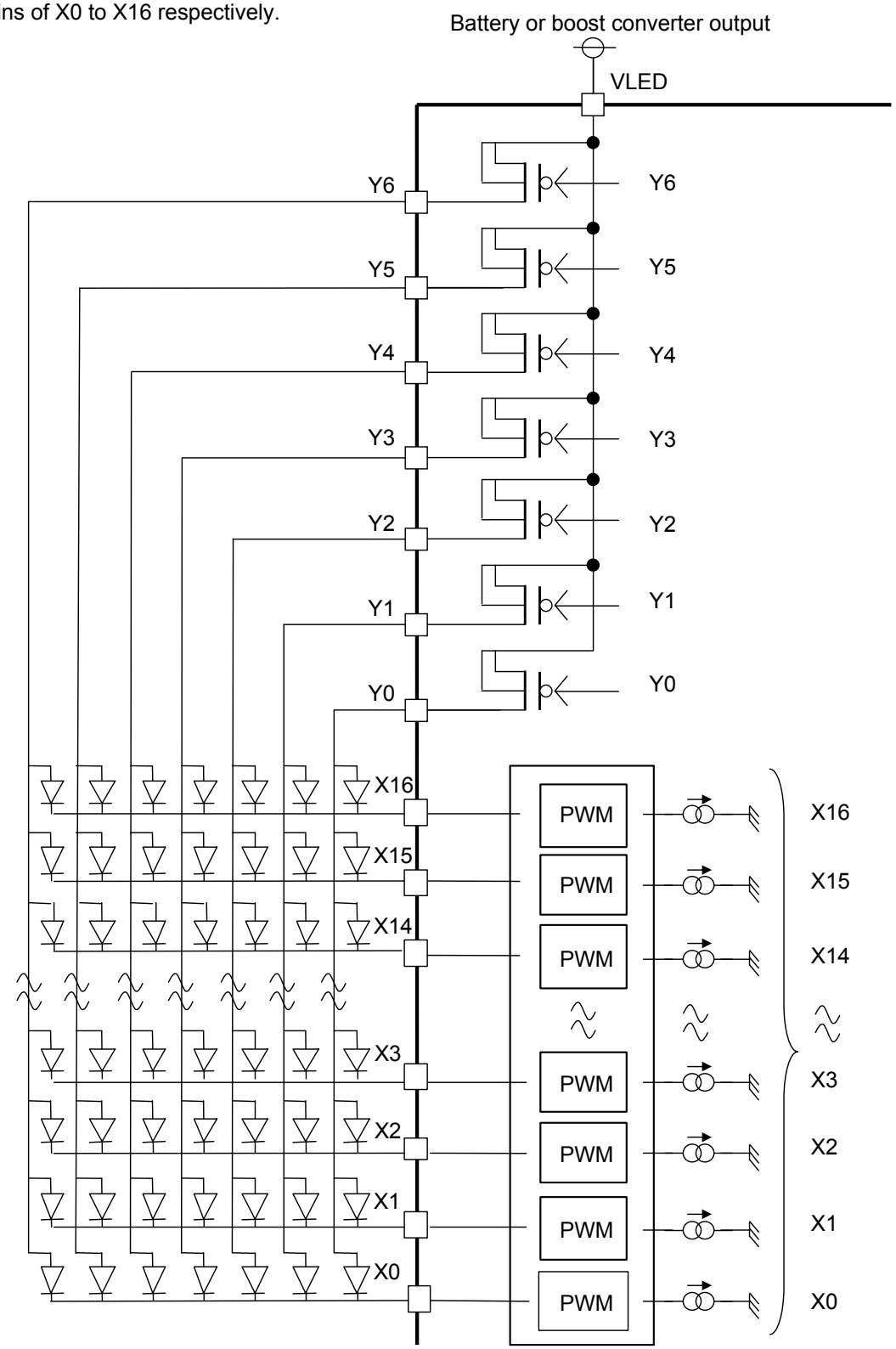
OPERATION (continued)

7. Functions and sequences of each block (continued)

7.1 LED matrix driver (continued)

- Actual driver composition is shown as the following figure.
- The anodes of 17 LEDs are connected to 7 pins of Y0 to Y6 respectively. The cathodes of 17 LEDs are connected to 17 pins of X0 to X16 respectively.



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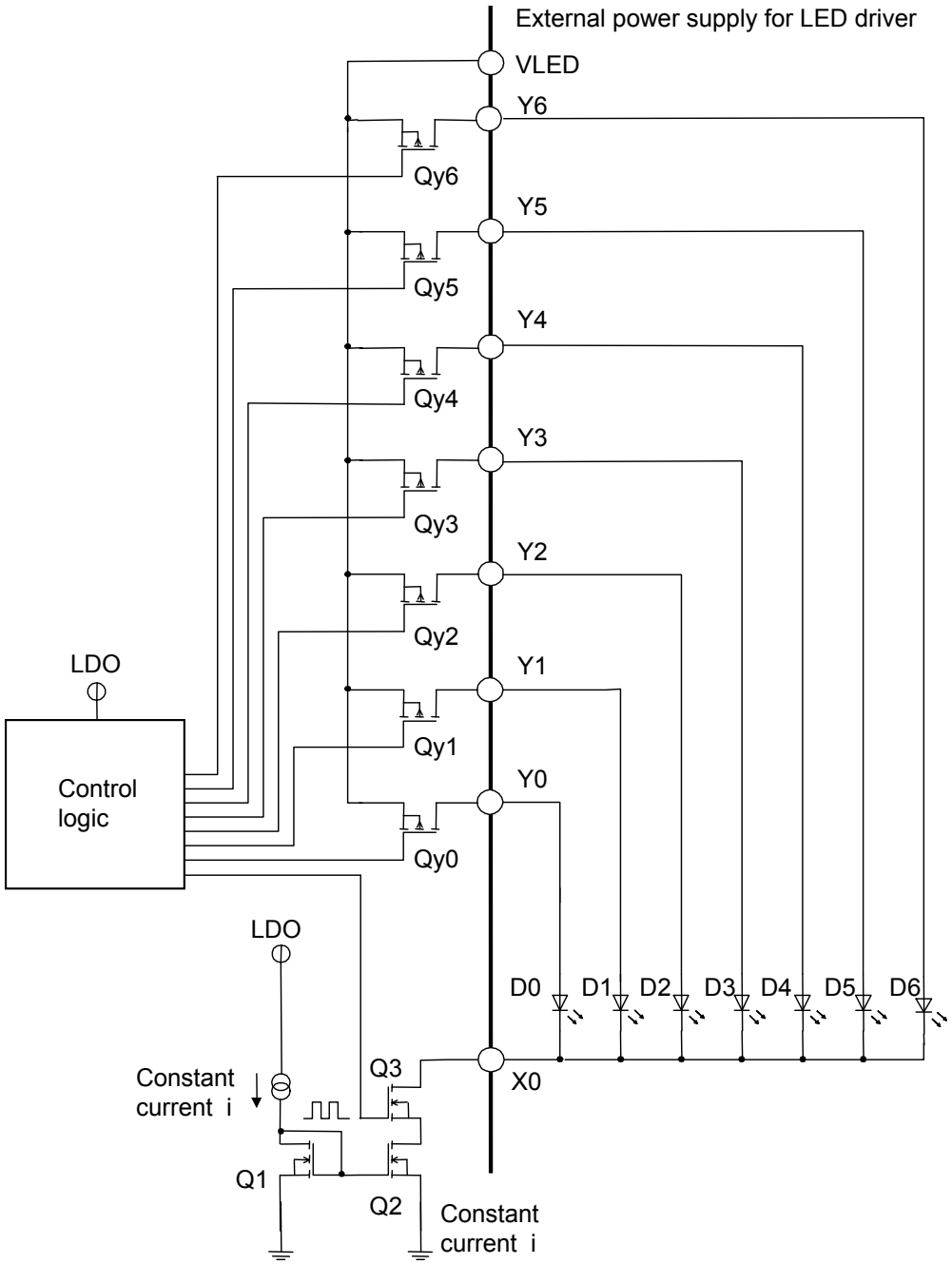
OPERATION (continued)

7. Functions and sequences of each block (continued)

7.1 LED matrix driver (continued)

- The figure below shows a specific circuit configuration about one column of Y0 to Y6 and X0. (The actual LSI has 17 internal circuit of the same configurations as the following figure. See the previous pages.)
- VLED is the external power supply for LED driver in this circuit.
- In the side of Y0 to Y6, MOS switches (Qy0 to Qy6) are turned ON/OFF by controlling the gate voltage in internal control logic circuit. and P-ch.
- In the side of X0, constant current-supply circuit is configured by Q1 and Q2. Q3 operates as a switch, and is controlled ON/OFF of the gate voltage by control logic. Moreover, it is possible to change luminance by varying the current value with serial control.
- For example, when Qy0 is ON (gate voltage : Low) and Q3 is ON (gate voltage : High), current flows into D0, and then LED lights up.
- Internal LDO (1.85 V) is used for power supply of internal logic circuit.



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OPERATION (continued)

7. Functions and sequences of each block (continued)

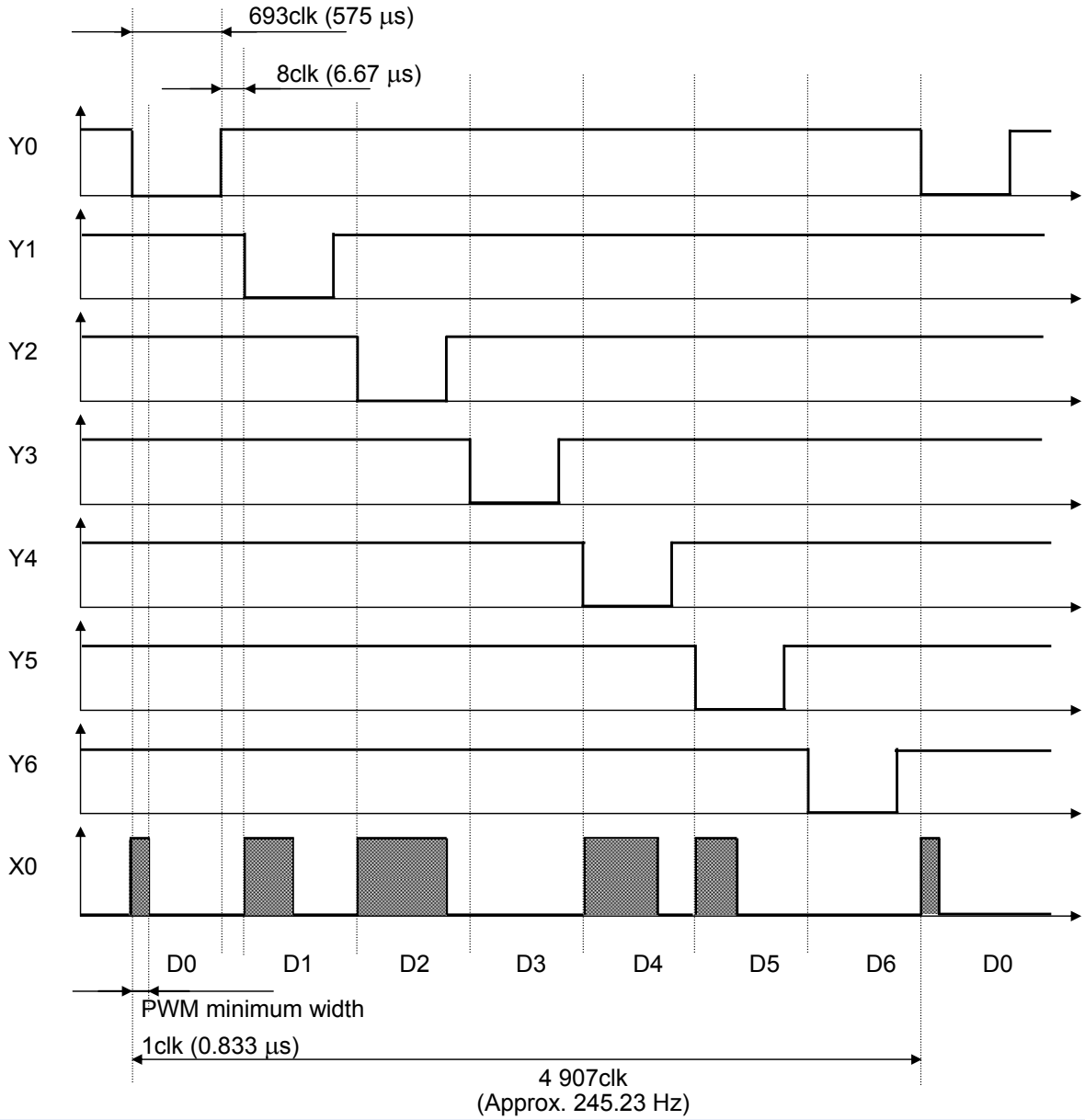
7.1 LED matrix driver (continued)

Y0 to Y6 operating description

The timing chart in operating is shown as the following figure.
Timing control is performed with the frequency of external clock which is input to EXTCLK pin (Pad No.42).
It operates with the internal clock of 1.2 MHz in default condition.
It is possible to switch as follows by setting register 04h : D0.

0 : Internal clock
1 : EXTCLK pin input

In the case of different input frequency, calculate the time based on the number of clock written together.
In the side of Y, scan switching of Y0 to Y6 is performed in order. the on-period of each pin is constant 693clk (575 μs), and includes the interval of 8clk (6.67 μs).
In the case of the following figure, black four corners are on-period. D3 and D6 turn off there.
7 × 17 matrix display is performed by controlling the lines of X1 to X16.
The following waveform is shown internal signal.
The condition in actual waveform of Yx pin is Hi-Z at Yx = Xx = Low.



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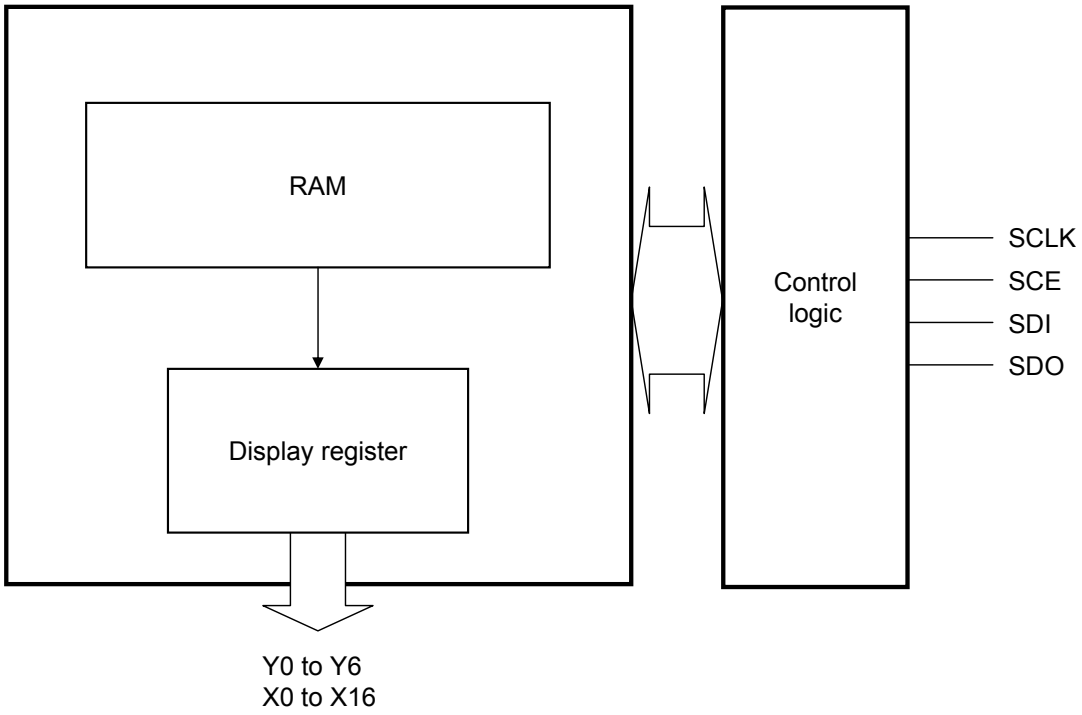
OPERATION (continued)

7. Functions and sequences of each block (continued)

7.2 Display method of RAM

This LSI has RAM 119 byte (7 × 17 matrix 1-side) for display.
It has RAM write data display for dot matrix display.
In this case, RAM data is directly transmitted to display register, and the dot matrix is displayed.
Block diagram is shown as follows.



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OPERATION (continued)

7. Functions and sequences of each block (continued)

7.2 Display method of RAM (continued)

The three parameters for display change are as follows.

1) Luminance

Current value can be setup with 16 steps from 0.00 mA to 21.00 mA.

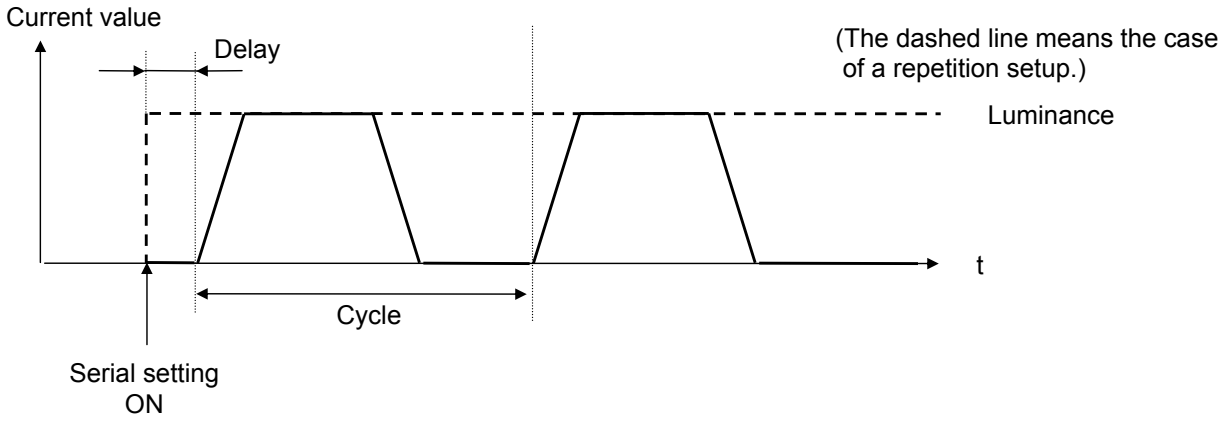
2) Cycle

Automatic luminance change like firefly can be set up by the register. It has 4 modes, “Keep lighting”, “1s” cycle, “2 s” cycle and “3 s” cycle.

3) Delay

It is possible to change the time (no delay or 25%, 50%, 75% of a cycle) from the timing of serial setup ON to the timing which current starts to flow into LED driver.

Illustration of the three parameters for display change



7.3 PWM lighting setup

(1) Content display of RAM

When displaying the contents of RAM onto the 7x17 matrix, it is necessary to perform the display setup for each LED.

In the case of RAM display, it is possible to set luminance, cycle, and delay.

Exp.) LED of A1 is made to light up

1-1) When using internal CLK

01h Write 00000001 : When 01h : D0 is set to 1, internal oscillator is ON.

1-2) When using external CLK(1.44 MHz_{max})

04h Write 00000001 : When 04h : D0 is set to 1, CLK is input externally after setting as EXTCLK operation.

Note) Be sure to set 1-1) or 1-2) first.

2) 09h Write 01010000 A1 display setting : 7.00 mA, Keep lighting, no delay

3) 05h Write 00000001 Matrix display ON setup

Note) Be sure to set 3) first.

It is possible to perform the continuous display of the contents of RAM by the above command instruction.

When lighting up all LED of 7 × 17, it is necessary to perform instruction of 2) to all LED (09h to 7Fh) of A1 to Q7.

The setup of luminance, cycle, and delay by the setup of 09h to 7Fh is shown in the next page.

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OPERATION (continued)

7. Functions and sequences of each block (continued)

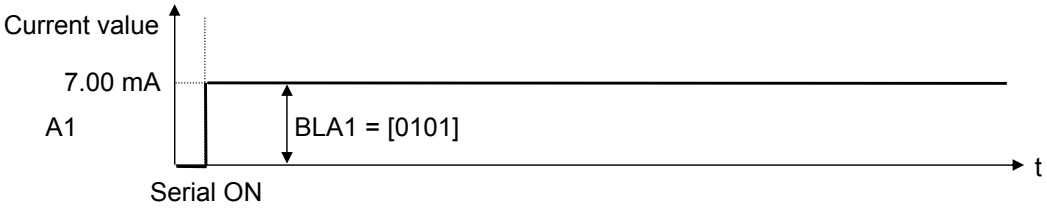
7.3 PWM lighting setup (continued)

(1) Content display of RAM (continued)

Setup for lighting Ex.

1) Example of initial setting "Keep lighting"

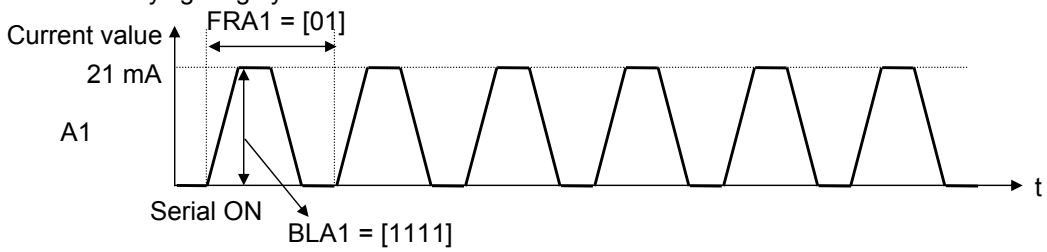
BLA1[3:0]				FRA1[1:0]		DLA1[1:0]	
0	1	0	1	0	0	0	0



2) Firefly lighting setting 1 s

BLA1[3:0]				FRA1[1:0]		DLA1[1:0]	
1	1	1	1	0	1	0	0

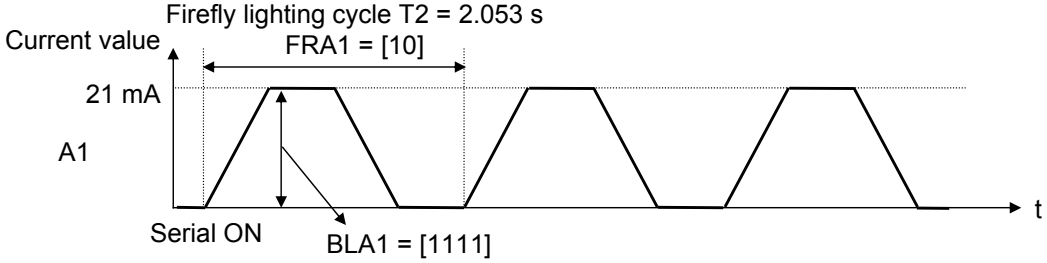
Firefly lighting cycle T = 1.026 s



Cycle change 1 s → 2 s

BLA1[3:0]				FRA1[1:0]		DLA1[1:0]	
1	1	1	1	1	0	0	0

Firefly lighting cycle T2 = 2.053 s

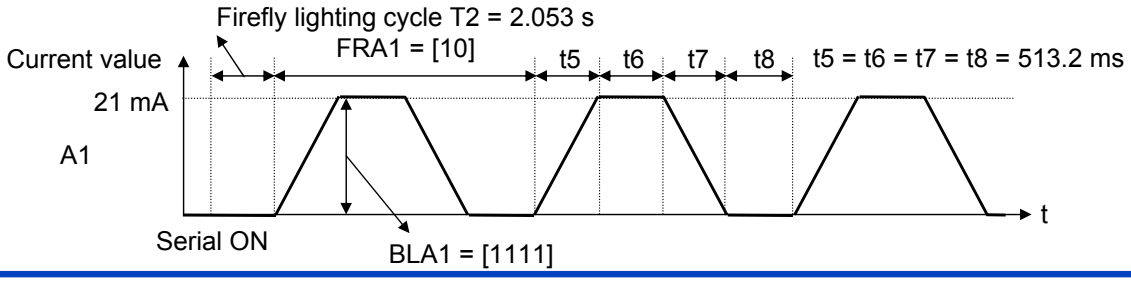


Delay change No delay → 25%

BLA1[3:0]				FRA1[1:0]		DLA1[1:0]	
1	1	1	1	1	0	0	1

DLA1 = [01]

Firefly lighting cycle T2 = 2.053 s



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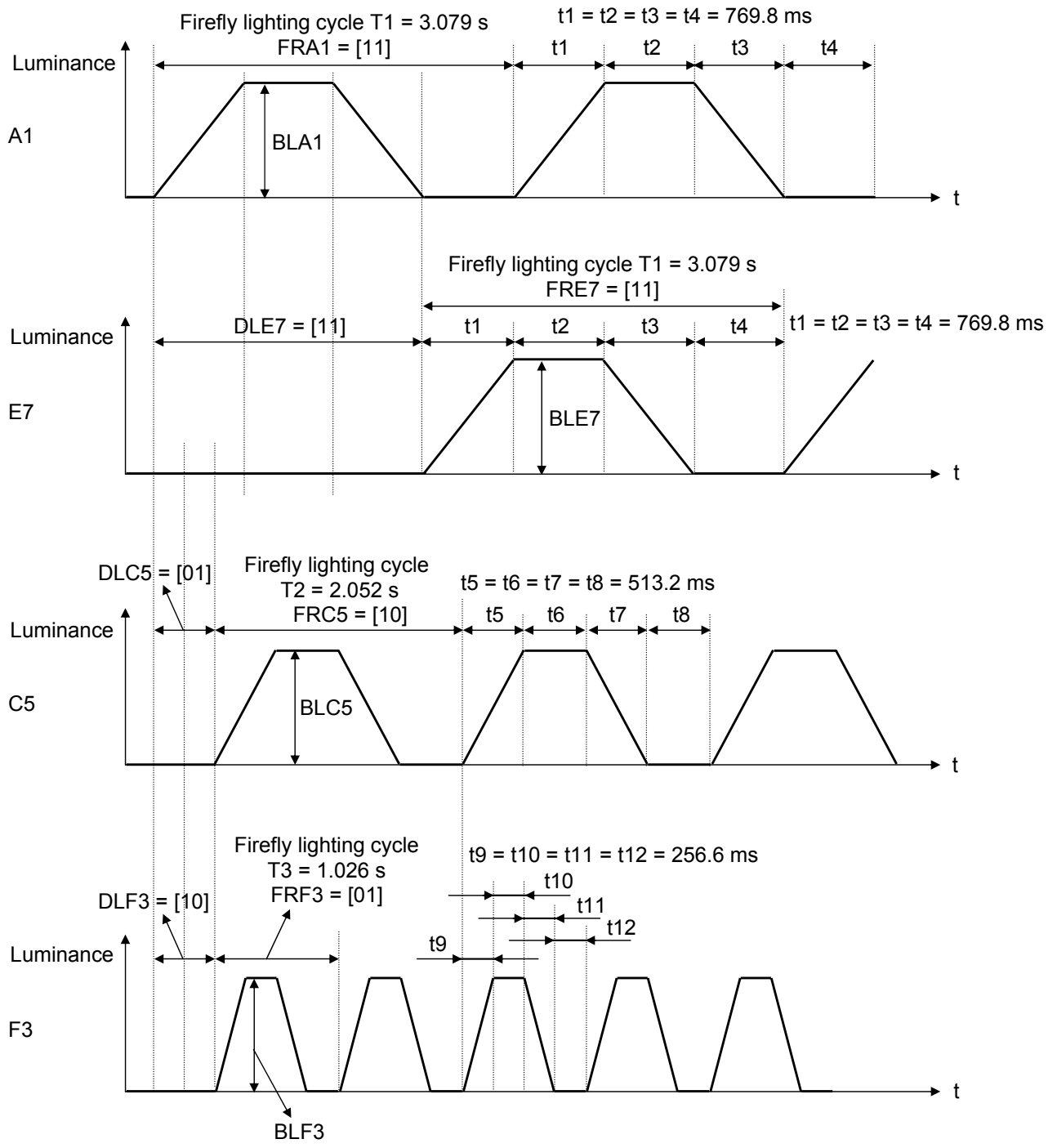
OPERATION (continued)

7. Functions and sequences of each block (continued)

7.3 PWM lighting setup (continued)

(1) Content display of RAM (continued)

Firefly lighting display



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OPERATION (continued)

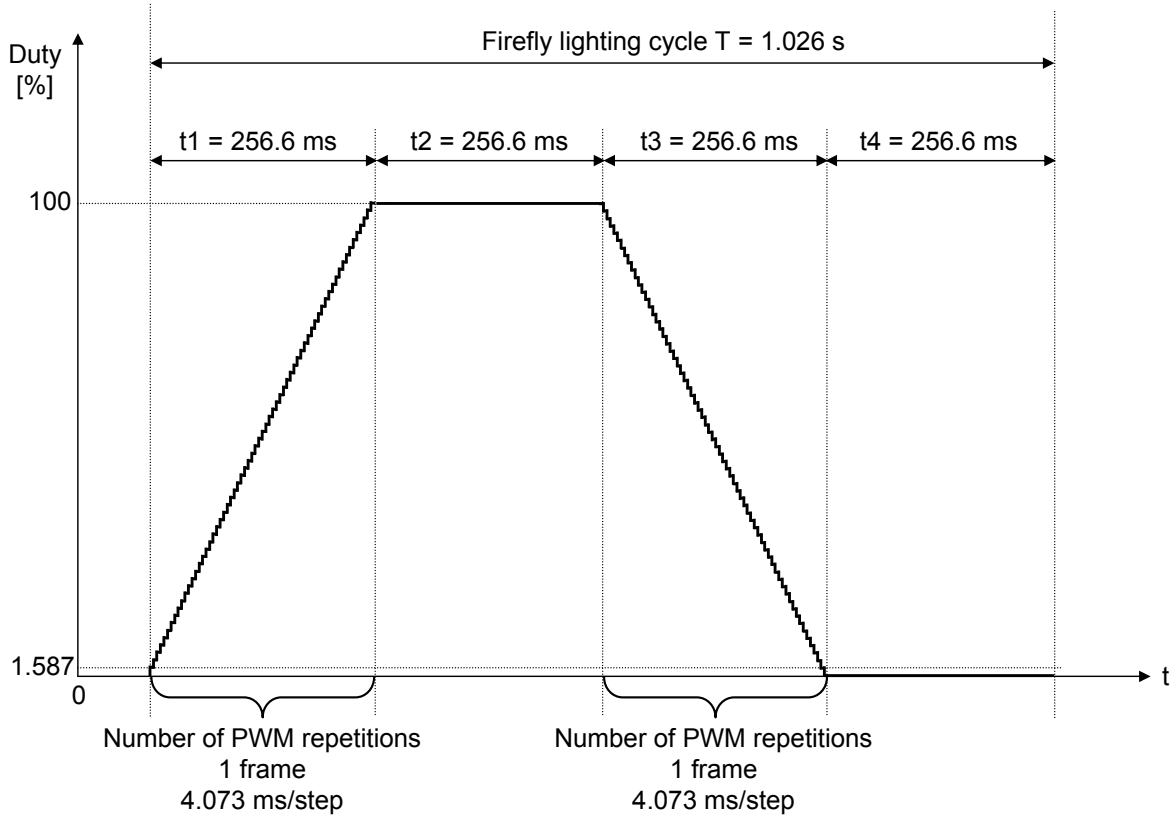
7. Functions and sequences of each block (continued)

7.3 PWM lighting setup (continued)

(1) Content display of RAM (continued)

Firefly lighting display (continued)

The following time is the time that the frequency of internal clock is the typical value (1.2 MHz).
And it is an example when setting a lighting cycle to 1 s. (When setting to 2 s or 3 s, each of the following time becomes twice or 3 times.)



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OPERATION (continued)

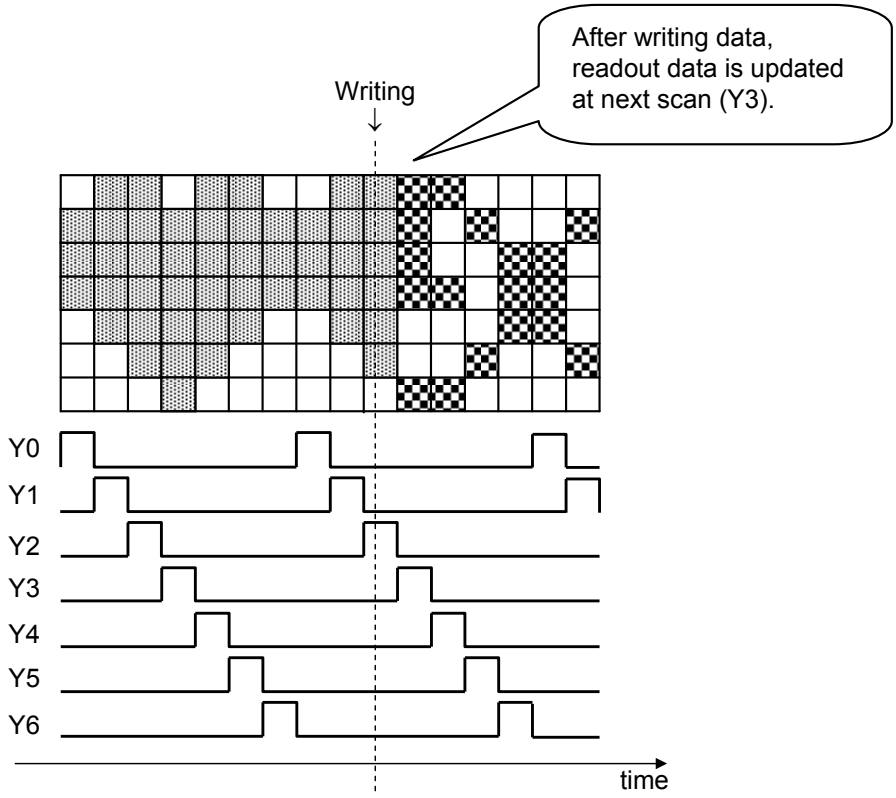
7. Functions and sequences of each block (continued)

7.4 Operation at Matrix block RAM data change (1)

Matrix LED display / Luminance change

1. Display / Luminance change writing
↓
2. Scan maintains the present state (No Reset)
↓
3. Data is updated from next scan

Ex.) Display change (Heart → Clock)



Change writing of display and luminance during scan operation

→ Scan operation is not reset, and display is reflected from the next scan data.

Established : 2009-07-23
Revised : 2013-04-01

OPERATION (continued)

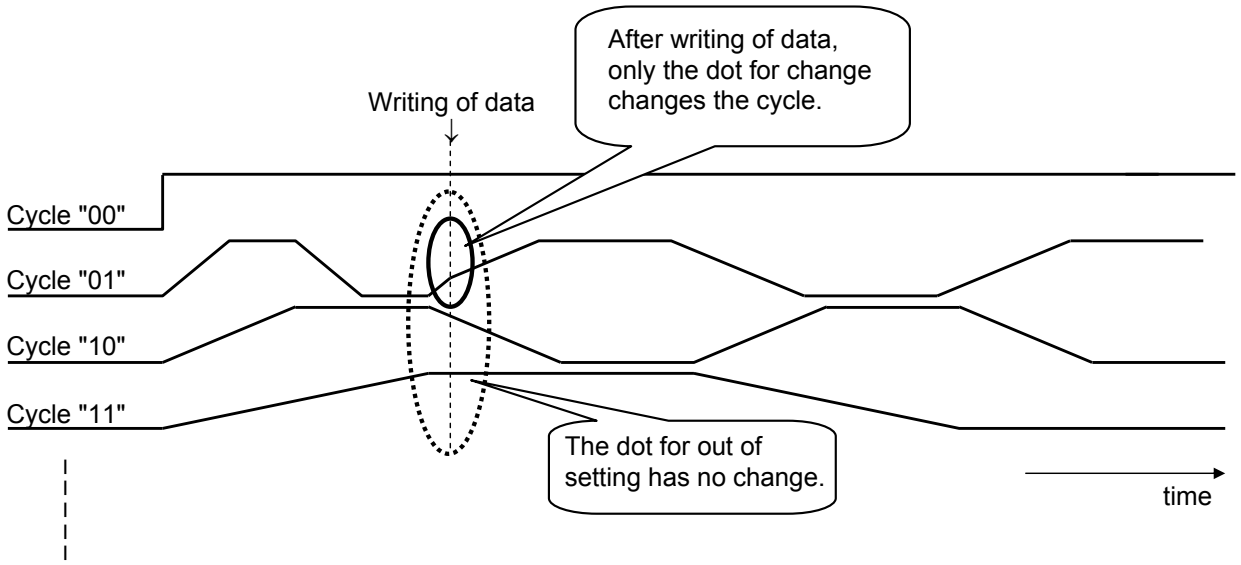
7. Functions and sequences of each block (continued)

7.4 Operation at Matrix block RAM data change (2)

Matrix LED firefly cycle change

1. Cycle change writing
↓
2. Only cycle change dot changes cycle (No Reset)

Ex.) Cycle change ("01" → "10")



Change writing of cycle

→ Only the dot for change of cycle is not reset, cycle change is reflected.

Established : 2009-07-23
Revised : 2013-04-01

OPERATION (continued)

7. Functions and sequences of each block (continued)

7.4 Operation at Matrix block RAM data change (3)

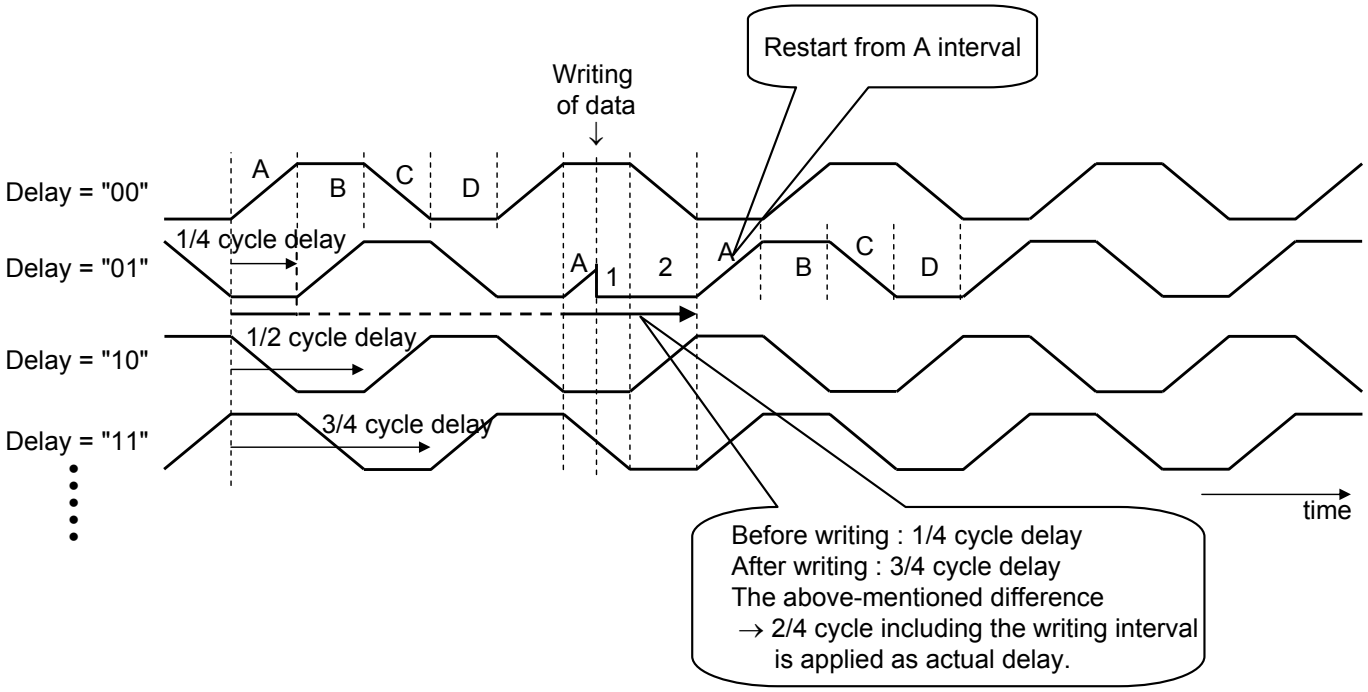
Matrix LED firefly delay change

(1) Delay change at A interval

1. Delay change writing
↓
2. Only the dot for change is reset
↓
3. The difference of a delay setup before and after writing is applied as actual delay.
↓
4. The dot for change restarts from A interval.

Ex.) Delay change ("01" → "11")

(1) Delay change at A interval (at the increase of duty)



Established : 2009-07-23
Revised : 2013-04-01

OPERATION (continued)

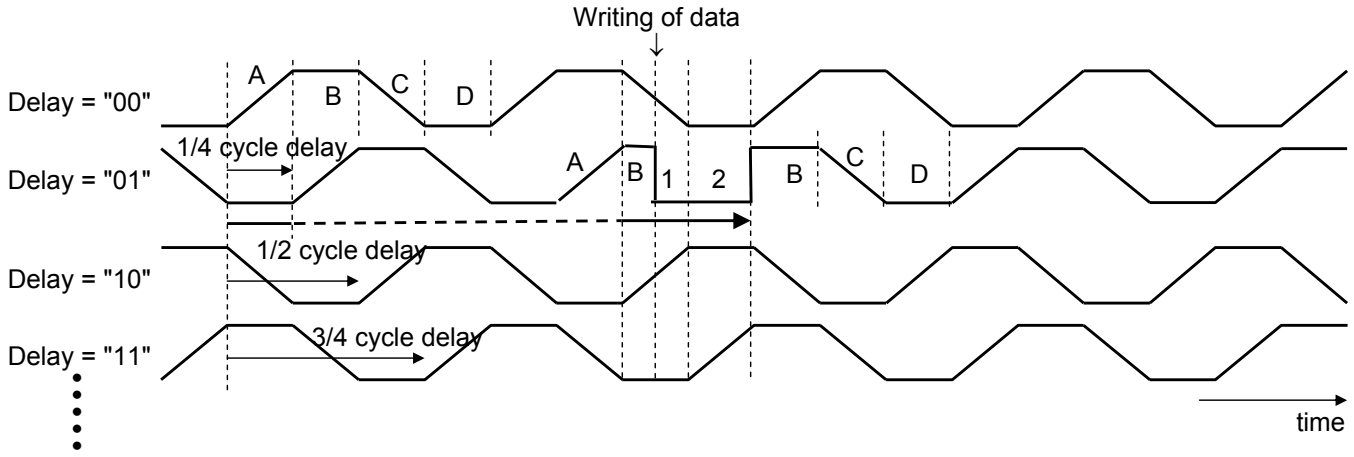
7. Functions and sequences of each block (continued)

7.4 Operation at Matrix block RAM data change (4)

Matrix LED firefly delay change (continued)

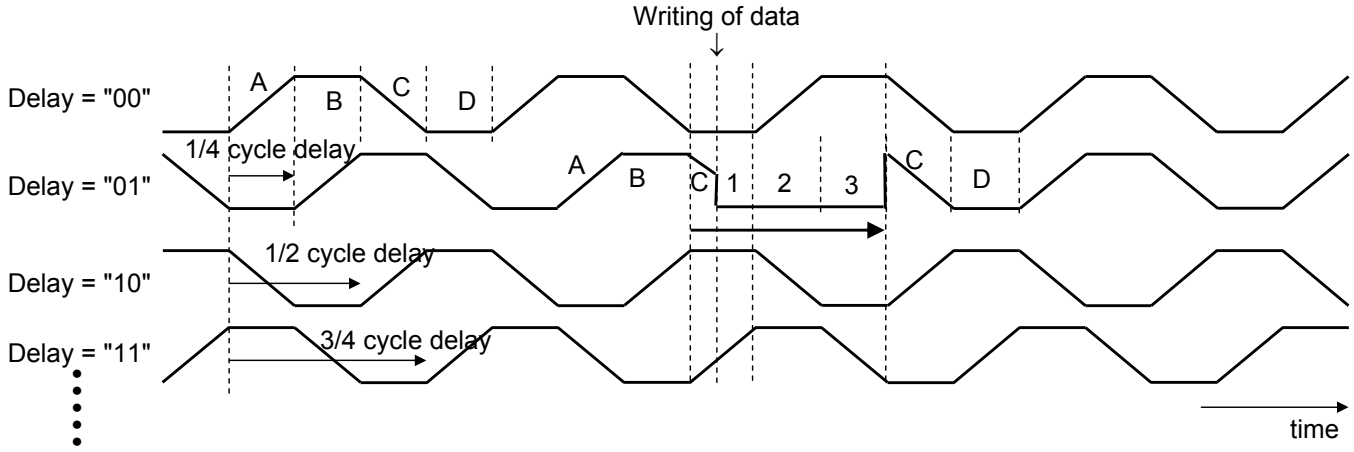
Ex.) Delay change ("01" → "11")

(2) Delay change at B interval (at Duty 100%)



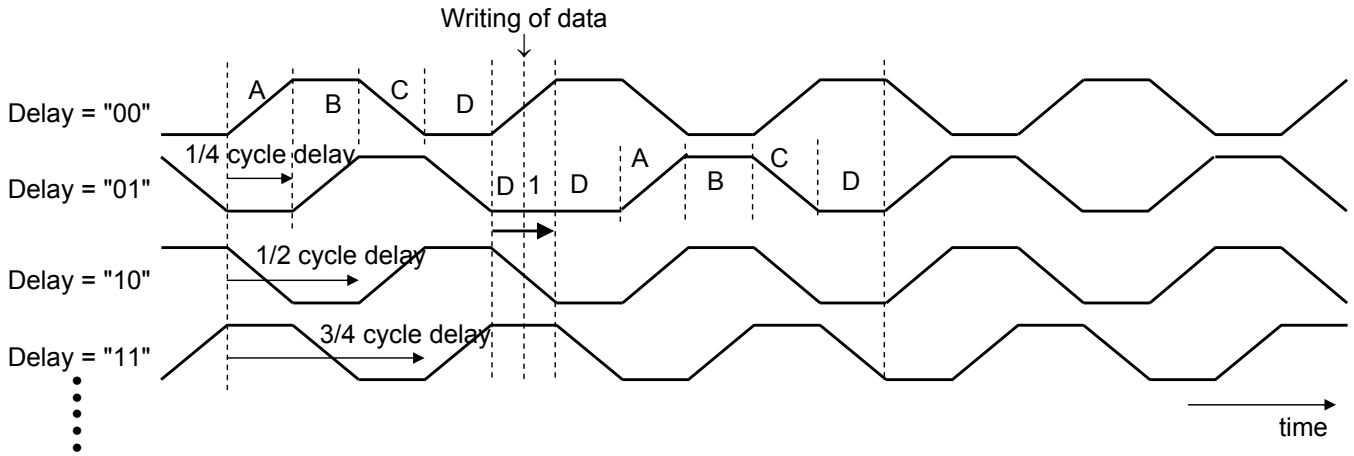
Ex.) Delay change ("01" → "00")

(3) Delay change at C interval (at the decrease of Duty)



Ex.) Delay change ("01" → "10")

(4) Delay change at D interval (at Duty 0%)



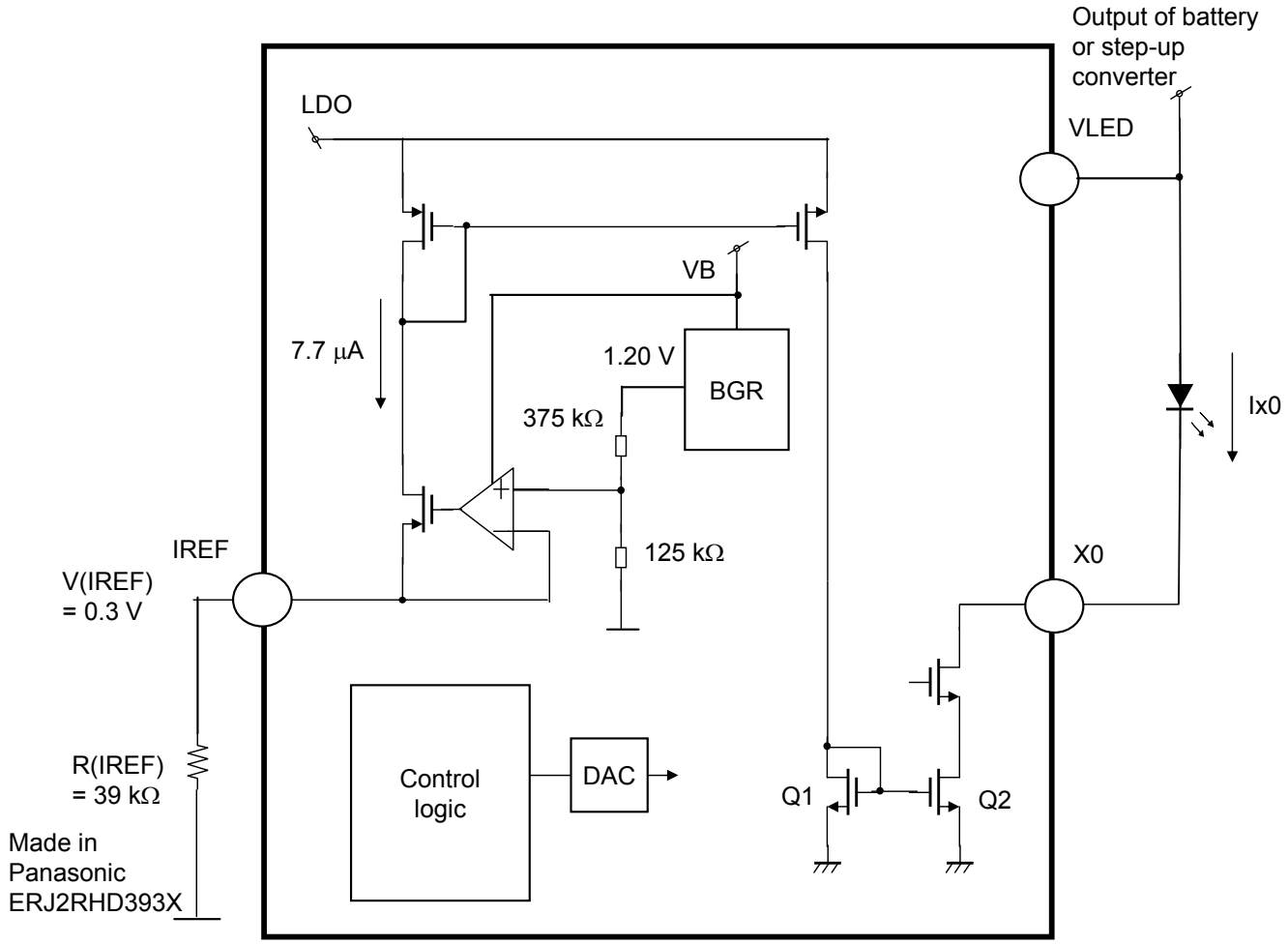
Established : 2009-07-23
Revised : 2013-04-01

OPERATION (continued)

7. Functions and sequences of each block (continued)

7.5 Equivalent circuit example of constant current driver block

In case of X0 pin (Dot matrix driver)



The constant current driver example of Matrix LED driver is shown in the above figure.
The constant current source for constant current driver is given by the following formula.

V(IREF) / R(IREF) = 0.3 V / 39 kΩ = 7.7 μA

The current value (Ix0) of LED can be set from 0.00 mA to 21.00 mA by adjusting the mirror ratio of Q1 and Q2 via serial interface at DAC

When R(IREF) is changed to 78 kΩ, which is 2 times the value shown in the above example, the constant current value decreases to 1/2 of each address setting value. (However, the accuracy of each current value in this case cannot be guaranteed.)
In addition, please take note that the constant current value of all LED drivers also decreases to 1/2 of each address setting value.

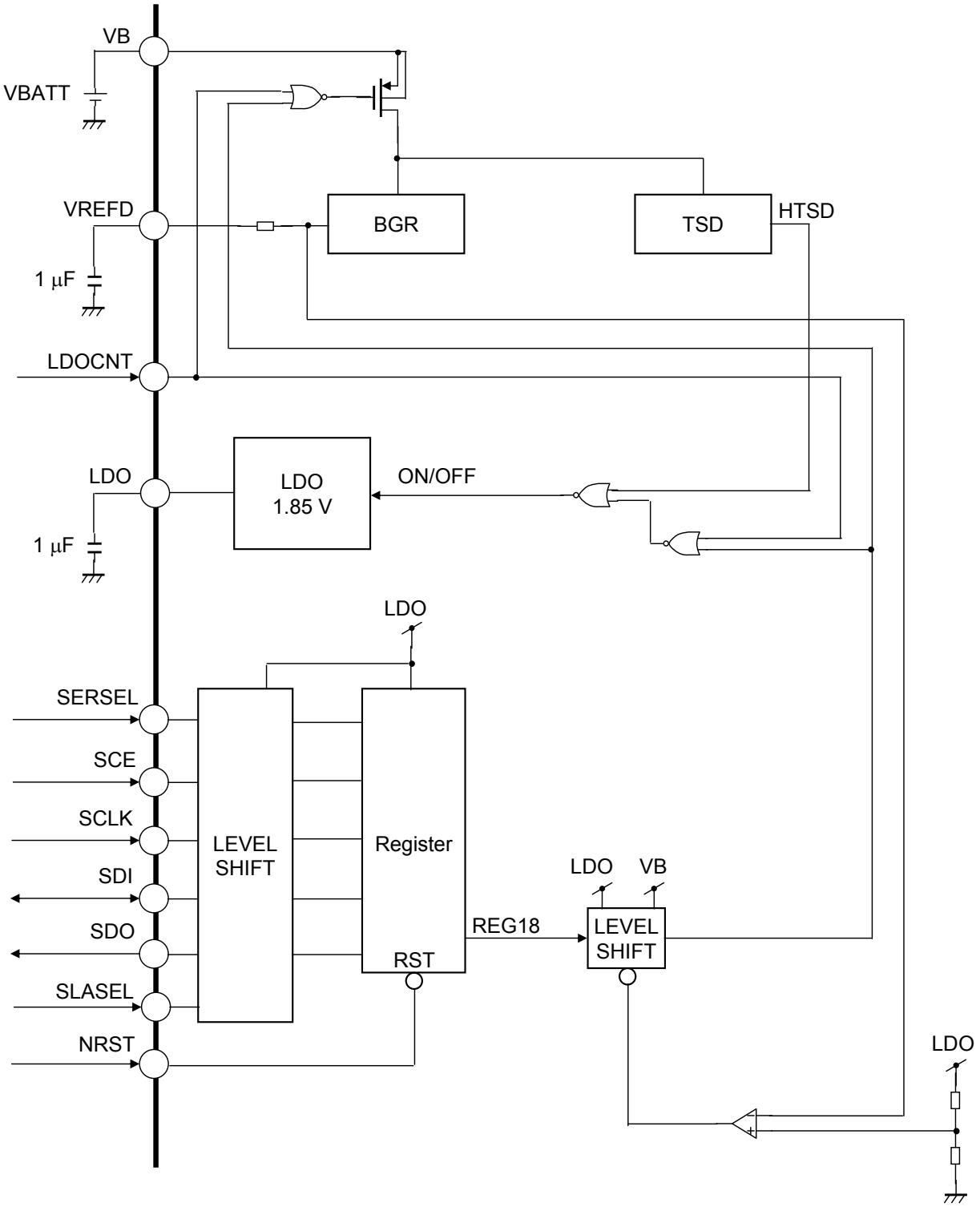
The accuracy of V(IREF) is 0.3 ± 0.1 V.
ERJ2RHD393X (±0.5%) made by Panasonic is recommended for R(IREF) to keep the accuracy of constant current value for LED.

Established : 2009-07-23
Revised : 2013-04-01

OPERATION (continued)

7. Functions and sequences of each block (continued)

7.6 RESET block configuration

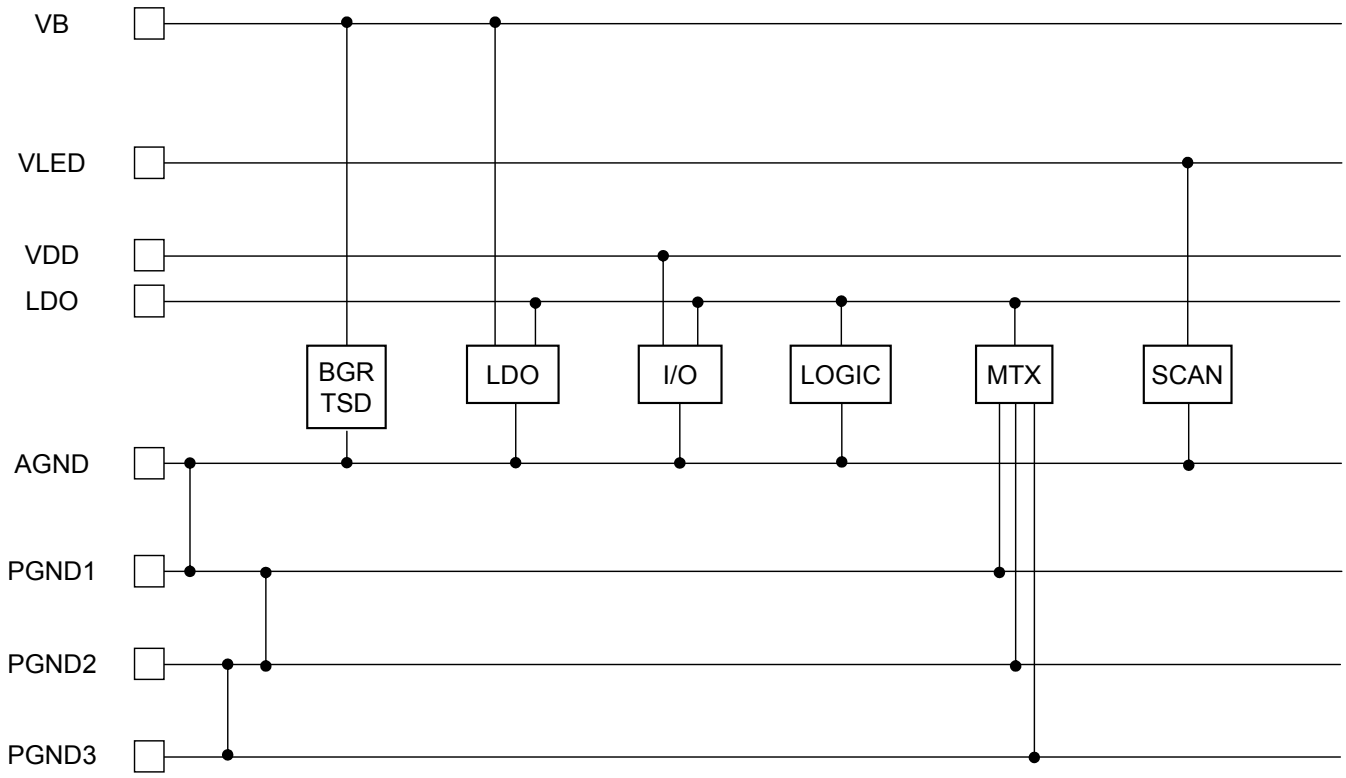


* All logic to which the power supply is not connected are connected to VB as power supplied.

Established : 2009-07-23
Revised : 2013-04-01

OPERATION (continued)

8. Connection between power supplies

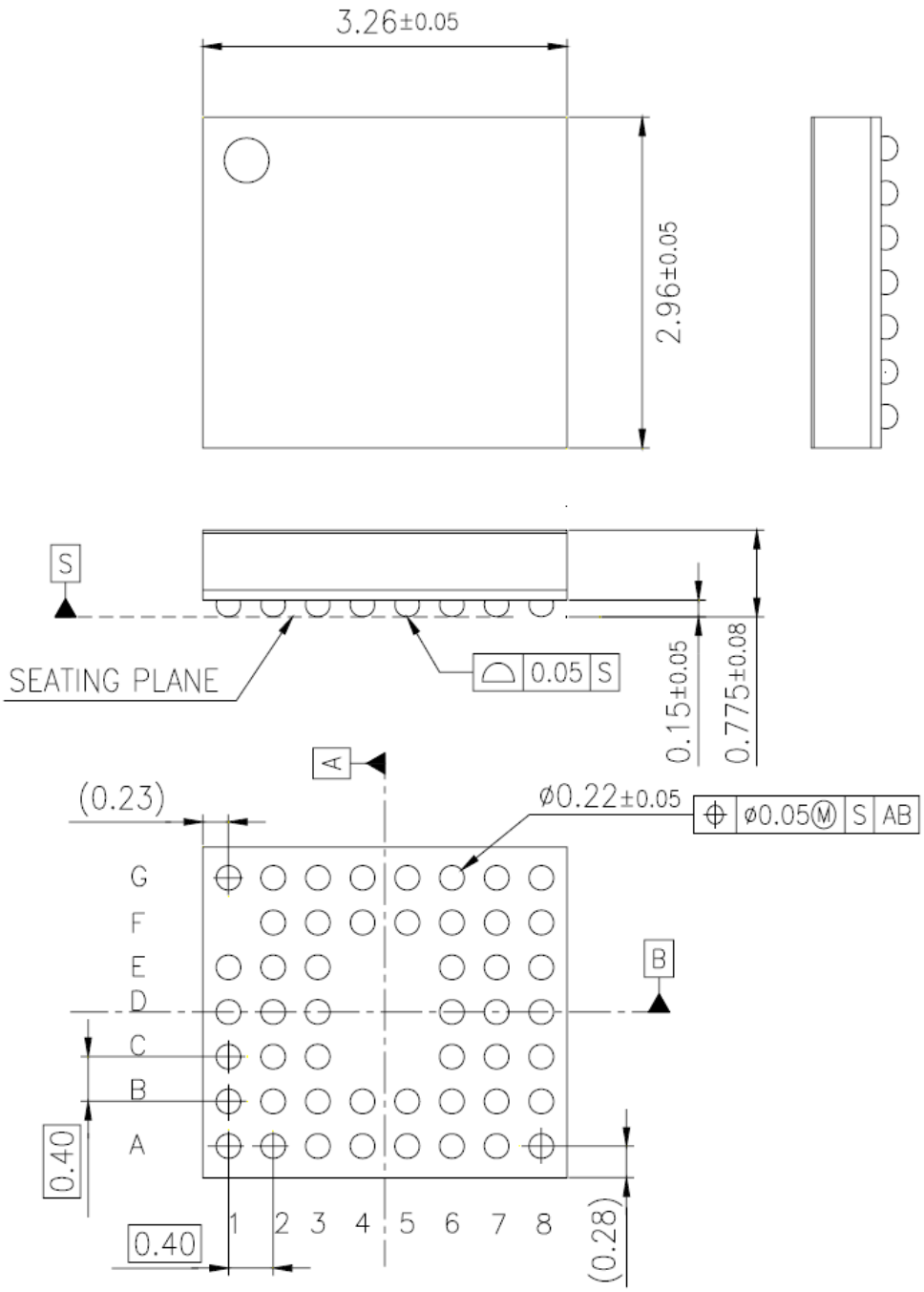


Established : 2009-07-23
Revised : 2013-04-01

PACKAGE INFORMATION (Reference Data)

Package Code : XBGA049-W-3033AEL

Unit:mm



Body Material	:	Br / Sb Free Epoxy Resin
Reroute Material	:	Cu
Bump	:	SnAgCu

Established : 2009-07-23
Revised : 2013-04-01

IMPORTANT NOTICE

1. When using the LSI for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this LSI, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
3. This LSI is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this LSI may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the LSI being used for any special application, unless our company agrees to the use of such special application.
4. This LSI is neither designed nor intended for use in automotive applications or environments unless the specific product is designated by our company as compliant with the ISO/TS 16949 requirements.
   Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the LSI being used in automotive application, unless our company agrees to such application in this book.
5. Please use this product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our LSI being used by our customers, not complying with the applicable laws and regulations.
6. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might emit smoke or ignite.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the semiconductor device. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
9. Take notice in the use of this product that it might be damaged or occasionally emit smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply..
10. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
    Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.
11. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
12. Verify the risks which might be caused by the malfunctions of external components.
13. Due to the unshielded structure of this LSI, functions and characteristics of the product cannot be guaranteed under the exposure of light. During normal operation or even under testing condition, please ensure that the LSI is not exposed to light.
14. Please ensure that your design does not have metal shield parts touching the chip surface as the surface potential is GND voltage.
15. Pay attention to the breakdown voltage of this LSI when using.
    More than + 1500 V or less than – 1500 V electrostatic discharge to all the pins might damage this product.

Established : 2009-07-23
Revised : 2013-04-01

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(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
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