DATA SHEET

BUJ103AX
Silicon Diffused Power Transistor

Product specification August 2018

WeEn
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Silicon Diffused Power Transistor | BUJ103AX

GENERAL DESCRIPTION

High-voltage, high-speed planar-passivated npn power switching transistor in a plastic full-pack envelope intended for use in high frequency electronic lighting ballast applications, converters, inverters, switching regulators, motor control systems, etc.

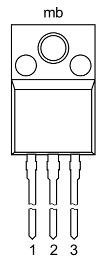
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{CESM}	Collector-emitter voltage peak value	V_{BE} = 0 V	-	700	V
V_{CBO}	Collector-Base voltage (open emitter)		-	700	V
V_{CEO}	Collector-emitter voltage (open base)		-	400	V
I_C	Collector current (DC)		-	4	A
I_{CM}	Collector current peak value		-	8	A
P_{tot}	Total power dissipation	$T_{hs} \leq 25$ ˚C	-	26	W
V_{CEsat}	Collector-emitter saturation voltage		0.25	1.0	V
h_{FEsat}	DC current gain	I_C = 3 A; V_{CE} = 5 V	12.5	-	
t_f	Fall time	Ic=2A,I_{B1}=0.4A	33	80	ns

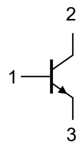
PINNING - SOT186A

PIN	DESCRIPTION
1	base
2	collector
3	emitter
mb	solated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CESM}	Collector to emitter voltage	V_{BE} = 0 V	-	700	V
V_{CEO}	Collector to emitter voltage (open base)		-	400	V
V_{CBO}	Collector to base voltage (open emitter)		-	700	V
I_C	Collector current (DC)		-	4	A
I_{CM}	Collector current peak value		-	8	A
I_B	Base current (DC)		-	2	A
I_{BM}	Base current peak value		-	4	A
P_{tot}	Total power dissipation	$T_{hs} \leq 25$ ˚C	-	26	W
T_{stg}	Storage temperature		-65	150	˚C
T_j	Junction temperature		-	150	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-hs}$	Junction to heatsink	with heatsink compound	-	4.8	K/W
$R_{th\ j-a}$	Junction to ambient	in free air	55	-	K/W

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

STATIC CHARACTERISTICS

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CES}	Collector cut-off current [1]	V_{BE} = 0 V; V_{CE} = $V_{CESMmax}$	-	-	1.0	mA
I_{CES}		V_{BE} = 0 V; V_{CE} = $V_{CESMmax}$; T_j = 125 ˚C	-	-	2.0	mA
I_{CBO}	Collector cut-off current [1]	V_{CBO} = $V_{CESMmax}$(700V)	-	-	0.1	mA
I_{CEO}		V_{CEO} = $V_{CEOMmax}$(400V)	-	-	0.1	mA
I_{EBO}	Emitter cut-off current	V_{EB} = 7 V; I_C = 0 A	-	-	0.1	mA
$V_{CEOsust}$	Collector-emitter sustaining voltage	I_B = 0 A; I_C = 10 mA; L = 25 mH	400	-	-	V
V_{CEsat}	Collector-emitter saturation voltage	I_C = 3.0 A; I_B = 0.6 A	-	0.25	1.0	V
V_{BEsat}	Base-emitter saturation voltage	I_C = 3.0 A; I_B = 0.6 A	-	0.97	1.5	V
h_{FE}	DC current gain	I_C = 1 mA; V_{CE} = 5 V	10	17	32	
h_{FE}		I_C = 0.5 A; V_{CE} = 5 V	12	20	32	
h_{FEsat}	DC current gain	I_C = 2 A; V_{CE} = 5 V	13.5	16	20	
		I_C = 3 A; V_{CE} = 5 V	-	12.5	-	

DYNAMIC CHARACTERISTICS

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
	Switching times (resistive load)	I_{Con} = 2.5 A; I_{Bon} = $-I_{Boff}$ = 0.5 A; R_L = 75 ohms; V_{BB2} = 4 V;			
t_{on}	Turn-on time		0.52	0.6	µs
t_s	Turn-off storage time		2.7	3.2	µs
t_f	Turn-off fall time		0.3	0.43	µs
	Switching times (inductive load)	I_{Con} = 2 A; I_{Bon} = 0.4 A; L_B = 1 µH; $-V_{BB}$ = 5 V			
t_s	Turn-off storage time		1.2	1.33	µs
t_f	Turn-off fall time		33	80	ns
	Switching times (inductive load)	I_{Con} = 2 A; I_{Bon} = 0.4 A; L_B = 1 µH; $-V_{BB}$ = 5 V; T_j = 100 ˚C			
t_s	Turn-off storage time		-	1.8	µs
t_f	Turn-off fall time		-	200	ns

1 Measured with half sine-wave voltage (curve tracer).

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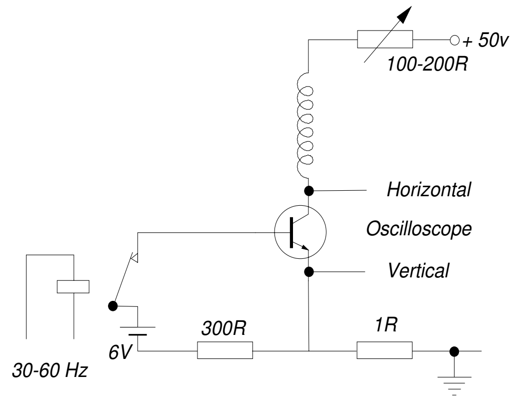

Fig.1. Test circuit for $V_{CEOsust}$.

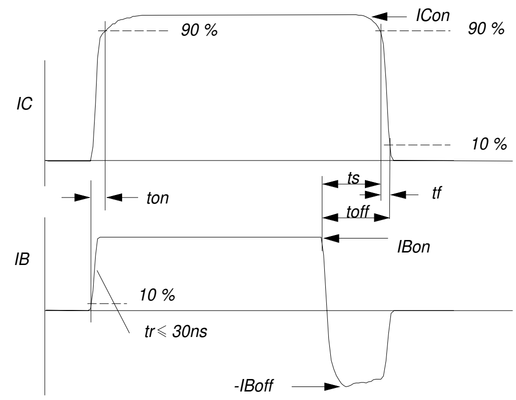

Fig.4. Switching times waveforms with resistive load.

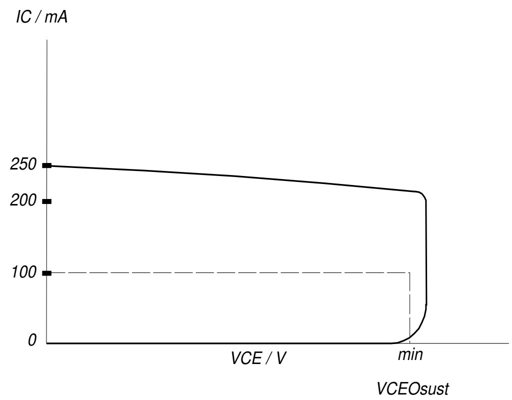

Fig.2. Oscilloscope display for $V_{CEOsust}$.

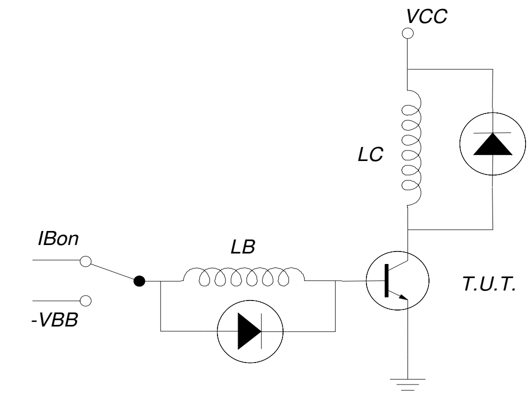

Fig.5. Test circuit inductive load.
V_{CC} = 300 V; $-V_{BE}$ = 5 V; L_C = 200 uH; L_B = 1 uH

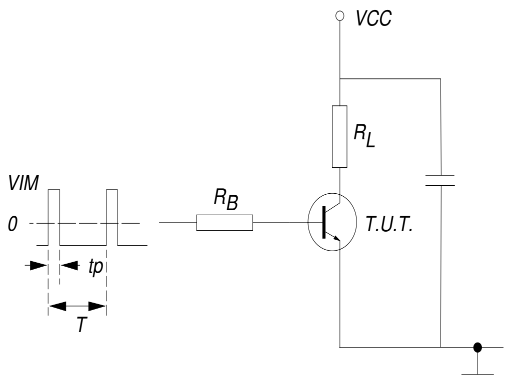

Fig.3. Test circuit resistive load. V_{IM} = -6 to +8 V
V_{CC} = 250 V; t_p = 20 µs; $\delta = t_p / T$ = 0.01.
R_B and R_L calculated from I_{Con} and I_{Bon} requirements.

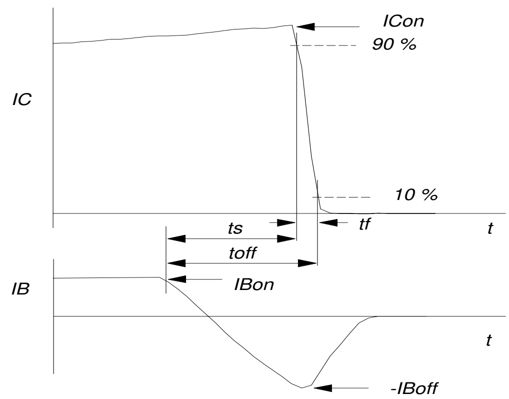

Fig.6. Switching times waveforms with inductive load.

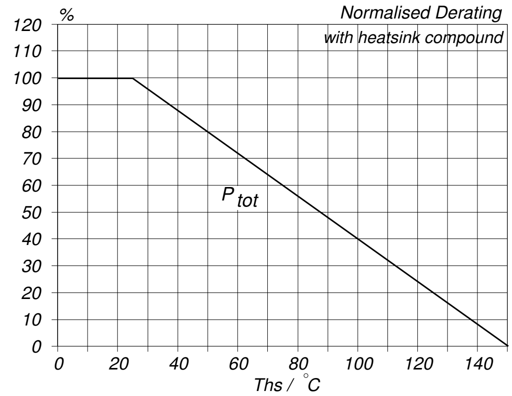

Fig.7. Normalised power dissipation.
$PD\% = 100 \cdot PD/PD_{25^\circ C} = f\,(T_{hs})$

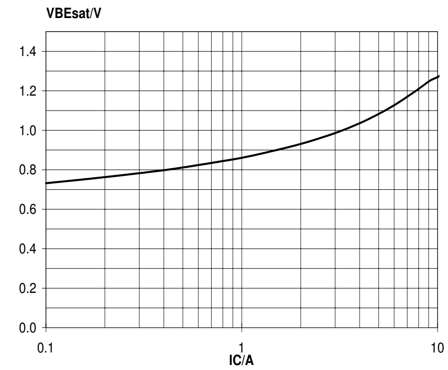

Fig.10. Base-Emitter saturation voltage.
Solid lines = typ values, $V_{BEsat} = f(IC)$; at IC/IB =4.

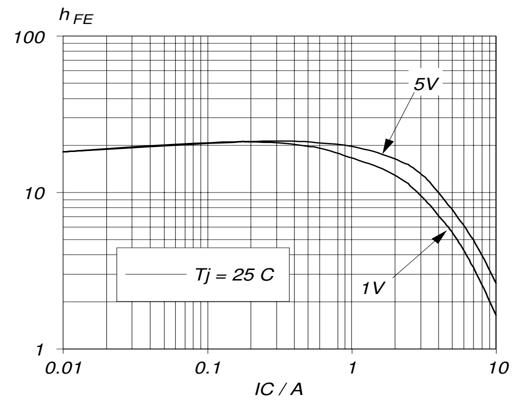

Fig.8. Typical DC current gain. $h_{FE} = f(I_C)$
parameter V_{CE}

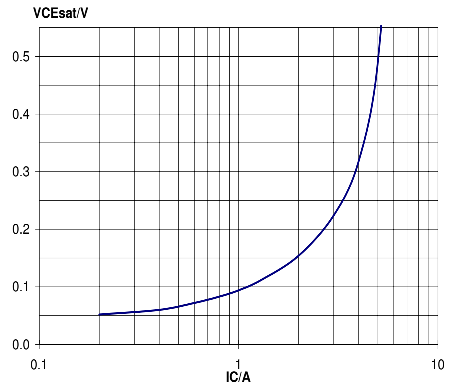

Fig.11. Collector-Emitter saturation voltage.
Solid lines = typ values, $V_{CEsat} = f(IC)$; at IC/IB =4.

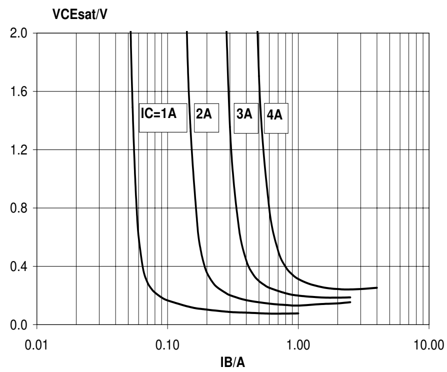

Fig.9. Collector-Emitter saturation voltage.
Solid lines = typ values, $V_{CEsat} = f(IB)$; T_j=25˚C.

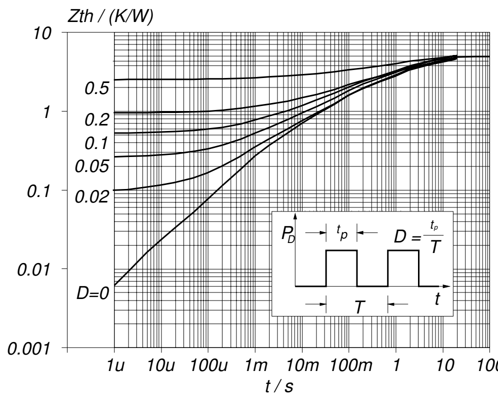

Fig.12. Transient thermal impedance.
$Z_{th\,j\text{-}hs} = f(t)$; parameter $D = t_p/T$

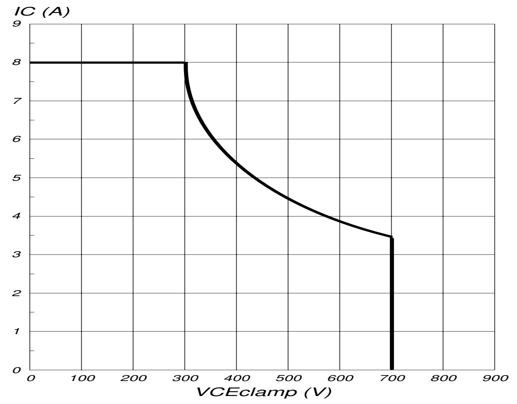

Fig.13. Reverse bias safe operating area. $T_j \leq T_{j\,max}$

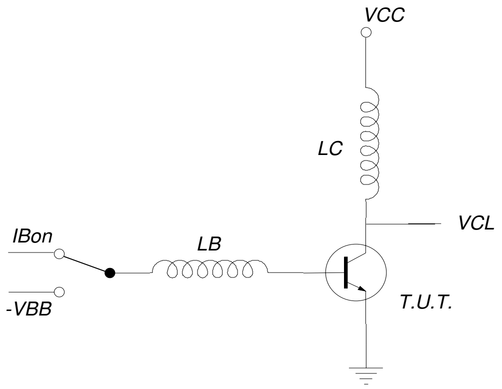

Fig.14. Test circuit for reverse bias safe operating area.
$V_{cl} \leq 1000V$; $V_{cc} = 150V$; $V_{BB} = -5V$; $L_B = 1\mu H$; $L_c = 200\mu H$

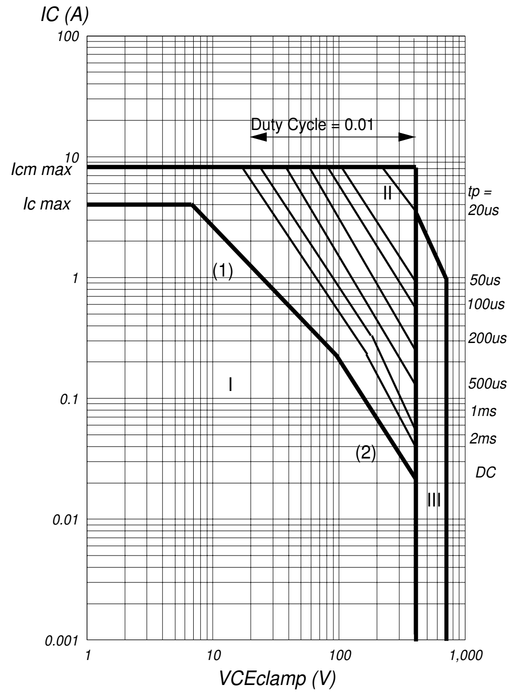

Fig.15. Forward bias safe operating area. $T_{hs} \leq 25$ ˚C

(1) P_{tot} max and P_{tot} peak max lines.
(2) Second breakdown limits.
I Region of permissible DC operation.
II Extension for repetitive pulse operation.
III Extension during turn-on in single transistor converters provided that $R_{BE} \leq 100\ \Omega$ and $t_p \leq 0.6\ \mu s$.
NB: Mounted with heatsink compound and 30 ± 5 newton force on the centre of the envelope.

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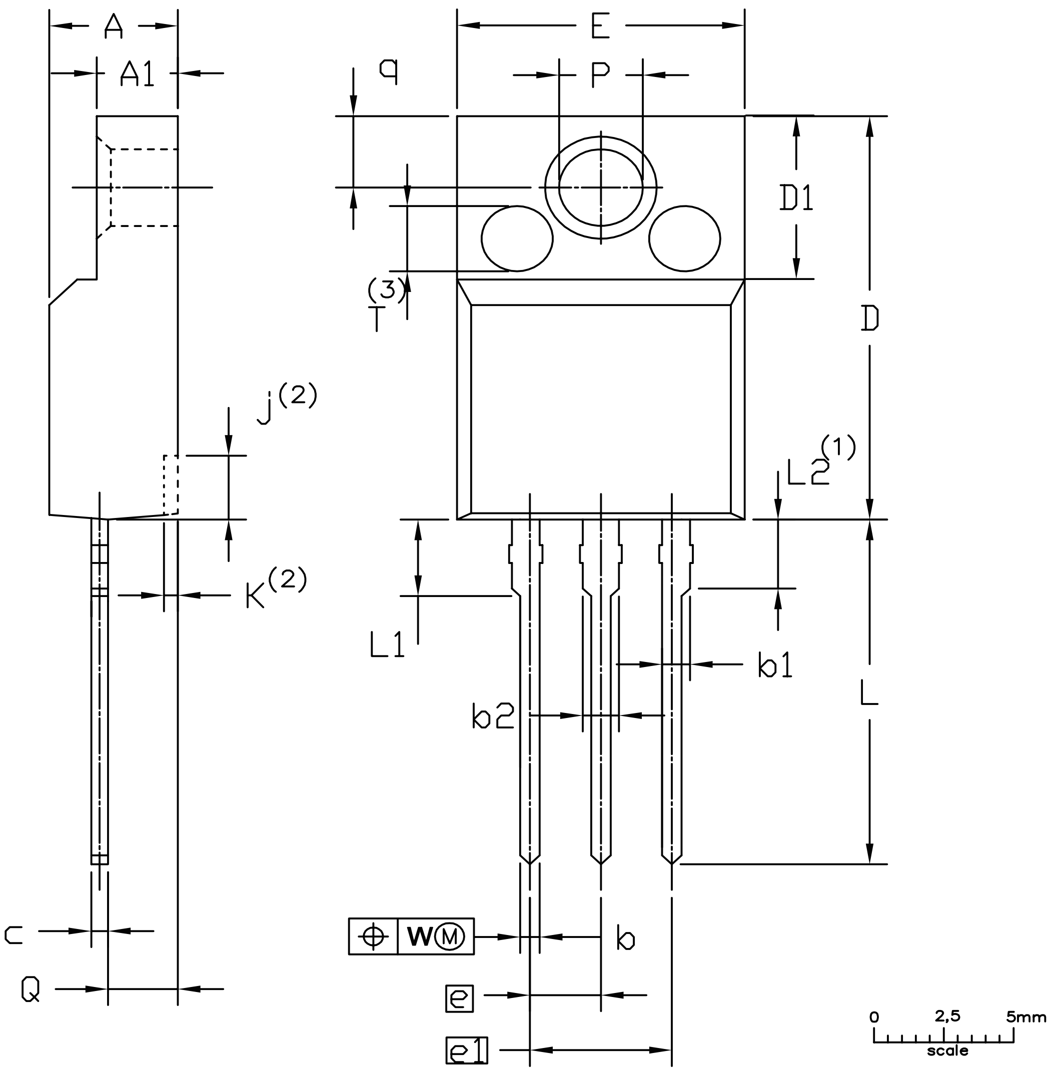
MECHANICAL DATA

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack" SOT186A



UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j(2)	K(2)	L	L_1	L_2(1) max.	P	Q	q	W	T(3)
mm	4.6	2.9	0.9	1.1	1.4	0.7	15.8	6.5	10.3	2.54	5.08	2.7	0.6	14.4	3.30	3	3.2	2.6	3.0	0.4	2.5
	4.0	2.5	0.7	0.9	1.0	0.4	15.2	6.3	9.7			1.7	0.4	13.5	2.79		3.0	2.3	2.6		

Notes
1. Terminal dimensions within this zone are uncotrolled
2. Dot lines area designs may vary
3. Eject pin mark is for reference only

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3 LEADS TO220F				2013-11-14

Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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