Document Number: A3T19H455W23S
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RF Power LDMOS Transistor

N–Channel Enhancement–Mode Lateral MOSFET

This 81 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 1930 to 1990 MHz.

1900 MHz

- Typical Doherty Single–Carrier W–CDMA Performance: V_{DD} = 30 Vdc, I_{DQA} = 540 mA, V_{GSB} = 0.6 Vdc, P_{out} = 81 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
1930 MHz	16.2	49.6	8.1	–31.0
1960 MHz	16.5	49.4	8.0	–32.1
1990 MHz	16.4	49.1	7.8	–32.6

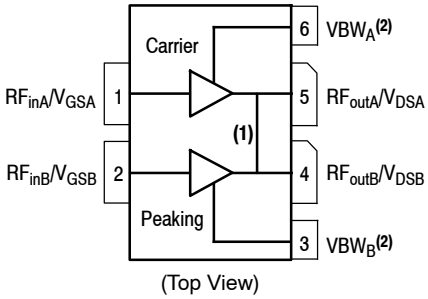
Features

- Advanced high performance in–package Doherty
- Designed for wide instantaneous bandwidth applications
- Greater negative gate–source voltage range for improved Class C operation
- Able to withstand extremely high output VSWR and broadband operating conditions
- Designed for digital predistortion error correction systems

A3T19H455W23SR6

1930–1990 MHz, 81 W AVG., 30 V AIRFAST RF POWER LDMOS TRANSISTOR

ACP–1230S–4L2S



(Top View)

Figure 1. Pin Connections

1. Pin connections 4 and 5 are DC coupled and RF independent.
2. Device can operate with V_{DD} current supplied through pin 3 and pin 6.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	-40 to +225	°C
CW Operation @ T_C = 25°C when DC current is fed through pin 3 and pin 6 Derate above 25°C	CW	172 0.7	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 81°C, 81 W Avg., W-CDMA, 30 Vdc, I_{DQA} = 600 mA, V_{GSB} = 0.6 Vdc, 1960 MHz	$R_{\theta JC}$	0.14	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Charge Device Model (per JESD22-C101)	C3

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	5	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics - Side A, Carrier					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 160 μAdc)	$V_{GS(th)}$	1.4	1.8	2.2	Vdc
Gate Quiescent Voltage (V_{DD} = 30 Vdc, I_{DA} = 540 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	2.2	2.6	3.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.6 Adc)	$V_{DS(on)}$	0.05	0.15	0.3	Vdc
On Characteristics - Side B, Peaking					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 360 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 3.6 Adc)	$V_{DS(on)}$	0.05	0.15	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com/RF/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
4. Side A and Side B are tied together for this measurement.

(continued)

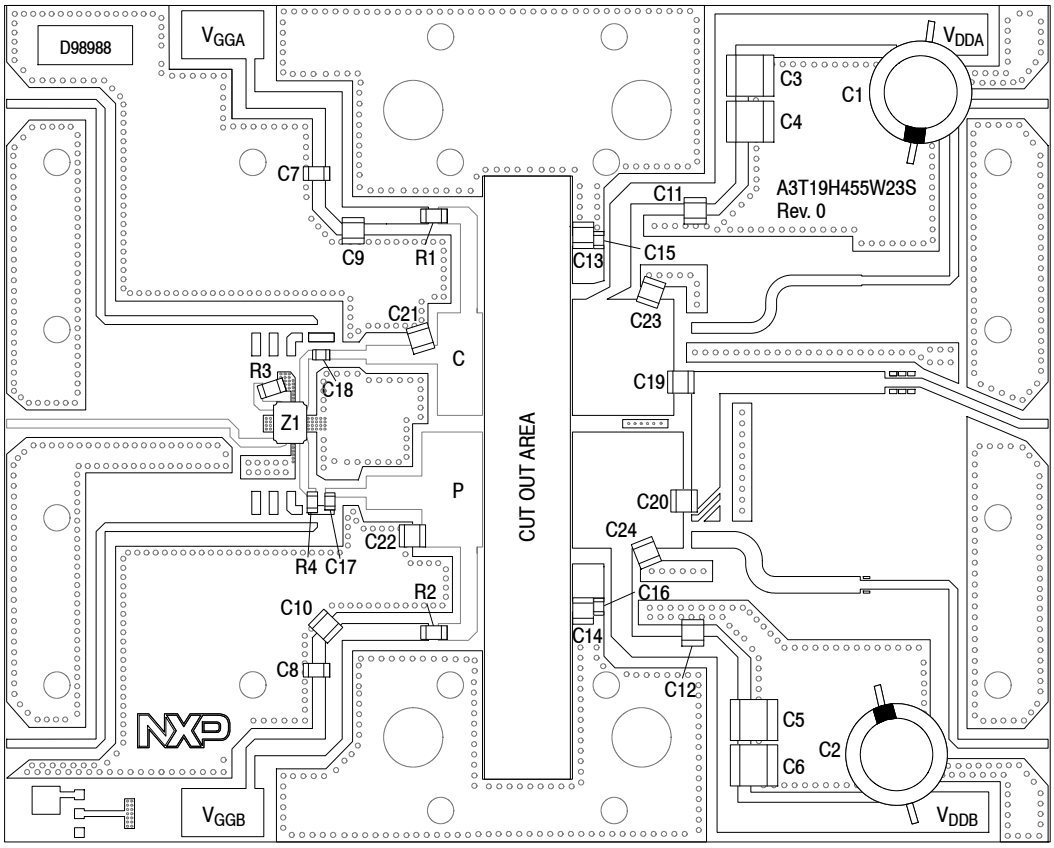
Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2,3) (In NXP Doherty Test Fixture, 50 ohm system) V_{DD} = 30 Vdc, I_{DQA} = 540 mA, V_{GSB} = 0.6 Vdc, P_{out} = 81 W Avg., f = 1990 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	15.2	16.4	17.7	dB
Drain Efficiency	η_D	46.0	49.1	—	%
P_{out} @ 3 dB Compression Point, CW	P3dB	56.0	56.9	—	dBm
Adjacent Channel Power Ratio	ACPR	—	–32.6	–28.0	dBc
Load Mismatch (3) (In NXP Doherty Test Fixture, 50 ohm system) I_{DQA} = 540 mA, V_{GSB} = 0.6 Vdc, f = 1960 MHz, 12 μsec(on), 10% Duty Cycle					
VSWR 10:1 at 32 Vdc, 490 W Pulsed CW Output Power (3 dB Input Overdrive from 340 W Pulsed CW Rated Power)	No Device Degradation				
Typical Performance (3) (In NXP Doherty Test Fixture, 50 ohm system) V_{DD} = 30 Vdc, I_{DQA} = 540 mA, V_{GSB} = 0.6 Vdc, 1930–1990 MHz Bandwidth					
P_{out} @ 3 dB Compression Point (4)	P3dB	—	541	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1930–1990 MHz bandwidth)	Φ	—	–29	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	200	—	MHz
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 81 W Avg.	G_F	—	0.3	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.009	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.004	—	dB/°C

Table 5. Ordering Information

Device	Tape and Reel Information	Package
A3T19H455W23SR6	R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel	ACP-1230S-4L2S

1. V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.
2. Part internally matched both on input and output.
3. Measurements made with device in an asymmetrical Doherty configuration.
4. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.



Note: V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.

Figure 2. A3T19H455W23SR6 Test Circuit Component Layout

Table 6. A3T19H455W23SR6 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2	470 μF, 63 V Electrolytic Capacitor	MCGPR63V477M13X26-RH	Multicomp
C3, C4, C5, C6	10 μF Chip Capacitor	C5750X7S2A106M230KB	TDK
C7, C8	220 nF Chip Capacitor	C1206C224Z5VACTU	Kemet
C9, C10, C11, C12, C20	10 pF Chip Capacitor	ATC100B100JT500XT	ATC
C13, C14	10 μF Chip Capacitor	C3225X7S1H106K	TDK
C15, C16, C17	10 pF Chip Capacitor	ATC600F100JT250XT	ATC
C18	8.2 pF Chip Capacitor	ATC600F8R2BT250XT	ATC
C19	5.1 pF Chip Capacitor	ATC100B5R1CT500XT	ATC
C21	1.3 pF Chip Capacitor	ATC100B1R3BW500XT	ATC
C22, C24	0.3 pF Chip Capacitor	ATC100B0R3BT500XT	ATC
C23	0.2 pF Chip Capacitor	ATC100B0R2BT500XT	ATC
R1, R2	3.3 Ω, 1/4 W Chip Resistor	WCR1206-3R3F	Welwyn
R3	50 Ω, 8 W Termination Chip Resistor	C8A50Z4A	Anaren
R4	0 Ω, 1/4 W Chip Resistor	CWCR08050000Z0EA	Vishay
Z1	1800-2200 MHz Band, 90°, 2 dB Directional Coupler	X3C20F1-02S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D98988	MTL

TYPICAL CHARACTERISTICS — 1930–1990 MHz

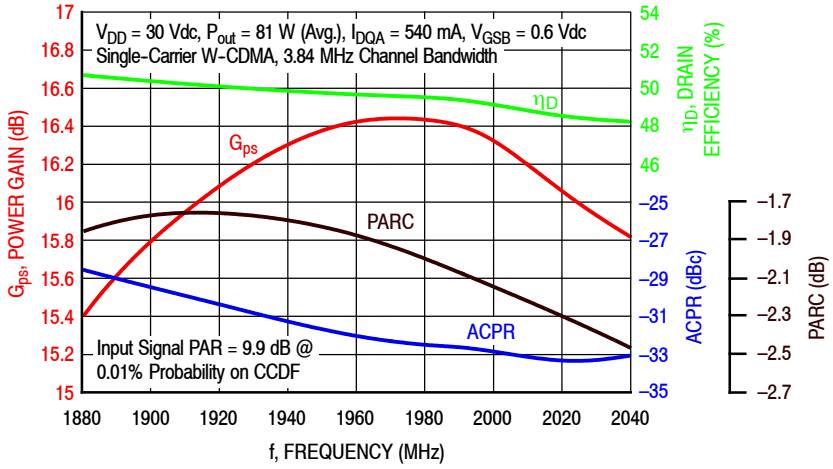


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 81 Watts Avg.

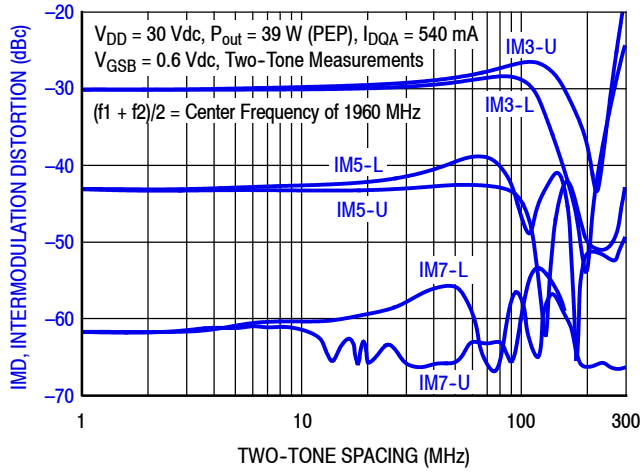


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

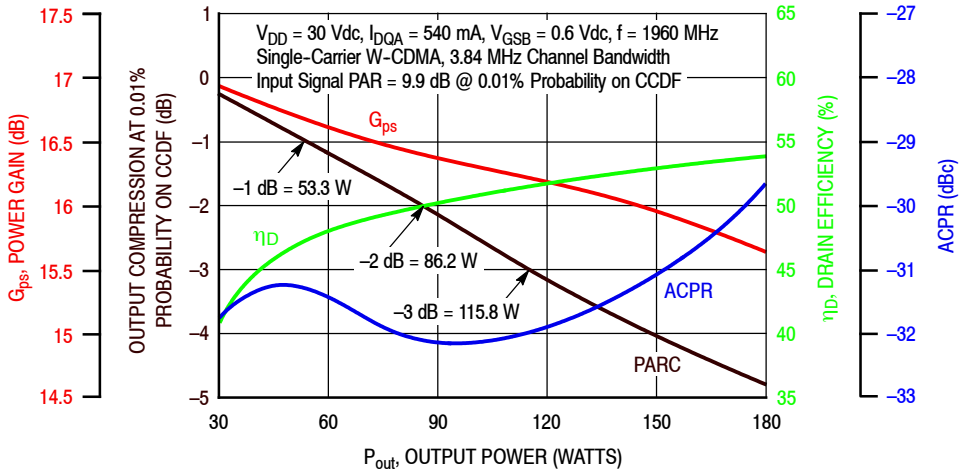


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 1930–1990 MHz

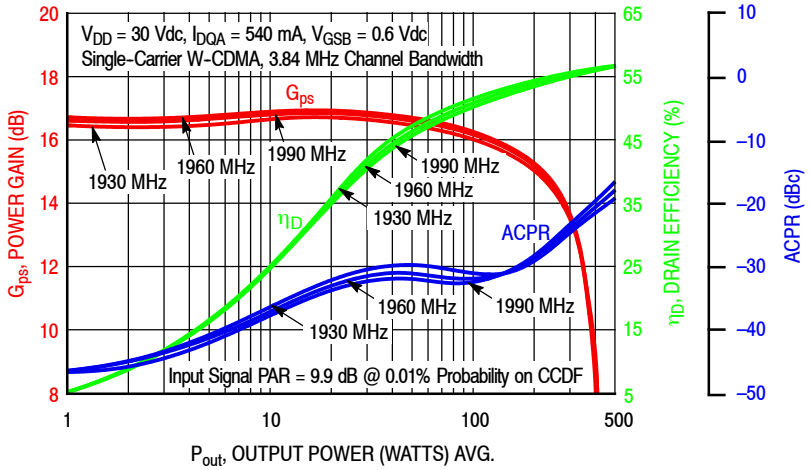


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

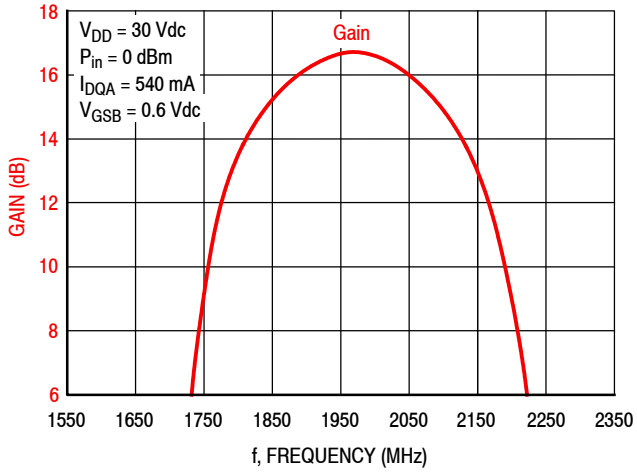


Figure 7. Broadband Frequency Response

Table 7. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 30 Vdc, I_{DQA} = 779 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	3.52 – j7.64	3.44 + j7.03	1.09 – j4.64	18.6	52.9	194	58.8	–14
1960	4.30 – j7.50	4.65 + j7.55	1.03 – j4.61	18.6	52.8	191	57.7	–14
1990	5.95 – j8.89	6.72 + j7.83	1.04 – j4.86	18.4	52.8	190	57.2	–15

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	3.52 – j7.64	3.33 + j7.60	1.06 – j4.73	16.4	53.6	229	59.3	–20
1960	4.30 – j7.50	4.78 + j8.27	1.03 – j5.00	16.2	53.6	228	57.2	–19
1990	5.95 – j8.89	7.14 + j9.00	1.04 – j4.94	16.3	53.6	227	58.1	–21

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 8. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 30 Vdc, I_{DQA} = 779 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	3.52 – j7.64	3.49 + j7.36	2.43 – j3.71	21.5	50.9	124	73.0	–21
1960	4.30 – j7.50	4.78 + j8.04	2.32 – j3.40	21.8	50.5	112	72.5	–21
1990	5.95 – j8.89	6.95 + j8.48	2.19 – j3.23	21.9	50.1	103	72.5	–23

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	3.52 – j7.64	3.46 + j7.73	2.66 – j4.05	19.3	51.6	145	72.0	–26
1960	4.30 – j7.50	4.88 + j8.52	2.50 – j3.81	19.5	51.4	137	71.6	–27
1990	5.95 – j8.89	7.08 + j9.14	2.07 – j3.99	19.1	51.9	154	71.4	–27

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

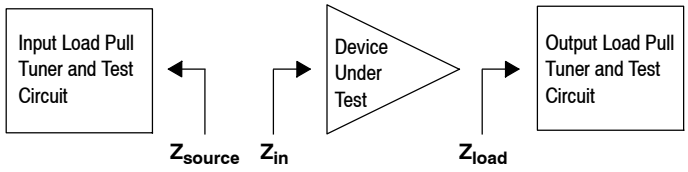


Table 9. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 30 Vdc, V_{GSB} = 0.6 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	2.29 – j6.45	1.80 + j5.63	2.37 – j5.99	13.5	56.0	400	52.9	–29
1960	3.54 – j6.53	2.40 + j6.06	2.60 – j5.99	13.8	56.0	399	54.1	–28
1990	4.98 – j6.44	3.24 + j6.51	2.78 – j5.86	13.9	55.9	392	54.2	–29

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	2.29 – j6.45	1.90 + j5.91	2.55 – j6.21	11.4	56.6	462	53.9	–35
1960	3.54 – j6.53	2.60 + j6.41	2.81 – j6.09	11.7	56.6	459	54.9	–35
1990	4.98 – j6.44	3.69 + j6.91	3.13 – j6.18	11.7	56.5	450	54.6	–34

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

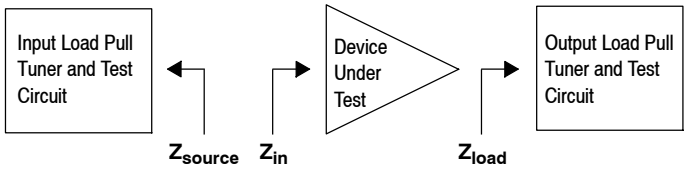
Table 10. Peaking Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 30 Vdc, V_{GSB} = 0.6 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	2.29 – j6.45	1.66 + j5.59	3.67 – j4.21	14.5	55.2	328	59.4	–33
1960	3.54 – j6.53	2.16 + j5.99	3.59 – j3.69	14.7	54.8	301	60.3	–33
1990	4.98 – j6.44	2.92 + j6.48	3.32 – j3.45	14.7	54.7	298	60.4	–33

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	2.29 – j6.45	1.82 + j5.90	3.95 – j4.87	12.2	56.1	403	59.5	–39
1960	3.54 – j6.53	2.49 + j6.40	4.03 – j4.56	12.4	55.9	393	60.1	–38
1990	4.98 – j6.44	3.49 + j6.92	3.84 – j4.23	12.5	55.8	384	60.1	–38

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1960 MHz

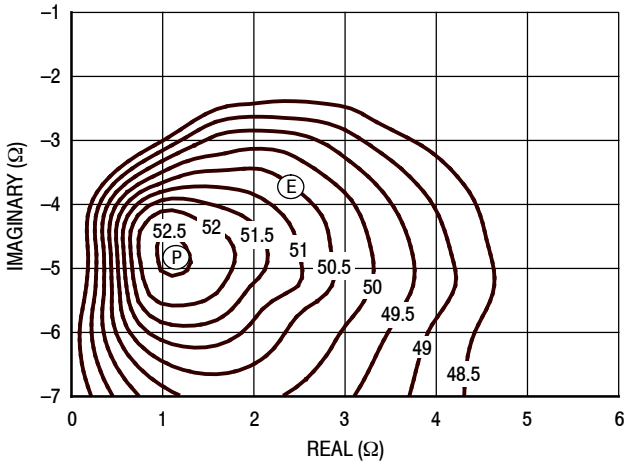


Figure 8. P1dB Load Pull Output Power Contours (dBm)

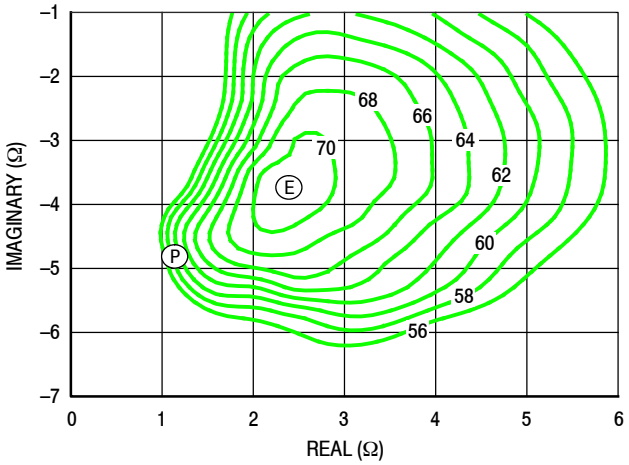


Figure 9. P1dB Load Pull Efficiency Contours (%)

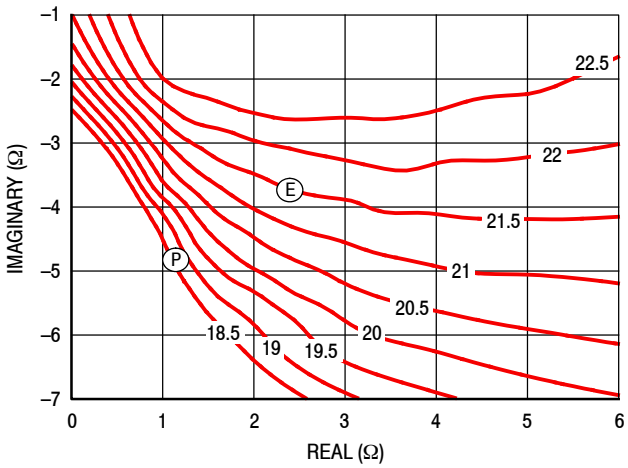


Figure 10. P1dB Load Pull Gain Contours (dB)

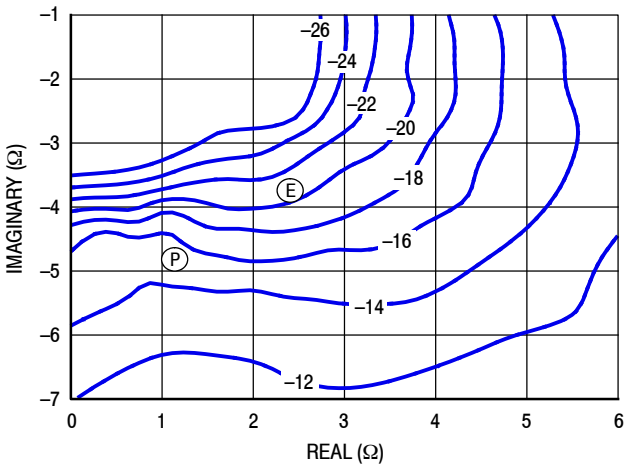


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1960 MHz

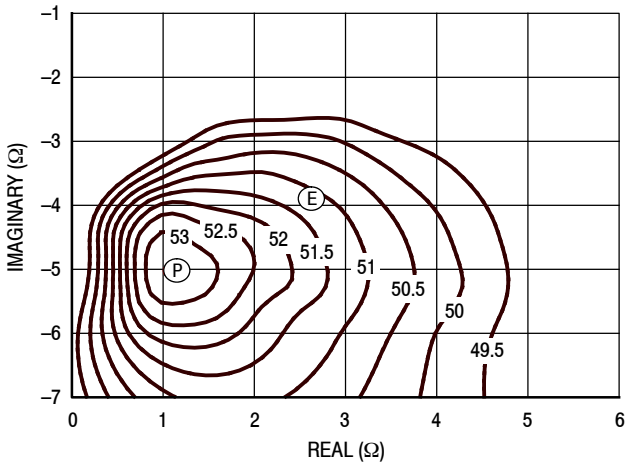


Figure 12. P3dB Load Pull Output Power Contours (dBm)

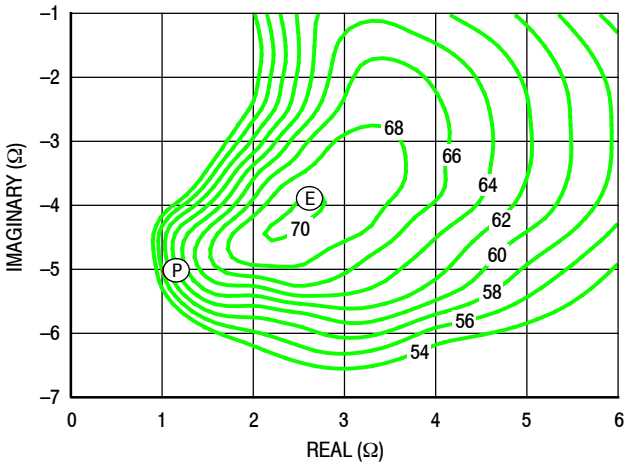


Figure 13. P3dB Load Pull Efficiency Contours (%)

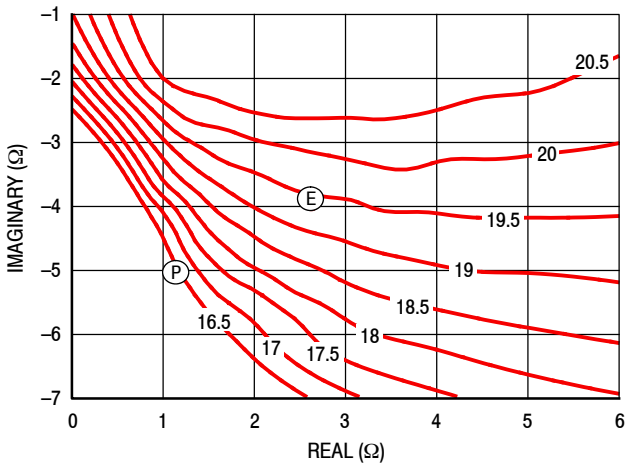


Figure 14. P3dB Load Pull Gain Contours (dB)

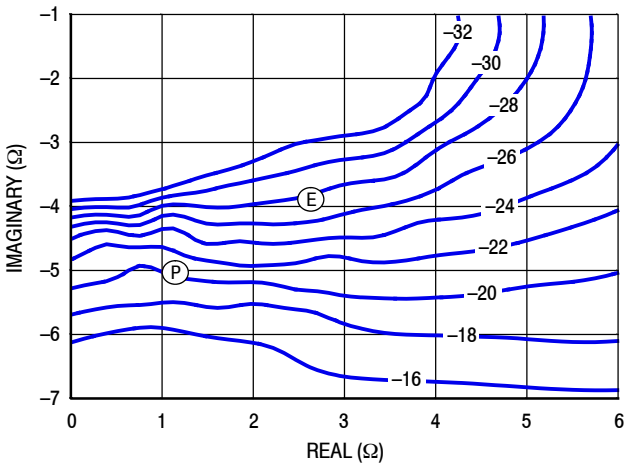


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 1960 MHz

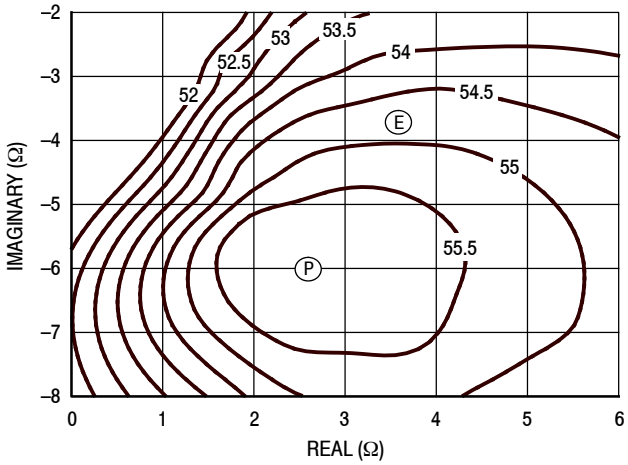


Figure 16. P1dB Load Pull Output Power Contours (dBm)

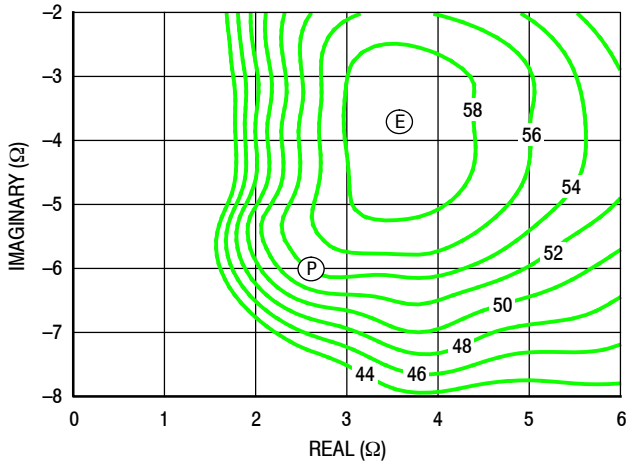


Figure 17. P1dB Load Pull Efficiency Contours (%)

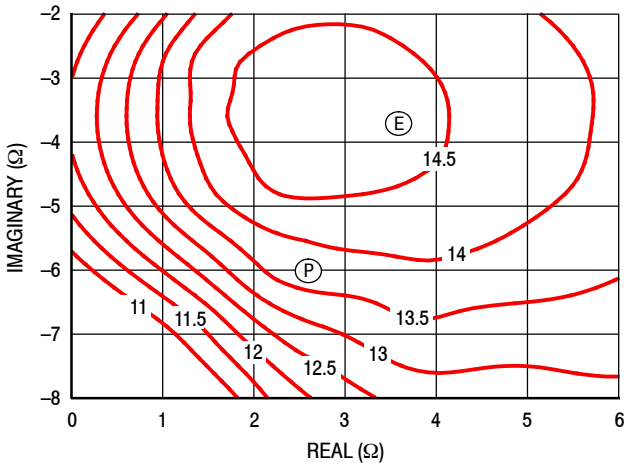


Figure 18. P1dB Load Pull Gain Contours (dB)

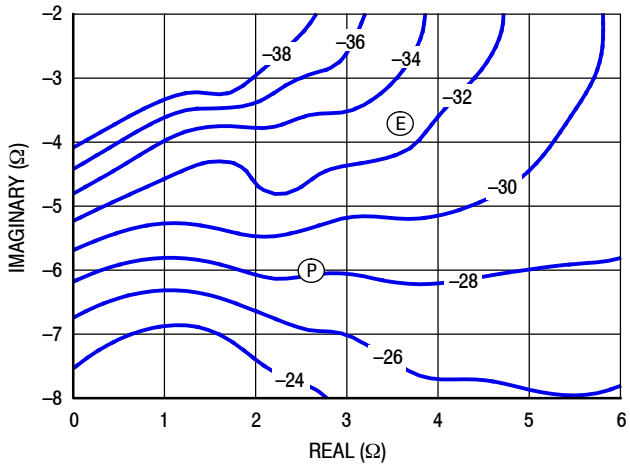


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 1960 MHz

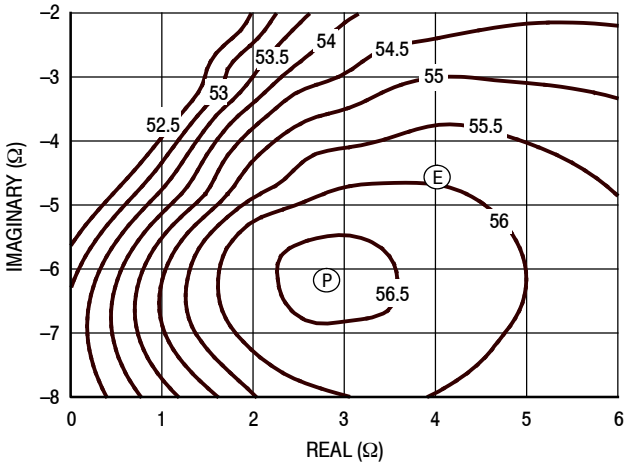


Figure 20. P3dB Load Pull Output Power Contours (dBm)

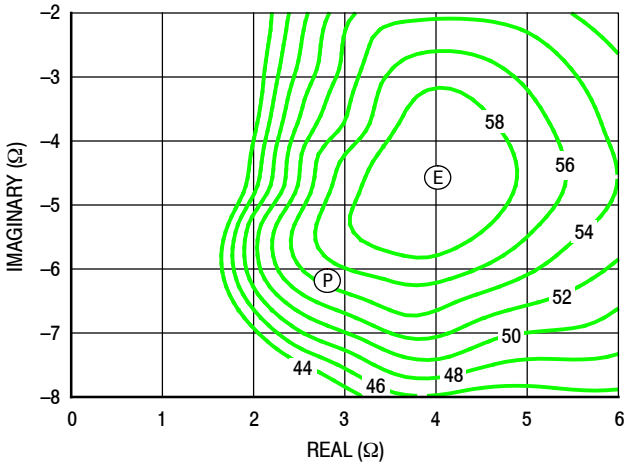


Figure 21. P3dB Load Pull Efficiency Contours (%)

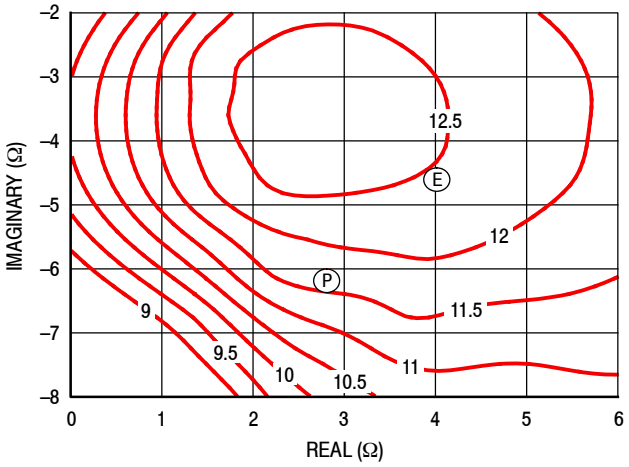


Figure 22. P3dB Load Pull Gain Contours (dB)

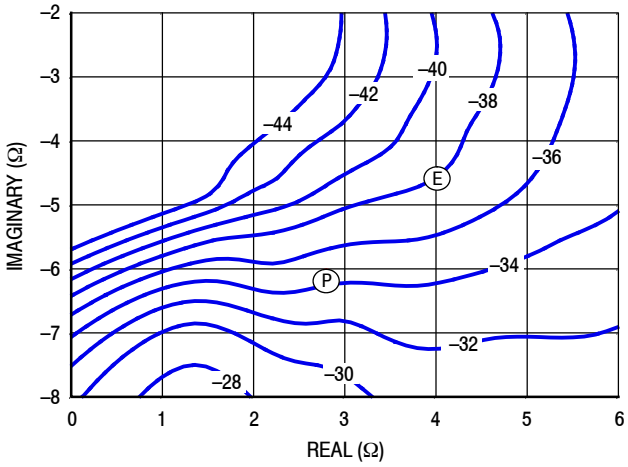


Figure 23. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

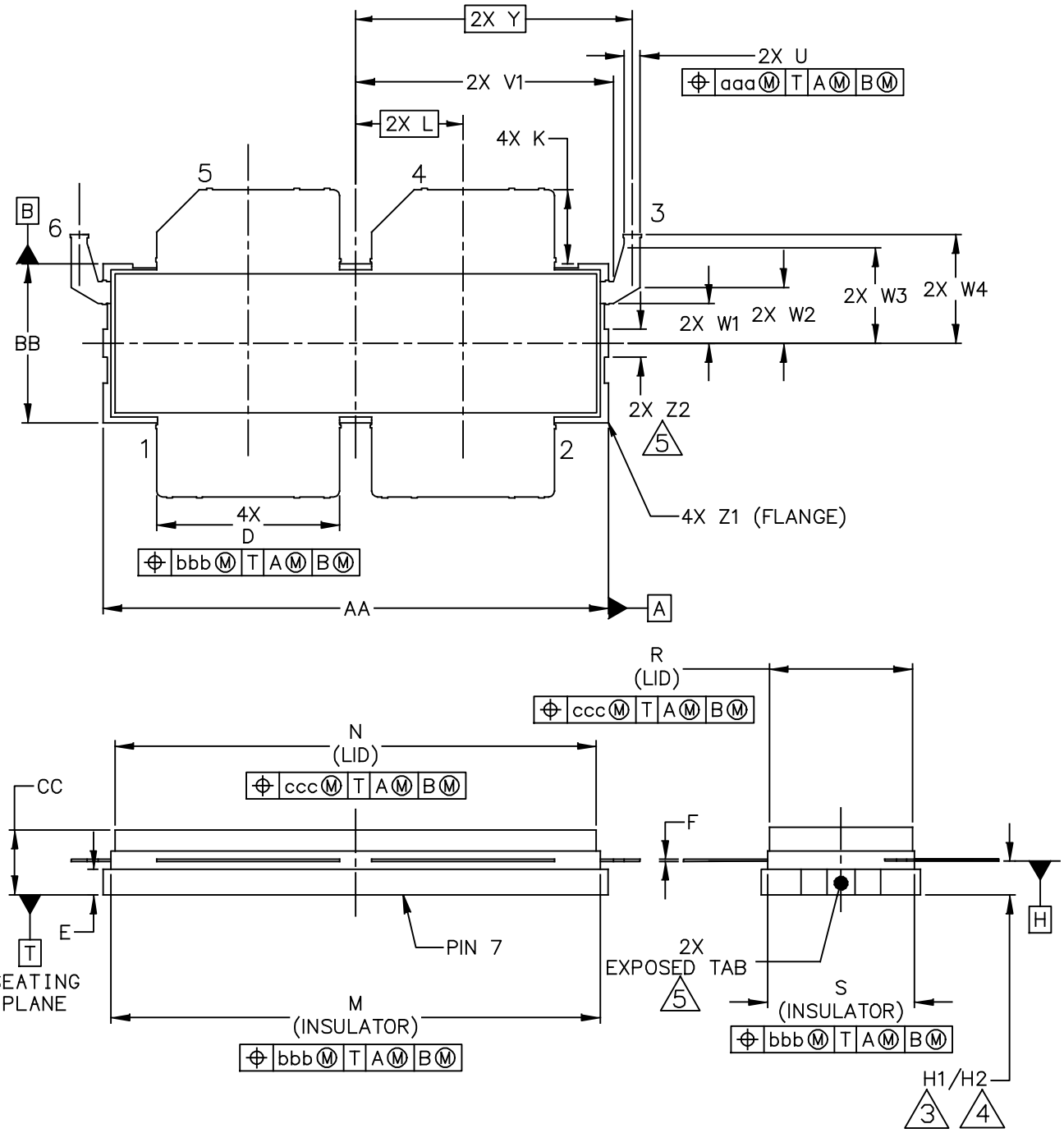
Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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TITLE: ACP–1230S–4L2S	DOCUMENT NO: 98ASA00974D	REV: A
	STANDARD: NON–JEDEC	
	SOT1800–4	21 JUN 2017

NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

2. CONTROLLING DIMENSION: INCH

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1, 2, 4 & 5. H2 APPLIES TO PINS 3 & 6.

4. TOLERANCE OF DIMENSION H2 IS TENTATIVE.

5. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

6. DATUM H IS LOCATED AT THE BOTTOM OF THE LEAD FRAME AND IS COINCIDENT WITH THE LEAD WHERE THE LEADS EXIT THE PLASTIC BODY.

7. DIMENSIONS M AND S DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .012 INCH (0.30 MM) PER SIDE. DIMENSIONS M AND S DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

8. DIMENSIONS D, U AND K DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .010 INCH (0.25 MM) TOTAL IN EXCESS OF THE D, U AND K DIMENSION AT MAXIMUM MATERIAL CONDITION.

9. DATUM A AND B TO BE DETERMINED AT DATUM T.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
AA	1.265	1.275	32.13	32.39	S	.365	.375	9.27	9.53
BB	.395	.405	10.03	10.29	U	.035	.045	0.89	1.14
CC	.160	.190	4.06	4.83	V1	.640	.655	16.26	16.64
D	.455	.465	11.56	11.81	W1	.105	.115	2.67	2.92
E	.062	.069	1.57	1.75	W2	.135	.145	3.43	3.68
F	.004	.007	0.10	0.18	W3	.245	.255	6.22	6.48
H1	.082	.090	2.08	2.29	W4	.265	.281	6.73	7.14
H2	.078	.094	1.98	2.39	Y	0.695 BSC		17.65 BSC	
K	.175	.195	4.45	4.95	Z1	R.000	R.040	R0.00	R1.02
L	0.270 BSC		6.86 BSC		Z2	.060	.100	1.52	2.54
M	1.219	1.241	30.96	31.52	aaa	.015		0.38	
N	1.218	1.242	30.94	31.55	bbb	.010		0.25	
R	.365	.375	9.27	9.53	ccc	.020		0.51	

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SOT1800–4 21 JUN 2017

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1908: Solder Reflow Attach Method for High Power RF Devices in Air Cavity Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Dec. 2017	• Initial release of data sheet

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Document Number: A3T19H455W23S
Rev. 0, 12/2017

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